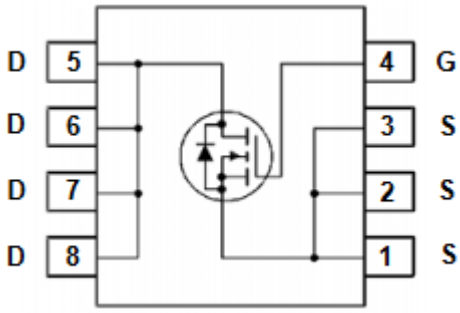
# MOSFET - Power, DUAL COOL® N-Channel, DFN8
## 120 V, 6.1 mΩ, 92 A
# NTMFSC006N12MC

| $V_{(BR)DSS}$ | $R_{DS(ON)}$ MAX | $I_D$ MAX |
|---|---|---|
| 120 V | 6.1 mΩ @ 10 V | 92 A |

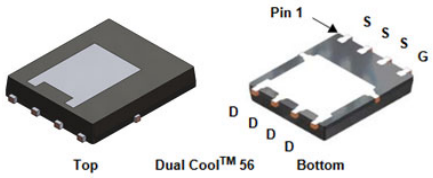
### Features
- Advanced Dual−sided Cooled Packaging
- Ulra Low $R_{DS(on)}$
- MSL1 Robust Packaging Design

### Typical Applications
- Primary DC−DC FET
- Synchronous Rectifier
- DC−DC Conversion

### N−CHANNEL MOSFET

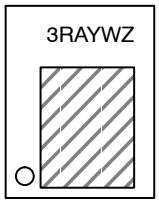



### MARKING DIAGRAM




**DFN8 5x6.15**
**CASE 506EG**

### MARKING DIAGRAM




3R = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

### MAXIMUM RATINGS ($T_J$ = 25°C unless otherwise noted)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 120 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3) | Steady State | $T_C$ = 25°C | $I_D$ | 92 | A |
| | | $T_C$ = 100°C | | 57 | |
| Power Dissipation $R_{\theta JC}$ (Note 1) | | $T_C$ = 25°C | $P_D$ | 104 | W |
| | | $T_C$ = 100°C | | 41 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3) | Steady State | $T_A$ = 25°C | $I_D$ | 14 | A |
| | | $T_A$ = 100°C | | 9 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 2) | | $T_A$ = 25°C | $P_D$ | 2.7 | W |
| | | $T_A$ = 100°C | | 1.1 | |
| Pulsed Drain Current | $T_C$ = 25°C, $t_p$ = 10 μs | | $I_{DM}$ | 1459 | A |
| Operating Junction / Storage Temperature Max | | | $T_J$, $T_{stg}$ | +150 | °C |
| Source Current (Body Diode) | | | $I_S$ | 86 | A |
| Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 53 A) | | | $E_{AS}$ | 114 | mJ |
| Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction−to−Case − Steady State | $R_{\theta JC}$ | 1.2 | °C/W |
| Junction−to−Case Top − Steady State | $R_{\theta JT}$ | 1.53 | |
| Junction−to−Ambient − Steady State (Note 2) | $R_{\theta JA}$ | 45 | |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 $mm^2$, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NTMFSC006N12MC | DFN8 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 120 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | $I_D$ = 250 μA, ref to 25°C | | | 16 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 120 V | $T_J$ = 25°C | | | 5 | μA |
| | | | $T_J$ = 125°C | | | 100 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = 20 V | | | | 100 | nA |
| **ON CHARACTERISTICS** (Note 4) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | | 2 | | 4 | V |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | $I_D$ = 250 μA, ref to 25°C | | | 9.8 | | mV/°C |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V | $I_D$ = 44 A | | 4.7 | 6.1 | mΩ |
| Gate−Resistance | $R_G$ | $T_A$ = 25°C | | | 1.4 | | Ω |
| **CHARGES & CAPACITANCES** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1 MHz, $V_{DS}$ = 60 V | | | 3040 | | pF |
| Output Capacitance | $C_{OSS}$ | | | | 1460 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | | 11.5 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 6 V, $V_{DS}$ = 60 V, $I_D$ = 44 A | | | 24.3 | | nC |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 60 V, $I_D$ = 44 A | | | 39 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 13.2 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 6.3 | | |
| Plateau Voltage | $V_{GP}$ | | | | 4.65 | | V |
| **SWITCHING CHARACTERISTICS** (Note 4) | | | | | | | |
| Turn−On Delay Time | $t_{d(ON)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 60 V, $I_D$ = 44 A, $R_G$ = 2.5 Ω | | | 15.2 | | ns |
| Rise Time | $t_r$ | | | | 5.3 | | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | 25.5 | | |
| Fall Time | $t_f$ | | | | 5.7 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 44 A | $T_J$ = 25°C | | 0.86 | | V |
| | | | $T_J$ = 125°C | | 0.74 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, $dI_S/dt$ = 1000 A/μs, $I_S$ = 44 A | | | 33.4 | | ns |
| Reverse Recovery Charge | $Q_{RR}$ | | | | 350.2 | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

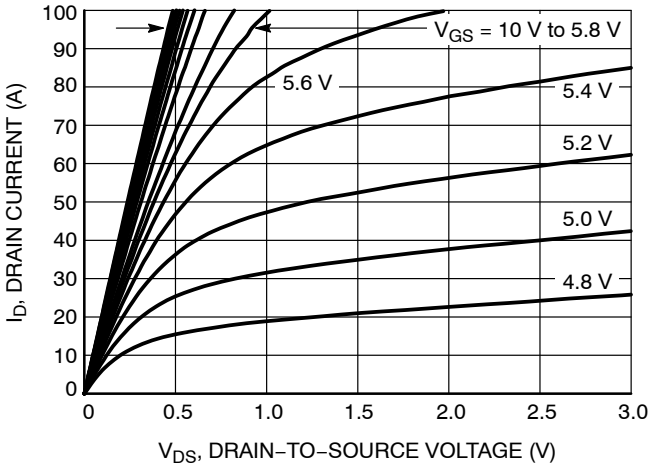



**Figure 1. On−Region Characteristics**

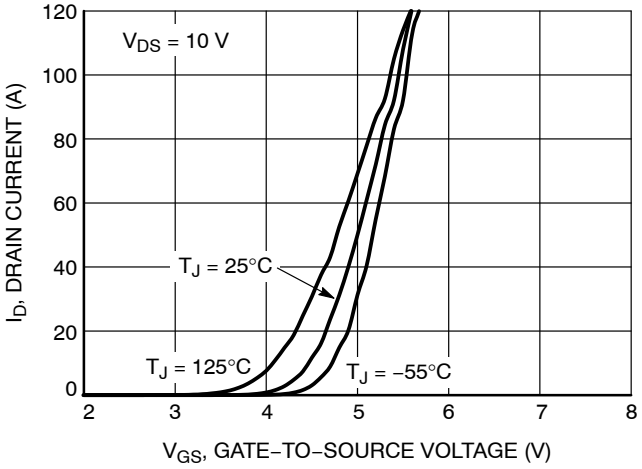



**Figure 2. Transfer Characteristics**

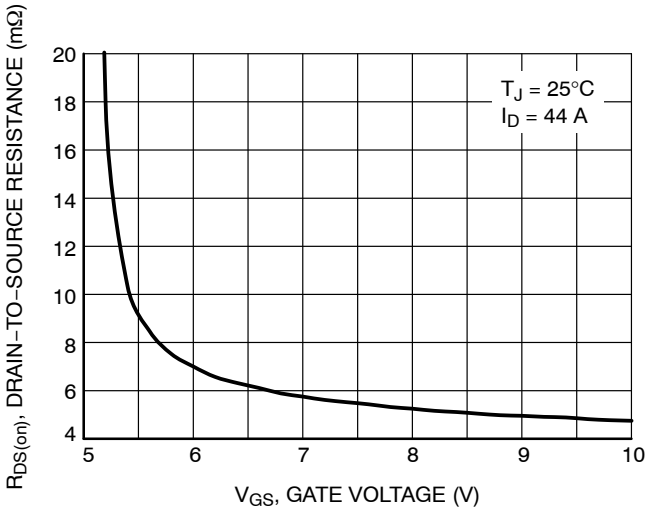



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

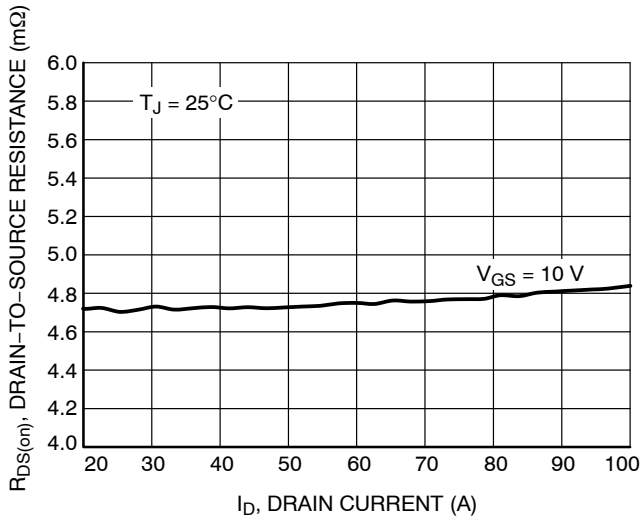



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

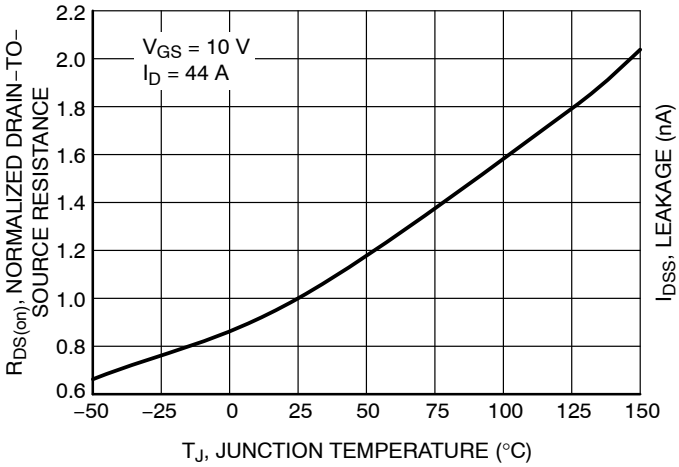



**Figure 5. On−Resistance Variation with Temperature**

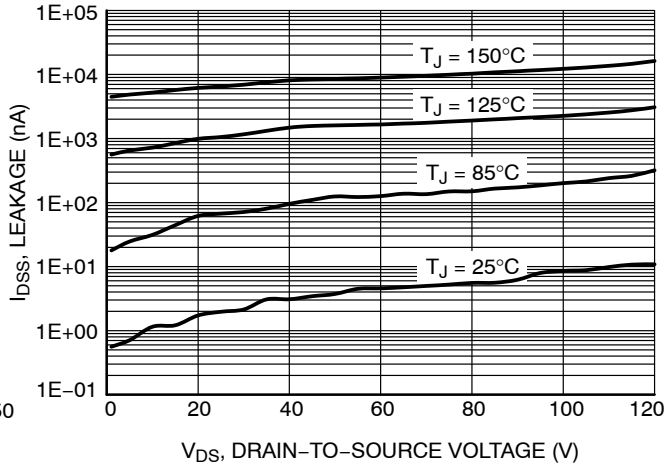



**Figure 6. Maximum Continuous Drain Current vs. Case Temperature**

## TYPICAL CHARACTERISTICS

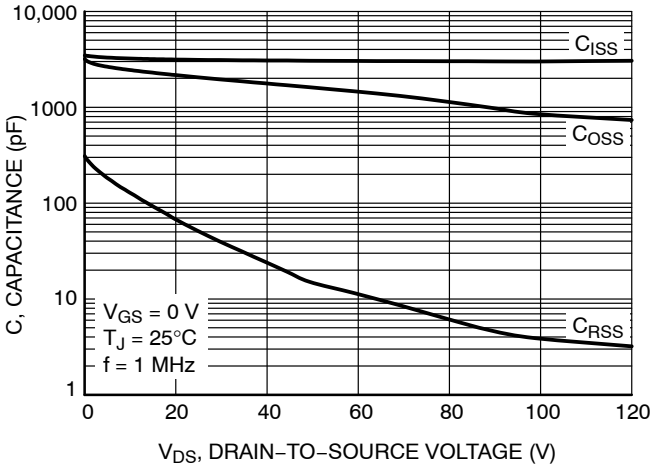



**Figure 7. Capacitance Variation**

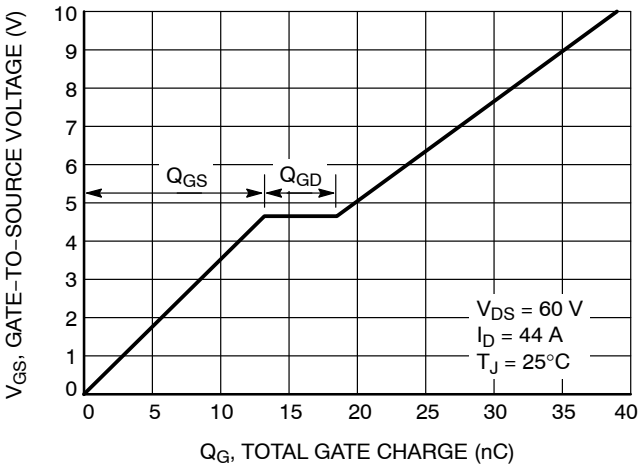



**Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge**

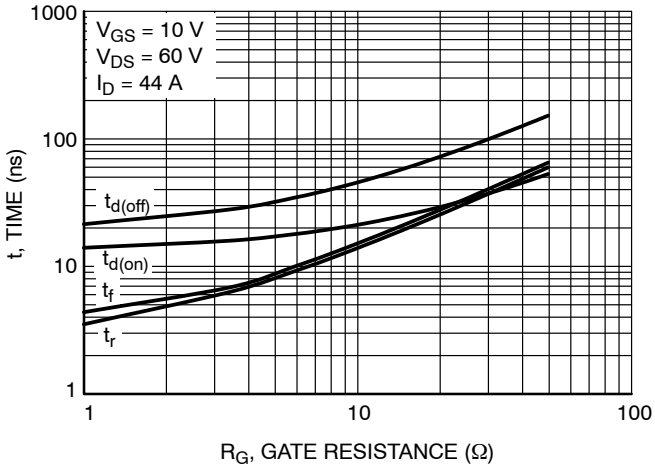



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

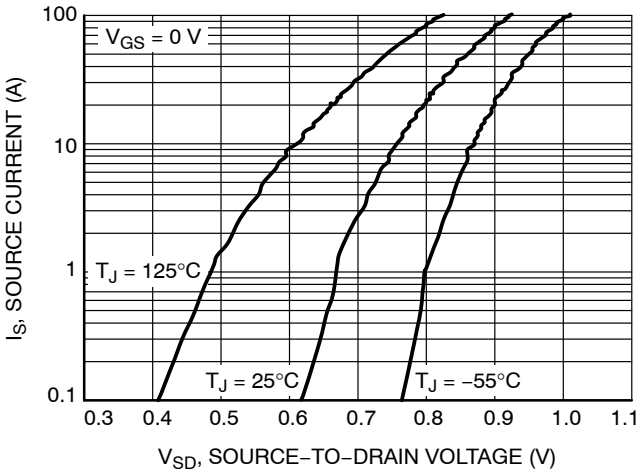



**Figure 10. Diode Forward Voltage vs. Current**

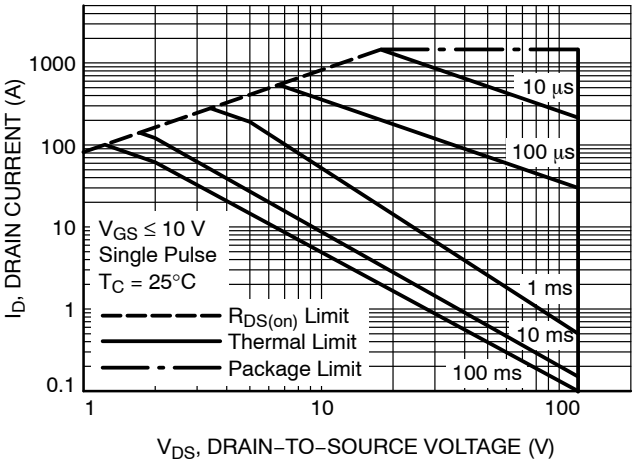



**Figure 11. Safe Operating Area**

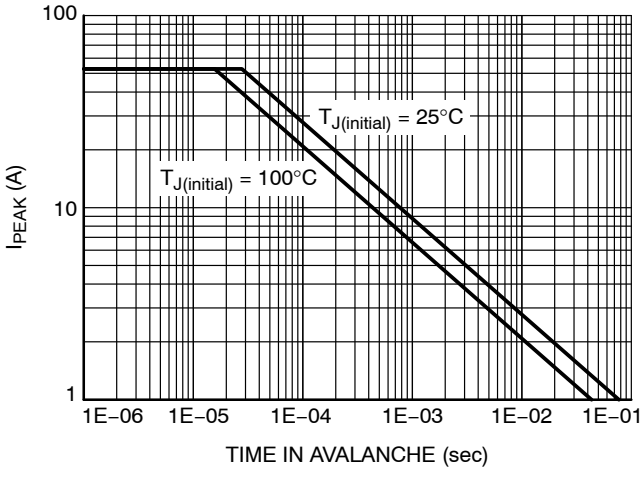



**Figure 12. $I_{PEAK}$ vs. Time in Avalanche**

## TYPICAL CHARACTERISTICS

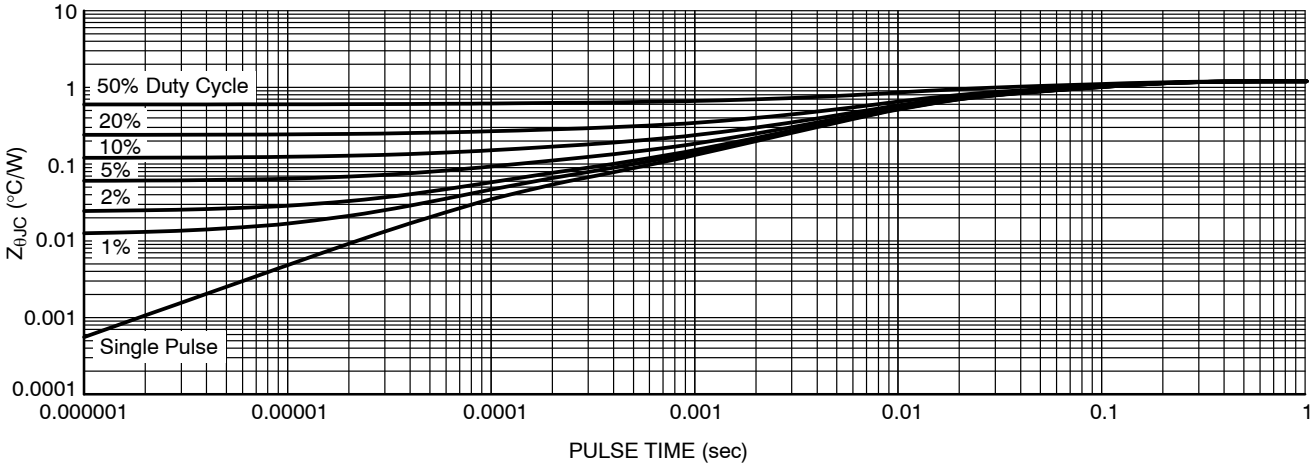


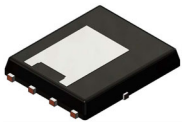

**Figure 13. Thermal Characteristics**

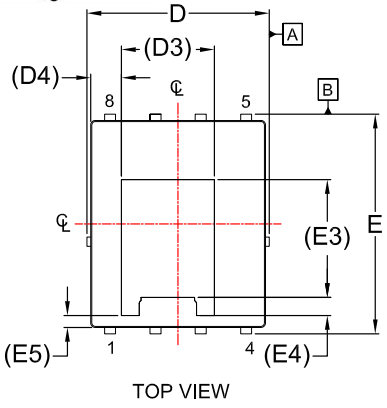
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

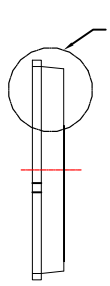
**DFN8 5x6.15, 1.27P, DUAL COOL**
CASE 506EG
ISSUE D

DATE 25 AUG 2020

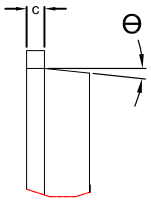





TOP VIEW



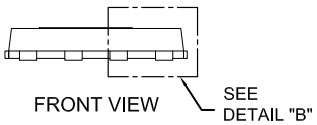

SIDE VIEW



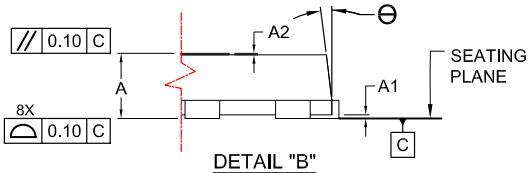

DETAIL "A"
SCALE: 2:1

NOTES:

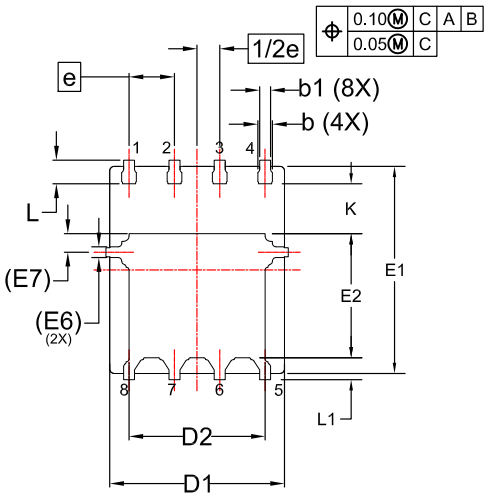
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



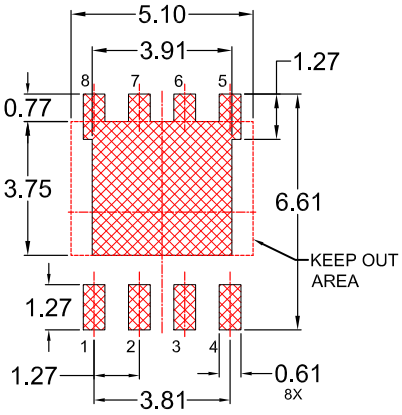

FRONT VIEW




DETAIL "B"
SCALE: 2:1




BOTTOM VIEW

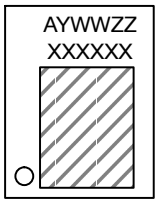



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.85 | 0.90 | 0.95 |
| A1 | - | - | 0.05 |
| A2 | - | - | 0.05 |
| b | 0.31 | 0.41 | 0.51 |
| b1 | 0.21 | 0.31 | 0.41 |
| c | 0.20 | 0.25 | 0.30 |
| D | 4.90 | 5.00 | 5.10 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.67 | 3.82 | 3.97 |
| D3 | 2.60 REF | | |
| D4 | 0.86 REF | | |
| E | 6.05 | 6.15 | 6.25 |
| E1 | 5.70 | 5.80 | 5.90 |
| E2 | 3.38 | 3.48 | 3.58 |
| E3 | 3.30 REF | | |
| E4 | 0.50 REF | | |
| E5 | 0.34 REF | | |
| E6 | 0.30 REF | | |
| E7 | 0.52 REF | | |
| e | 1.27 BSC | | |
| 1/2e | 0.635 BSC | | |
| K | 1.30 | 1.40 | 1.50 |
| L | 0.56 | 0.66 | 0.76 |
| L1 | 0.52 | 0.62 | 0.72 |
| Θ | 0° | --- | 12° |

**GENERIC MARKING DIAGRAM***




XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON84257G** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **DFN8 5x6.15, 1.27P, DUAL COOL** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales