# Ultra-Broadband Differential Silicon Capacitor Pair UBDC 0402M 2x10nF BV11

Rev. 3.01

## General description

UBDC Ultra-Broadband Differential silicon Capacitor pair targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.

The UBDC is suitable for DC blocking and AC coupling applications in all broadband optoelectronics and High-speed data system.

The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive Solutions, offers unique performances with low insertion loss, low reflection and phase stability from 160 kHz to 60 GHz+.

These Ultra-Broadband MOS Silicon Differential Capacitors pairs (UBDC) in silicon have been developed in a semiconductor process, in order to combine ultra-deep trench MOS capacitors for high capacitance value of **min 10nF** (for kHz–MHz range) and high frequency MIM capacitors for low capacitance value for GHz range), both in a SMT 0402 [1.00 x 0.50 mm].

The UBDC capacitor pair provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability.

UBDC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature.

## Key features

- Ultra-Broadband performance up to 67 GHz
- Resonance free & phase stability
- 100Ω differential characteristic impedance
- Differential insertion loss < 0.9dB up to 60GHz
- Differential return loss > 12dB(*)
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/K (-55 °C to +150 °C)
  - Voltage <-0.1%/Volt
  - Negligible capacitance loss through ageing
- Low profile: 140µm including bump height
- Break down voltage: 11V
- Low leakage current < 100pA
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- SAC305 40µm bumps after reflow

## Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- Volume limited applications
- Broadband test equipment

(*) in 100Ω differential impedance Microstrip

## Functional diagram

The next figure provides implementation set-up of the differential capacitor pair (4 connections).

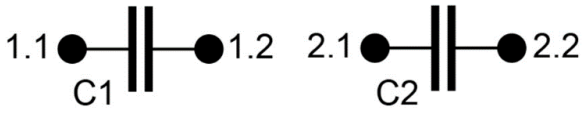



*Figure 1: Electrical diagram*

## Electrical performances

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| C | Capacitance value | @+25°C | 10 | 11.8 | 13.6 | nF |
| $\Delta C_P$ | Capacitance tolerance (1) | @+25°C | -15 | - | +15 | % |
| $T_{OP}$ | Operating temperature | | -55 | - | 150 | °C |
| $T_{STG}$ | Storage temperature (2) | | -70 | - | 165 | °C |
| $\Delta C_T$ | Capacitance temperature variation | -55 °C to 150 °C | - | 70 | - | ppm/K |
| $RV_{DC}$ | Rated voltage (3) | | - | - | 3.8(4)<br>3.4(5) | $V_{DC}$ |
| BV | Break down voltage | @+25°C | 11 | - | - | V |
| $\Delta C_{RVDC}$ | Capacitance voltage variation | From 0 V to $RV_{DC}$, @+25°C | - | - | -0.1 | %/$V_{DC}$ |
| IR | Insulation resistor | @$RV_{DC}$, +25°C, 120s | - | 10 | - | GΩ |
| Fc-3dB | Cut-off frequency at 3dB | @+25°C | - | 135 | 160 | kHz |
| Diff | Diff. characteristic impedance | @+25°C | - | 100 | - | Ω |
| IL | Differential insertion loss (100Ω)(6) (Microstrip) | @ 20 GHz, @+25°C | - | 0.2 | - | dB |
| | | @ 40 GHz, @+25°C | - | 0.5 | - | dB |
| | | @ 60 GHz, @+25°C | - | 1 | - | dB |
| | Differential return loss (100Ω) (Coplanar) | @ 20 GHz, @+25°C | - | 0.6 | - | dB |
| | | @ 40 GHz, @+25°C | - | 0.8 | - | dB |
| | | @ 50 GHz, @+25°C | - | 1 | - | dB |
| RL | Differential return loss (100Ω)(6) (Microstrip) | Up to 60 GHz, @+25°C | - | 12 | - | dB |
| | Differential return loss (100Ω) (Coplanar) | Up to 50 GHz, @+25°C | - | 12 | - | dB |
| ESD | HBM stress (7) | JS-001-2017 | 2 | - | - | kV |

*Table 1 - Electrical performances*

(1): Other tolerance available upon request
(2): Without packaging
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
(4): 10 years of intrinsic lifetime prediction at 100°C continuous operation
(5): 10 years of intrinsic lifetime prediction at 150°C continuous operation
(6): Simulated based on correlations between simulations and measurement results performed in coplanar mode
(7): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

## Simulation results of 2x10nF UBDC in transmission mode on microstrip transmission line

### Module S-parameters

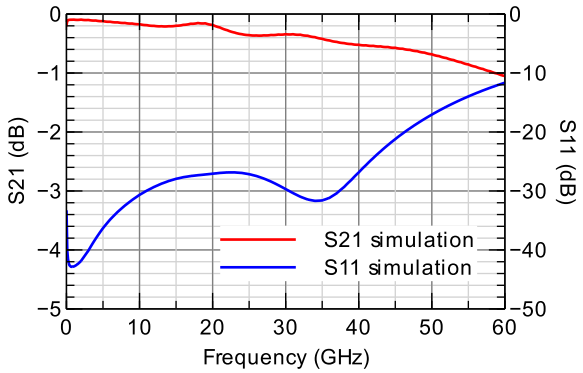



*Figure 2 - 2x10nF UBDC simulation results (100Ω differential)*

### Test bench

**4-mils (101µm) Rogers RO4350B**
Nominal Pad dimensions – pad length = 0.150 mm, pad width and line width = 0.150 mm, pad gap = 0.100 mm
100 Ohm differential – 18µm Cu thickness – full GND plane

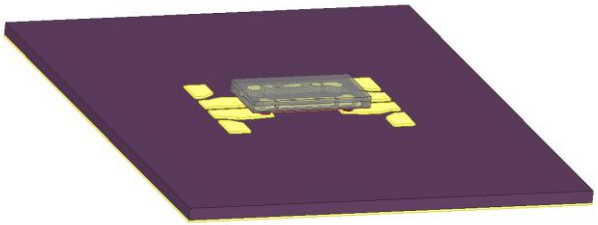


*Figure 3 - Microstrip simulation board*

## Simulation and Measurements results correlation of 2x10nF UBDC in transmission mode on coplanar transmission line

### Module S-parameters

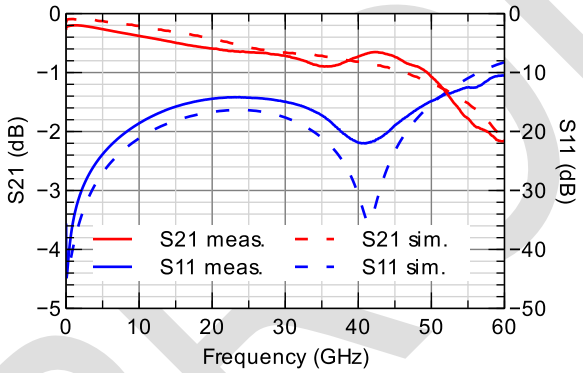
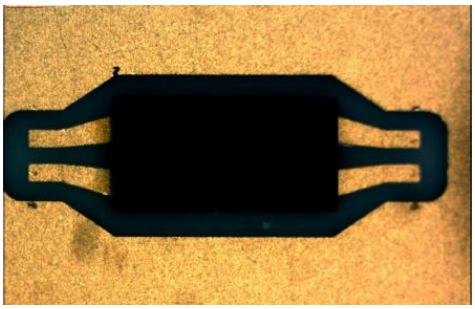



*Figure 4 - 2x10nF UBDC measurement results (100Ω differential)*

### Test bench

**25-mils (635µm) alumina**
1-3µm Au thickness
Measured with GSSG probes and 4-ports VNA



FREE S-Parameters-Based Linear Simulation Models for ADS

http://www.modelithics.com/mvpmurata.asp

*Figure 5 - 2x10nF UBDC soldered on its test board*

## 4x50Ω single ports to 2x100 Ω differential ports transposition (measurement and simulation)

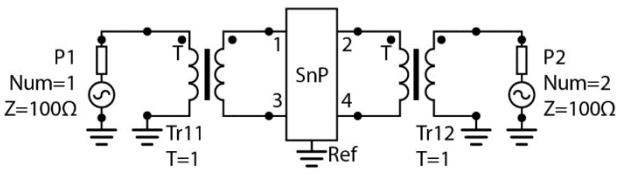



*Figure 6 - singe-to-differential transposition*

## Pinning definition

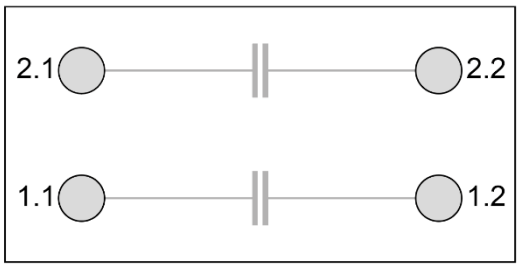



*Figure 7 Pinning definition*

| pin # | Symbol | Coordinates X / Y [µm] |
|---|---|---|
| 1.1 | Signal1 | -350.0 / -125.0 |
| 1.2 | Signal1 | 350.0 / -125.0 |
| 2.1 | Signal2 | -350.0 / 125.0 |
| 2.2 | Signal2 | 350.0 / 125.0 |

*Table 2 - Pining description. Reference (0,0) located at the centre of the die.*

## Ordering Information

Murata Integrated Passive Devices delivers products with AQL level II (0.65). Tighter quality levels are available upon request.

| Part number | Package | | |
|---|---|---|---|
| | Packaging | Finishing | Description |
| 939301421510-F1S | 6” film frame carrier(1) | SAC(2) | UBDC402M – 2x10nF – 4 pads – 1mm x 0.5mm x 0.10 mm (4) |
| 939301421510-T3S | 7’’ T&R with 1Kpieces / reel(3) | SAC(2) | UBDC402M – 2x10nF – 4 pads – 1mm x 0.5mm x 0.10 mm (4) |

*Table 3 - Packaging and ordering information*

(1) Other film frame carrier are possible on request
(2) ENIG + SAC305 type 6
(3) missing capacitors can reach 0.5%
(4) Refer to Figure9.

| Product Name | Die Name | Description |
|---|---|---|
| UBDC421.510 | XCA1D510 | UBDC 2x10nF/0402M/BV11 – 4 pads – 1 x 0.5 x 0.10 mm |

*Table 4 - Die information*

## Pad Metallization

This surface mounted Silicon Capacitor is delivered as standard with SAC305 type 6 bumping (Refer to Figure6). Other Metallization, such as ENIG (0.1µm Au / 5µm Ni) (Refer to Figure7), Copper, Thick Gold or Aluminium pads are possible on request.
UBDC series is compatible with standard reflow process.

It is recommended to design mirror pads on the PCB.

Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

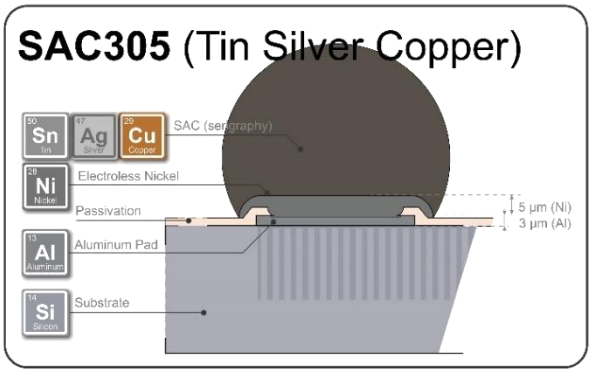



*Figure 8 – Top electrode description of SAC305 pre-bumped version*

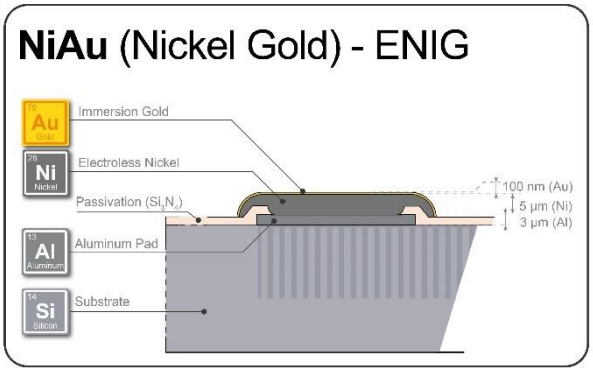



*Figure 9 – Top electrode description of ENIG finishing version*

## Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

## Package outline

The product is delivered as a bare silicon die.

*Figure 10 - Micro photography of Capacitor*

| L (mm) | W (mm) | T (mm) | c (mm) | P (mm) | e (mm) | t (mm) |
|---|---|---|---|---|---|---|
| 1.00 ±0.02 | 0.50 ±0.02 | 0.10 ±0.015 | 0.09 | 0.70 | 0.25 | 0.04(1)<br>0.05(2) |

(1) Solder joint height after reflow on board.
(2) Solder bump height before assembly

*Table 5 - Dimensions and tolerances*

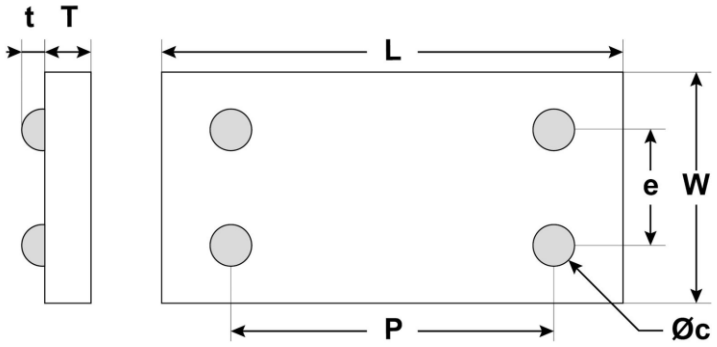



*Figure 11 - Package outline Capacitor*

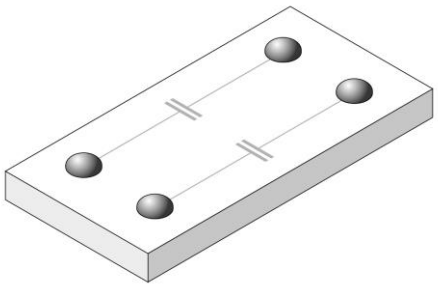


*Figure 12 - Package isometric view*

## Assembly

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

*Figure 13 Scan this QR Code to access the Murata Silicon Capacitor web page*

## Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

**Tape and Reel:**

Dies are flipped in the tape cavity (bump down) with die ID located near the driving holes of the tape.

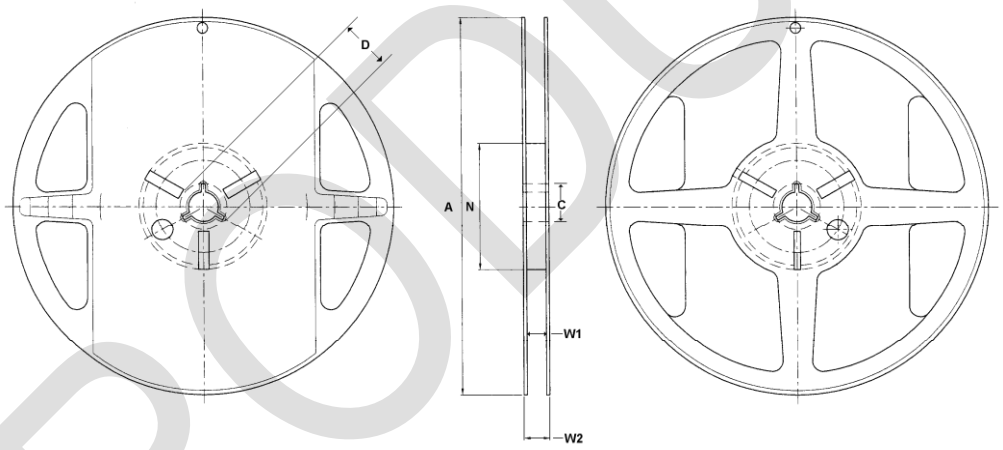



*Figure 14 - Reel drawing*

| Tape Width | Diameter A | C | D | Hub N | W1 | W2 |
|---|---|---|---|---|---|---|
| 8 | 178 (7 inches) | 13.5 | 20.2 | 60 | 9.3 | 11.5 |

*Table 6 – Reel dimensions (mm)*

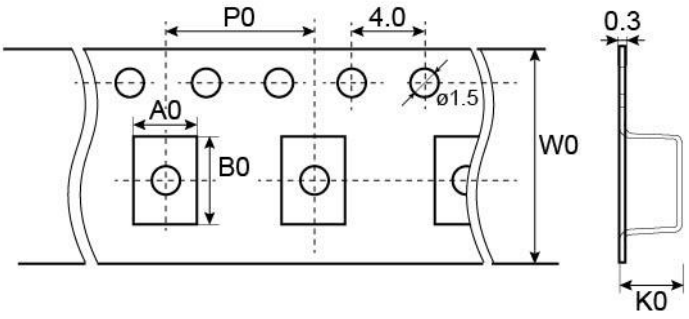



*Figure 15 - Tape drawing*

| Cavity dimensions | | | Carrier tape width W0 | Carrier tape pitch P0 | Reel Capacity |
|---|---|---|---|---|---|
| Ao | Bo | Ko | | | |
| 0.59 | 1.09 | 0.20 | 8 | 4 | 1000 |

*Table 7 - Tape dimensions (mm)*

**Film frame carrier:**

With UV curable dicing tape (UV performed).

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

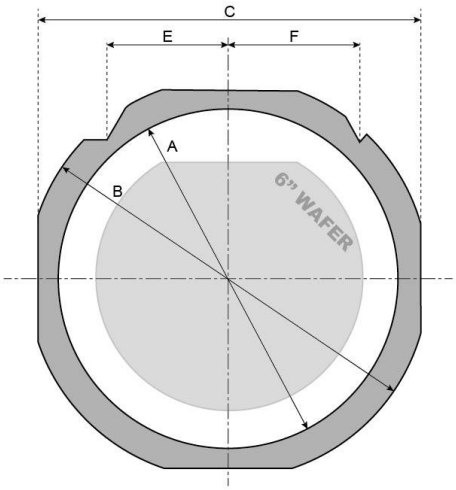



*Figure 16 FF070 Frame with a 6" wafer*

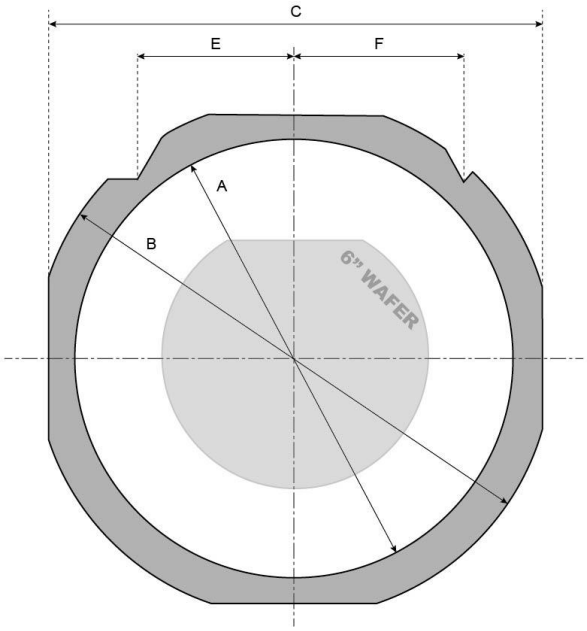



*Figure 17 FF108 Frame with a 6" wafer*

| Frame Reference | Frame Style | Inside diameter A | Outside diameter B | Width C | Thickness | Pin location E | Pin location F |
|---|---|---|---|---|---|---|---|
| FF070 (1) | DTF-2-6-1 | 7.638” | 8.976” | 8.346” | 0.048’’ | 2.370” | 2.5’’ |
| FF108 (1) | DTF-2-8-1 | 9.842” | 11.653” | 10.866” | 0.048” | 2.381” | 2.5’’ |

*Table 8 - Frame dimensions (inches)*

(1) or equivalent

## Definitions

Data sheet status

**Objective specification:** This data sheet contains target or goal specifications for product development.

**Preliminary specification:** This data sheet contains preliminary data; supplementary data may be published later.

**Product specification:** This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

## Revision history

| Revision | Date | Description | Author |
|---|---|---|---|
| Release 1.00 | 2017 Sept. 15th | Objective specification | OGA + SBO |
| Release 1.09 | 2020 April 20th | General update | OGA |
| Release 1.10 | 2021 Jan 15th | Drawings and template update | OGA+DDE+LLE+ SCA+CGU |
| Release 2.00 | 2021 April 23rd | New template and drawings. Preliminary status Update graphs | SCA+OGA+LLR |
| Release 2.01 | 2021 June 25th | Minor update | SCA+OGA+LLR |
| Release 3.01 | 2023 May 25th | Finishing cross section added | SCA+OGA+LLR |

## Disclaimer / Life support applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.



www.murata.com
mis@murata.com