Power Management IC for Automotive Application

Data Sheet

ADP5140

FEATURES

- Buck regulators
  - BUCK1, 2.5 A maximum continuous output current range with DVS
  - BUCK2, 2.5 A maximum continuous output current range with adjustable output voltage
  - BUCK3, 3 A maximum continuous output current range with adjustable output voltage
  - BUCK4, 3 A maximum continuous output current range with low noise output
- Boost regulator: fixed 5 V output, 400 mA output current range
- Seven LDO regulators with low noise output
  - LDO1: 300 mA
  - LDO2: 2.3 A
  - LDO3: 1.4 A
  - LDO4: 1.2 A
  - LDO5: 500 mA
  - LDO6: 50 mA
  - LDO7: 400 mA
- 2.2 MHz (typical) switching frequency
- Synchronization input or output
- Out of phase between buck regulators
- Integrated soft start and compensation for all regulators
- Overcurrent and thermal protection for all power rails
- 2 window voltage monitors
- 2 window watchdogs with pulse detection
- One QA watchdog
- Wake-up input
- SPI for control and diagnostics
- $\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, and $\overline{\text{STATUS}}$ outputs
- 56-terminal LGA
- AEC-Q100 qualified for automotive applications

APPLICATIONS

- Advanced driver assistance (ADAS)
- Automotive electronics
- Infotainment system
- Industrial and instrumentation

GENERAL DESCRIPTION

The ADP5140 integrates four high performance, synchronous, step-down buck regulators (BUCK1 to BUCK4), one boost regulator, and seven low noise, low dropout (LDO) regulators (LDO1 to LDO7). The buck regulators support input voltages from 2.7 V to 5.5 V and provide output currents from 2.5 A to 3 A. The boost regulator provides a fixed 5 V output and provides a 400 mA load current. The seven LDOs provide a clean output voltage for the system. LDO5 provides an ultralow noise output that can be used to power noise sensitive loads.

The ADP5140 runs in a fixed 2.2 MHz switching frequency (f_{SW}) or can synchronize to an external clock from its 1.9 MHz to 2.4 MHz synchronization range, which is outside of the amplitude modulation (AM) band. The four buck regulators run at 90° out of phase to reduce the input ripple current and the input capacitor size, which lowers the system electromagnetic interference (EMI).

All regulators integrate internal compensation to simplify the design. The internal soft start circuitry and power-up sequencing reduce the input inrush current.

Each voltage rail is monitored internally and any fault event is reported to the system through the $\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, and $\overline{\text{STATUS}}$ pins. Two window watchdogs (WD0 and WD1) and one question answer (QA) watchdog monitor the processor or other devices in the system to ensure that any software or hardware errors are detected. The ADP5140 integrates a serial peripheral interface (SPI) for system control and diagnostics.

Additional protection includes current-limit protection, overvoltage protection, undervoltage protection, and thermal shutdown (TSD).

The ADP5140 operates over a junction temperature range of −40°C to +150°C and is available in a 56-terminal, land grid array (LGA).

Rev. 0
Document Feedback

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REVISION HISTORY

8/2022—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

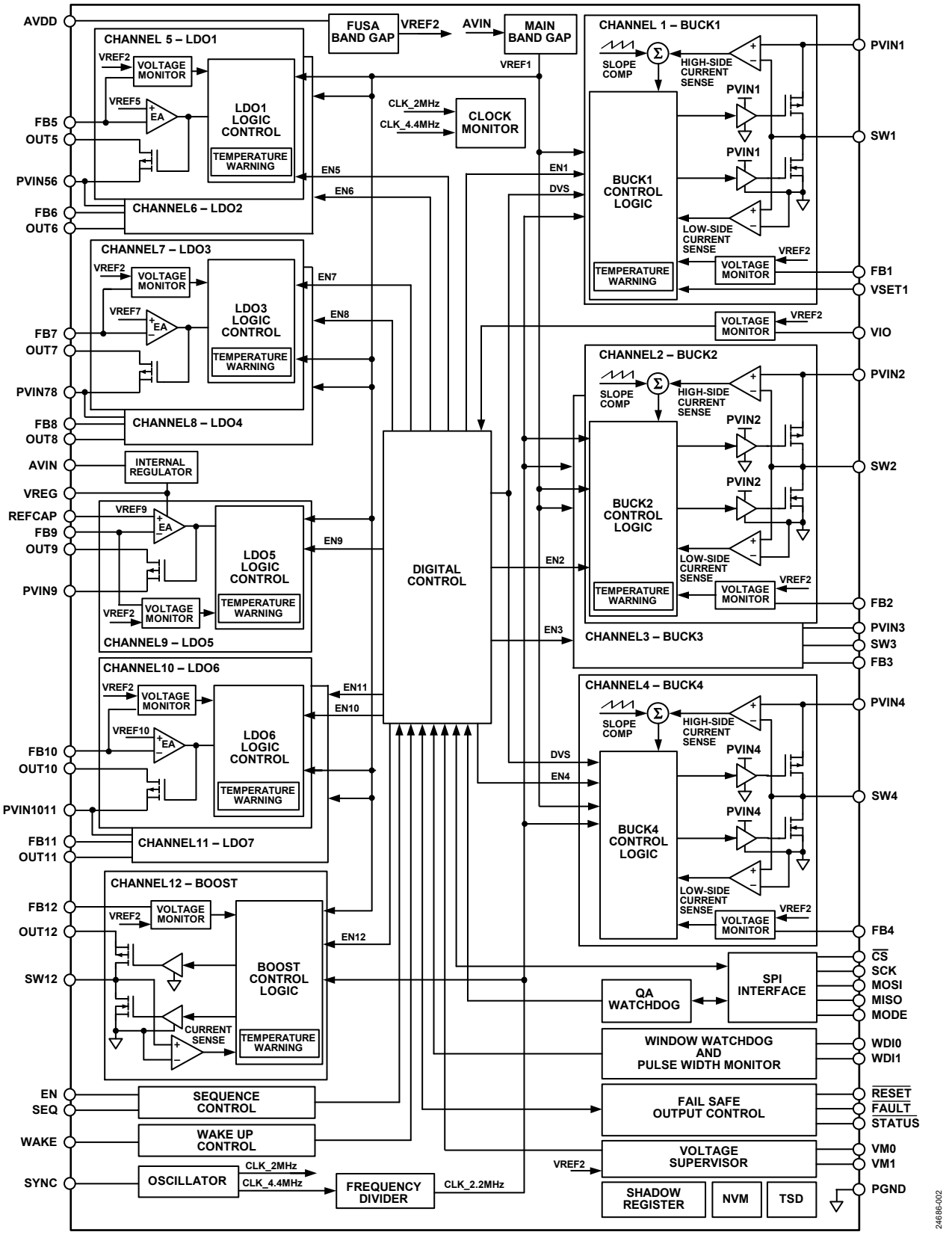

Figure 1.

TYPICAL APPLICATION CIRCUIT

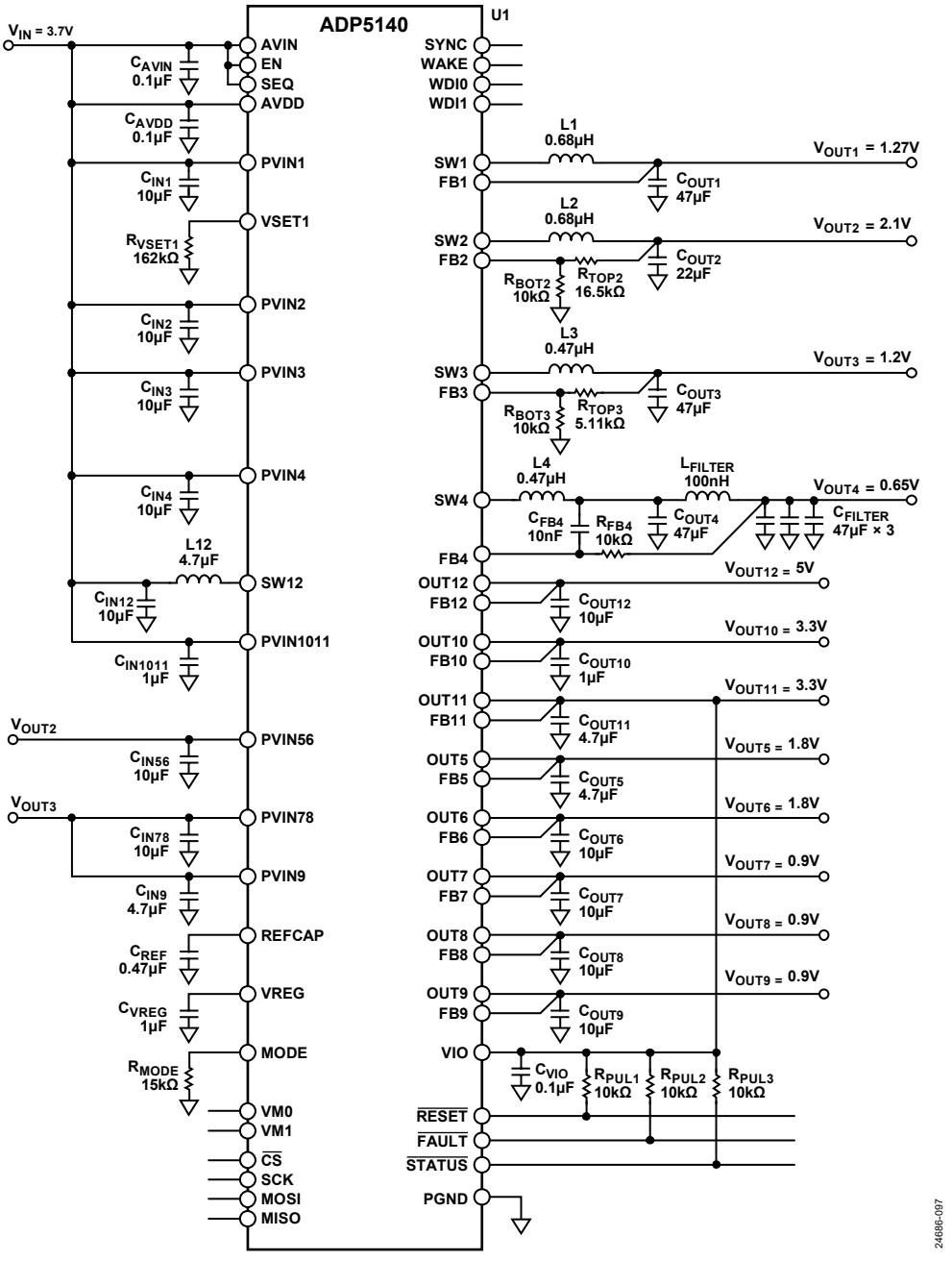

Figure 2.

SPECIFICATIONS

AVIN voltage (V_{AVIN}) = AVDD voltage (V_{AVDD}) = 3.7 V, VIO voltage (V_{IO}) = 3.3 V, T_J = −40°C to +150°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER INPUT						
AVIN Voltage Range	V_{AVIN}	AVIN pin	2.7		5.5	V
AVDD Voltage Range	V_{AVDD}	AVDD pin	2.7		5.5	V
Quiescent Current	$I_{Q\_AVIN\_AVDD}$	No switching, the AVIN pin and AVDD pin are connected together	9.5	12	16.5	mA
	I_{Q_IO}	VIO = 3.3 V	4	6.6	10	µA
Input Undervoltage Lockout (UVLO) Threshold						
AVIN UVLO Rising	$V_{AVIN\_UVLO\_R}$			2.5	2.6	V
AVIN UVLO Falling	$V_{AVIN\_UVLO\_F}$		2.3	2.4		V
AVDD UVLO Rising	$V_{AVDD\_UVLO\_R}$			2.5	2.6	V
AVDD UVLO Falling	$V_{AVDD\_UVLO\_F}$		2.3	2.4		V
ENABLE (EN)						
First Stage High Threshold	V_{EN_RGH}			0.76	1.1	V
Second Stage Rising Threshold	V_{EN_R}			1.2	1.28	V
Second Stage Falling Threshold	V_{EN_F}		1.02	1.1		V
EN Pull-Down Resistance				1.3		MΩ
INPUT/OUTPUT VOLTAGE SUPPLY (VIO)	V_{VIO}					
VIO UVLO Falling Threshold	$V_{IO\_UV\_F}$	V_{VIO} = 1.8 V	1.62	1.67		V
		V_{VIO} = 3.3 V	2.95	3.05		V
VIO UVLO Rising Threshold	$V_{IO\_UV\_R}$	V_{VIO} = 1.8 V		1.71	1.75	V
		V_{VIO} = 3.3 V		3.1	3.17	V
VIO UVLO Deglitch Time			10		20	µs
WAKE-UP INPUT (WAKE)						
High Voltage Threshold			1.2			V
Low Voltage Threshold					0.4	V
Deglitch Time	t_{D_WAKE}			15		µs
Internal Pull-Down Resistance				1		MΩ
SYNCHRONIZATION (SYNC)						
SYNC Input		SYNC is configured as an input				
Synchronization Range			1.9		2.4	MHz
Minimum On Pulse Width			80			ns
Minimum Off Pulse Width			80			ns
High Voltage Threshold			0.7 × V_{VIO}			V
Low Voltage Threshold					0.3 × V_{VIO}	V
SYNC Output		SYNC is configured as an output				
Frequency on SYNC Pin		SYNC_DIV = 0		f_{SW}		
		SYNC_DIV = 1		f_{SW}/5		
High Voltage Threshold		Sync source current (I_{SYNC_SOURCE}) = 2 mA	V_{VIO} − 0.2			V
Low Voltage Threshold		Sync sink current (I_{SYNC_SINK}) = 2 mA			0.4	V
Duty				50		%
FB1 TO FB3 VOLTAGE MONITORING		BUCK1, BUCK2, and BUCK3, warning and fault				
High Threshold						
Accuracy, 4% Window			102.8	104	105.2	%
Hysteresis, 4% Window				0.5		%
Accuracy, 5% Window			103.95	105.15	106.35	%

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Hysteresis, 5% Window				0.8		%
Accuracy, 6% Window			105.1	106.3	107.5	%
Hysteresis, 6% Window				0.9		%
Accuracy, 8% Window			107.1	108.3	109.5	%
Hysteresis, 8% Window				0.9		%
Low Threshold Accuracy						
Accuracy, 4% Window			95.1	96.3	97.5	%
Hysteresis, 4% Window				1		%
Accuracy, 5% Window			94.15	95.35	96.55	%
Hysteresis, 5% Window				1		%
Accuracy, 6% Window			93.05	94.25	95.45	%
Hysteresis, 6% Window				1		%
Accuracy, 8% Window			91.1	92.3	93.5	%
Hysteresis, 8% Window				1		%
FB4 VOLTAGE MONITORING		BUCK4, warning and fault				
High Threshold						
Accuracy, 4% Window			102.8	104	105.2	%
Hysteresis, 4% Window				0.35		%
Accuracy, 5% Window			104	105.2	106.4	%
Hysteresis, 5% Window				0.7		%
Accuracy, 6% Window			104.9	106.1	107.3	%
Hysteresis, 6% Window				0.5		%
Accuracy, 8% Window			107	108.2	109.4	%
Hysteresis, 8% Window				0.7		%
Low Threshold Accuracy						
Accuracy, 4% Window			95.1	96.3	97.5	%
Hysteresis, 4% Window				1		%
Accuracy, 5% Window			94.3	95.5	96.7	%
Hysteresis, 5% Window				1		%
Accuracy, 6% Window			93.15	94.35	95.55	%
Hysteresis, 6% Window				1		%
Accuracy, 8% Window			91.2	92.4	93.6	%
Hysteresis, 8% Window				1		%
FB5 TO FB11 VOLTAGE MONITORING		LDO1 to LDO7, warning and fault				
High Threshold						
Accuracy, 4% Window			103.1	104.3	105.5	%
Hysteresis, 4% Window				0.9		%
Accuracy, 5% Window			104.15	105.35	106.55	%
Hysteresis, 5% Window				1.15		%
Accuracy, 6% Window			105.3	106.5	107.7	%
Hysteresis, 6% Window				1.15		%
Accuracy, 8% Window			107.15	108.35	109.55	%
Hysteresis, 8% Window				1		%
Low Threshold Accuracy						
Accuracy, 4% Window			95	96.2	97.4	%
Hysteresis, 4% Window				1.2		%
Accuracy, 5% Window			94.15	95.35	96.55	%
Hysteresis, 5% Window				1		%
Accuracy, 6% Window			93	94.2	95.4	%
Hysteresis, 6% Window				1.15		%
Accuracy, 8% Window			91.05	92.25	93.45	%
Hysteresis, 8% Window				1.1		%

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FB12 VOLTAGE MONITORING		Boost, warning and fault				
High Threshold						
Accuracy, 4% Window			103.1	104.3	105.5	%
Hysteresis, 4% Window				0.9		%
Accuracy, 5% Window			104.2	105.4	106.6	%
Hysteresis, 5% Window				1.2		%
Accuracy, 6% Window			105.3	106.5	107.7	%
Hysteresis, 6% Window				1.2		%
Accuracy, 8% Window			107.2	108.4	109.6	%
Hysteresis, 8% Window				1		%
Low Threshold Accuracy						
Accuracy, 4% Window			95	96.2	97.4	%
Hysteresis, 4% Window				1.2		%
Accuracy, 5% Window			94.15	95.35	96.55	%
Hysteresis, 5% Window				1		%
Accuracy, 6% Window			93.05	94.25	95.45	%
Hysteresis, 6% Window				1.1		%
Accuracy, 8% Window			91.05	92.25	93.45	%
Hysteresis, 8% Window				1.1		%
VM0 AND VM1 VOLTAGE MONITORING		VM0 and VM1, warning and fault				
High Threshold		Reference to 600 mV				
Accuracy, 4% Window			103.15	104.35	105.55	%
Hysteresis, 4% Window				0.8		%
Accuracy, 5% Window			104.25	105.45	106.65	%
Hysteresis, 5% Window				1.1		%
Accuracy, 6% Window			105.4	106.6	107.8	%
Hysteresis, 6% Window				1.1		%
Accuracy, 8% Window			107.25	108.45	109.65	%
Hysteresis, 8% Window				1		%
Low Threshold Accuracy		Reference to 600 mV				
Accuracy, 4% Window			95.2	96.4	97.6	%
Hysteresis, 4% Window				1.1		%
Accuracy, 5% Window			94.3	95.5	96.7	%
Hysteresis, 5% Window				0.9		%
Accuracy, 6% Window			93.15	94.35	95.55	%
Hysteresis, 6% Window				1.1		%
Accuracy, 8% Window			91.25	92.45	93.65	%
Hysteresis, 8% Window				1.05		%
VOLTAGE MONITOR BLANK TIME						
Blank Time Range		SPI programmable range	16		352	µs
Blank Time Accuracy			−10		+10	%
DIE TEMPERATURE AND TSD						
TSD Threshold	T_{SD}			170		°C
TSD Hysteresis	T_{SD_HY}			20		°C
TSD Deglitch Time				10		µs
WDI WINDOW WATCHDOG AND PULSE MONITOR						
Watchdog Fast Window Time	t_{WD0_FAST}	Default for WD0	27	30	33	ms
	t_{WD1_FAST}	Default for WD1	27	30	33	ms
		SPI programmable time range	0		134.2	sec
Watchdog Slow Window Time	t_{WD0_SLOW}	Default for WD0	108	120	132	ms
	t_{WD1_SLOW}	Default for WD1	108	120	132	ms
		SPI programmable time range	0		134.2	sec

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
WDI Fast Pulse Width	$t_{WDI0\_PULSE\_FAST}$	Default for WDI0	383	425	468	µs
	$t_{WDI1\_PULSE\_FAST}$	Default for WDI1	383	425	468	µs
		SPI programmable time range	0		131	ms
		SPI programmable time step		0.5		µs
WDI Slow Pulse Width	$t_{WDI0\_PULSE\_SLOW}$	Default for WDI0	518	575	633	µs
	$t_{WDI1\_PULSE\_SLOW}$	Default for WDI1	518	575	633	µs
		SPI programmable time range	0		131	ms
		SPI programmable time step		0.5		µs
WDIx High Voltage Threshold			1.2			V
WDIx Low Voltage Threshold					0.4	V
WDIx Minimum Pulse Width			1			µs
QA WATCHDOG						
QA Watchdog Fast Window Time	$t_{WD\_QA\_FAST}$	Default for QA watchdog		0		ms
		SPI programmable time range	0		134.2	sec
QA Watchdog Slow Window Time	$t_{WD\_QA\_SLOW}$	Default for QA watchdog	0.9	1	1.1	sec
		SPI programmable time range	0		134.2	sec
$\overline{\text{RESET}}$		$\overline{\text{RESET}}$ pin				
$\overline{\text{RESET}}$ Hold Low Time	t_{HOLD}	After POR or from standby mode	6.3	7	7.7	ms
$\overline{\text{RESET}}$ Timeout Period	t_{RP}		3.6	4	4.4	ms
$\overline{\text{RESET}}$ Output Low Voltage		Sink current on the $\overline{\text{RESET}}$ pin (I_{RESET}) = 1 mA		30	100	mV
$\overline{\text{RESET}}$ Leakage Current		Voltage on the $\overline{\text{RESET}}$ pin (V_{RESET}) = 3.3 V			1	µA
$\overline{\text{RESET}}$ Input High Voltage Threshold			0.7 × V_{VIO}			V
$\overline{\text{RESET}}$ Input Low Voltage Threshold					0.3 × V_{VIO}	V
$\overline{\text{RESET}}$ Input Read Blank Time				3		µs
$\overline{\text{RESET}}$ External Timeout	t_{RESET_EXT}	SPI programmable range	5		160	µs
		SPI programmable step		5		µs
$\overline{\text{STATUS}}$		$\overline{\text{STATUS}}$ pin				
$\overline{\text{STATUS}}$ Output Low Voltage		Sink current on the $\overline{\text{STATUS}}$ pin (I_{STATUS}) = 1 mA		30	100	mV
$\overline{\text{STATUS}}$ Leakage Current		Voltage on the $\overline{\text{STATUS}}$ pin (V_{STATUS}) = 3.3 V			1	µA
$\overline{\text{STATUS}}$ Input High Voltage Threshold				1.2	1.28	V
$\overline{\text{STATUS}}$ Input Low Voltage Threshold			1.02	1.1		V
$\overline{\text{STATUS}}$ Input Read Blank Time				3		µs
$\overline{\text{STATUS}}$ External Timeout	t_{STATUS_EXT}	SPI programmable range	5		160	µs
		SPI programmable step		5		µs
$\overline{\text{FAULT}}$		$\overline{\text{FAULT}}$ pin				
$\overline{\text{FAULT}}$ Output Low Voltage		Sink current on the $\overline{\text{FAULT}}$ pin (I_{FAULT}) = 1 mA		30	100	mV
$\overline{\text{FAULT}}$ Leakage Current		Voltage on the $\overline{\text{FAULT}}$ pin (V_{FAULT}) = 3.3 V			1	µA
$\overline{\text{FAULT}}$ Input High Voltage Threshold				1.2	1.28	V
$\overline{\text{FAULT}}$ Input Low Voltage Threshold			1.02	1.1		V
$\overline{\text{FAULT}}$ Input Read Blank Time				3		µs
$\overline{\text{FAULT}}$ External Timeout	t_{FAULT_EXT}	SPI programmable range	5		160	µs
		SPI programmable step		5		µs

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SEQ						
SEQ High Voltage Threshold				1.2	1.28	V
SEQ Low Voltage Threshold			1.02	1.1		V
SEQ Deglitch Time			10		20	µs
SEQ Pull-Down Resistance				1		MΩ
POWER-UP SEQUENCE						
Initial Delay	t_D			3		ms
Power-Up Delay 1	t_{DR1}			200		µs
Power-Up Delay 2	t_{DR2}			248		µs
POWER-DOWN SEQUENCE						
Power-Down Threshold	VM_{DW}	On FB11			1.8	V
TIMEOUT						
Self Check Timeout	t_{EXP1}			20		ms
System Ramp-Up Timeout	t_{EXP2}			20		ms
Peripheral Ramp-Up Timeout	t_{EXP3}			20		ms
SPI INTERFACE						
Input High Threshold		$\overline{CS}$, SCK, and MOSI	0.7 × V_{VIO}			V
Input Low Threshold		$\overline{CS}$, SCK, and MOSI			0.3 × V_{VIO}	V
MISO High Threshold		Source current on the MISO pin (I_{SOURCE}) = 4 mA	0.9 × V_{VIO}			V
MISO Low Threshold		Sink current on the MISO pin (I_{SINK}) = 4 mA			0.1 × V_{VIO}	V
Maximum SPI Clock Frequency	t_{SCK}	See Figure 3 and Figure 4			10	MHz
SCK Pulse Width High	t_{PWH}	See Figure 3	45			ns
SCK Pulse Width Low	t_{PWL}	See Figure 3	45			ns
$\overline{CS}$ Falling to SCK Falling Delay Time	t_{DCS}	See Figure 3	45			ns
SCK Rising to $\overline{CS}$ Rising Delay Time	t_{CSD}	See Figure 3	45			ns
$\overline{CS}$ High Time	t_{CSH}	See Figure 3	5			µs
Data Setup Time	t_{DS}	MOSI to SCK, see Figure 3	12.5			ns
Data Hold Time	t_{DH}	MOSI to SCK, see Figure 3	12.5			ns
Data Valid Time	t_{DV}	MISO to SCK, 80 pF load, see Figure 4			27.5	ns

TIMING DIAGRAMS

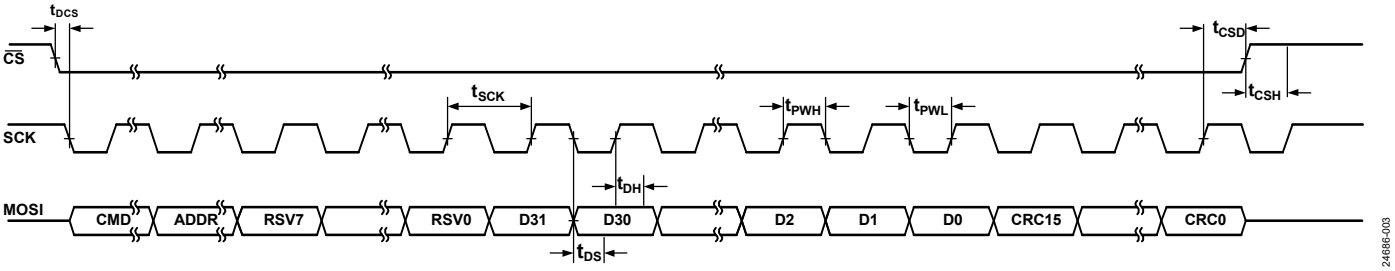

Figure 3. Timing Diagram for SPI Single Write

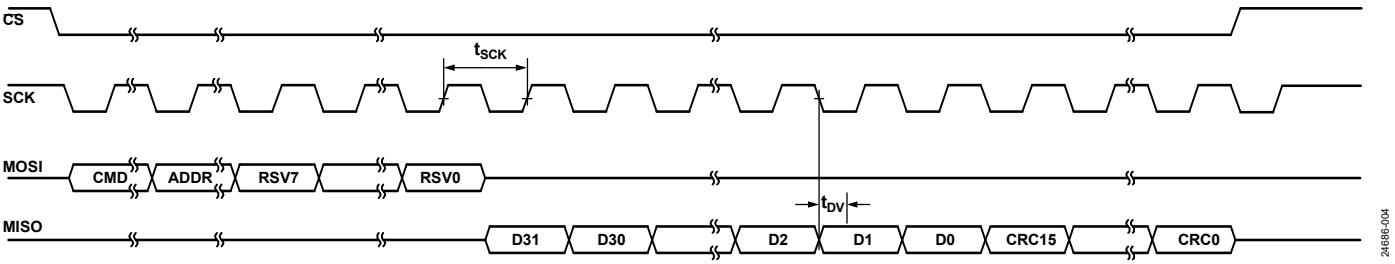

Figure 4. Timing Diagram for SPI Single Read

BUCK REGULATOR SPECIFICATIONS

V_{AVIN} = V_{AVDD} = PVIN1 voltage (V_{PVIN1}) = PVIN2 voltage (V_{PVIN2}) = PVIN3 voltage (V_{PVIN3}) = PVIN4 voltage (V_{PVIN4}) = 3.7 V, T_J = −40°C to +150°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
BUCK1 (REGULATOR 1)						
Input Voltage Range	V_{PVIN1}		2.7		5.5	V
Output Current Range	I_{OUT1}			2.5		A
Quiescent Current		The AVIN pin and PVIN1 pin are connected together		1.2		mA
Output Voltage Range	V_{OUT1}	External resistor setting or SPI selectable	0.8		1.4	V
Output Voltage Accuracy			−1.25		+1.25	%
High-Side On Resistance[1]	R_{DSON_HS1}			57	120	mΩ
Low-Side On Resistance[1]	R_{DSON_LS1}			27	80	mΩ
SW1 Minimum On Time				45	65	ns
SW1 Minimum Off Time				45		ns
High-Side Peak Current Limit			3.2	3.9	4.6	A
Low-Side Source Current Limit			2.7	3.4	4.1	A
Low-Side Sink Current Limit				−1		A
Switching Frequency	f_{SW}		2.0	2.2	2.4	MHz
Phase Shift		Reference to the internal clock		0		Degrees
Soft Start Time	t_{S1}			1		ms
Overtemperature Threshold				160		°C
Overtemperature Hysteresis				20		°C
Overtemperature Deglitch Time			30	35	40	µs
Discharge Resistance				110		Ω
BUCK2 (REGULATOR 2)						
Input Voltage Range	V_{PVIN2}		2.7		5.5	V
Output Current Range	I_{OUT2}			2.5		A
Quiescent Current		The AVIN pin and PVIN2 pin are connected together		1.2		mA
FB2 Regulation Voltage			0.790	0.800	0.810	V
High-Side On Resistance[1]	R_{DSON_HS2}			57	120	mΩ
Low-Side On Resistance[1]	R_{DSON_LS2}			27	80	mΩ
SW2 Minimum On Time				45	65	ns
SW2 Minimum Off Time				60		ns
High-Side Peak Current Limit			3.5	4.2	4.9	A
Low-Side Source Current Limit			3	3.7	4.4	A
Low-Side Sink Current Limit				−1		A
Switching Frequency	f_{SW}		2.0	2.2	2.4	MHz
Phase Shift		Reference to the internal clock		180		Degrees
Soft Start Time	t_{S2}			1		ms
Overtemperature Threshold				160		°C
Overtemperature Hysteresis				20		°C
Overtemperature Deglitch Time			30	35	40	µs
BUCK3 (REGULATOR 3)						
Input Voltage Range	V_{PVIN3}		2.7		5.5	V
Output Current Range	I_{OUT3}			3		A
Quiescent Current		The AVIN pin and PVIN3 pin are connected together		1.2		mA
FB3 Regulation Voltage			0.79	0.800	0.810	V
High-Side On Resistance[1]	R_{DSON_HS3}			57	120	mΩ
Low-Side On Resistance[1]	R_{DSON_LS3}			27	80	mΩ
SW3 Minimum On Time				45	65	ns
SW3 Minimum Off Time				45		ns
High-Side Peak Current Limit			3.9	4.6	5.3	A

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Low-Side Source Current Limit			3.5	4.3	5.1	A
Low-Side Sink Current Limit				−1		A
Switching Frequency	f_{SW}		2.0	2.2	2.4	MHz
Phase Shift		Reference to the internal clock		90		Degrees
Soft Start Time	t_{S3}			1		ms
Overtemperature Threshold				160		°C
Overtemperature Hysteresis				20		°C
Overtemperature Deglitch Time			30	35	40	µs
Discharge Resistance				110		Ω
BUCK4 (REGULATOR 4)						
Input Voltage Range	V_{PVIN4}		2.7		5.5	V
Output Current Range	I_{OUT4}			3		A
Quiescent Current		The AVIN pin and PVIN4 pin are connected together		1.6		mA
Output Voltage Range	V_{OUT4}	SPI selectable	0.55		1.20	V
Output Voltage Accuracy			−1.25		+1.25	%
High-Side On Resistance[1]	R_{DSON_HS4}			57	120	mΩ
Low-Side On Resistance[1]	R_{DSON_LS4}			27	80	mΩ
SW4 Minimum On Time				45	65	ns
SW4 Minimum Off Time				45		ns
High-Side Peak Current Limit			3.9	4.6	5.3	A
Low-Side Source Current Limit			3.5	4.3	5.1	A
Low-Side Sink Current Limit				−1		A
Switching Frequency	f_{SW}		2.0	2.2	2.4	MHz
Phase Shift		Reference to the internal clock		270		Degrees
Soft Start Time	t_{S4}			1		ms
Overtemperature Threshold				160		°C
Overtemperature Hysteresis				20		°C
Overtemperature Deglitch Time			30	35	40	µs
Discharge Resistance				110		Ω

[1] Pin to pin measurement.

BOOST REGULATOR SPECIFICATIONS

V_{AVIN} = V_{AVDD} = PVIN1 = PVIN2 voltage (V_{PVIN12}) = 3.7 V, T_J = −40°C to +150°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
BOOST REGULATOR						
Input Voltage Range	V_{PVIN12}	Input voltage of the boost power stage	2.7		4.1	V
Output Current Range	I_{OUT12}			400		mA
Output Voltage	V_{OUT12}			5		V
Output Voltage Accuracy			−2		+2	%
Quiescent Current	I_{Q12}			1.1		mA
Main Field Effect Transistor (FET) On Resistance[1]	R_{DSON_MAIN}			208	500	mΩ
Sync FET On Resistance[1]	R_{DSON_SYNC}			235	450	mΩ
Main FET Current Limit			0.8	1	1.2	A
Switching Frequency	f_{SW}		2.0	2.2	2.4	MHz
SW12 Minimum On Time				70		ns
SW12 Minimum Off Time				100		ns
Phase Shift		Reference to internal clock		0		Degree
Soft Start Time	t_{S12}			1		ms

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Overtemperature Threshold				160		°C
Overtemperature Hysteresis				20		°C
Overtemperature Deglitch Time			30	35	40	µs
Discharge Resistance				110		Ω

[1] Pin to pin measurement.

LDO1 (REGULATOR 5) SPECIFICATIONS

V_{AVIN} = V_{AVDD} = 3.7 V, V_{PVIN56} > output voltage for Regulator 5 (V_{OUT5}) + 0.3 V or V_{PVIN56} = 2.1 V (whichever is greater), PVIN56 input capacitance (C_{IN56}) = 10 µF, output capacitance for Regulator 5 (C_{OUT5}) = 4.7 µF, T_J = −40°C to +150°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LDO1 (REGULATOR 5)						
Input Voltage Range	V_{PVIN56}		1.7		5.5	V
Output Current Range	I_{OUT5}			300		mA
Input UVLO Rising Threshold		On PVIN56			1.6	V
Input UVLO Falling Threshold		On PVIN56	1.3			V
Input UVLO Hysteresis				100	110	mV
Input Overvoltage Lockout (OVLO) Rising Threshold		On PVIN56	5.45	5.7	5.95	V
Input OVLO Hysteresis				90	110	mV
Quiescent Current		On PVIN56, no load		120	180	µA
Output Voltage Range	V_{OUT5}	SPI programmable range	1.755		2.070	V
Output Voltage Accuracy		V_{PVIN56} = V_{OUT5} + 0.3 V to 5.5 V	−1.5		+1.5	%
Dropout Voltage		V_{OUT5} = 1.8 V, output current for Regulator 5 (I_{OUT5}) = 300 mA		60	150	mV
Current-Limit Threshold			350	500	650	mA
Soft Start Time	t_{SS}			200		µs
Output Noise	OUT_{NOISE5}	10 Hz to 100 kHz, V_{PVIN56} = 2.1 V, V_{OUT5} = 1.8 V		13		µV rms
Noise Spectral Density	OUT_{NSD5}	10 kHz, V_{PVIN56} = 2.1 V, V_{OUT5} = 1.8 V, I_{OUT5} = 300 mA		42		nV/√Hz
		100 kHz, V_{PVIN56} = 2.1 V, V_{OUT5} = 1.8 V, I_{OUT5} = 300 mA		30		nV/√Hz
Power Supply Rejection Ratio (PSRR)	$PSRR_{LDO1}$	10 kHz, V_{PVIN56} = 2.1 V, V_{OUT5} = 1.8 V, I_{OUT5} = 300 mA		56		dB
		100 kHz, V_{PVIN56} = 2.1 V, V_{OUT5} = 1.8 V, I_{OUT5} = 300 mA		50		dB
Overtemperature Threshold				160		°C
Overtemperature Hysteresis				20		°C
Overtemperature Deglitch Time			30	35	40	µs

LDO2 (REGULATOR 6) SPECIFICATIONS

V_{AVIN} = V_{AVDD} = 3.7 V, V_{PVIN56} > output voltage for Regulator 6 (V_{OUT6}) + 0.3 V or V_{PVIN56} = 2.1 V (whichever is greater), C_{IN56} = 10 µF, output capacitance for Regulator 6 (C_{OUT6}) = 10 µF, T_J = −40°C to +150°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 5.

Parameter	Symbol	Test Conditions / Comments	Min	Typ	Max	Unit
LDO2 (REGULATOR 6)						
Input Voltage Range	V_{PVIN56}		1.7		5.5	V
Output Current Range	I_{OUT6}			2.3		A
Input UVLO Rising Threshold		On PVIN56			1.6	V
Input UVLO Falling Threshold		On PVIN56	1.3			V
Input UVLO Hysteresis				100	110	mV
Input OVLO Rising Threshold		On PVIN56	5.45	5.7	5.95	V

Parameter	Symbol	Test Conditions / Comments	Min	Typ	Max	Unit
Input OVLO Hysteresis				90	110	mV
Quiescent Current		On PVIN56, no load		500	1000	µA
Output Voltage Range	V_{OUT6}	SPI programmable range	1.755		2.070	V
Output Voltage Accuracy		V_{PVIN56} = V_{OUT6} + 0.3 V to 5.5 V	−1.5		+1.5	%
Dropout Voltage		V_{OUT6} = 1.8 V, output current for Regulator 6 (I_{OUT6}) = 1.0 A		30	70	mV
Current-Limit Threshold			2.7	3.1	3.5	A
Soft Start Time	t_{S6}			1		ms
Output Noise	OUT_{NOISE6}	10 Hz to 100 kHz, V_{PVIN56} = 2.1 V, V_{OUT6} = 1.8 V		17		µV rms
Noise Spectral Density	OUT_{NSD6}	10 kHz, V_{PVIN56} = 2.1 V, V_{OUT6} = 1.8 V, I_{OUT6} = 1.9 A		60		nV/√Hz
		100 kHz, V_{PVIN56} = 2.1 V, V_{OUT6} = 1.8 V, I_{OUT6} = 1.9 A		32		nV/√Hz
PSRR	$PSRR_{LDO2}$	10 kHz, V_{PVIN56} = 2.1 V, V_{OUT6} = 1.8 V, I_{OUT6} = 1.9 A		68		dB
		100 kHz, V_{PVIN56} = 2.1 V, V_{OUT6} = 1.8 V, I_{OUT6} = 1.9 A		51		dB
Overtemperature Threshold				160		°C
Overtemperature Hysteresis				20		°C
Overtemperature Deglitch Time			30	35	40	µs
Discharge Resistance				170		Ω

LDO3 (REGULATOR 7) SPECIFICATIONS

V_{AVIN} = V_{AVDD} = 3.7 V, V_{PVIN78} > output voltage for Regulator 7 (V_{OUT7}) + 0.3 V or V_{PVIN78} = 1.2 V (whichever is greater), PVIN78 input capacitance (C_{IN78}) = 10 µF, output capacitance for Regulator 7 (C_{OUT7}) = 10 µF, T_J = −40°C to +150°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 6.

Parameter	Symbol	Test Conditions / Comments	Min	Typ	Max	Unit
LDO3 (REGULATOR 7)						
Input Voltage Range	V_{PVIN78}		0.9		1.98	V
Output Current Range	I_{OUT7}			1.4		A
Input UVLO Rising Threshold		On PVIN78			0.85	V
Input UVLO Falling Threshold		On PVIN78	0.7			V
Input UVLO Hysteresis				50	60	mV
Input OVLO Rising Threshold		On PVIN78	1.98	2.05	2.12	V
Input OVLO Hysteresis				80	90	mV
Quiescent Current		On PVIN78, no load		600	2200	µA
Output Voltage Range	V_{OUT7}		0.864		1.116	V
Output Voltage Accuracy		V_{PVIN78} = V_{OUT7} + 0.3 V to 1.98 V	−1.5		+1.5	%
Dropout Voltage		V_{OUT7} = 0.9 V, output current for Regulator 7 (I_{OUT7}) = 0.7 A		27	70	mV
Current-Limit Threshold			1.7	2.1	2.5	A
Soft Start Time	t_{S7}			200		µs
Output Noise	OUT_{NOISE7}	10 Hz to 100 kHz, V_{PVIN78} = 1.2 V, V_{OUT7} = 0.9 V		9.6		µV rms
Noise Spectral Density	OUT_{NSD7}	10 kHz, V_{PVIN78} = 1.2 V, V_{OUT7} = 0.9 V, I_{OUT7} = 1.4 A		21		nV/√Hz
		100 kHz, V_{PVIN78} = 1.2 V, V_{OUT7} = 0.9 V, I_{OUT7} = 1.4 A		12		nV/√Hz
PSRR	$PSRR_{LDO3}$	10 kHz, V_{PVIN78} = 1.2 V, V_{OUT7} = 0.9 V, I_{OUT7} = 1.4 A		72		dB
		100 kHz, V_{PVIN78} = 1.2 V, V_{OUT7} = 0.9 V, I_{OUT7} = 1.4 A		69		dB
Overtemperature Threshold				160		°C
Overtemperature Hysteresis				20		°C
Overtemperature Deglitch Time			30	35	40	µs
Discharge Resistance				70		Ω

LDO4 (REGULATOR 8) SPECIFICATIONS

V_{AVIN} = V_{AVDD} = 3.7 V, V_{PVIN78} > output voltage for Regulator 8 (V_{OUT8}) + 0.3 V or V_{PVIN78} = 1.2 V (whichever is greater), C_{IN78} = 10 µF, output capacitance for Regulator 8 (C_{OUT8}) = 10 µF, T_J = −40°C to +150°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 7.

Parameter	Symbol	Test Conditions / Comments	Min	Typ	Max	Unit
LDO4 (REGULATOR 8)						
Input Voltage Range	V_{PVIN78}		0.9		1.98	V
Output Current Range	I_{OUT8}			1.2		A
Input UVLO Rising Threshold		On PVIN78			0.85	V
Input UVLO Falling Threshold		On PVIN78	0.7			V
Input UVLO Hysteresis				50	60	mV
Input OVLO Rising Threshold		On PVIN78	1.98	2.05	2.12	V
Input OVLO Hysteresis				80	90	mV
Quiescent Current		On PVIN78, no load		600	2200	µA
Output Voltage Range	V_{OUT8}		0.864		1.116	V
Output Voltage Accuracy		V_{PVIN78} = V_{OUT8} + 0.3 V to 1.98 V	−1.5		+1.5	%
Dropout Voltage		V_{OUT8} = 0.9 V, output current for Regulator 8 (I_{OUT8}) = 0.6 A		19	70	mV
Current-Limit Threshold			1.35	1.7	2.05	A
Soft Start Time	t_{S8}			200		µs
Output Noise	OUT_{NOISE8}	10 Hz to 100 kHz, V_{PVIN78} = 1.2 V, V_{OUT8} = 0.9 V		9.6		µV rms
Noise Spectral Density	OUT_{NSD8}	10 kHz, V_{PVIN78} = 1.2 V, V_{OUT8} = 0.9 V, I_{OUT8} = 1.2 A		21		nV/√Hz
		100 kHz, V_{PVIN78} = 1.2 V, V_{OUT8} = 0.9 V, I_{OUT8} = 1.2 A		12		nV/√Hz
PSRR	$PSRR_{LDO4}$	10 kHz, V_{PVIN78} = 1.2 V, V_{OUT8} = 0.9 V, I_{OUT8} = 1.2 A		67		dB
		100 kHz, V_{PVIN78} = 1.2 V, V_{OUT8} = 0.9 V, I_{OUT8} = 1.2 A		65		dB
Overtemperature Threshold				160		°C
Overtemperature Hysteresis				20		°C
Overtemperature Deglitch Time			30	35	40	µs
Discharge Resistance				70		Ω

LDO5 (REGULATOR 9) SPECIFICATIONS

V_{AVIN} = V_{AVDD} = 3.7 V, V_{PVIN9} > output voltage for Regulator 9 (V_{OUT9}) + 0.3 V or V_{PVIN9} = 1.2 V (whichever is greater), PVIN9 input capacitance (C_{IN9}) = 10 µF, output capacitance for Regulator 9 (C_{OUT9}) = 10 µF, T_J = −40°C to +150°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 8.

Parameter	Symbol	Test Conditions / Comments	Min	Typ	Max	Unit
LDO5 (REGULATOR 9)						
Input Voltage Range	V_{PVIN9}		0.9		1.98	V
Output Current Range	I_{OUT9}			500		mA
Input UVLO Rising Threshold		On PVIN9			0.85	V
Input UVLO Falling Threshold		On PVIN9	0.7			V
Input UVLO Hysteresis				50	60	mV
Input OVLO Rising Threshold		On PVIN9	1.98	2.05	2.12	V
Input OVLO Hysteresis				80	90	mV
Quiescent Current		On PVIN9, no load		400	1200	µA
Output Voltage Range	V_{OUT9}		0.864		1.116	V
Output Voltage Accuracy		V_{PVIN9} = V_{OUT9} + 0.3 V to 1.98 V	−1.5		+1.5	%
Dropout Voltage		V_{OUT9} = 0.9 V, output current for Regulator 9 (I_{OUT9}) = 400 mA		28	70	mV
Current-Limit Threshold			0.7	0.9	1.115	A
Soft Start Time	t_{S9}			200		µs

Parameter	Symbol	Test Conditions / Comments	Min	Typ	Max	Unit
Output Noise	OUT_{NOISE9}	10 Hz to 100 kHz, V_{PVIN9} = 1.2 V, V_{OUT9} = 0.9 V		1.2		μV rms
Noise Spectral Density	OUT_{NSD9}	10 kHz, V_{PVIN9} = 1.2 V, V_{OUT9} = 0.9 V, I_{OUT9} = 500 mA		2.9		nV/√Hz
		100 kHz, V_{PVIN9} = 1.2 V, V_{OUT9} = 0.9 V, I_{OUT9} = 500 mA		2.2		nV/√Hz
PSRR	$PSRR_{LDO5}$	100 kHz, V_{PVIN9} = 1.2 V, V_{OUT9} = 0.9 V, I_{OUT9} = 500 mA		70		dB
		1 MHz, V_{PVIN9} = 1.2 V, V_{OUT9} = 0.9 V, I_{OUT9} = 500 mA		60		dB
Overtemperature Threshold				160		°C
Overtemperature Hysteresis				20		°C
Overtemperature Deglitch Time			30	35	40	μs
Discharge Resistance				70		Ω

LDO6 (REGULATOR 10) SPECIFICATIONS

V_{AVIN} = V_{AVDD} = 3.7 V, $V_{PVIN1011}$ > output voltage for Regulator 10 (V_{OUT10}) + 0.3 V or $V_{PVIN1011}$ = 3.7 V (whichever is greater), PVIN1011 input capacitance (C_{IN1011}) = 4.7 μF, output capacitance for Regulator 10 (C_{OUT10}) = 1 μF, T_J = −40°C to +150°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 9.

Parameter	Symbol	Test Conditions / Comments	Min	Typ	Max	Unit
LDO6 (REGULATOR 10)						
Input Voltage Range	$V_{PVIN1011}$		2.7		5.5	V
Output Current Range	I_{OUT10}			50		mA
Quiescent Current		On PVIN1011, no load		55	140	μA
Output Voltage Range	V_{OUT10}		3.2		3.4	V
Output Voltage Accuracy		$V_{PVIN1011}$ = V_{OUT10} + 0.3 V to 5.5 V	−1.5		+1.5	%
Dropout Voltage		V_{OUT10} = 3.3 V, output current for Regulator 10 (I_{OUT10}) = 50 mA		20	70	mV
Current-Limit Threshold			65	90	115	mA
Soft Start Time	t_{S10}			200		μs
Output Noise	$OUT_{NOISE10}$	10 Hz to 100 kHz, $V_{PVIN1011}$ = 3.7 V, V_{OUT10} = 3.3 V		15		μV rms
Noise Spectral Density	OUT_{NSD10}	10 kHz, $V_{PVIN1011}$ = 3.7 V, V_{OUT10} = 3.3 V, I_{OUT10} = 50 mA		42		nV/√Hz
		100 kHz, $V_{PVIN1011}$ = 3.7 V, V_{OUT10} = 3.3 V, I_{OUT10} = 50 mA		27		nV/√Hz
PSRR	$PSRR_{LDO6}$	10 kHz, $V_{PVIN1011}$ = 3.7 V, V_{OUT10} = 3.3 V, I_{OUT10} = 50 mA		61		dB
		100 kHz, $V_{PVIN1011}$ = 3.7 V, V_{OUT10} = 3.3 V, I_{OUT10} = 50 mA		63		dB
Overtemperature Threshold				160		°C
Overtemperature Hysteresis				20		°C
Overtemperature Deglitch Time			30	35	40	μs
Discharge Resistance				60		Ω

LDO7 (REGULATOR 11) SPECIFICATIONS

V_{AVIN} = V_{AVDD} = 3.7 V, $V_{PVIN1011}$ > output voltage for Regulator 11 (V_{OUT11}) + 0.3 V or $V_{PVIN1011}$ = 3.7 V (whichever is greater), C_{IN1011} = 4.7 μF, Regulator 11 output capacitance (C_{OUT11}) = 4.7 μF, T_J = −40°C to +150°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 10.

Parameter	Symbol	Test Conditions / Comments	Min	Typ	Max	Unit
LDO7 (REGULATOR 11)						
Input Voltage Range	$V_{PVIN1011}$		2.7		5.5	V
Output Current Range	I_{OUT11}				500	mA
Quiescent Current		On PVIN1011, no load		125	280	μA
Output Voltage Range	V_{OUT11}		3.2		3.4	V
Output Voltage Accuracy		$V_{PVIN1011}$ = V_{OUT11} + 0.3 V to 5.5 V	−1.5		+1.5	%
Dropout Voltage		V_{OUT11} = 3.3 V, output current for Regulator 11 (I_{OUT11}) = 400 mA		24	70	mV

Parameter	Symbol	Test Conditions / Comments	Min	Typ	Max	Unit
Current-Limit Threshold			450	600	750	mA
Soft Start Time	t_{S11}			200		µs
Output Noise	$OUT_{NOISE11}$	10 Hz to 100 kHz, $V_{PVIN1011}$ = 3.7 V, V_{OUT11} = 3.3 V		15		µV rms
Noise Spectral Density	OUT_{NSD11}	10 kHz, $V_{PVIN1011}$ = 3.7 V, V_{OUT11} = 3.3 V, I_{OUT11} = 400 mA		42		nV/√Hz
		100 kHz, $V_{PVIN1011}$ = 3.7 V, V_{OUT11} = 3.3 V, I_{OUT11} = 400 mA		28		nV/√Hz
PSRR	$PSRR_{LDO7}$	10 kHz, $V_{PVIN1011}$ = 3.7 V, V_{OUT11} = 3.3 V, I_{OUT11} = 400 mA		60		dB
		100 kHz, $V_{PVIN1011}$ = 3.7 V, V_{OUT11} = 3.3 V, I_{OUT11} = 400 mA		55		dB
Overtemperature Threshold				160		°C
Overtemperature Hysteresis				20		°C
Overtemperature Deglitch Time			30	35	40	µs
Discharge Resistance				65		Ω

ABSOLUTE MAXIMUM RATINGS

Table 11.

Parameter	Rating
AVIN, AVDD, VIO, EN, and SEQ	−0.3 V to +6 V
WAKE	−0.3 V to +6 V
SYNC	−0.3 V to V_{VIO}
PVIN1, PVIN2, PVIN3, and PVIN4	−0.3 V to +6 V
SW1, SW2, SW3, and SW4	−1 V to +6 V
FB1, FB2, FB3, and FB4	−0.3 V to +6 V
VSET1	−0.3 V to +6 V
PVIN56, OUT5, OUT6, FB5, and FB6	−0.3 V to +6 V
PVIN78, OUT7, FB7, OUT8, FB8, PVIN9, OUT9, FB9, REFCAP, and VREG	−0.3 V to +2.16 V
SW1, SW2, OUT12, and FB12	−0.3 V to +6 V
PVIN1011, OUT10, OUT11, FB10, and FB11	−0.3 V to +6 V
VM0 and VM1	−0.3 V to +6 V
MODE	−0.3 V to +6 V
$\overline{\text{RESET}}$, $\overline{\text{STATUS}}$, and $\overline{\text{FAULT}}$	−0.3 V to +6 V
WDI0 and WDI1	−0.3 V to V_{VIO}
$\overline{\text{CS}}$, SCK, MOSI, and MISO	−0.3 V to V_{VIO}
PGND	−0.3 V to +0.3 V
Operating Junction Temperature Range	−40°C to +150°C
Storage Temperature Range	−50°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance of the device, and θ_{JC} is the junction to case thermal resistance of the device. Both θ_{JA} and θ_{JC} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 12. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
56-Terminal LGA	17.4	12.5	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADP5140

Table 13. ADP5140, 56-Terminal LGA

ESD Model	Withstand Threshold (V)	Class Level
HBM	2000	AEC Q100-002, H1C
CDM	750 (corner pins)	AEC Q100-011, C4B
	500 (all other pins)	

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

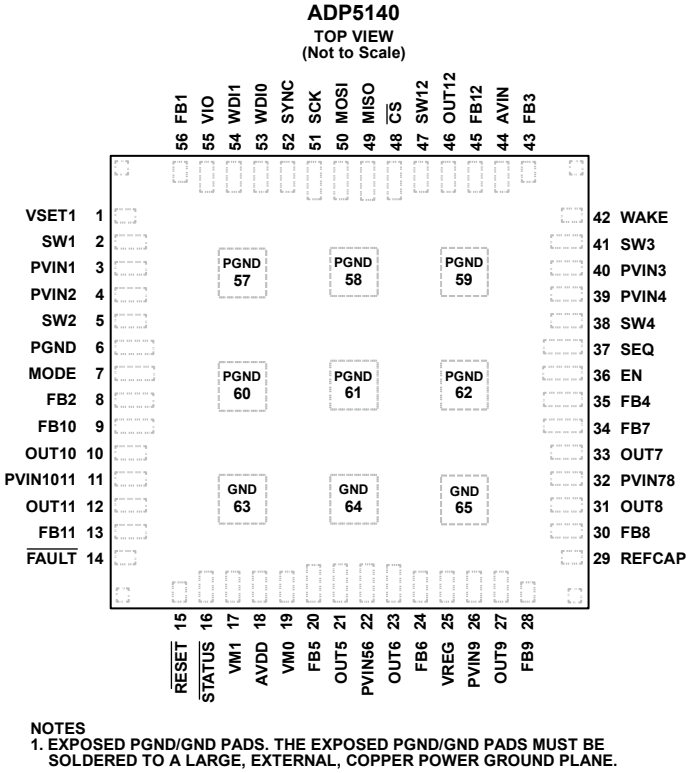

Figure 5. Pin Configuration (Top View)

Table 14. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VSET1	Output Voltage Setting for BUCK1. Connect a resistor between VSET1 and GND.
2	SW1	Switch Node for BUCK1.
3	PVIN1	Power Input for BUCK1.
4	PVIN2	Power Input for BUCK2.
5	SW2	Switch Node for BUCK2.
6	PGND	Power Ground.
7	MODE	Connect a resistor between MODE and ground to configure different functions (see the MODE Pin Setting section for more information). The three MODE functions include the following: Enable or disable debug mode. Set the device index of the ADP5140. Selecting of the V_{IO}.
8	FB2	Feedback Voltage Sense Input for BUCK2. Connect FB2 to a resistor divider from the output voltage of BUCK2 (V_{OUT2}).
9	FB10	Feedback Voltage Sense Input for LDO6 (Regulator 10). Connect FB10 to OUT10 directly.
10	OUT10	Output for LDO6 (Regulator 10).
11	PVIN1011	Power Input for LDO6 (Regulator 10) and LDO7 (Regulator 11).
12	OUT11	Output of LDO7 (Regulator 11).
13	FB11	Feedback Voltage Sense Input for LDO7 (Regulator 11). Connect FB11 to OUT11 directly.
14	$\overline{\text{FAULT}}$	Fault Output for the ADP5140. $\overline{\text{FAULT}}$ is bidirectional, open-drain, and active low.
15	$\overline{\text{RESET}}$	Reset Signal for the Processor. $\overline{\text{RESET}}$ is bidirectional, open-drain, and active low.
16	$\overline{\text{STATUS}}$	Status of the ADP5140. $\overline{\text{STATUS}}$ is bidirectional, open-drain, and active low.
17	VM1	Input for Voltage Monitor 1 (VM1).
18	AVDD	Supply Voltage for Monitoring Circuits. Place a 1 µF ceramic capacitor between AVDD and GND.
19	VM0	Input for Voltage Monitor 0 (VM0).
20	FB5	Feedback Voltage Sense Input for LDO1 (Regulator 5). Connect FB5 to OUT5 directly.
21	OUT5	Output for LDO1 (Regulator 5).

Pin No.	Mnemonic	Description
22	PVIN56	Power Input for LDO1 (Regulator 5) and LDO2 (Regulator 6).
23	OUT6	Output for LDO2 (Regulator 6).
24	FB6	Feedback Voltage Sense Input for LDO2 (Regulator 6). Connect FB6 to OUT6 directly.
25	VREG	Regulated Input Supply for IC. Bypass VREG to GND with a ≥1 µF capacitor. Do not connect a load to ground.
26	PVIN9	Power Input for LDO5 (Regulator 9).
27	OUT9	Output for LDO5 (Regulator 9).
28	FB9	Feedback Voltage Sense Input for LDO5 (Regulator 9). Connect FB9 to OUT9 directly.
29	REFCAP	Reference Filter for LDO5. Connect a 0.47 µF capacitor between REFCAP and GND.
30	FB8	Feedback Voltage Sense Input for LDO4 (Regulator 8). Connect FB8 to OUT8 directly.
31	OUT8	Output of LDO4 (Regulator 8).
32	PVIN78	Power Input for LDO3 (Regulator 7) and LDO4 (Regulator 8).
33	OUT7	Output of LDO3 (Regulator 7).
34	FB7	Feedback Voltage Sense Input for LDO3 (Regulator 7). Connect FB7 to OUT7 directly.
35	FB4	Feedback Voltage Sense Input for BUCK4. Connect FB4 to OUT4 directly.
36	EN	Enable Input. Pull EN high to enable the ADP5140. Connect EN to ground to disable the ADP5140.
37	SEQ	Sequence Input Signal. Use SEQ to control the power-up sequence.
38	SW4	Switch Node for BUCK4.
39	PVIN4	Power Input for BUCK4.
40	PVIN3	Power Input for BUCK3.
41	SW3	Switch Node for BUCK3.
42	WAKE	Wake-Up Input.
43	FB3	Feedback Voltage Sense Input for BUCK3. Connect FB3 to a resistor divider from the output voltage of BUCK3 (V_{OUT3}).
44	AVIN	Analog Voltage Power Supply for Control Circuits. Place a 1 µF ceramic capacitor between AVIN and GND.
45	FB12	Feedback Voltage Sense Input for Boost Regulator. Connect FB12 to OUT12 directly.
46	OUT12	Output of Boost Regulator.
47	SW12	Switch Node for Boost Regulator.
48	$\overline{CS}$	SPI Chip Select. $\overline{CS}$ is an active low signal asserted by the SPI master to initiate communication (start of the frame). Deassertion of $\overline{CS}$ ends the current frame.
49	MISO	SPI, Master In, Slave Out. MISO is a push pull output supplied by V_{VIO}.
50	MOSI	SPI, Master Out, Slave In.
51	SCK	SPI, Clock Driven by the SPI Master.
52	SYNC	Synchronization. SYNC can be configured as an input or an output by the SPI, and the default is an input. When configured as an output, SYNC outputs a clock in phase with BUCK1.
53	WDI0	Input for the Watchdog 0 (WD0) Window.
54	WDI1	Input for the Watchdog 1 (WD1) Window.
55	VIO	Power Supply for the Digital Interface.
56	FB1	Feedback Voltage Sense Input for BUCK1. Connect FB1 to OUT1 directly.
57 to 62	EP, PGND	Exposed PGND Pads. The exposed PGND pads must be soldered to a large, external, copper power ground plane.
63 to 65	EP, GND	Exposed GND Pads. The exposed GND pads must be soldered to a large, external, copper power ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{AVIN} = V_{AVDD} = V_{PVIN1} = V_{PVIN2} = V_{PVIN3} = V_{PVIN4} = 3.7 V, and f_{SW} = 2.2 MHz, unless otherwise noted. V_{OUTx} is the output voltage on a single power channel.

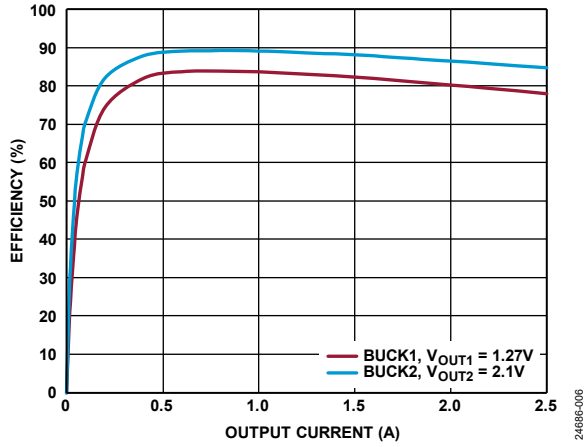

Figure 6. Efficiency vs. Output Current (BUCK1 and BUCK2)

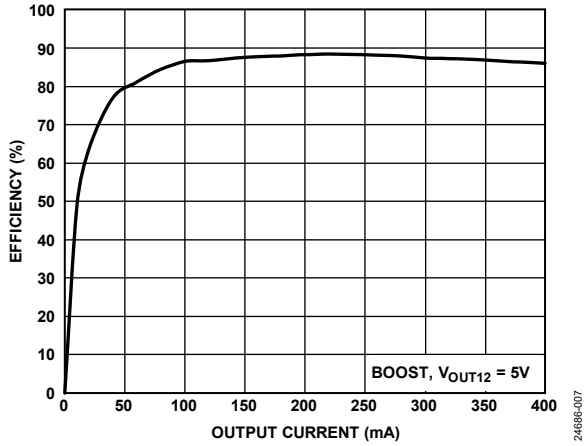

Figure 7. Efficiency vs. Output Current (Boost Regulator)

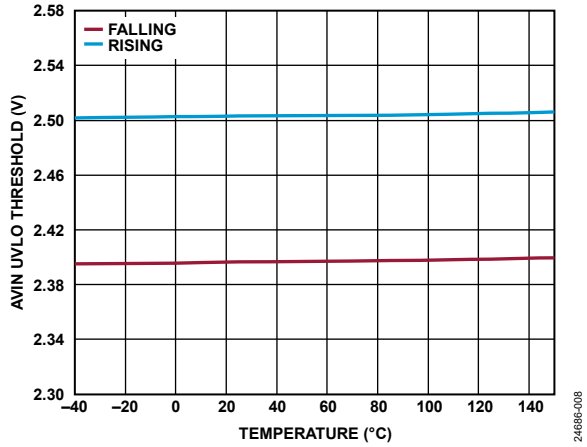

Figure 8. AVIN UVLO Threshold vs. Temperature

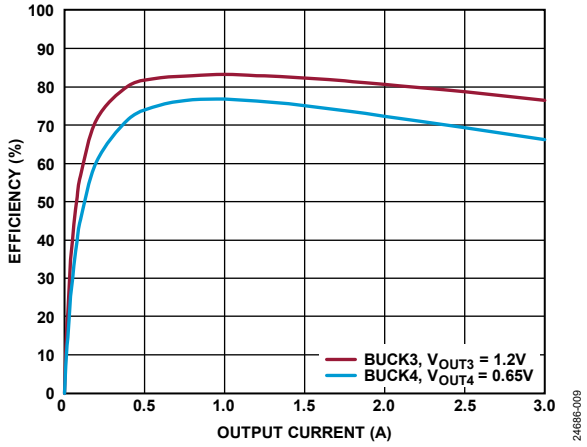

Figure 9. Efficiency vs. Output Current (BUCK3 and BUCK4)

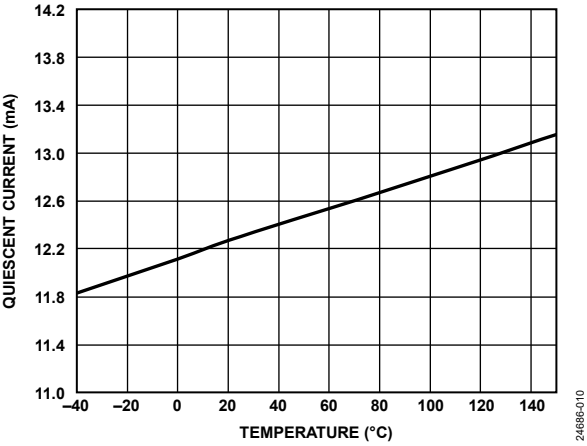

Figure 10. Quiescent Current vs. Temperature

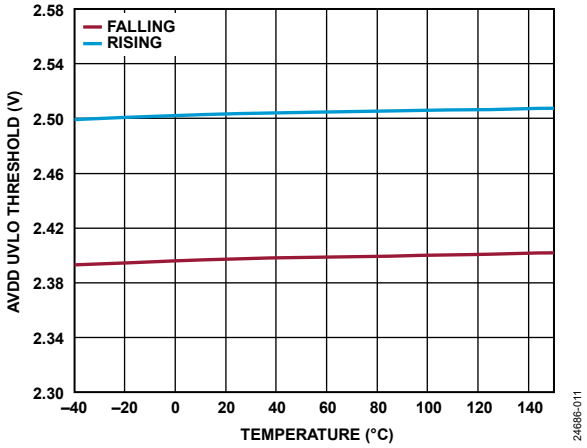

Figure 11. AVDD UVLO Threshold vs. Temperature

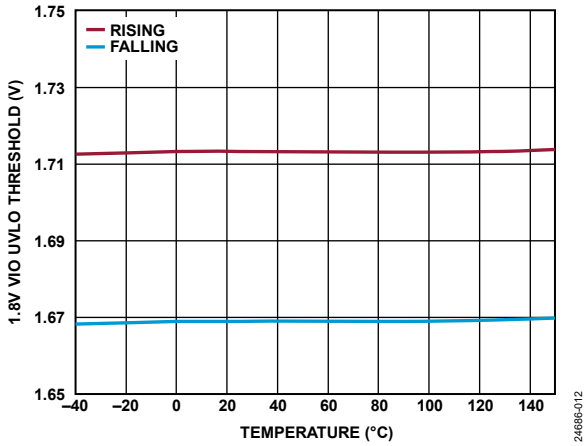

Figure 12. 1.8 V VIO UVLO Threshold vs. Temperature

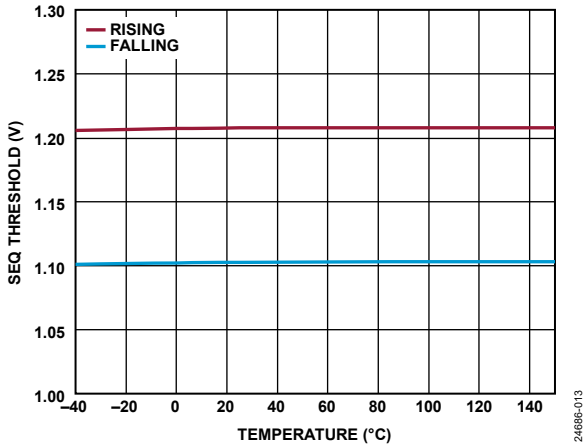

Figure 13. SEQ Threshold vs. Temperature

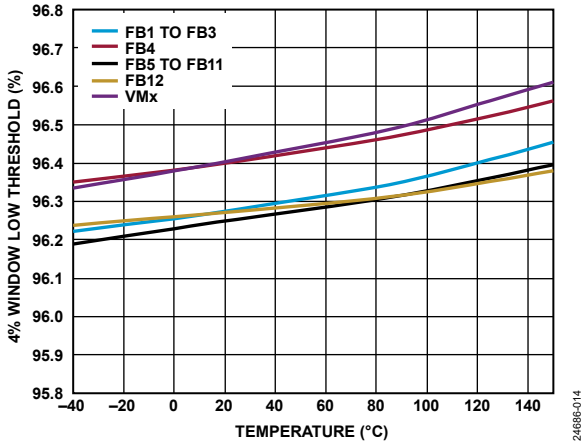

Figure 14. 4% Window Low Threshold vs. Temperature

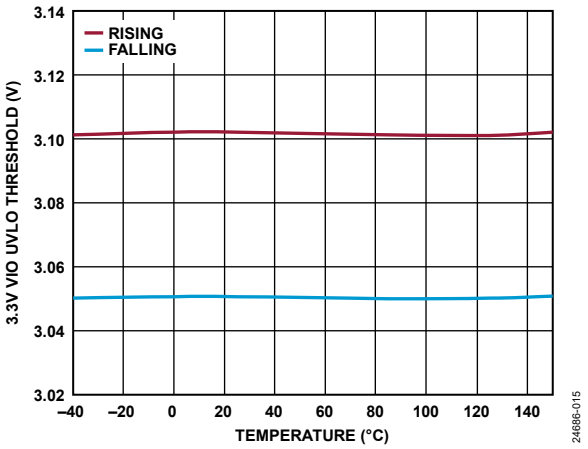

Figure 15. 3.3 V VIO UVLO Threshold vs. Temperature

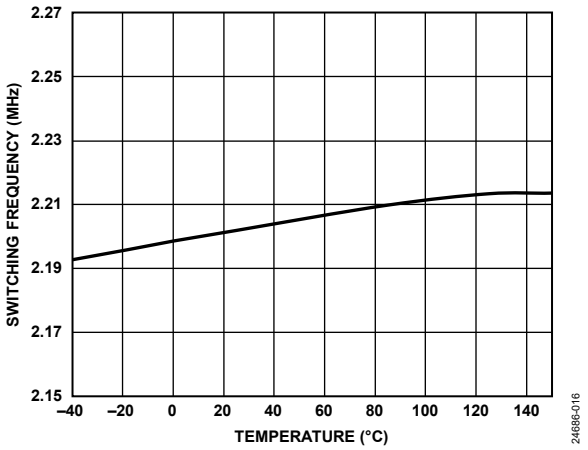

Figure 16. Switching Frequency vs. Temperature

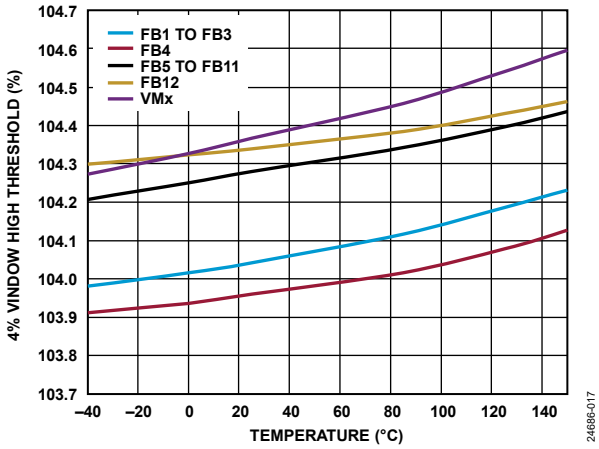

Figure 17. 4% Window High Threshold vs. Temperature

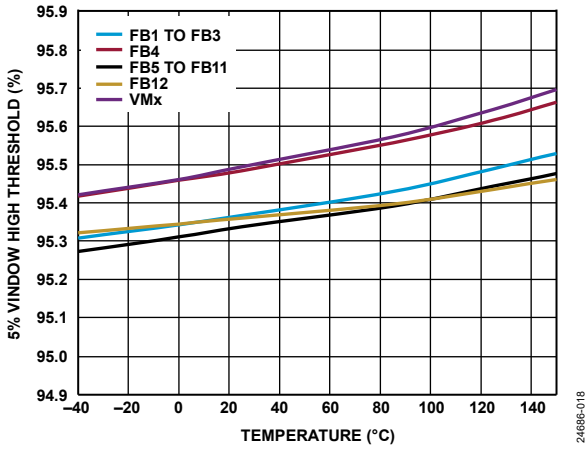

Figure 18. 5% Window Low Threshold vs. Temperature

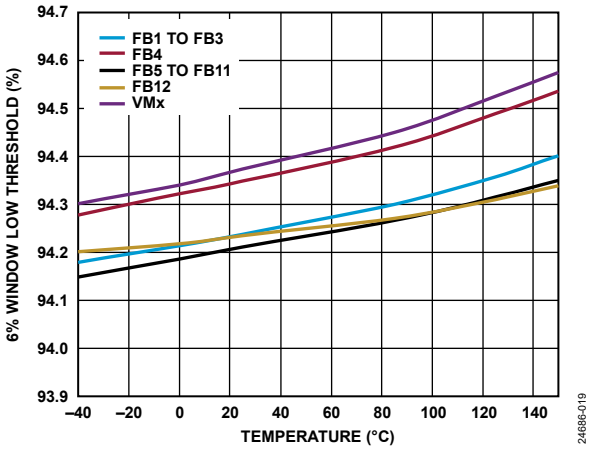

Figure 19. 6% Window Low Threshold vs. Temperature

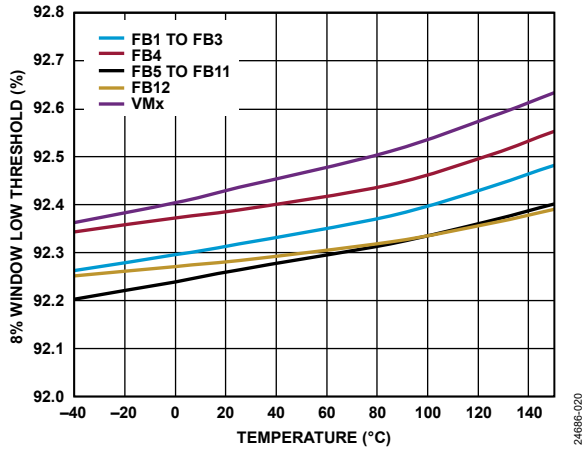

Figure 20. 8% Window Low Threshold vs. Temperature

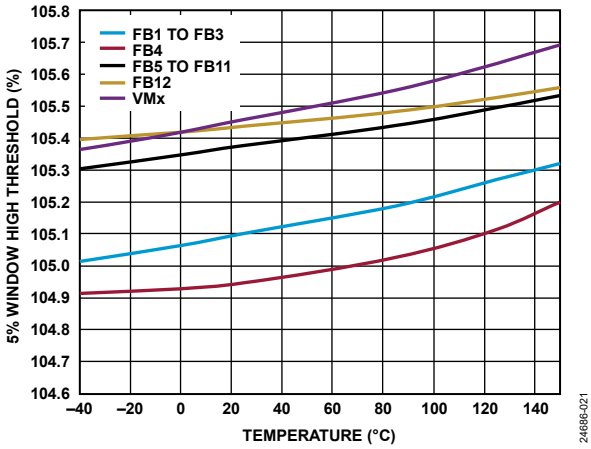

Figure 21. 5% Window High Threshold vs. Temperature

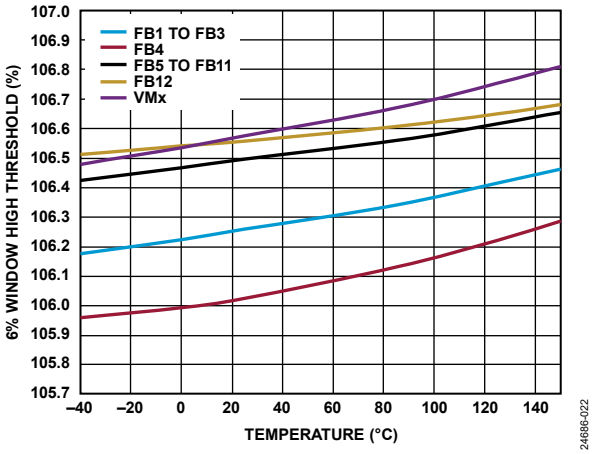

Figure 22. 6% Window High Threshold vs. Temperature

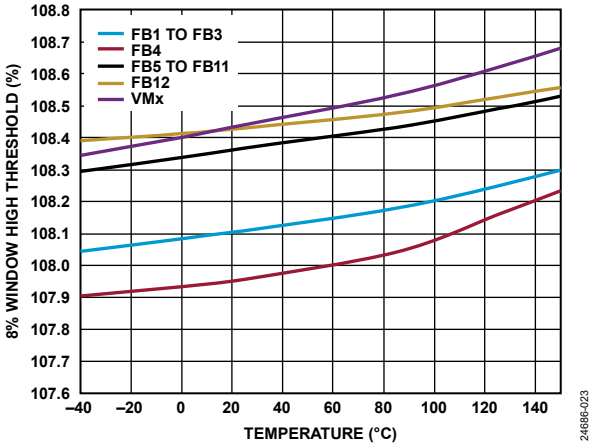

Figure 23. 8% Window High Threshold vs. Temperature

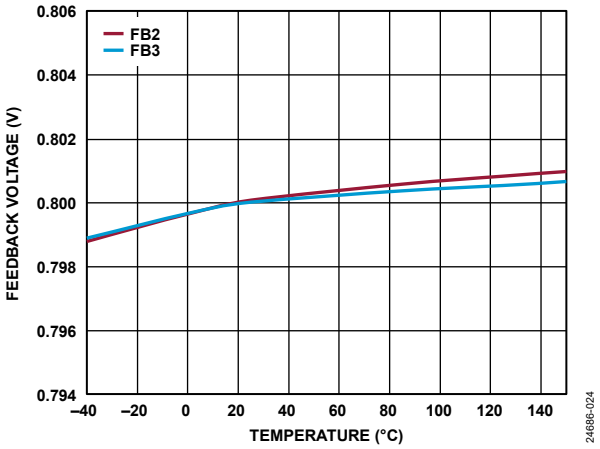

Figure 24. Feedback Voltage vs. Temperature (BUCK2 and BUCK3)

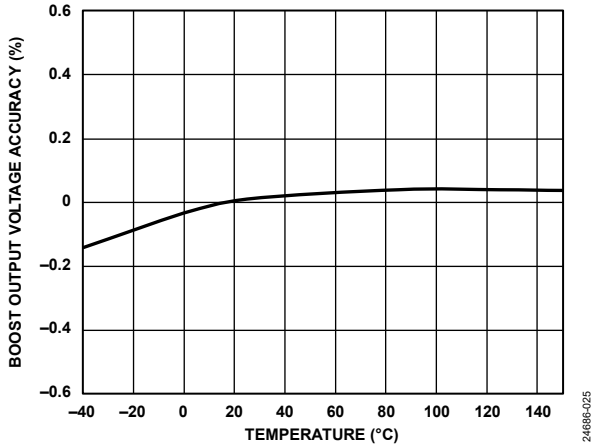

Figure 25. Boost Output Voltage Accuracy vs. Temperature

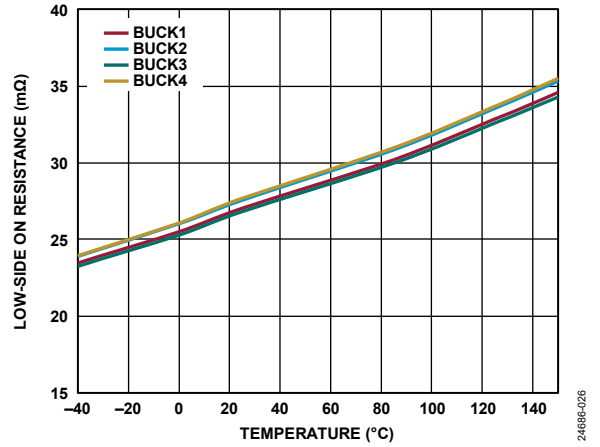

Figure 26. Low-Side On Resistance vs. Temperature (BUCK1 to BUCK4)

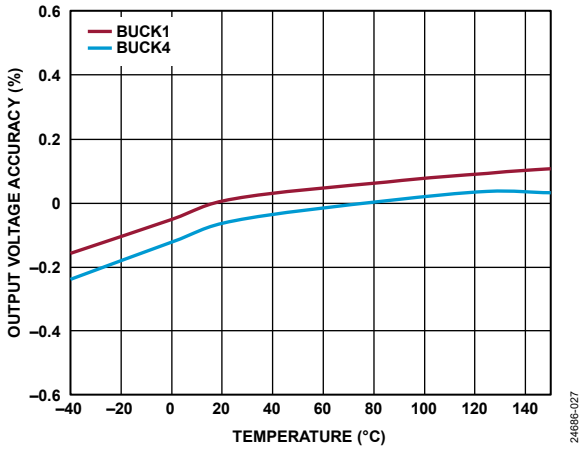

Figure 27. Output Voltage Accuracy vs. Temperature (BUCK1 and BUCK4)

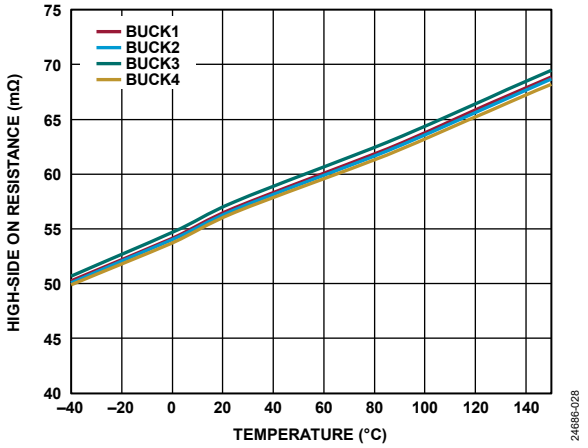

Figure 28. High-Side On Resistance vs. Temperature (BUCK1 to BUCK4)

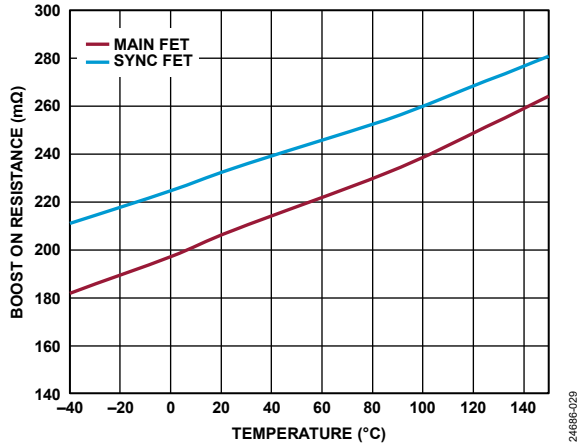

Figure 29. Boost On Resistance vs. Temperature

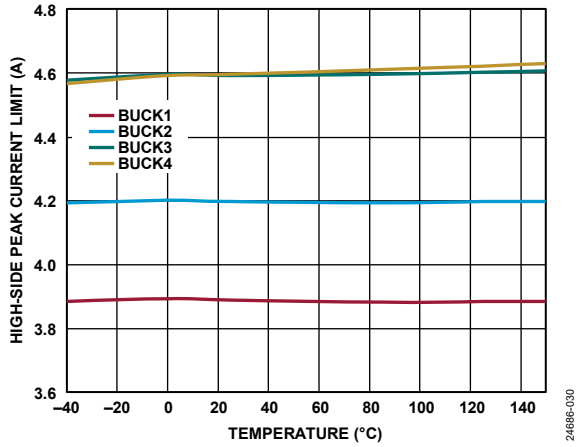

Figure 30. High-Side Peak Current Limit vs. Temperature (BUCK1 to BUCK4)

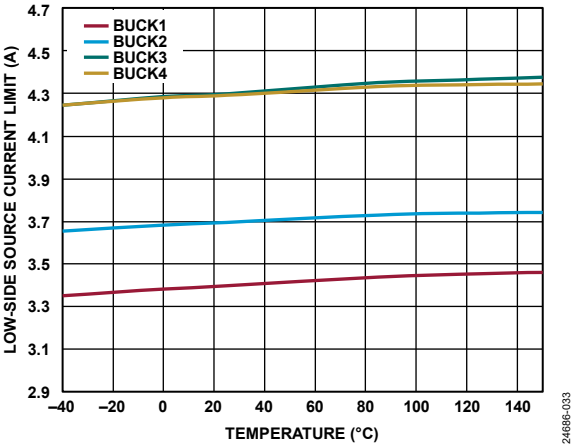

Figure 33. Low-Side Source Current Limit vs. Temperature (BUCK1 to BUCK4)

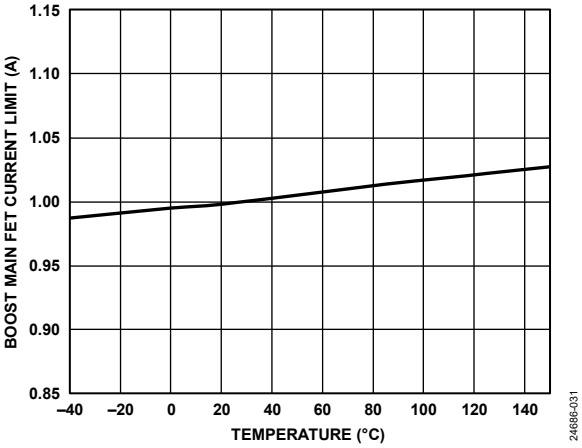

Figure 31. Boost Main FET Current Limit vs. Temperature

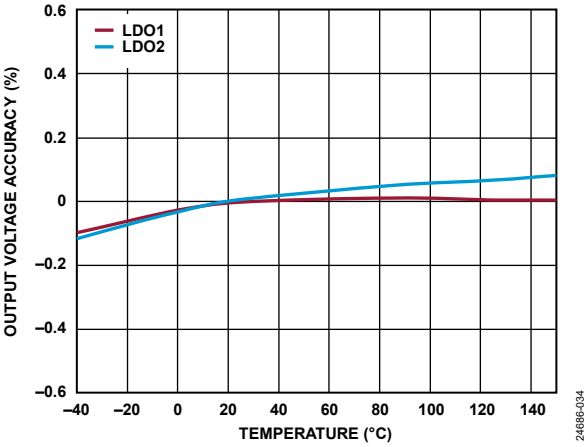

Figure 34. Output Voltage Accuracy vs. Temperature (LDO1 and LDO2)

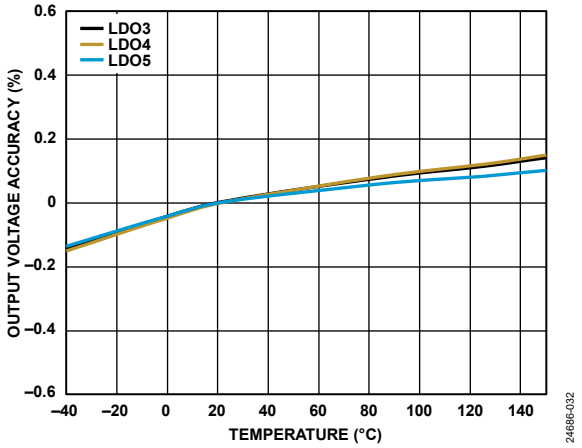

Figure 32. Output Voltage Accuracy vs. Temperature (LDO3 to LDO5)

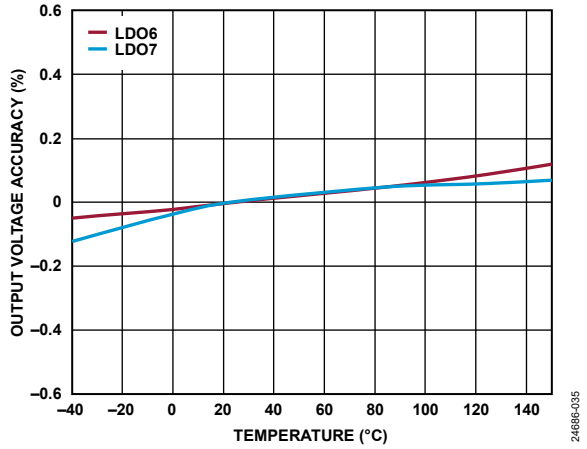

Figure 35. Output Voltage Accuracy vs. Temperature (LDO6 and LDO7)

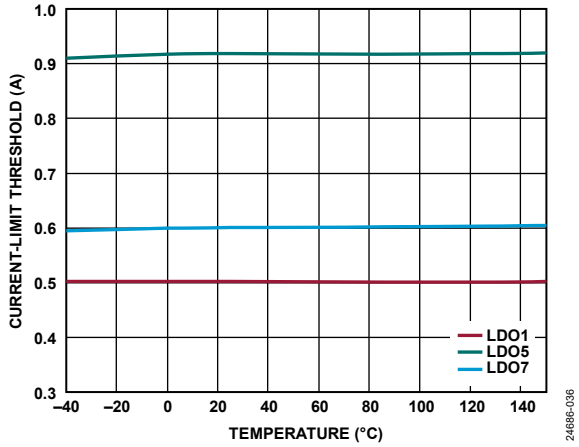

Figure 36. Current-Limit Threshold vs. Temperature (LDO1, LDO5, LDO7)

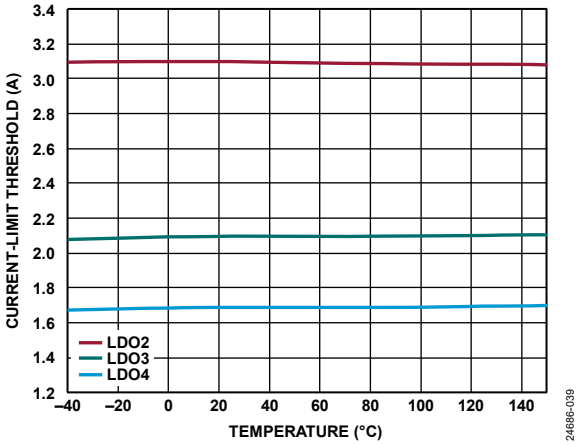

Figure 39. Current-Limit Threshold vs. Temperature (LDO2 to LDO4)

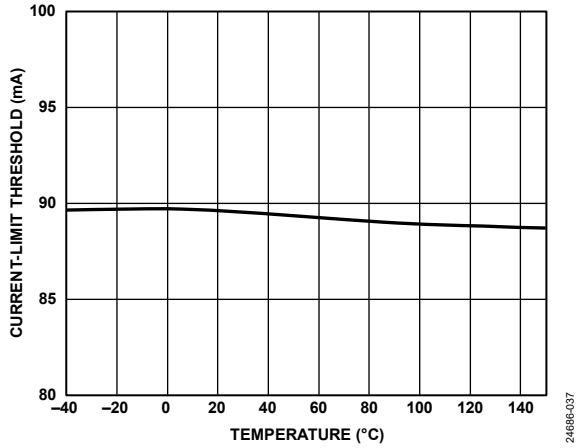

Figure 37. Current-Limit Threshold vs. Temperature (LDO6)

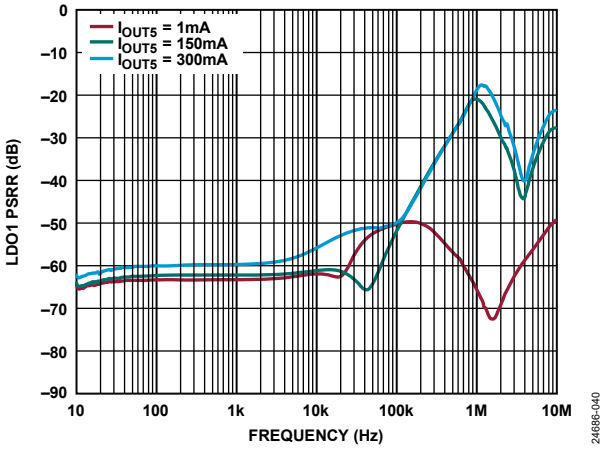

Figure 40. LDO1 PSRR vs. Frequency, V_{PVIN56} = 2.1 V, V_{OUT5} = 1.8 V

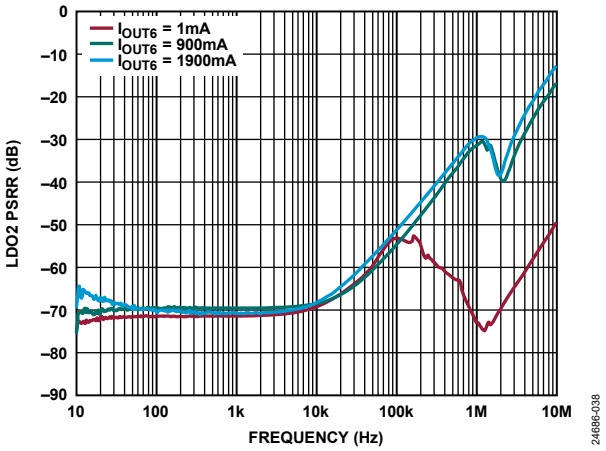

Figure 38. LDO2 PSRR vs. Frequency, V_{PVIN56} = 2.1 V, V_{OUT6} = 1.8 V

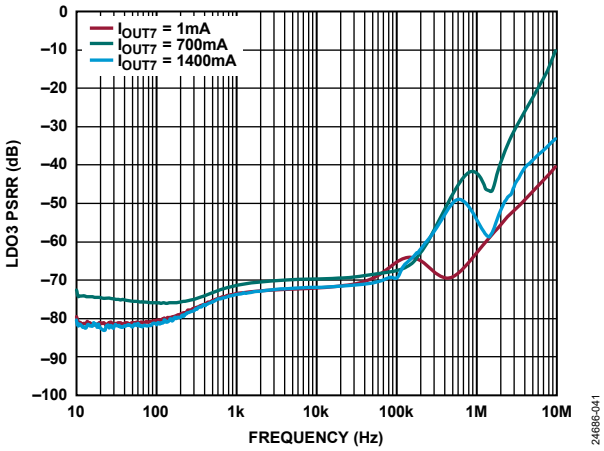

Figure 41. LDO3 PSRR vs. Frequency, V_{PVIN78} = 1.2 V, V_{OUT7} = 0.9 V

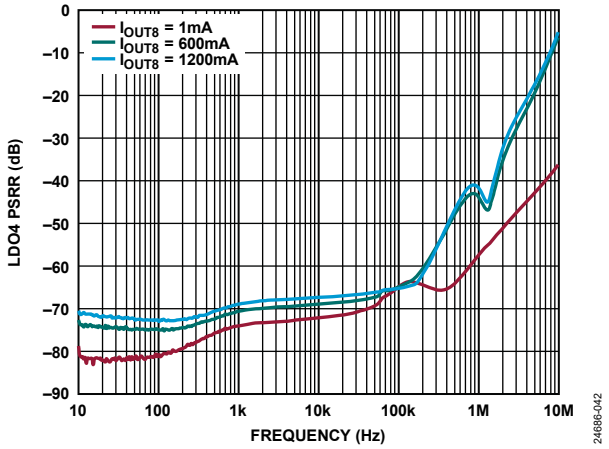

Figure 42. LDO4 PSRR vs. Frequency, V_{PVIN78} = 1.2 V, V_{OUT8} = 0.9 V

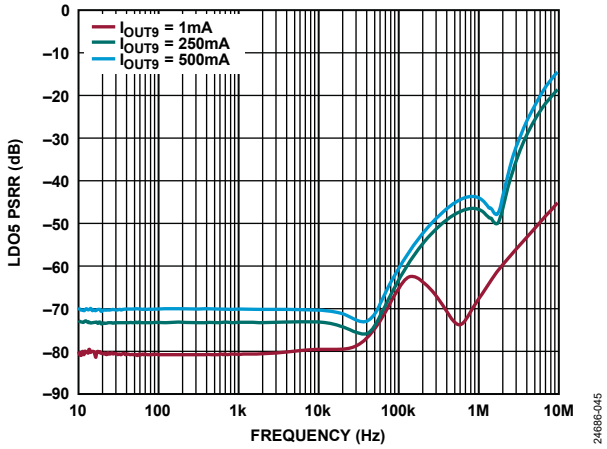

Figure 45. LDO5 PSRR vs. Frequency, V_{PVIN9} = 1.2 V, V_{OUT9} = 0.9 V

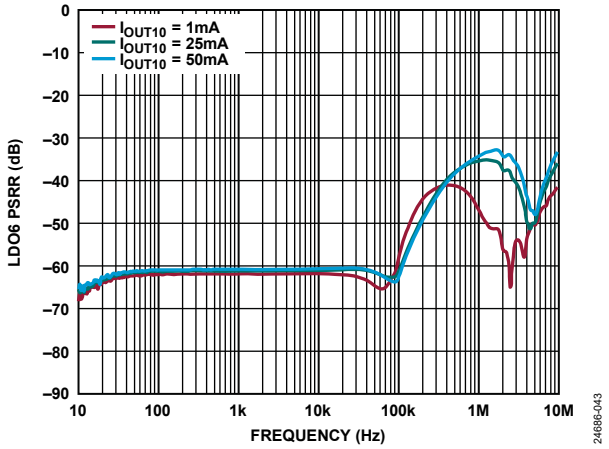

Figure 43. LDO6 PSRR vs. Frequency, $V_{PVIN1011}$ = 3.7 V, V_{OUT10} = 3.3 V

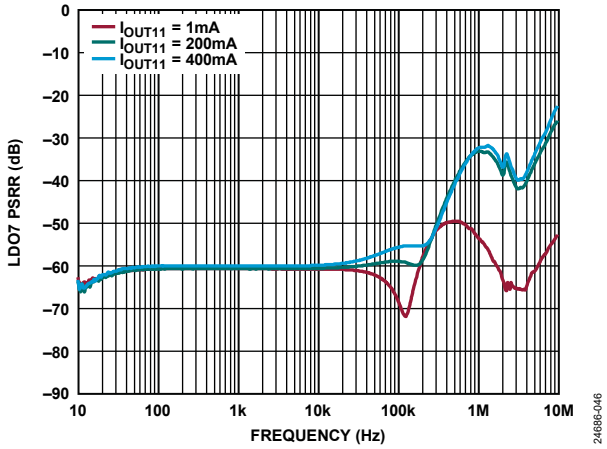

Figure 46. LDO7 PSRR vs. Frequency, $V_{PVIN1011}$ = 3.7 V, V_{OUT11} = 3.3 V

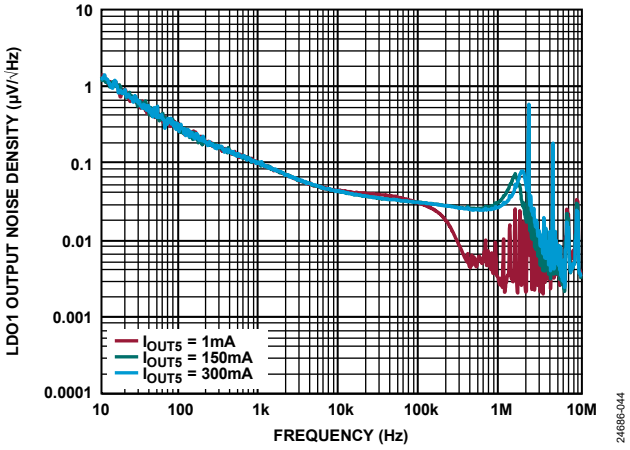

Figure 44. LDO1 Output Noise Density vs. Frequency, V_{PVIN56} = 2.1 V, V_{OUT5} = 1.8 V

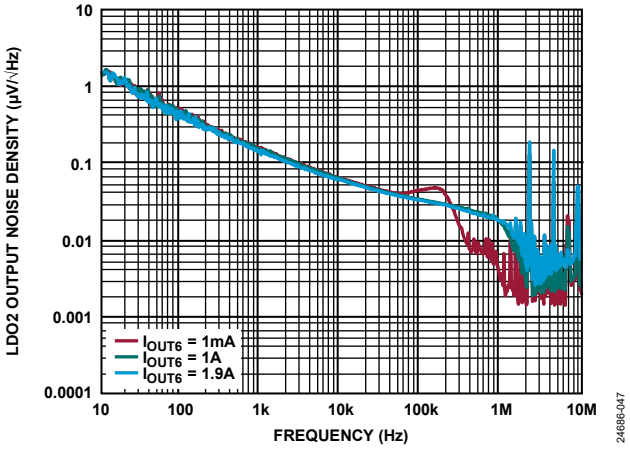

Figure 47. LDO2 Output Noise Density vs. Frequency, V_{PVIN56} = 2.1 V, V_{OUT6} = 1.8 V

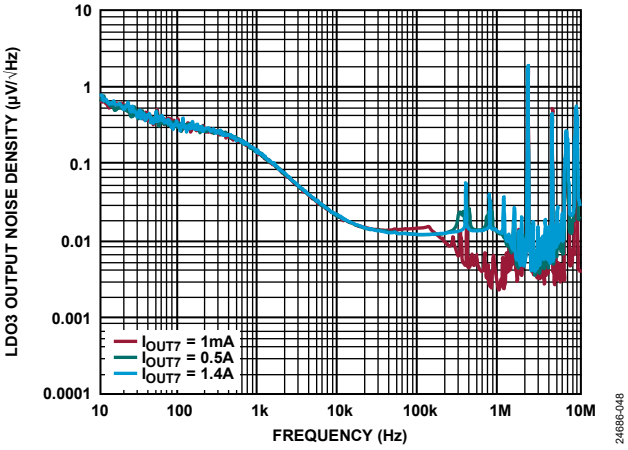

Figure 48. LDO3 Output Noise Density vs. Frequency, V_{PVIN78} = 1.2 V, V_{OUT7} = 0.9 V

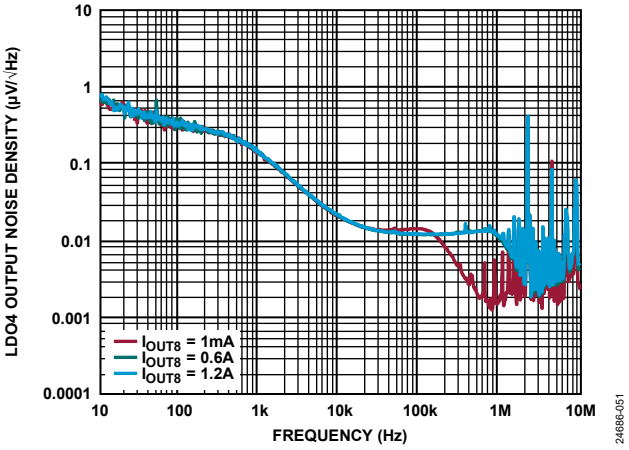

Figure 51. LDO4 Output Noise Density vs. Frequency, V_{PVIN78} = 1.2 V, V_{OUT8} = 0.9 V

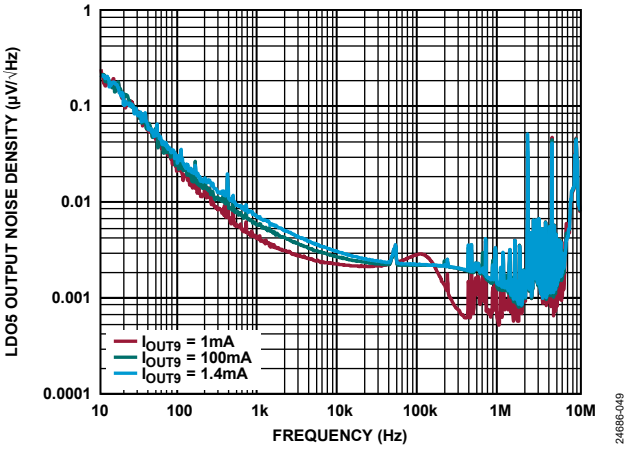

Figure 49. LDO5 Output Noise Density vs. Frequency, V_{PVIN9} = 1.2 V, V_{OUT9} = 0.9 V

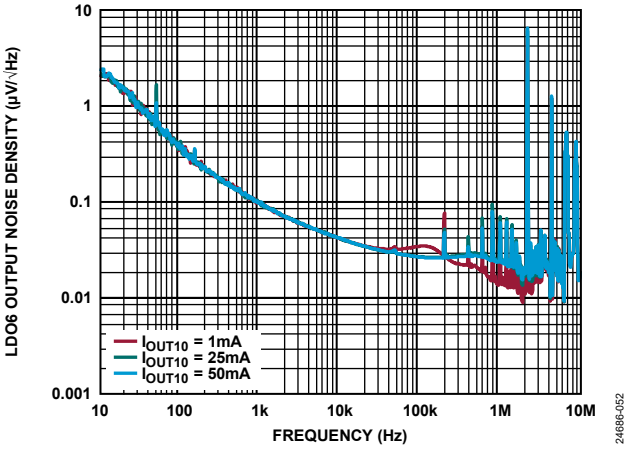

Figure 52. LDO6 Output Noise Density vs. Frequency, VPVIN1011 = 3.7 V, VOUT10 = 3.3 V

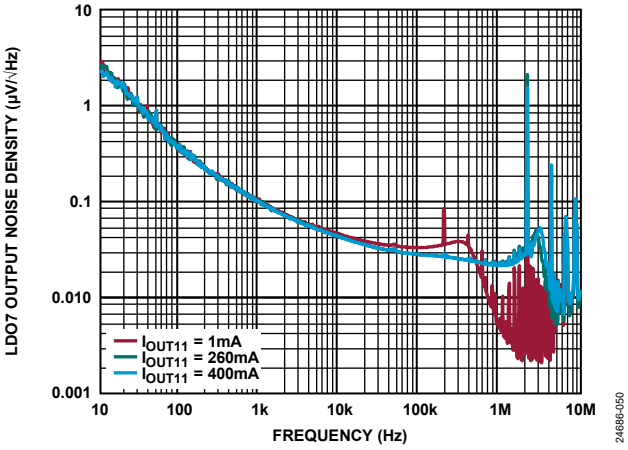

Figure 50. LDO7 Output Noise Density vs. Frequency, VPVIN1011 = 3.7 V, VOUT11 = 3.3 V

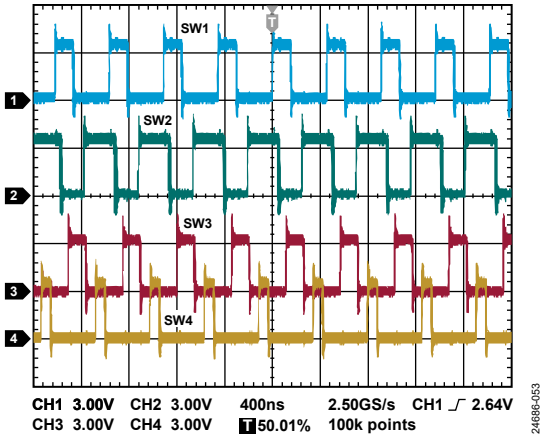

Figure 53. Phase Shift

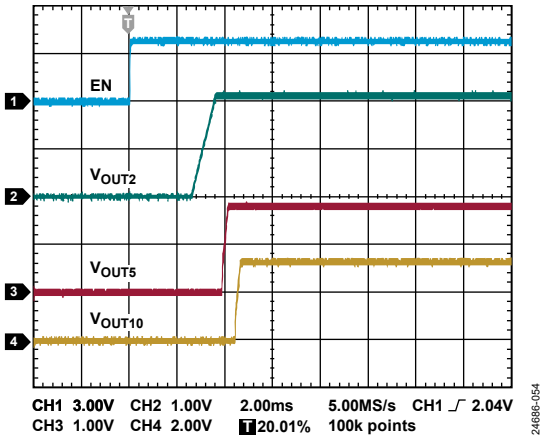

Figure 54. Startup with Full Load (EN, V_{OUT2}, V_{OUT5}, and V_{OUT10})

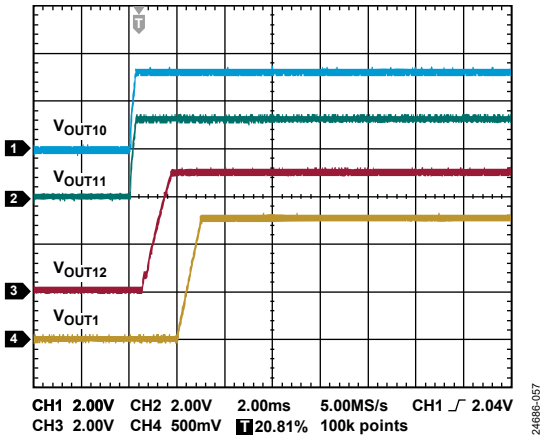

Figure 57. Startup with Full Load (V_{OUT1} and V_{OUT10} to V_{OUT12})

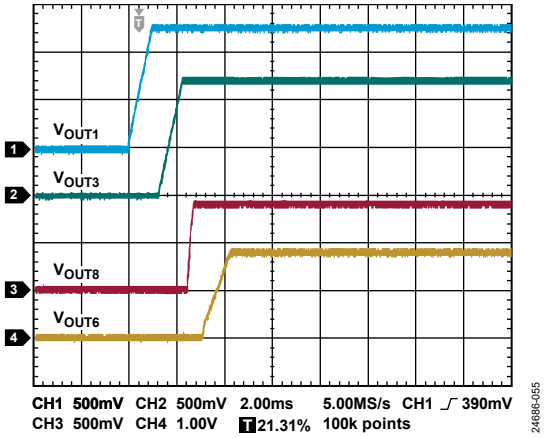

Figure 55. Startup with Full Load (V_{OUT1}, V_{OUT3}, V_{OUT6}, and V_{OUT8})

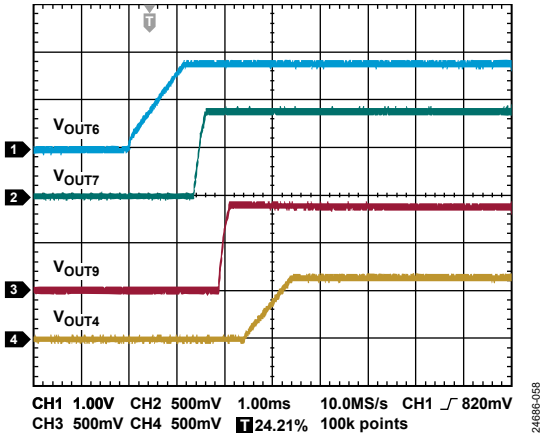

Figure 58. Startup with Full Load (V_{OUT4}, V_{OUT6}, V_{OUT7}, and V_{OUT9})

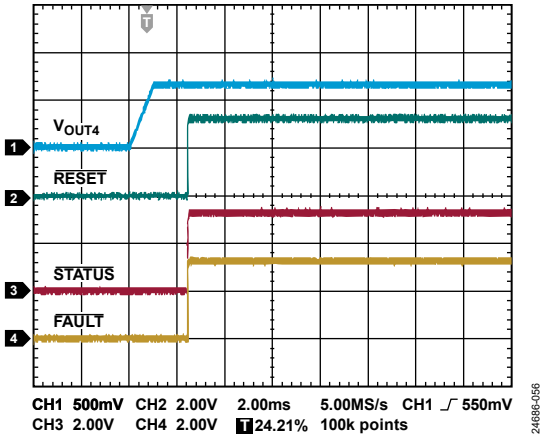

Figure 56. Startup with Full Load (V_{OUT4}, $\overline{RESET}$, $\overline{STATUS}$, and $\overline{FAULT}$)

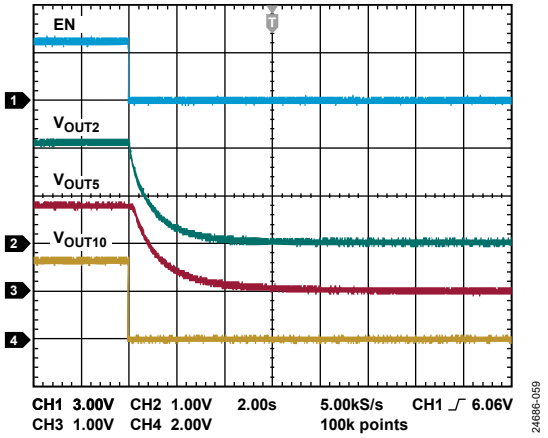

Figure 59. Shutdown with No Load (EN, V_{OUT2}, V_{OUT5}, and V_{OUT10})

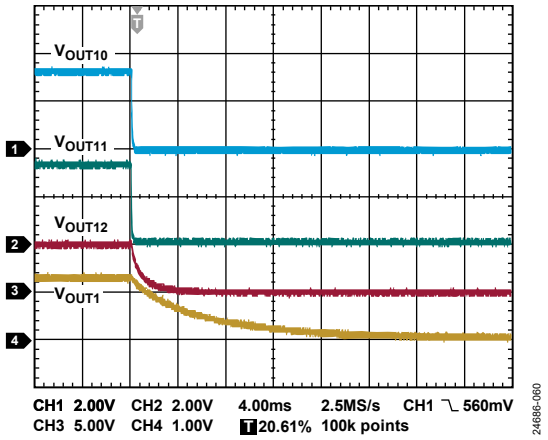

Figure 60. Shutdown with No Load (V_{OUT1} and V_{OUT10} to V_{OUT12})

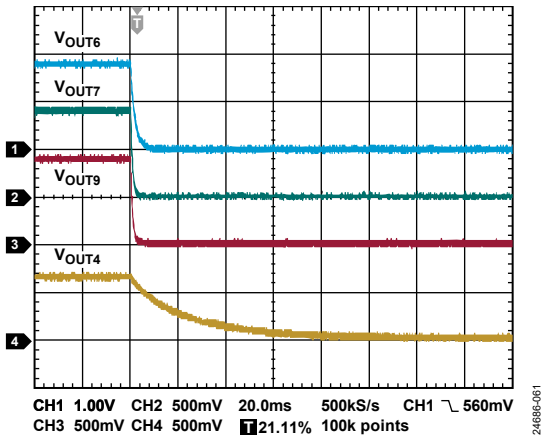

Figure 61. Shutdown with No Load (V_{OUT4}, V_{OUT6}, V_{OUT7}, and V_{OUT9})

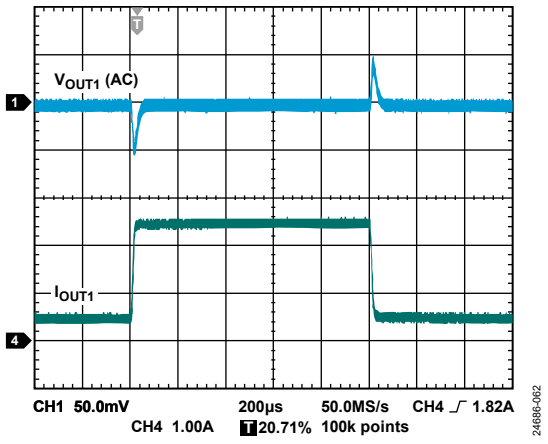

Figure 62. Load Transient Response of BUCK1 (1.27 V), 0.5 A to 2.5 A

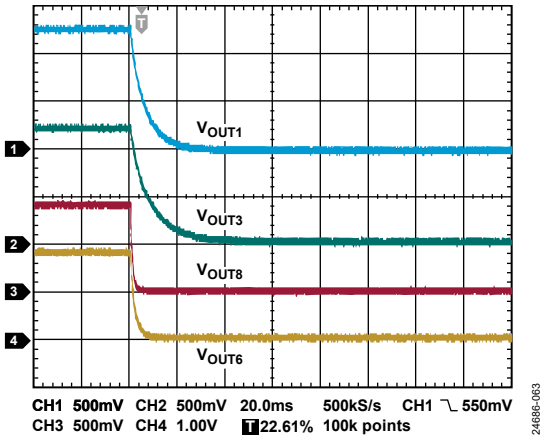

Figure 63. Shutdown with No Load (V_{OUT1}, V_{OUT3}, V_{OUT6}, and V_{OUT8})

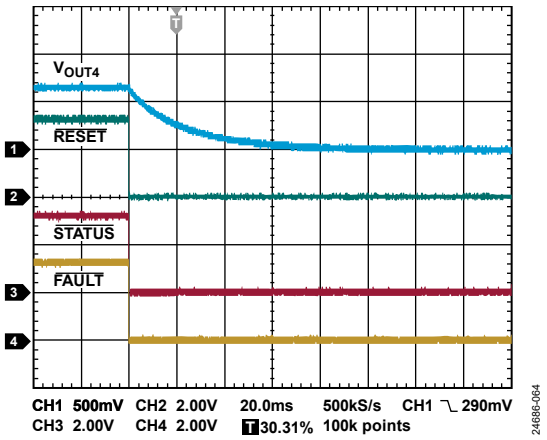

Figure 64. Shutdown with No Load (V_{OUT4}, $\overline{RESET}$, $\overline{STATUS}$, and $\overline{FAULT}$)

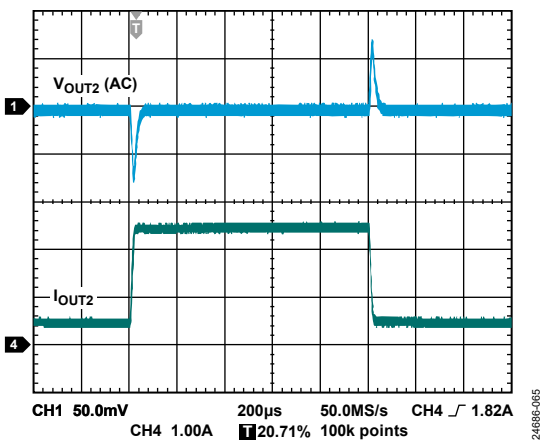

Figure 65. Load Transient Response of BUCK2 (2.1 V), 0.5 A to 2.5 A

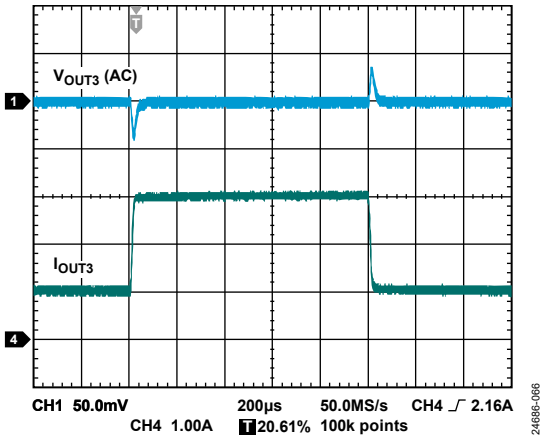

Figure 66. Load Transient Response of BUCK3 (1.2 V), 1 A to 3 A

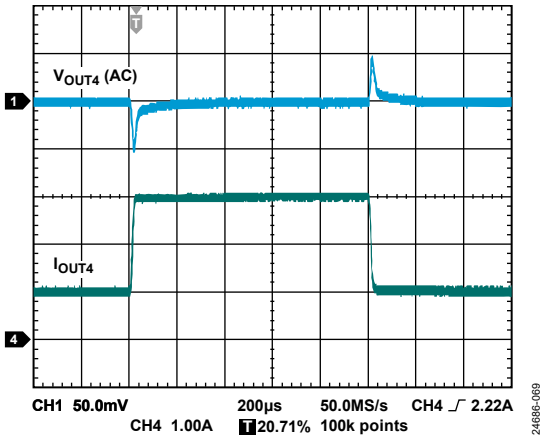

Figure 69. Load Transient Response of BUCK4 (0.65 V), 1 A to 3 A

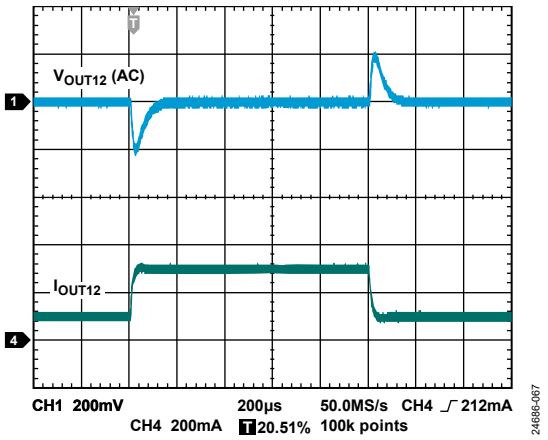

Figure 67. Load Transient Response of Boost (5 V), 0.1 A to 0.3 A

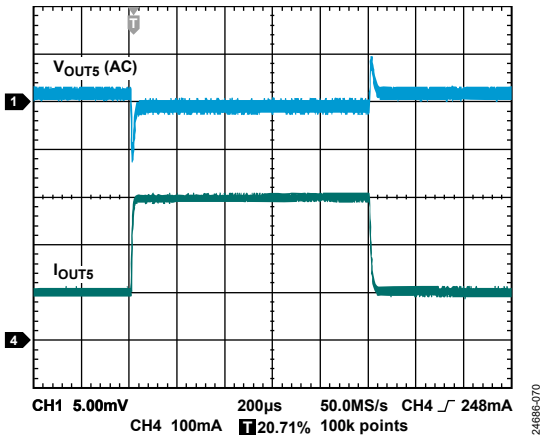

Figure 70. Load Transient Response of LDO1 (1.8 V), 0.1 A to 0.3 A

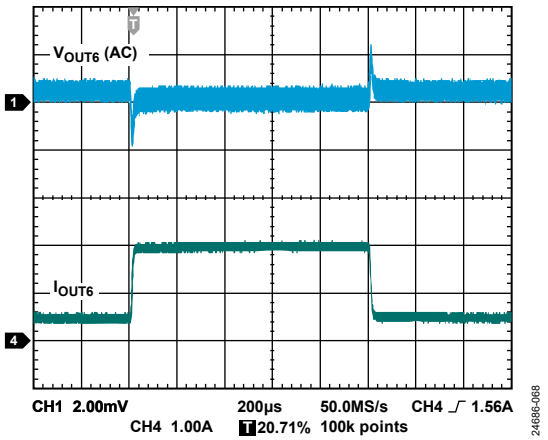

Figure 68. Load Transient Response of LDO2 (1.8 V), 0.5 A to 2 A

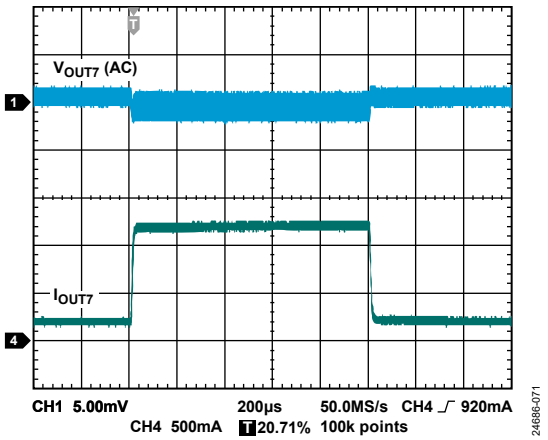

Figure 71. Load Transient Response of LDO3 (0.9 V), 0.2 A to 1.2 A

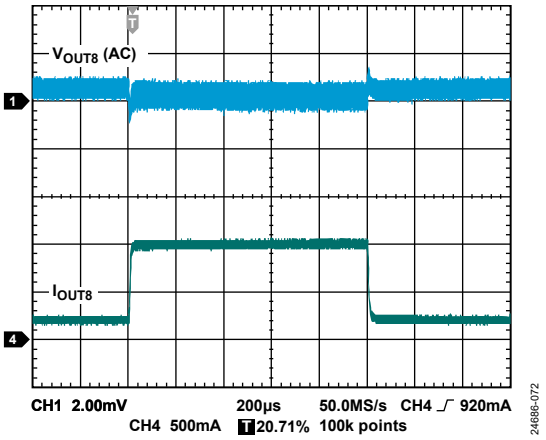

Figure 72. Load Transient Response of LDO4 (0.9 V), 0.2 A to 1 A

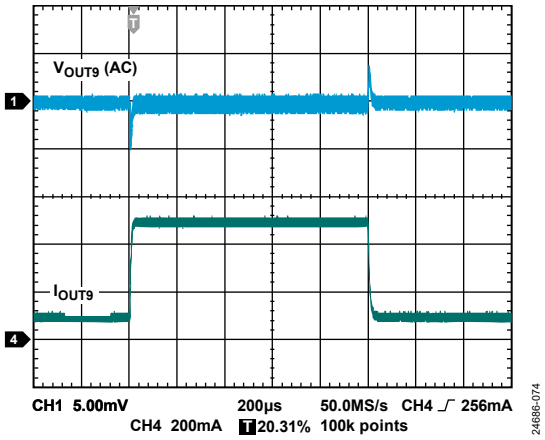

Figure 74. Load Transient Response of LDO5 (0.9 V), 0.1 A to 0.5 A

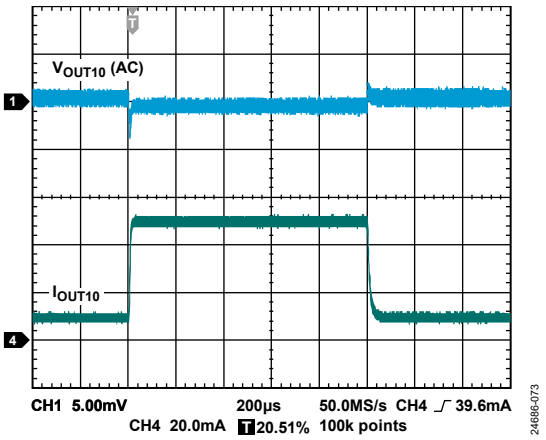

Figure 73. Load Transient Response of LDO6 (3.3 V), 10 mA to 50 mA

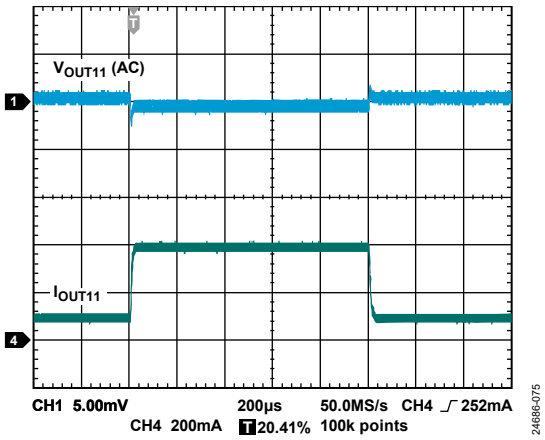

Figure 75. Load Transient Response of LDO7 (3.3 V), 0.1 A to 0.4 A

THEORY OF OPERATION

The ADP5140 is a power management IC that integrates four buck regulators, one boost regulator and seven low noise LDO regulators in a 56-terminal LGA. The device can operate with an input voltage from 2.7 V to 5.5 V and can regulate multiple output voltages in a wide range from 0.55 V to 5 V. The ADP5140 provides an input UVLO feature and monitors the output voltage of each power rail. The device integrates power-up and power-down sequence circuitry, watchdog inputs, and $\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, and $\overline{\text{STATUS}}$ outputs to enhance system reliability. The ADP5140 provides an SPI to achieve fast communication with the processor.

SYNCHRONOUS BUCK REGULATORS

The ADP5140 integrates four high performance, synchronous buck regulators, BUCK1, BUCK2, BUCK3, and BUCK4. Both high-side and low-side metal oxide silicon field effect transistors (MOSFETs) of each buck regulator are integrated into the device. The buck regulators operate with an input voltage from 2.7 V to 5.5 V. BUCK1 and BUCK2 provide an output current of up to 2.5 A, and BUCK3 and BUCK4 provide an output current of up to 3 A.

Control Scheme

The buck regulators in the ADP5140 use a fixed frequency, peak current mode, pulse-width modulation (PWM) control architecture. At the start of each oscillator cycle, the high-side MOSFET turns on and places a positive voltage across the inductor. The inductor current increases until the current sense signal crosses the peak inductor current threshold that turns off the high-side MOSFET and turns on the low-side MOSFET, which places a negative voltage across the inductor and causes the inductor current to reduce. The low-side MOSFET stays on for the remainder of the cycle until the next cycle starts.

Oscillator and Phase Shift

The buck regulators in the ADP5140 run in a 2.2 MHz fixed frequency. BUCK1 to BUCK4 run at an even phase shift, as shown in Figure 76, which reduces the input ripple current and the input voltage spikes to help lower the system EMI.

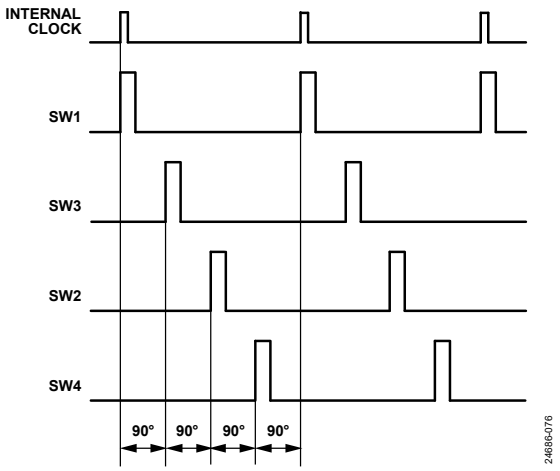

Figure 76. Even Phase Shift Between Buck Regulators

Output Voltage Setting

The BUCK1 output voltage (V_{OUT1}) is either programmed with an external resistor or programmed through the SPI. Connect a resistor (R_{SET1}) between the VSET1 pin and ground to set V_{OUT1} as shown in Table 15.

Table 15. R_{SET1} vs. V_{OUT1}

R_{SET1} (kΩ)	V_{OUT1} (V)
5.62	0.8
7.87	0.85
11	0.9
15.4	0.95
21.5	1.0
30.1	1.05
42.2	1.1
59	1.15
84.5	1.2
115	1.25
162	1.27
232	1.3
316	1.35
475	1.4

Note that R_{SET1} must have ±1% tolerance with a 100 ppm temperature coefficient.

When BUCK1 receives an SPI command to change the output voltage, the SPI command takes over control of the output voltage setting. The BUCK4 output voltage (V_{OUT4}) is programmed through SPI with 0.65 V as the default. Table 16 and Table 17 show the SPI programmable options for V_{OUT1} and V_{OUT4}, respectively.

Table 16. SPI Programmable Options for V_{OUT1}

BUCK1_VOUTSET, Bits[5:0]	V_{OUT1} (V)
000000	0.8
000001	0.81
000010	0.82
000011	0.83
000100	0.84
000101	0.85
000110	0.86
000111	0.87
001000	0.88
001001	0.89
001010	0.9
001011	0.91
001100	0.92
001101	0.93
001110	0.94
001111	0.95
010000	0.96
010001	0.97
010010	0.98
010011	0.99
010100	1
010101	1.01
010110	1.02
010111	1.03
011000	1.04
011001	1.05
011010	1.06
011011	1.07
011100	1.08
011101	1.09
011110	1.1
011111	1.11
100000	1.12
100001	1.13
100010	1.14
100011	1.15
100100	1.16
100101	1.17
100110	1.18
100111	1.19
101000	1.2
101001	1.21
101010	1.22
101011	1.23
101100	1.24
101101	1.25
101110	1.26
101111	1.27
110000	1.28
110001	1.29
110010	1.3
110011	1.31
110100	1.32
110101	1.33
110110	1.34
110111	1.35
111000	1.36
111001	1.37
111010	1.38
111011	1.39
111100	1.4

Table 17. SPI Programmable Options for V_{OUT4}

BUCK4_VOUTSET, Bits[3:0]	V_{OUT4} (V)
0000	0.55
0001	0.60
0010	0.65
0011	0.70
0100	0.75
0101	0.80
0110	0.85
0111	0.90
1000	0.95
1001	1.00
1010	1.05
1011	1.10
1100	1.15
1101	1.20

V_{OUT2} is programmed by an external resistor divider, as shown in Figure 77.

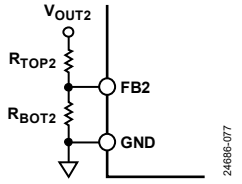

Figure 77. Output Voltage Setting for BUCK2

Use the following equation to set V_{OUT2}:

$$V_{OUT2} = 0.8 \times (1 + (R_{TOP2}/R_{BOT2}))$$

where:
R_{TOP2} is the top resistor of the resistor divider of BUCK2.
R_{BOT2} is the bottom resistor of the resistor divider of BUCK2.
Ensure that the R_{BOT2} resistor value is less than 20 kΩ.

V_{OUT3} is programmed by an external resistor divider, as shown in Figure 78.

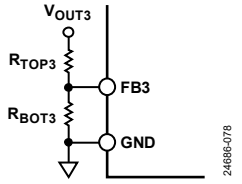

Figure 78. Output Voltage Setting for BUCK3

Use the following equation to set V_{OUT3}:

$$V_{OUT3} = 0.8 \times (1 + (R_{TOP3}/R_{BOT3}))$$

where:
R_{TOP3} is the top resistor of the resistor divider of BUCK3.
R_{BOT3} is the bottom resistor of the resistor divider of BUCK3.
Ensure that the R_{BOT3} resistor value is less than 20 kΩ.

Output DVS Function

BUCK1 and BUCK4 support the dynamic voltage scaling (DVS) function, as shown in Figure 79. The output voltage can be programmed in real time and the interval during the transition is programmable through the SPI, as shown in Table 18. The

output voltage of the DVS ranges from 0.8 V to 1.4 V for BUCK1 with a fixed 10 mV step and from 0.55 V to 1.20 V for BUCK4 with a fixed 12.5 mV step.

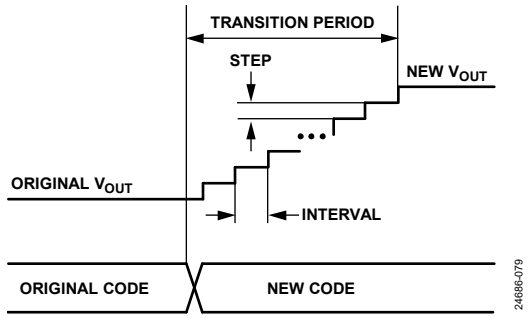

Figure 79. Dynamic Voltage Scaling

Table 18. DVS Interval Options

BUCK1_INTERVAL, Bits[1:0]	BUCK4_INTERVAL, Bits[1:0]	Interval Time (µs)
00 (Default)	00 (default)	10
01	01	20
10	10	30
11	11	40

Buck Regulator Current Limit

The buck regulators have a peak current-limit protection circuit to prevent current runaway. When the peak inductor current reaches the high-side MOSFET current-limit threshold, the high-side MOSFET turns off and the low-side MOSFET turns on. When the low-side MOSFET turns on, the internal circuit continues monitoring the current flowing through the low-side MOSFET. At the end of each clock cycle, if the low-side MOSFET source current is greater than the low-side source current-limit threshold, the high-side MOSFET remains off and the low-side MOSFET remains on for the next cycle. The high-side MOSFET turns on again when the low-side source current is below the low-side source current-limit threshold at the start of a cycle.

The current limitation induces a duty cycle reduction, leads to output voltage drops, and can cause an undervoltage condition. The current limitation does not turn off the buck regulator.

The low-side MOSFET in the buck regulator can sink a current from the load. If the low-side sink current limit is exceeded, both the low-side and high-side MOSFETs turn off until the next cycle starts.

Undervoltage and Overvoltage Protection for Buck Regulator Output Voltages

A window comparator monitors the V_{OUTx} of each buck regulator through each regulator feedback pin (FBx). If the voltage on the feedback pin is outside of the warning or fault window, an output voltage warning or fault event is detected. The window comparator uses a dedicated reference for safety consideration.

The warning or fault threshold of the undervoltage protection and overvoltage protection is programmable through the SPI. Refer to the Feedback Voltage Monitor section for more information.

Buck Regulator Local Temperature Warning

Each buck regulator has a local temperature monitor that provides thermal warning protection. If the local temperature of the buck regulator is higher than the overtemperature threshold, an overtemperature warning event occurs. This warning event is reported in the OT_STATUS register and OT_LATCH register. The buck regulator still functions when an overtemperature warning occurs.

SYNCHRONOUS BOOST REGULATOR

The boost regulator integrates both the main FET and the synchronous FET and runs at a fixed 2.2 MHz switching frequency in phase with BUCK1. The output voltage of the boost regulator is fixed at 5 V and provides a load current of up to 400 mA. The boost regulator has the true shutdown feature that allows the input voltage and the output voltage of the boost regulator to be isolated when the boost regulator is disabled.

Boost Regulator Current Limit

The boost regulator integrates the cycle-by-cycle current-limit circuit to prevent current runaway. When the inductor peak current exceeds the current-limit threshold of the main FET, the main FET turns off and the synchronous FET turns on. The synchronous FET also has negative current protection. If the negative current flowing through the synchronous FET exceeds the negative current-limit threshold, both the main FET and the synchronous FET turn off until the next cycle.

The current-limit feature induces a duty cycle reduction and leads to output voltage drops that can cause an undervoltage condition. The current-limit feature does not turn the boost regulator off.

Undervoltage and Overvoltage Protection for Boost Regulator Output Voltage

A window comparator monitors the output voltage of the boost regulator through the FB12 pin. If the voltage on the FB12 pin is outside of the warning or fault window, an output voltage warning or fault event is detected. The window comparator uses a dedicated reference for safety consideration.

The warning or fault threshold is programmable through the SPI. Refer to the Feedback Voltage Monitor section for more information.

Boost Regulator Local Temperature Warning

A local temperature monitor is integrated into the boost regulator to provide thermal warning protection. If the local temperature of the boost regulator is higher than the overtemperature threshold, an overtemperature warning event occurs. This warning event is reported in the OT_STATUS register and OT_LATCH register. The boost regulator still functions when an overtemperature warning occurs.

LDO REGULATORS

The ADP5140 integrates seven LDO regulators with low dropout voltages and low noise performance. Each LDO regulator has a different input voltage range, different output voltage options, and different output load capabilities.

Each LDO regulator integrates a soft start circuit to reduce the inrush current during power-up.

LDO1 (Regulator 5)

LDO1 is a 300 mA LDO regulator with an input voltage range from 1.7 V to 5.5 V. The output voltage is programmable through the SPI with eight options available: 1.755 V, 1.8 V, 1.845 V, 1.89 V, 1.935 V, 1.98 V, 2.025 V, and 2.070 V. The default output voltage for this regulator is 1.8 V.

LDO1 integrates input undervoltage and overvoltage detection circuits on the corresponding input power supply (V_{PVIN56}). When undervoltage or overvoltage on the input is detected, it is reported in the OTHER1_STATUS register and OTHER1_LATCH register.

LDO2 (Regulator 6)

LDO2 is a high current LDO regulator that provides an output load current of up to 2.3 A. The input voltage range is from 1.7 V to 5.5 V and the output voltage is programmable through the SPI with eight options available: 1.755 V, 1.8 V, 1.845 V, 1.89 V, 1.935 V, 1.98 V, 2.025 V, and 2.070 V. The default output voltage for this regulator is 1.8 V.

LDO2 integrates input undervoltage and overvoltage detection circuits on the corresponding input power supply (V_{PVIN56}). When undervoltage or overvoltage on the input is detected, it is reported in the OTHER1_STATUS register and OTHER1_LATCH register.

LDO3 (Regulator 7)

LDO3 is a high current LDO regulator that provides an output load current of up to 1.4 A. The input voltage range is from 0.9 V to 1.98 V and the output voltage is programmable through the SPI with eight options available: 0.864 V, 0.9 V, 0.936 V, 0.972 V, 1.008 V, 1.044 V, 1.08 V, and 1.116 V. The default output voltage for this regulator is 0.9 V.

LDO3 integrates input undervoltage and overvoltage detection circuits on the corresponding input power supply (V_{PVIN78}). When undervoltage or overvoltage on the input is detected, it is reported in the OTHER1_STATUS register and OTHER1_LATCH register.

LDO4 (Regulator 8)

LDO4 is a high current LDO regulator that provides an output load current of up to 1.2 A. The input voltage range is from 0.9 V to 1.98 V and the output voltage is programmable through the SPI with eight options available: 0.864 V, 0.9 V, 0.936 V, 0.972 V, 1.008 V, 1.044 V, 1.08 V, and 1.116 V. The default output voltage for this regulator is 0.9 V.

LDO4 integrates input undervoltage and overvoltage detection circuits on the corresponding input power supply (V_{PVIN78}). When undervoltage or overvoltage on the input is detected, it is reported in the OTHER1_STATUS register and OTHER1_LATCH register.

LDO5 (Regulator 9)

LDO5 is a low noise LDO regulator that provides an output load current of up to 500 mA. The input voltage range is from 0.9 V to 1.98 V and the output voltage is programmable through the SPI with eight options available: 0.864 V, 0.9 V, 0.936 V, 0.972 V, 1.008 V, 1.044 V, 1.08 V, and 1.116 V. The default output voltage for this regulator is 0.9 V.

LDO5 integrates input undervoltage and overvoltage detection circuits on the corresponding input power supply (V_{PVIN9}). When undervoltage or overvoltage on the input is detected, it is reported in the OTHER1_STATUS register and OTHER1_LATCH register.

LDO6 (Regulator 10)

LDO6 is a 50 mA LDO regulator with an input voltage range from 2.7 V to 5.5 V. The output voltage is programmable through the SPI with four options available: 3.2 V, 3.3 V, 3.35 V, and 3.4 V. The default output voltage for this regulator is 3.3 V.

LDO7 (Regulator 11)

LDO7 is a 400 mA LDO regulator with an input voltage range from 2.7 V to 5.5 V. The output voltage is programmable through the SPI with four options available: 3.2 V, 3.3 V, 3.35 V, and 3.4 V. The default output voltage for this regulator is 3.3 V.

LDO Regulator Current Limits

Each LDO regulator has internal current-limit protection. When the output current exceeds the current-limit threshold, the output current maintains as a constant current while the output voltage is reduced, which can cause an undervoltage event.

Output Undervoltage and Overvoltage Protection for LDO Regulators

A window comparator monitors the output voltage of each LDO regulator through each regulator feedback pin or output pin. If the output voltage is outside of the warning or fault window, an output voltage warning or fault event is detected. The window comparator uses a dedicated reference for safety consideration.

The warning or fault threshold is programmable through the SPI. Refer to the Feedback Voltage Monitor section for more information.

LDO Regulator Local Temperature Warnings

Each LDO regulator has a local temperature monitor that provides thermal warning protection. If the local temperature of the LDO regulator is higher than the overtemperature threshold, an overtemperature warning event occurs. This warning event is reported in the OT_STATUS register and OT_LATCH register. The LDO regulator still functions when an overtemperature warning occurs.

AVIN AND AVDD

The ADP5140 integrates an input UVLO circuit on the input supply. When V_{AVIN} or V_{AVDD} drops below 2.4 V (typical), an input UVLO event is detected, and the device turns off. When the input voltage recovers from the UVLO event, and the input voltage exceeds 2.5 V (typical), the device is active, and a power-on reset (POR) signal generates.

ENABLE FUNCTION

The ADP5140 has an enable pin (EN) to control turning the device on or off. The EN pin has two voltage thresholds, the first stage threshold (V_{EN_RGH}) and the second stage threshold (V_{EN_R}).

When the voltage on the EN pin (V_{EN}) is below V_{EN_RGH}, the device is in shutdown mode.

When V_{EN} is between V_{EN_RGH} and V_{EN_R}, the device can enter initial mode (see the Initial Mode section for more details).

When V_{EN} is above V_{EN_R}, the device exits initial mode and can operate in normal mode (see the Normal Mode section for more details).

An internal pull-down resistor prevents the device from enabling accidentally if the EN pin is left floating.

ACTIVE OUTPUT DISCHARGE

Except for BUCK2 and LDO1, all other buck regulators, LDO regulators, and the boost regulator on the ADP5140 integrate the output discharge function. The discharge function is enabled when a regulator is disabled, which helps discharge the output capacitor quickly.

SYNCHRONIZATION

The SYNC pin can be configured as an input, output, or high impendence pin through the SPI. The default configuration is as a high impedance pin. When the SYNC pin is configured as an output, the pin outputs a clock that is in phase with BUCK1. If the SYNC_DIV bit in the FREQ_CONFG register is set to 0, the frequency on the SYNC pin is equal to the f_{SW} of BUCK1. If the SYNC_DIV bit is set to 1, the frequency on the SYNC pin is equal to 1/5 of the BUCK1 f_{SW}.

When the SYNC pin is configured as an input, connect an external clock ranging from 1.9 MHz to 2.4 MHz to the SYNC pin. The f_{SW} of the buck regulators and boost regulator is synchronized to the external clock applied to the SYNC pin. The f_{SW} of BUCK1 runs in phase with the clock on the SYNC pin. The f_{SW} of all regulators on the ADP5140 clamp at 1.8 MHz if the external clock frequency is too slow and at 2.5 MHz if the external clock frequency is too fast.

When the SYNC pin is configured as an input, the frequency spread spectrum function inside the ADP5140 is disabled.

FREQUENCY SPREAD SPECTRUM

The ADP5140 integrates a triangular frequency spread architecture to reduce system EMI, as shown in Figure 80. The frequency spread spectrum function can be enabled or disabled through the SP_EN bit in the FREQ_CONFG register. The SP_EN bit is disabled by default. The sweep frequency (f_{SF}) and sweep depth (SD) can be programmed through the SPI register, FREQ_CONFG, as shown in Table 19 and Table 20.

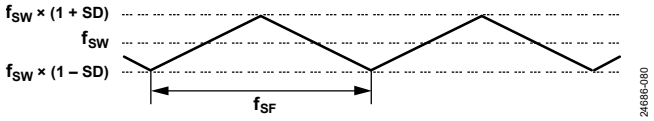

Figure 80. Triangular Spreading

Table 19. Sweep Frequency Option

SF, Bits[5:3]	Sweep Frequency (kHz)
000 (Default)	5
001	10.42
010	15.63
011	20.83
100	25
101	31.25
110	41.67
111	62.5

Table 20. Sweep Depth Option

SD, Bits[8:6]	Sweep Depth (%)
000 (Default)	2
001	4
010	6
011	8
100	10

FEEDBACK VOLTAGE MONITOR

Each power rail has a window comparator to monitor the voltage on the FBx pin. The reference of the FBx window comparator is derived from an independent band gap and is powered by the AVDD pin. The window comparator has two window thresholds: warning and fault. If the output voltage is outside of the warning window or the fault window, a warning or fault event is triggered accordingly, as shown in Figure 81.

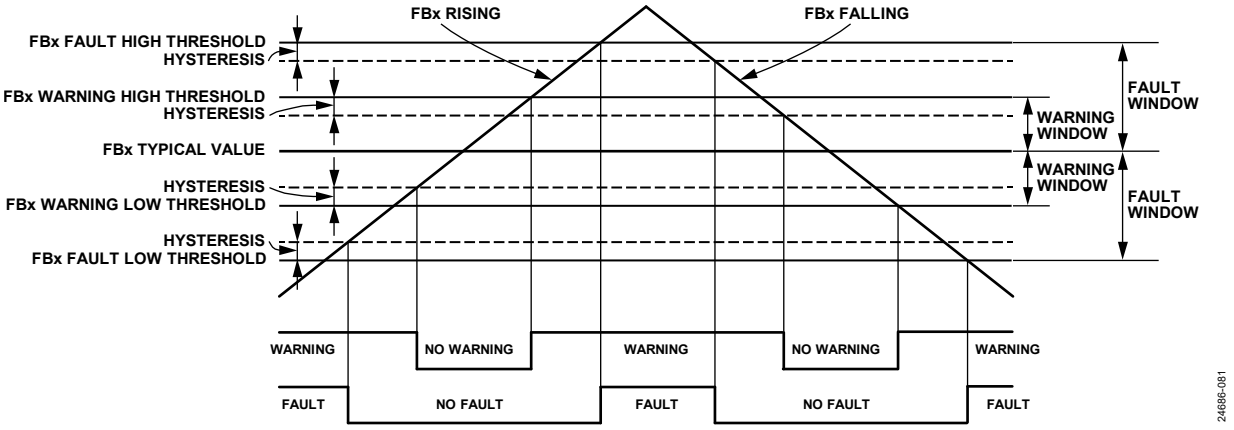

Figure 81. FBx Voltage Window Comparator

If the voltage on the FBx pin is outside of the warning window, the regulator still functions and sets the corresponding warning bit in the WARN_STATUS register and WARN_LATCH register.

If the voltage on the FBx pin is lower than the fault low threshold, the regulator still functions and sets the corresponding x_UV_STATUS bit in the UV_STATUS register and UV_LATCH register.

If the voltage on the FBx pin is higher than the fault high threshold, the regulator turns off and sets the corresponding x_OV_STATUS bit in the OV_STATUS register and OV_LATCH register.

The warning window and fault window are programmable through the FBx_WARN_WINDOW and FBx_FAULT_WINDOW bits in the WARN_WINDOW and FAULT_WINDOW SPI registers. The programmable range is from 4% to 8%, as shown in Table 21 and Table 22, with a fixed hysteresis. These threshold windows are referenced to the normal output voltage on the power rail. See Table 1 for the detailed specification.

Table 21. FBx Voltage Monitor Warning Window

FBx_WARN_WINDOW, Bits[1:0]	Warning Window (%)
00	4
01 (Default)	5
10	6
11	8

Table 22. FBx Voltage Monitor Fault Window

FBx_FAULT_WINDOW, Bits[1:0]	Fault Window (%)
00	4
01	5
10 (Default)	6
11	8

The blank time of the FBx voltage monitor is programmable through the FBx_BLANK_TIME bits in the VOLTAGE_BLANK_TIME0 and VOLTAGE_BLANK_TIME1 SPI registers. The programmable range is from 16 µs to 352 µs, as shown in Table 23.

Table 23. Voltage Monitor Blank Time

FBx_BLANK_TIME, Bits[3:0]	Blank Time (µs)
0000	16
0001	32
0010 (Default)	48
0011	64
0100	80
0101	96
0110	112
0111	128
1000	144
1001	160
1010	176
1011	192
1100	208
1101	240
1110	288
1111	352

VMx VOLTAGE SUPERVISOR

The ADP5140 integrates two voltage supervisors, VM0 and VM1. The VMx voltage supervisors monitor the voltage added on the VMx pin and compare the voltage with the internal 600 mV reference voltage. The voltage monitor function of VMx is disabled by default and can be enabled as a single overvoltage or undervoltage monitor or window monitor according to the VMx_TYP bits settings in the VM_TYP_CONFIGURATION register. The reference of VMx is derived from an independent band gap powered by the AVDD pin.

When VMx is configured as a window monitor, and the voltage on the VMx pin is out of the monitoring window, a warning or fault event is reported in the WARN_STATUS, OV_STATUS, and UV_STATUS registers, and the relevant latch bits in the WARN_LATCH, OV_LATCH, and UV_LATCH registers are set.

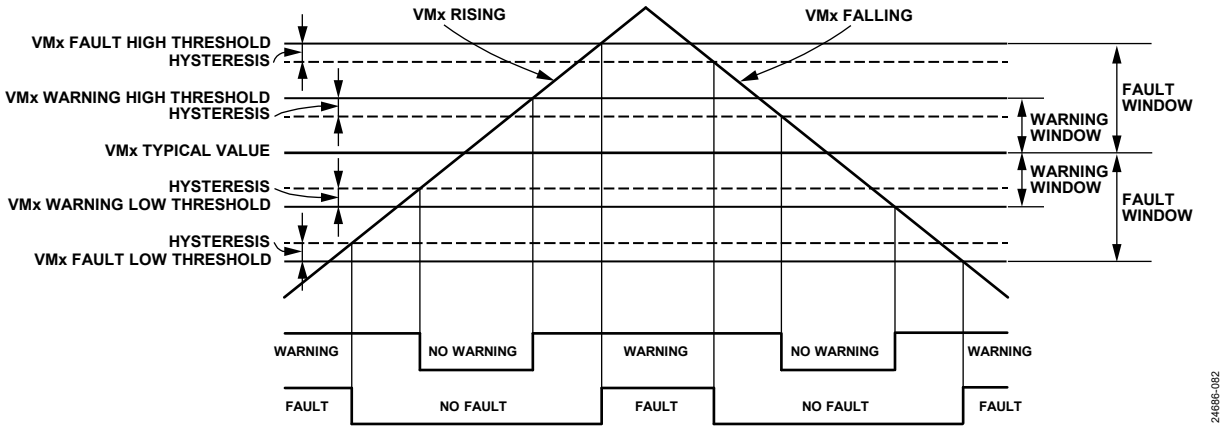

Figure 82. VMx Voltage Window Comparator

The warning and fault threshold windows are programmable through the VMx_WARN_WINDOW bits and VMx_FAULT_WINDOW bits in the WARN_WINDOW and FAULT_WINDOW SPI registers. The programmable range is from 4% to 8%, as shown in Table 24 and Table 25, with a fixed hysteresis. These threshold windows are referenced to 600 mV. See Table 1 for the detailed specification.

Table 24. VMx Voltage Monitor Warning Window

VMx_WARN_WINDOW, Bits[1:0]	Warning Window (%)
00	4
01 (Default)	5
10	6
11	8

Table 25. VMx Voltage Monitor Fault Window

VMx_FAULT_WINDOW, Bits[1:0]	Fault Window (%)
00	4
01	5
10	6
11 (Default)	8

The blank time of the VMx pin is programmable through the VMx_BLANK_TIME bits in the VOLTAGE_BLANK_TIME0 SPI register. The programmable range is from 16 µs to 352 µs with 48 µs as the default, as shown in Table 26.

Table 26. VMx Voltage Monitor Blank Time

VM_BLANK_TIME, Bits[2:0]	Blank Time (µs)
0000	16
0001	32
0010 (Default)	48
0011	64
0100	80
0101	96
0110	112
0111	128
1000	144
1001	160
1010	176
1011	192
1100	208
1101	240
1110	288
1111	352

MODE PIN SETTING

The ADP5140 has a MODE pin to set different functions with different resistances between the MODE pin and ground. Three functions are available: debug mode setting, device index setting, and V_{IO} selecting. Table 27 shows the relationship of the resistance between the MODE pin and ground (R_{MODE}) and the function settings.

Table 27. MODE Pin Setting

R_{MODE} (kΩ)	Debug Mode	Device Index	V_{IO} (V)
12.1	Enable	0	1.8
15.0	Enable	0	3.3
19.1	Enable	1	1.8
23.7	Enable	1	3.3
29.4	Disable	0	1.8
36.5	Disable	0	3.3
45.3	Disable	1	1.8
57.6	Disable	1	3.3
73.2	Enable	2	1.8
90.9	Enable	2	3.3
118	Enable	3	1.8
147	Enable	3	3.3
182	Disable	2	1.8
237	Disable	2	3.3
309	Disable	3	1.8
464	Disable	3	3.3

The debug function enables or disables debug mode. When in debug mode, all faults related to watchdogs are ignored.

The device index setting function sets the device index for the ADP5140. Four device indexes can be set with different resistance between the MODE pin and ground. See the SPI section for more information.

Use the I/O voltage selection function to select the I/O voltage. The ADP5140 supports a 1.8 V or 3.3 V I/O supply voltage.

An SPI register, MODE_PIN_STATUS, records the MODE pin configuration and is readable through the SPI.

V_{IO} SUPPLY

V_{IO} provides the power supply for the digital interface on the ADP5140. The VIO pin supports a voltage of either 3.3 V or 1.8 V, and the resistance between the MODE pin and ground determines which voltage is supported.

The VIO pin has a UVLO monitoring circuit. If V_{IO} is below the VIO UVLO threshold, an input and output UVLO fault event occurs. The ADP5140 sets the VIO_UVLO_STATUS bit in the UV_STATUS register and the VIO_UVLO_LATCH bit in the UV_LATCH register.

WAKE-UP FUNCTION AND EXTERNAL EVENT DETECTION

The WAKE pin supports either the wake-up function or the external event detection function, depending on the configuration in the WAKEPIN_EVT SPI register. The WAKE pin default setting is the wake-up function.

When configured for the wake-up function, a low voltage level on the WAKE pin wakes up the ADP5140 and the device exits standby mode (see the Standby Mode section for more information). The wake-up function is effective only in standby mode.

When configured for the external event detection function, a low voltage level with a duration time longer than the deglitch time (t_{D_WAKE}) on the WAKE pin sets a latch event in the ADP5140. This latch event is reflected on the $\overline{\text{RESET}}$, $\overline{\text{STATUS}}$, or $\overline{\text{FAULT}}$ pin depending on the SPI settings.

An internal 1 MΩ pull-down resistor keeps the voltage on the WAKE pin below the WAKE low voltage threshold (see Table 1) when the WAKE pin is left floating.

WATCHDOG

The ADP5140 integrates two window watchdogs, Watchdog 0 (WD0) and Watchdog 1 (WD1), and one QA watchdog (QA_WD). WD0 and WD1 are fed through the WDI0 pin and WDI1 pin. QA_WD is fed through the SPI, which detects the software fault of the processor.

Window Watchdog

There are three trigger modes that feed each window watchdog from the WDIx pin: rising edge trigger, falling edge trigger, or both rising and falling edge trigger, as shown in Figure 83, Figure 84, and Figure 85, respectively. The WDTx_TRIG_EDGE_SEL bits in the WDTx_CTRL register determine the trigger mode for the window watchdog.

Table 28. Window Watchdog Trigger Edge Configuration

WDTx_TRIG_EDGE_SEL, Bits[1:0]	Trigger Edge
00	Both edges
01 (Default)	Rising edge
10	Falling edge
11	Both edge

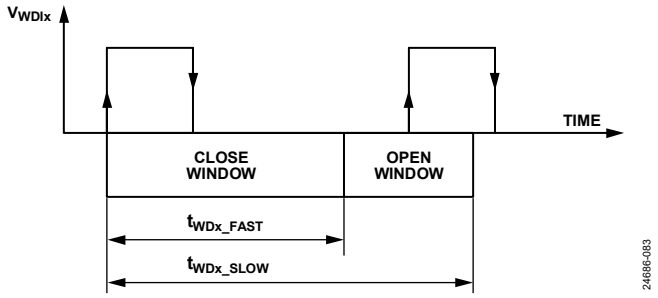

Figure 83. Rising Edge Signal Triggers WDx

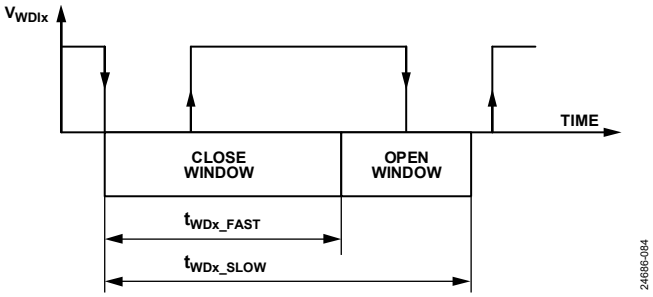

Figure 84. Falling Edge Signal Triggers WDx

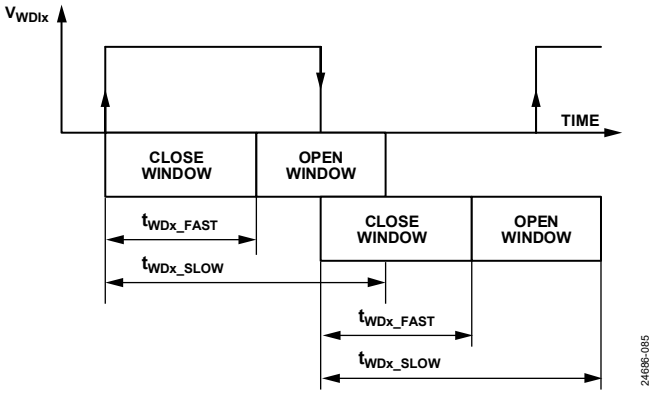

Figure 85. Both Rising and Falling Edge Signals Trigger WDx (V_{WDIx} is the Voltage on the WDx Pin)

When the window watchdog is enabled, the watchdog monitors the trigger edge on the WDIx pin. The window watchdog timer resets at the trigger edge or when the window watchdog timer expires if no feeding occurs within the slow window time. The trigger edge of the WDIx signal must fit into the open window between the watchdog fast window (t_{WDx_FAST}) and the watchdog slow window (t_{WDx_SLOW}). If the trigger edge of the WDIx signal appears outside of the open window, a bad watchdog feed event occurs, and the watchdog fault counter (the WDTx_FAULT_COUNTER bits in the WDTx_STATUS register) increments. If the trigger edge of the WDIx signal appears within the open window, a good watchdog feed event occurs and the watchdog fault counter decrements. If the watchdog fault counter value is equal to or higher than the watchdog fault threshold value (the WDTx_FAULT_THRESHOLD bits in the WDTx_CTRL register), a window watchdog fault event occurs, which sets the relevant watchdog fail bit in the OTHER_STATUS register and OTHER_LATCH register.

Window Watchdog Fault Counter

The window watchdog fault counter has overflow saturation and underflow saturation. When the window watchdog fault counter is 7, the counter remains at 7 if a bad watchdog feed event occurs. When the window watchdog fault counter is 0, the counter remains at 0 if a good watchdog feed event occurs. The window watchdog fault counter resets when the AVIN voltage goes below the UVLO threshold or when the watchdog is re-enabled from the disable status.

Window Watchdog Window Setting

t_{WDx_FAST} and t_{WDx_SLOW} are programmable through the SPI and the equations to calculate the values are as follows:

$$t_{WDx\_FAST} = WDTx\_FAST\_WINDOW \times Time\ Tick$$

$$t_{WDx\_SLOW} = WDTx\_SLOW\_WINDOW \times Time\ Tick$$

where:
WDTx_FAST_WINDOW is the value of the WDTx_FAST_WINDOW bits in the WDTx_WINDOW register in decimal form, and the default value is 3750.
WDTx_SLOW_WINDOW is the value of the WDTx_SLOW_WINDOW bits in the WDTx_WINDOW register in decimal form, and the default value is 15,000.
Time Tick is determined by the internal 2 MHz clock and the scale factor, as follows:

$$Time\ Tick = SCALE\_FACTOR/2\ MHz$$

where:
SCALE_FACTOR depends on the WDTx_PRE_SCALE bits setting in the WDTx_CTRL register. The default value is 16, as shown in Table 29.

Table 29. Window Watchdog Scale Factor and Time Tick

WDTx_PRE_SCALE, Bits[1:0]	SCALE_FACTOR	Time Tick (µs)
00	1	0.5
01 (Default)	16	8
10	256	128
11	4096	2048

The default values of t_{WDx_FAST} and t_{WDx_SLOW} are 30 ms and 120 ms, respectively.

The window watchdog needs 2× the time ticks duration time to reset. Set t_{WDx_FAST} and t_{WDx_SLOW} to no less than 40× the time ticks to keep the accuracy of the fast window and slow window at <5%.

Window Watchdog SPI Feeding

Besides using the WDIx signal to feed the window watchdog, the user can also write an SPI command to the WDTx_SPI_FEED bits in the WDTx_CTRL register to reset the watchdog timer. Write 0x51 to the WDT0_SPI_FEED bits to reset the WD0 timer. Write 0x52 to the WDT1_SPI_FEED bits to reset the WD1 timer.

WD0 and WD1 are disabled by default and can be enabled through the SPI. The WDTx_EN_CTRL bit in the WDTx_CTRL register controls the window watchdogs. Set the WDTx_EN_CTRL bit to enable the window watchdog and allow the internal watchdog timer to start counting immediately. Clear the WDTx_EN_CTRL bit to disable the window watchdog.

Window Watchdog Synchronization

The first feed signal is used for synchronization. As long as the first feed signal is within the slow window, there is no increment or decrement on the window watchdog fault counter, and the watchdog timer resets. If the first feed signal does not come within the slow window, the watchdog timer expires, the watchdog timer resets, and the watchdog fault counter increments. The window watchdog still waits for the first feed signal and treats the first feed signal as described in this section.

QA Watchdog

The ADP5140 integrates a QA watchdog fed through the SPI. The QA watchdog can detect software faults of the processor.

The QA_WD_EN_CTRL bit in the QA_WD_CTRL register controls the QA watchdog. Set the QA_WD_EN_CTRL bit to enable the QA watchdog, or clear the QA_WD_EN_CTRL bit to disable the QA watchdog. The default value of the QA_WD_EN_CTRL bit is 1 (enabled).

When initialization is complete, the QA watchdog generates a token and a corresponding watchdog internal answer. The QA watchdog requires the processor to read the token through the QA_WD_TOKEN register and then send back the calculated answer by writing to the QA_WD_ANSWER register. Table 30 shows the relationship between the token and answer.

Table 30. Relationship Between Token and Answer

QA_WD_TOKEN, Bits[3:0]	QA_WD_ANSWER, Bits[31:0]
0x0	0x000FF0FF
0x1	0xE3EC131C
0x2	0x9B946B64
0x3	0x78778887
0x4	0x5659A6A9
0x5	0xB5BA454A
0x6	0xCDC23D32
0x7	0x2E21DED1
0x8	0x2D22DDD2
0x9	0xCEC13E31
0xA	0xB6B94649
0xB	0x555AA5AA
0xC	0x7B748B84
0xD	0x98976867
0xE	0xE0EF101F
0xF	0x030CF3FC

The interaction between QA watchdog and the processor follows the sequence diagram shown in Figure 86.

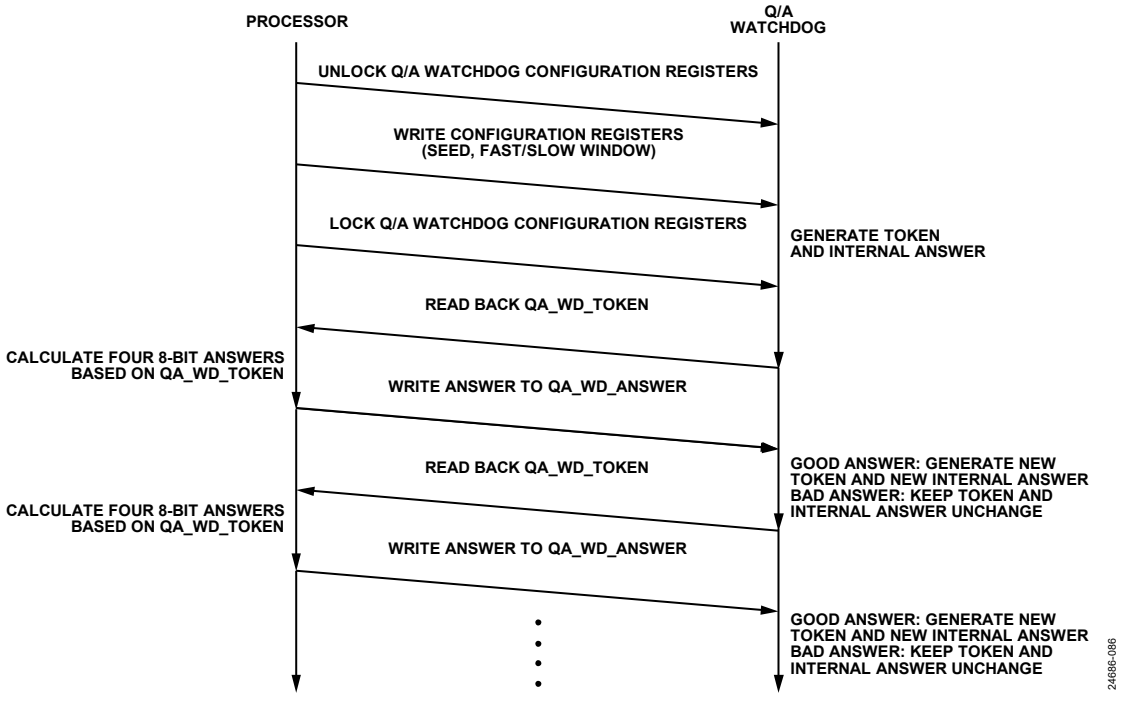

Figure 86. QA Watchdog and Processor Interaction Sequence Diagram

The QA watchdog waits for the answer from the processor. When the QA watchdog receives the answer from the processor, the watchdog compares the answer to the internal answer. If the two answers match, a good answer flag is set. If the two answers do not match, a bad answer flag is set. The answer from the processor must fit into the open window between $t_{WD\_QA\_FAST}$, and $t_{WD\_QA\_SLOW}$ as shown in Figure 87. The QA watchdog timer resets when it gets a good answer or the watchdog timer expires (no good feeding within $t_{WD\_QA\_SLOW}$). A bad answer does not reset the QA watchdog timer. The bad answer is treated as no feed.

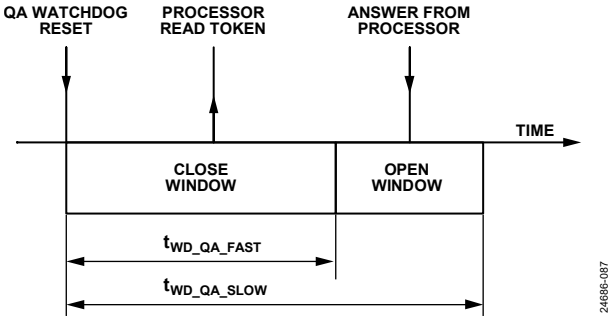

Figure 87. QA Watchdog Operation Sequence

QA Watchdog Fault Counter

The four possible QA watchdog fault situations include the following:

- The ADP5140 receives a good answer within the open window. A good QA watchdog feed event occurs, and the QA watchdog fault counter (QA_WD_FAULT_COUNTER bits in the QA_WD_STATUS register) decrements.
- The ADP5140 receives a good answer but the feeding time is outside the open window. A bad QA watchdog feed event occurs, and the QA watchdog fault counter increments.
- The ADP5140 receives a bad answer, no matter if the feeding time is within or outside the open window. This instance is treated as a no feed event, and the QA watchdog fault counter remains unchanged.
- The ADP5140 receives no answer within the slow window time. A bad QA watchdog feed event occurs, and the QA watchdog fault counter increments.

If the QA watchdog fault counter value is equal to or higher than the QA watchdog fault threshold value, a QA watchdog fault event occurs, and the relevant QA watchdog fail bit in the OTHER_STATUS register and OTHER_LATCH register is set.

The QA watchdog fault counter has overflow saturation and underflow saturation. When the QA watchdog fault counter is 7, the counter remains at 7 if a bad QA watchdog feed event occurs. When the QA watchdog fault counter is 0, the counter remains at 0 if a good QA watchdog feed event occurs. The QA watchdog fault counter resets when V_{AVIN} is less than the UVLO threshold or when the QA watchdog is re-enabled from the disable status.

QA Watchdog Window Setting

$t_{WD\_QA\_FAST}$ and $t_{WD\_QA\_SLOW}$ are programmable through the SPI and the equations are as follows:

$$t_{WD\_QA\_FAST} = QA\_WD\_FAST\_WINDOW \times QA\ Time\ Tick$$

$$t_{WD\_QA\_SLOW} = QA\_WD\_SLOW\_WINDOW \times QA\ Time\ Tick$$

where:
QA_WD_FAST_WINDOW is the value of the QA_WD_FAST_WINDOW bits in the QA_WD_WINDOW register in decimal form, and the default value is 0.
QA_WD_SLOW_WINDOW is the value of the QA_WD_SLOW_WINDOW bits in the QA_WD_WINDOW register in decimal form, and the default value is 7813.
QA Time Tick is determined by the internal 2 MHz clock and the QA scale factor, as follows:

$$QA\ Time\ Tick = QA\_SCALE\_FACTOR/2\ \text{MHz}$$

where:
QA_SCALE_FACTOR depends on the QA_WD_PRE_SCALE bits setting in the QA_WD_CTRL register. The default value of the QA scale factor is 256, as shown in Table 31.

Table 31. QA Watchdog Scale Factor and Time Tick

QA_WD_PRE_SCALE, Bits [1:0]	QA_SCALE_FACTOR	QA Time Tick (µs)
00	1	0.5
01	16	8
10 (Default)	256	128
11	4096	2048

The default values of $t_{WD\_QA\_FAST}$ and $t_{WD\_QA\_SLOW}$ are 0s and 1s, respectively.

The QA watchdog needs 2× the QA time ticks duration time to reset. Set $t_{WD\_QA\_FAST}$ and $t_{WD\_QA\_SLOW}$ to no less than 40× the QA time ticks to keep the accuracy of the fast window and slow window at less than 5%.

QA Watchdog Synchronization

The first feed signal is used for synchronization. As long as the first feed signal is within the slow window, there is no increment or decrement on the QA watchdog fault counter, and the QA watchdog timer resets. If the first feed signal does not come within the slow window, the QA watchdog timer expires and resets, and the QA watchdog fault counter increments. The QA watchdog still waits for the first feed signal and treats the first feed signal as described in this section.

The QA_WD_TOKEN register and QA_WD_ANSWER register are not controlled by the lock and unlock method and can be directly written or read without writing the correct key to the PMIC_PSWD register.

Watchdog Parameters Configuration

Parameters related to the watchdogs can be programed through the SPI, and the new value takes effect when the next feed signal arrives.

The watchdog configuration related registers are locked by default. To unlock these registers, write 1 to the WDTx_LOCK bit or the QA_WD_LOCK bit in the WDTx_CTRL register or QA_WD_CTRL register, respectively.

To change the watchdog configuration safely, take the following steps:

1. Wait until the open window arrives.
2. Feed the watchdog.
3. Unlock the watchdog configuration registers and change the register values.
4. Wait until the open window arrives.
5. Feed the watchdog so that the new parameters take effect.

PULSE WIDTH MONITOR

The ADP5140 integrates the pulse width monitor circuit to monitor the pulse width of the signal on the WDIx pins. The pulse width monitor circuit is disabled by default and can be enabled through the SPI. The WDIx_PULSE_EN bit in the WDIx_PULSE_CTRL register controls the pulse width monitor circuit. Set the WDIx_PULSE_EN bit to enable the pulse width monitor, and clear the WDIx_PULSE_EN bit to disable the pulse width monitor.

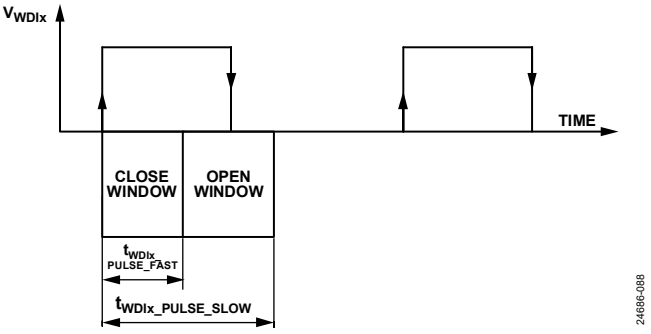

Figure 88. Positive Pulse Width Monitoring

When the pulse width monitor function is enabled, a rising edge on the WDIx pin resets the pulse width timer and starts counting until there is a falling edge on the WDIx pin.

The two possible cases for the pulse width monitor fault are as follows:

- If the pulse width is smaller than the fast pulse width ($t_{WDIx\_PULSE\_FAST}$) and the WDIx_PULSE_LOWER_MASK bit in the WDIx_PULSE_CTRL register is 0, a pulse width fault event occurs.
- If the pulse width is larger than the slow pulse width ($t_{WDIx\_PULSE\_SLOW}$) and the WDIx_PULSE_UPPER_MASK bit in the WDIx_PULSE_CTRL register is 0, a pulse width fault event occurs.

When the pulse width fault event occurs, the relevant bits in the OTHER_STATUS register and the OTHER_LATCH register are set.

$t_{WDIx\_PULSE\_FAST}$ and $t_{WDIx\_PULSE\_SLOW}$ are programmable through the SPI, and the equations to calculate the values are as follows:

$$t_{WDIx\_PULSE\_FAST} = WDIx\_PULSE\_LOW \times (1 \div 2\ MHz)$$

$$t_{WDIx\_PULSE\_SLOW} = WDIx\_PULSE\_HIGH \times (1 \div 2\ MHz)$$

where:
WDIx_PULSE_LOW is the WDIx_PULSE_LOW register value in decimal format, and the default value is 850.
WDIx_PULSE_HIGH is the WDIx_PULSE_HIGH register value in decimal format, and the default value is 1150.
The default values of $t_{WDIx\_PULSE\_FAST}$ and $t_{WDIx\_PULSE\_SLOW}$ are 425 µs and 575 µs, respectively.

WDIx PIN AS EXTERNAL EVENTS DETECTION

The WDIx pin can be configured as an external event detection pin. When configured for the external event detection function, a low voltage level with a duration time longer than 8 µs on the WDIx pin sets a latch event in the ADP5140. This latch event is reflected on the $\overline{\text{RESET}}$, $\overline{\text{STATUS}}$, or $\overline{\text{FAULT}}$ pin, depending on the SPI settings.

An internal 1 MΩ pull-down resistor keeps the voltage on the WDIx pin below the WDIx low voltage threshold (see Table 1) when the WDIx pin is left floating.

TSD

Besides the local temperature monitor of each regulator, the ADP5140 also monitors the central die temperature. If the central die temperature exceeds the TSD threshold (T_{SD}), the ADP5140 enters shutdown mode. T_{SD_HY} is included so that the ADP5140 does not recover from shutdown mode until the central die temperature drops below $T_{SD} - T_{SD\_HY}$. Upon recovery, a POR initiates.

$\overline{\text{RESET}}$, $\overline{\text{STATUS}}$, AND $\overline{\text{FAULT}}$ FAIL-SAFE PINS

$\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ pin is an open-drain, bidirectional pin. The $\overline{\text{RESET}}$ pin is asserted when an event listed in the status registers occurs, and the corresponding bit in the appropriate mask registers is set to 1.

The status registers include the following:

- UV_STATUS
- OV_STATUS
- WARN_STATUS
- OT_STATUS
- OTHER_STATUS
- OTHER1_STATUS

The mask registers include the following:

- UV_RST_MASK
- OV_RST_MASK
- WARN_RST_MASK
- OT_RST_MASK
- OTHER_RST_MASK
- OTHER1_RST_MASK

When the $\overline{\text{RESET}}$ pin is asserted, the pin is pulled low for a reset period time (t_{RP}) and then released. When the $\overline{\text{RESET}}$ pin is asserted, both the $\overline{\text{FAULT}}$ pin and $\overline{\text{STATUS}}$ pin are pulled low.

An external low voltage level with a duration time longer than the reset external timeout period (t_{RESET_EXT}) on the $\overline{\text{RESET}}$ pin sets an external pin fail event in the ADP5140. This fail event is reflected on the $\overline{\text{RESET}}$, $\overline{\text{STATUS}}$, or $\overline{\text{FAULT}}$ pin, depending on the SPI register settings.

If a reset external pin fail event occurs and the $\overline{\text{RESET}}$_EXT_FAIL_RST_MASK bit in the OTHER_RST_MASK register is set to 1, the ADP5140 initiates a reset sequence. All power rails restart with the programmed power-up sequence.

The reset external timeout period is programmable through the SPI FAIL_SAFE_PIN_TIMEOUT register from 5 µs to 160 µs with a 5 µs step.

During power-up, the $\overline{\text{RESET}}$ pin does not pull high until all of the following conditions are met and are followed by a t_{HOLD} delay, as shown in Figure 89:

- Regulator 1 (BUCK1) is in regulation.
- Regulator 2 (BUCK2) is in regulation.
- Regulator 5 (LDO1) is in regulation.
- Regulator 10 (LDO6) is in regulation.
- Regulator 11 (LDO7) is in regulation.
- Regulator 12 (boost) is in regulation.
- SEQ is high.
- No other system fault event that is mapped on the $\overline{\text{RESET}}$ pin occurs.

$\overline{\text{STATUS}}$ Pin

The $\overline{\text{STATUS}}$ pin is an open-drain, bidirectional pin. The $\overline{\text{STATUS}}$ pin is asserted (pull low) as long as the latch bit is set to 1 in the appropriate latch registers, and the corresponding bits in the appropriate status pin mask registers are set to 1.

The latch registers include the following:

- UV_LATCH
- OV_LATCH
- WARN_LATCH
- OT_LATCH
- OTHER_LATCH
- OTHER1_LATCH

Status pin mask registers include the following:

- UV_INT_MASK
- OV_INT_MASK
- WARN_INT_MASK
- OT_INT_MASK
- OTHER_INT_MASK
- OTHER1_INT_MASK

An external low voltage level with a duration time longer than the status external time out period (t_{STATUS_EXT}) on the $\overline{\text{STATUS}}$ pin sets an external pin fail event in the ADP5140. This fail event is reflected on the $\overline{\text{RESET}}$, $\overline{\text{STATUS}}$, or $\overline{\text{FAULT}}$ pin, depending on the SPI register settings.

The status external timeout period is programmable through the SPI FAIL_SAFE_PIN_TIMEOUT register from 5 µs to 160 µs with a 5 µs step. When the $\overline{\text{RESET}}$ pin is asserted, the $\overline{\text{STATUS}}$ pin is pulled low.

The $\overline{\text{STATUS}}$ pin is also controllable through the SPI directly through the SPI_PIN_CTRL register while ignoring the latch and mask register settings. When the $\overline{\text{STATUS}}$_SPI_CTRL_EN bit is set to 1, the $\overline{\text{STATUS}}$ pin is controlled by the $\overline{\text{STATUS}}$_SPI_CTRL_DATA bit value.

$\overline{\text{FAULT}}$ Pin

The $\overline{\text{FAULT}}$ pin is an open-drain, bidirectional pin. The $\overline{\text{FAULT}}$ pin is asserted (pull low) as long as the latch bit is set to 1 in the latch registers, and the corresponding bits in the appropriate fault pin mask registers are set to 1.

See the $\overline{\text{STATUS}}$ Pin section for the list of latch registers used.

The fault pin mask registers include:

- UV_FAULT_MASK
- OV_FAULT_MASK
- WARN_FAULT_MASK
- OT_FAULT_MASK
- OTHER_FAULT_MASK
- OTHER1_FAULT_MASK

An external low voltage level with a duration time longer than the fault external timeout period (t_{FAULT_EXT}) on the $\overline{\text{FAULT}}$ pin sets an external pin fail event in the ADP5140. This fail event is reflected on the $\overline{\text{RESET}}$, $\overline{\text{STATUS}}$, or $\overline{\text{FAULT}}$ pin, depending on the SPI register settings.

The fault external time out period is programmable through SPI FAIL_SAFE_PIN_TIMEOUT register from 5 µs to 160 µs with a 5 µs step. When the $\overline{\text{RESET}}$ pin is asserted, the $\overline{\text{FAULT}}$ pin is pulled low.

The $\overline{\text{FAULT}}$ pin is also controllable through the SPI directly through the SPI_PIN_CTRL register while ignoring the latch and mask register settings. When the $\overline{\text{FAULT}}$_SPI_CTRL_EN bit is set to 1, the $\overline{\text{FAULT}}$ pin is controlled by the $\overline{\text{FAULT}}$_SPI_CTRL_DATA bit value.

POWER-UP AND POWER-DOWN SEQUENCES

All regulators in the ADP5140 integrate a soft start circuit to reduce the inrush current on the input voltage during startup.

Power-Up Sequence

A fixed power-up sequence, as shown in Figure 89, is applied to all regulators when enabled. There is a typical 3 ms (t_D) delay for the ADP5140 initial and self test time, and t_{DR1} or t_{DR2} delays between each rail.

Regulator 10 and Regulator 11 power up at the same time.

Regulator 12 does not power up until both Regulator 10 and Regulator 11 are above the fault low threshold followed by thee t_{DR2} delay time.

The SEQ pin controls the power-up sequence. When the Regulator 1 powers up, the other power rails on the ADP5140 do not ramp up until the SEQ pin goes high.

Regulator 3 does not power up until Regulator 1 is above the fault low threshold followed by the t_{DR1} delay time, and the SEQ pin is high.

The $\overline{\text{RESET}}$ pin does not pull high until all of the following conditions are met and are followed by a t_{HOLD} delay:

- Regulator 1 is in regulation.
- Regulator 2 is in regulation.
- Regulator 5 is in regulation.
- Regulation 10 is in regulation.
- Regulation 11 is in regulation.
- Regulation 12 is in regulation.
- SEQ is high.
- No other system fault event is mapped on the $\overline{\text{RESET}}$ pin occurs.

The $\overline{\text{FAULT}}$ and $\overline{\text{STATUS}}$ pins keep low until all power rails are above the fault low threshold and the $\overline{\text{RESET}}$ pin is released.

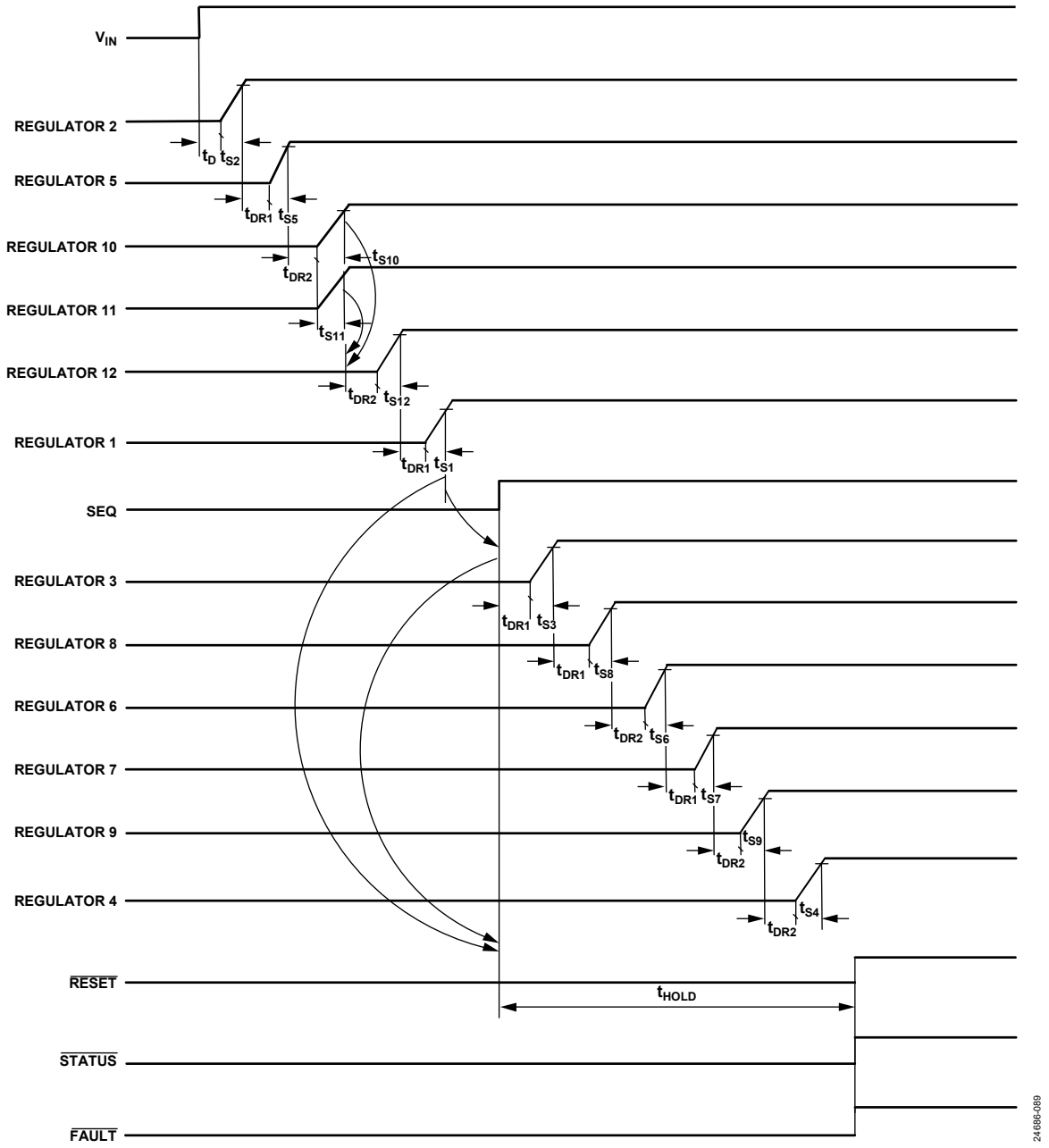

Figure 89. ADP5140 Power-Up Sequence

Power-Down Sequence

When the ADP5140 receives the SPI command to power off (power-down mode (SPI_CMD1)), all power rails turn off at the same time except for Regulator 2 and Regulator 5. Regulator 2 and Regulator 5 do not power off until the output voltage of Regulator 11 is below VM_{DW}, as shown in Figure 90.

If the input voltage on the AVIN pin is below the AVIN UVLO falling threshold or Regulator 11 is disabled, a fast discharge switch turns on in Regulator 11. The fast discharge switch is a 2 Ω MOSFET between the OUT11 pin and ground, and the gate driver comes from the OUT11 pin.

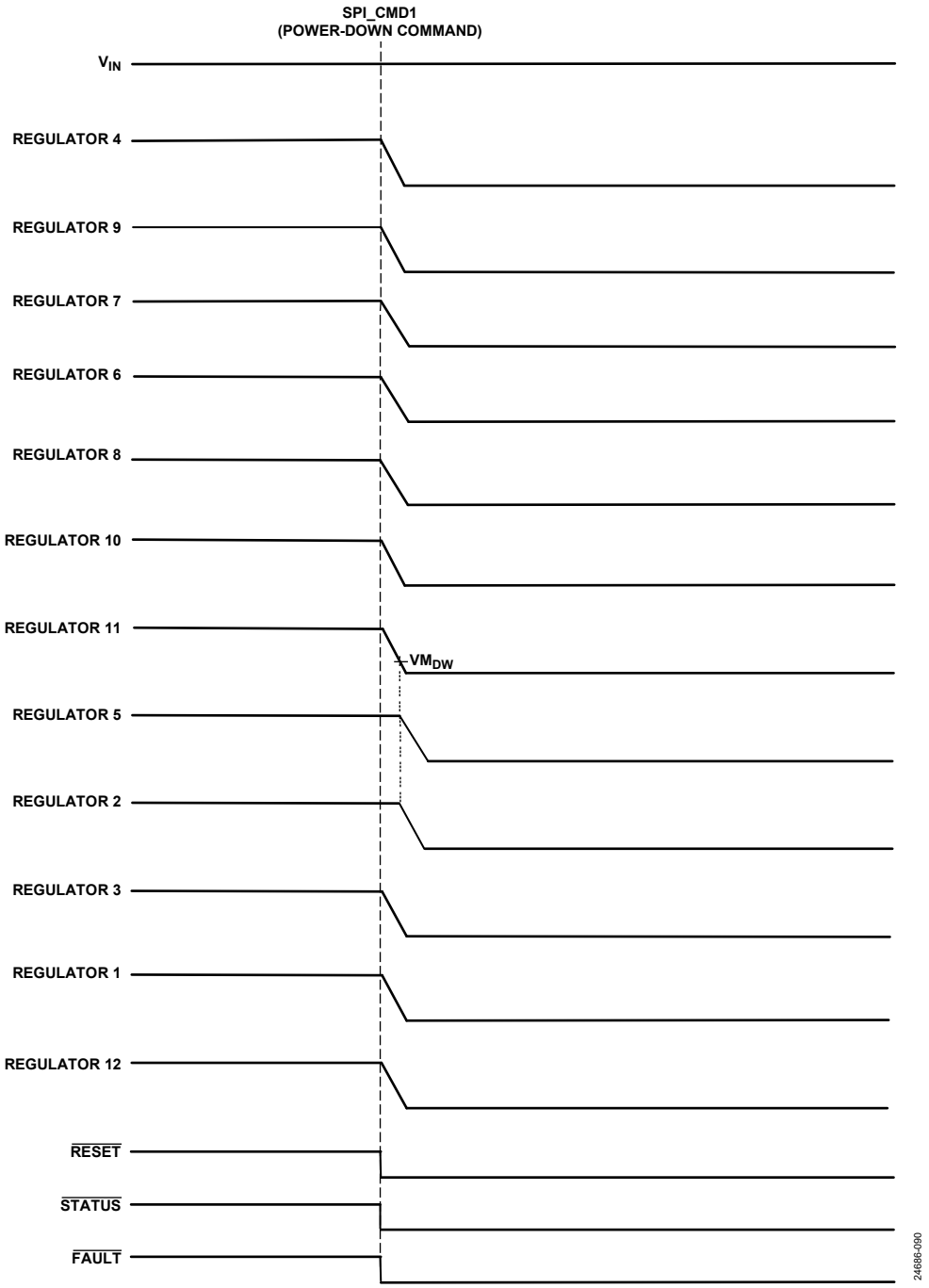

Figure 90. Power-Down Sequence

SPI

The ADP5140 uses the SPI to communicate with the processor. The ADP5140 is always the slave and has a single input and output mode.

SPI Mode 0 and Mode 3 are supported in the ADP5140. In Mode 0 (clock polarity (CPOL) = clock phrase (CPHA) = 0), SCK is low when the clock is inactive. In Mode 3 (CPOL = CPHA = 1), SCK is high when the clock is inactive. In both modes, bits are always sampled at the rising edge of the clock and driven at the falling edge of the clock. The ADP5140 detects which mode is used automatically when receiving bit streams from the host.

Through the SPI, the processor can configure the ADP5140 functionalities and set the device parameters. The processor can also read back the status of the ADP5140. Refer to the SPI Register Map section for detailed information on the ADP5140 registers.

Figure 91 shows the SPI bit frame that has two phases. The first phase is the instruction phase that includes the command, address, and reserve. The second phase is the data phase that includes the data and cyclic redundancy check (CRC).

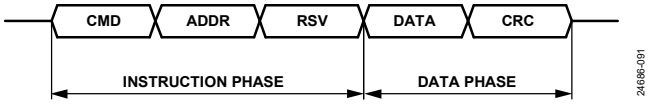

Figure 91. SPI Bit Frame

Command (CMD)

CMD is an 8-bit field that indicates the action that the host wants to perform, as shown in Table 32.

Table 32. Command Byte Description

Bit(s)	Description
7	0: write operation 1: read operation
6	0: broadcast disable 1: broadcast enable
5	Reserved
4	0: little Endian 1: big Endian (default)
3	0: MSB first (default) 1: LSB first
[2:1]	Device index
0	0: write operation 1: read operation

Bit 7 and Bit 0 in this field indicate whether the host wants to perform a write (00) or a read (11) operation, respectively. Note that 01 and 10 are invalid values.

Bit 1 and Bit 2 in this field indicate the device index of the ADP5140 to which the host wants to communicate. The device index is determined by the MODE pin configuration in Table 27.

Bit 3 and Bit 4 in this field indicate the SPI communication command mode of the ADP5140 with big Endian and MSB first as the default. The command mode is programmable through the SPI IF_CFGA register. The ADP5140 supports the following four types of command modes:

- Mode 0: little Endian and MSB first.
- Mode 1: little Endian and LSB first.
- Mode 2: big Endian and MSB first (default).
- Mode 3: big Endian and LSB first.

Note that if the broadcast feature is enabled (Bit 6 in CMD is set to 1), any device with the $\overline{CS}$ pin pulled low is under communication despite the device index value (Bit 1 and Bit 2 in CMD).

Address (ADDR)

ADDR is a 2-byte field that contains the register address the host wants to access. The ADDR field duration is 16 SCK cycles. Refer to the SPI Register Map section for more information.

Reserved (RSV)

RSV is a 1-byte field reserved by the ADP5140. The RSV field duration is eight SCK cycles.

Data (DATA)

DATA is a 4-byte field that contains the data to transfer. The DATA field duration is 32 SCK cycles.

CRC

The ADP5140 uses the CRC field to detect data communication errors in each SPI frame. The CRC field in the SPI frame is a 16-bit field containing the computed CRC value.

CRC is always sent MSB first and spans over the CMD, ADDR, RSV, and DATA fields.

The default polynomial used to calculate CRC is $x^{16} + x^{15} + x^{12} + x^7 + x^6 + x^4 + x^3 + 1$ (0x90D9), and the default initial seed value to calculate CRC is 0x5555. Both the polynomial and initial seed values can be configured in the SPI_CRC_PARAM register.

Figure 92 and Figure 93 show the time sequence of SPI write and read operations.

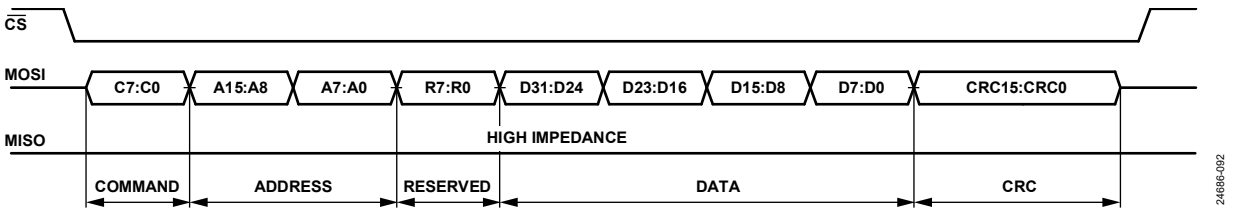

Figure 92. SPI Write Operation

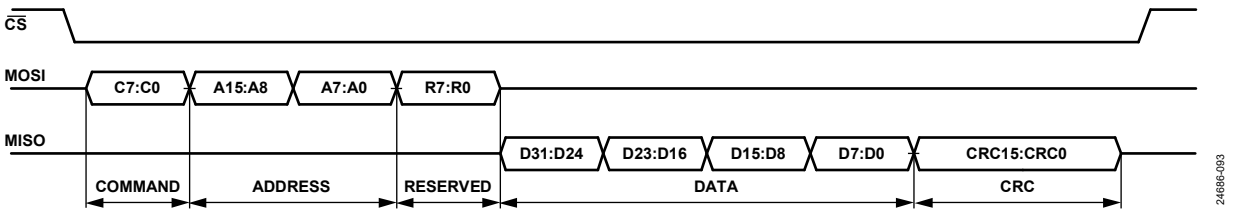

Figure 93. SPI Read Operation

STATE DIAGRAM

Figure 94 shows the state diagram of the ADP5140.

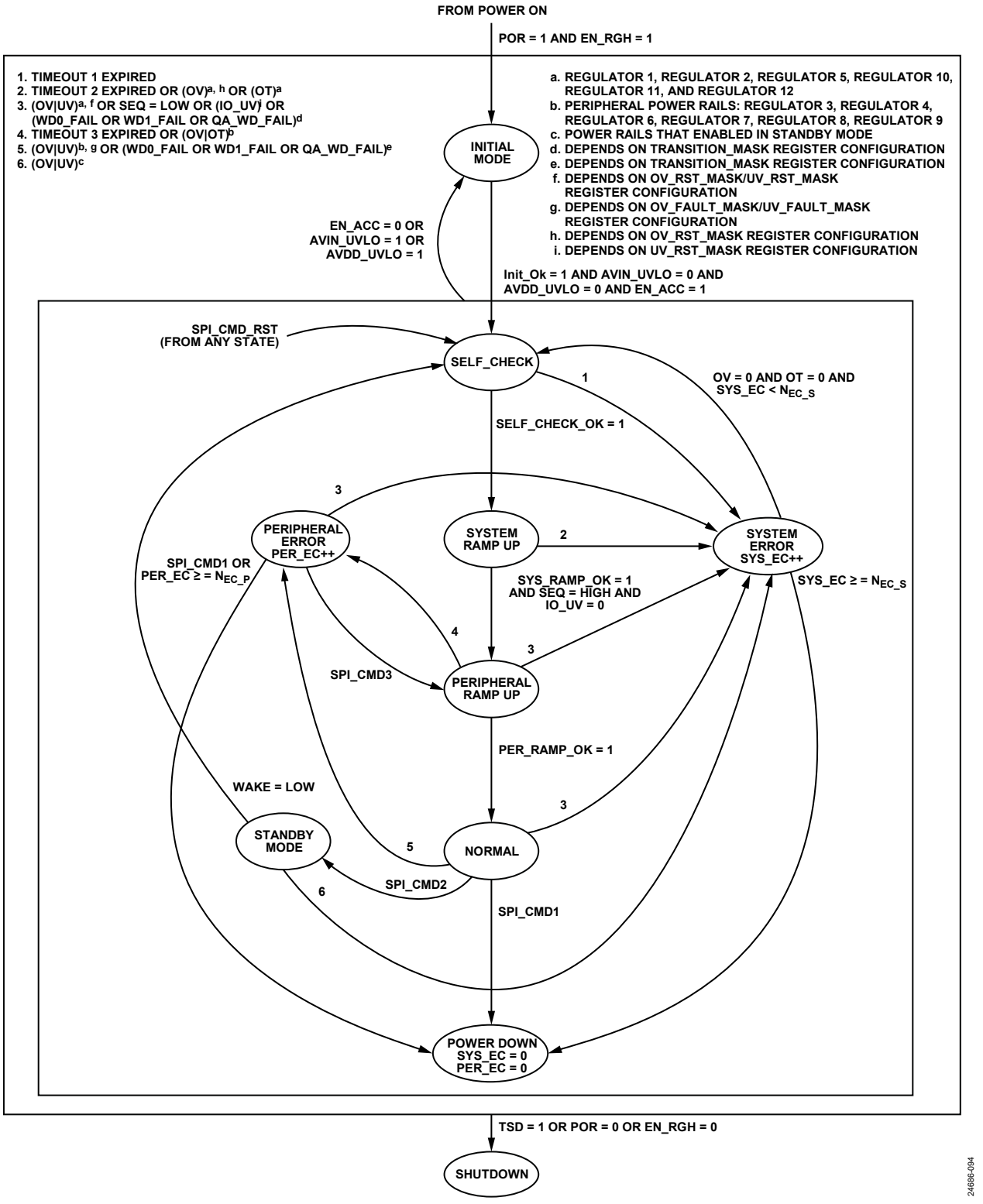

Figure 94. State Diagram

Initial Mode

The conditions to enter initial mode include the following:

- Enter initial mode from the POR when V_{EN} is higher than V_{EN_RGH} (EN_RGH = 1).
- Enter initial mode from any mode except for shutdown mode when $V_{AVIN} < V_{AVIN\_UVLO\_F}$ (AVIN_UVLO = 1), $V_{AVDD} < V_{AVDD\_UVLO\_F}$ (AVDD_UVLO = 1), or $V_{EN} < V_{EN\_F}$ (EN_ACC = 0).

The conditions to exit initial mode include the following:

- Exit initial mode and enter self check mode when initial mode is completed. Both the V_{AVIN} and V_{AVDD} are higher than the corresponding UVLO thresholds and $V_{EN} > V_{EN\_R}$.
- Exit initial mode and enter shutdown mode when the TSD, the POR, or $V_{EN} < V_{EN\_RGH}$ occurs.

In initial mode, the ADP5140 loads the trimmed data and reads the pin configuration. All power rails turn off and the ADP5140 monitors the input voltage and the die temperature. The $\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, and $\overline{\text{STATUS}}$ pins remain low.

Self Check Mode

The conditions to enter self check mode when $V_{AVIN} > V_{AVIN\_UVLO\_R}$ (AVIN_UVLO = 0), $V_{AVDD} > V_{AVDD\_UVLO\_R}$ (AVDD_UVLO = 0), and $V_{EN} > V_{EN\_R}$ (EN_ACC = 1) include the following:

- From initial mode when initial mode completes.
- From standby mode when getting a wake-up signal from the WAKE pin.
- From system error mode if the system error counter, (SYS_EC) < system error counter threshold (NEC_S) and no overtemperature and overvoltage events happen on any power rail.
- From any mode when getting a self check mode from any mode (SPI_CMD_RST) command.

Conditions of exiting self check mode include the following:

- Entering system ramp-up mode when self check mode completes (SELF_CHECK_OK = 1).
- Entering system error mode when self check mode times out (t_{EXP1}).
- Entering initial mode when $V_{AVIN} < V_{AVIN\_UVLO\_F}$ or $V_{AVDD} < V_{AVDD\_UVLO\_F}$ or $V_{EN} < V_{EN\_F}$.
- Entering shutdown mode when the TSD or the POR or $V_{EN} < V_{EN\_RGH}$ occurs.

During self check mode, the ADP5140 runs the self test and checks all of the analog and digital circuits for monitoring. All of the power rails are turned off, and the ADP5140 monitors the input voltage and the die temperature. SPI registers are reset in self check mode, except for the SYS_EC. The $\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, and $\overline{\text{STATUS}}$ pins keep low.

System Ramp-Up Mode

The ADP5140 enters system ramp-up mode from self check mode when the self check completes while $V_{AVIN} > V_{AVIN\_UVLO\_R}$, $V_{AVDD} > V_{AVDD\_UVLO\_R}$, and $V_{EN} > V_{EN\_R}$.

The conditions to exit system ramp-up mode include the following:

- Entering peripheral ramp-up mode when the system ramp-up completes (SYS_RAMP_OK = 1) when the SEQ pin is high and $V_{VIO} > V_{IO\_UV}$ (IO_UV = 0).
- Entering system error mode when the system ramp-up times out (t_{EXP2}), when an overtemperature event occurs on Regulator 1, Regulator 2, Regulator 5, Regulator 10, Regulator 11, or Regulator 12, or an overvoltage event occurs on Regulator 1, Regulator 2, Regulator 5, Regulator 10, Regulator 11, or Regulator 12 and the fault event is not masked in the OV_RST_MASK register.
- Entering initial mode when $V_{AVIN} < V_{AVIN\_UVLO\_F}$, $V_{AVDD} < V_{AVDD\_UVLO\_F}$, or $V_{EN} < V_{EN\_F}$.
- Entering shutdown mode when the TSD, the POR, or $V_{EN} < V_{EN\_RGH}$ occurs.

During system ramp-up mode, Regulator 1, Regulator 2, Regulator 5, Regulator 10, Regulator 11, and Regulator 12 power up in a fixed sequence. The $\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, and $\overline{\text{STATUS}}$ pins keep low.

Peripheral Ramp Up Mode

The conditions to enter peripheral ramp-up mode when $V_{AVIN} > V_{AVIN\_UVLO\_R}$, $V_{AVDD} > V_{AVDD\_UVLO\_R}$ and $V_{EN} > V_{EN\_R}$ include the following:

- Entering peripheral ramp-up mode from system ramp-up mode when the system ramp-up completes, the SEQ pin is high, and $V_{VIO} > V_{IO\_UV}$.
- Entering peripheral ramp-up mode from peripheral error mode when receiving a peripheral ramp-up mode (SPI_CMD3) command.

The conditions to exit peripheral ramp-up mode include the following:

- Entering normal mode when peripheral ramp-up mode completes (PER_RAMP_OK = 1).
- Entering system error mode when an overvoltage or undervoltage event occurs on Regulator 1, Regulator 2, Regulator 5, Regulator 10, Regulator 11, or Regulator 12, and the fault event is not masked in the OV_RST_MASK register or the UV_RST_MASK register, when SEQ is low, when an undervoltage event occurs on the VIO pin and the fault event is not masked in the UV_RST_MASK register, or when a fault occurs on one of the watchdogs (WD0, WD1, or QA_WD) and the fault is not masked in the TRANSITION_MASK register.

- Entering peripheral error mode when the peripheral ramp up times out (t_{EXP3}) or when an overvoltage or undervoltage event occurs on Regulator 3, Regulator 4, Regulator 6, Regulator 7, Regulator 8, or Regulator 9.
- Entering initial mode when $V_{AVIN} < V_{AVIN\_UVLO\_F}$, $V_{AVDD} < V_{AVDD\_UVLO\_F}$, or $V_{EN} < V_{EN\_F}$.
- Entering shutdown mode when the TSD, the POR, or $V_{EN} < V_{EN\_RGH}$ occurs.

During peripheral ramp-up mode, Regulator 3, Regulator 4, Regulator 6, Regulator 7, Regulator 8, and Regulator 9 power up in a fixed sequence. The $\overline{\text{FAULT}}$ and the $\overline{\text{STATUS}}$ pins keep low, while the $\overline{\text{RESET}}$ pin is pulled high after a t_{HOLD} delay time.

Normal Mode

A condition for entering normal mode when $V_{AVIN} > V_{AVIN\_UVLO\_R}$, $V_{AVDD} > V_{AVDD\_UVLO\_R}$, and $V_{EN} > V_{EN\_R}$ is from the peripheral ramp-up mode when peripheral ramp-up mode completes.

The conditions to exit normal mode include the following:

- Entering power-down mode when receiving an SPI_CMD1 command.
- Entering standby mode when receiving a standby mode (SPI_CMD2) command.
- Entering system error mode when an overvoltage or undervoltage event occurs on Regulator 1, Regulator 2, Regulator 5, Regulator 10, Regulator 11, or Regulator 12, and the fault event is not masked in the OV_RST_MASK register or the UV_RST_MASK register, when SEQ is low, when an undervoltage event occurs on the VIO pin, and the fault event is not masked in the UV_RST_MASK register, or when a fault occurs on one of the watchdogs (WD0, WD1, or QA_WD), and the fault is not masked in the TRANSITION_MASK register.
- Entering peripheral error mode when an overvoltage or undervoltage event occurs on Regulator 3, Regulator 4, Regulator 6, Regulator 7, Regulator 8, or Regulator 9, and the fault event is not masked in the OV_FAULT_MASK register or UV_FAULT_MASK register, or when a fault occurs on one of the watchdogs (WD0, WD1, or QA_WD), and the fault is not masked in the TRANSITION_MASK register.
- Entering initial mode when $V_{AVIN} < V_{AVIN\_UVLO\_F}$, $V_{AVDD} < V_{AVDD\_UVLO\_F}$, or $V_{EN} < V_{EN\_F}$.
- Entering shutdown mode when the TSD, the POR, or $V_{EN} < V_{EN\_RGH}$ occurs.

During normal mode, all power rails are turned on, and all functions are active except for the WAKE function. WD0, WD1, and the sequenced QA watchdog can be enabled in normal mode. Different events are mapped to the $\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, and $\overline{\text{STATUS}}$ pins according to the SPI register configurations.

Power-Down Mode

The conditions to enter power-down mode when $V_{AVIN} > V_{AVIN\_UVLO\_R}$, $V_{AVDD} > V_{AVDD\_UVLO\_R}$, and $V_{EN} > V_{EN\_R}$ include the following:

- Entering power-down mode from normal mode when receiving an SPI_CMD1 command.
- Entering power-down mode from peripheral error mode when receiving an SPI_CMD1 command or when peripheral error counter (PER_EC) ≥ peripheral error counter threshold (N_{EC_P}).
- Entering power-down mode from system error mode when SYS_EC ≥ N_{EC_S}.

The conditions to exit power-down mode include the following:

- Entering initial mode when $V_{AVIN} < V_{AVIN\_UVLO\_F}$, $V_{AVDD} < V_{AVDD\_UVLO\_F}$, or $V_{EN} < V_{EN\_F}$.
- Entering shutdown mode when the TSD, the POR, or $V_{EN} < V_{EN\_RGH}$ occurs.

During power-down mode, all power rails power down in a fixed sequence and stay in this mode. SYS_EC and PER_EC reset. The ADP5140 monitors the input voltage and the die temperature. The $\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, and $\overline{\text{STATUS}}$ pins keep low.

System Error Mode

The conditions to enter system error mode when $V_{AVIN} > V_{AVIN\_UVLO\_R}$, $V_{AVDD} > V_{AVDD\_UVLO\_R}$, and $V_{EN} > V_{EN\_R}$ include the following:

- Entering system error mode from self check mode when self check mode times out (t_{EXP1}).
- Entering system error mode from system ramp-up mode when the system ramp-up times (t_{EXP2}), when an overvoltage or undervoltage event occurs on Regulator 1, Regulator 2, Regulator 5, Regulator 10, Regulator 11, or Regulator 12, or when an overvoltage event occurs on Regulator 1, Regulator 2, Regulator 5, Regulator 10, Regulator 11, or Regulator 12, and the fault event is not masked in the OV_RST_MASK register.
- Entering system error mode from peripheral ramp-up mode when an overvoltage or undervoltage event occurs on Regulator 1, Regulator 2, Regulator 5, Regulator 10, Regulator 11, or Regulator 12, and the fault event is not masked in the OV_RST_MASK register or the UV_RST_MASK register, when SEQ is low, when an undervoltage event occurs on the VIO pin, and the fault event is not masked in the UV_RST_MASK register, or when a fault occurs on one of the watchdogs (WD0, WD1, or QA_WD), and the fault is not masked in the TRANSITION_MASK register.
- Entering system error mode from normal mode when an overvoltage or undervoltage event occurs on Regulator 1, Regulator 2, Regulator 5, Regulator 10, Regulator 11, or Regulator 12, and the fault event is not masked in the OV_RST_MASK register or the UV_RST_MASK register, when SEQ is low, or when an undervoltage occurs on the VIO pin, and the fault event is not masked in the UV_RST_MASK register, or when a fault occurs on one of the watchdogs (WD0, WD1, or QA_WD), and the fault is not masked in the TRANSITION_MASK register.

- Entering system error mode from peripheral error mode when an overvoltage or undervoltage event occurs on Regulator 1, Regulator 2, Regulator 5, Regulator 10, Regulator 11, or Regulator 12, and the fault event is not masked in the OV_RST_MASK register or the UV_RST_MASK register, when SEQ is low, when an undervoltage event occurs on the VIO pin, and the fault event is not masked in the UV_RST_MASK register, or when a fault even occurs on one of the watchdogs (WD0, WD1, or QA_WD), and the fault is not masked in the TRANSITION_MASK register.
- Entering system error mode from standby mode when an overvoltage or undervoltage event occurs on any regulator that is enabled in the standby mode.

The conditions to exit system error mode include the following:

- Entering power-down mode if SYS_EC ≥ N_{EC_S}.
- Entering self check mode if SYS_EC < N_{EC_S} and no overtemperature or overvoltage events occur on any power rails.
- Entering initial mode when $V_{AVIN} < V_{AVIN\_UVLO\_F}$, $V_{AVDD} < V_{AVDD\_UVLO\_F}$, or $V_{EN} < V_{EN\_F}$.
- Entering shutdown mode when the TSD, the POR, or $V_{EN} < V_{EN\_RGH}$ occurs.

During system error mode, all power rails are turned off. The ADP5140 monitors the input voltage, the output voltage, and the die temperature. The system error counter increments. The RESET, FAULT, and STATUS pins keep low.

System error mode has higher priority than peripheral error mode. If the exiting condition of any mode meets both the system error mode and the peripheral mode exiting conditions, the device enters system error mode instead of peripheral mode.

Peripheral Error Mode

The conditions to enter peripheral error mode when $V_{AVIN} > V_{AVIN\_UVLO\_R}$, $V_{AVDD} > V_{AVDD\_UVLO\_R}$, and $V_{EN} > V_{EN\_R}$ include the following:

- Entering peripheral error mode from peripheral ramp-up mode when the peripheral ramp-up times out (t_{EXP3}) or when an overvoltage or undervoltage event occurs on Regulator 3, Regulator 4, Regulator 6, Regulator 7, Regulator 8, or Regulator 9.
- Entering peripheral error mode from normal mode when an overvoltage or undervoltage event occurs on Regulator 3, Regulator 4, Regulator 6, Regulator 7, Regulator 8, or Regulator 9, and the fault event is not masked in the OV_FAULT_MASK register or the UV_FAULT_MASK register, or when a fault occurs on one of the watchdogs (WD0, WD1, or QA_WD), and the fault is not masked in the TRANSITION_MASK register.

The conditions to exit peripheral error mode include the following:

- Entering power-down mode when receiving an SPI_CMD1 command or when PER_EC ≥ N_{EC_P}.
- Entering peripheral ramp-up mode when receiving an SPI_CMD3 command.
- Entering system error mode when an overvoltage or undervoltage event occurs on Regulator 1, Regulator 2, Regulator 5, Regulator 10, Regulator 11, or Regulator 12, and the fault event is not masked in the OV_RST_MASK register or the UV_RST_MASK register, or SEQ is low, when an undervoltage event occurs on the VIO pin, and the fault event is not masked in the UV_RST_MASK register, or when a fault event occurs on one of the watchdogs (WD0, WD1, or QA_WD), and the fault is not masked in the TRANSITION_MASK register.
- Entering initial mode when $V_{AVIN} < V_{AVIN\_UVLO\_F}$,$V_{AVDD} < V_{AVDD\_UVLO\_F}$, or $V_{EN} < V_{EN\_F}$.
- Entering shutdown mode when the TSD, the POR, or $V_{EN} < V_{EN\_RGH}$ happens.

During peripheral error mode, the peripheral counter increments. WD0 and the sequenced QA watchdog still work in this mode, if enabled. The RESET pin is pulled high, and the FAULT and STATUS pins are pulled low.

Power rail management in the peripheral error mode works under the following conditions:

- If a fault on Regulator 3 occurs, Regulator 3, Regulator 4, Regulator 6, Regulator 7, Regulator 8, and Regulator 9 turn off, and other regulators still work.
- If no fault on Regulator 3 occurs, Regulator 4, Regulator 6, Regulator 7, Regulator 8, and Regulator 9 turn off, and other regulators still work.

Standby Mode

The ADP5140 enters standby mode from normal mode. The device receives an SPI_CMD2 command if the WAKE pin is not pulled low while $V_{AVIN} > V_{AVIN\_UVLO\_R}$, $V_{AVDD} > V_{AVDD\_UVLO\_R}$, and $V_{EN} > V_{EN\_R}$.

The conditions to exit standby mode include the following:

- Entering self check mode when the WAKE pin is driven low externally during standby mode.
- Entering system error mode when an overvoltage or undervoltage event occurs on any regulator that is enabled in standby mode.
- Entering initial mode when $V_{AVIN} < V_{AVIN\_UVLO\_F}$, $V_{AVDD} < V_{AVDD\_UVLO\_F}$, or $V_{EN} < V_{EN\_F}$.
- Entering shutdown mode when the TSD, the POR, or $V_{EN} < V_{EN\_RGH}$ occurs.

During standby mode, only Regulator 12, Regulator 11, Regulator 5, Regulator 3, and Regulator 2 are allowed to be active, which is controlled by the STANDBY_RAIL_ACTIVE register. All other regulators are turned off. The wake-up block works in standby mode and monitors the WAKE pin. The ADP5140 monitors the input voltage, the output voltage, and the die temperature. The $\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, and $\overline{\text{STATUS}}$ pins keep low.

Shut Down Mode

The conditions to enter shutdown mode include the following:

- Thermal shutdown occurs.
- The input voltage is lower than the POR threshold.
- The EN pin voltage is lower than V_{EN_RGH}.

The condition to exit shutdown mode is entering initial mode when receiving a POR, and V_{EN} is higher than V_{EN_RGH}.

During shutdown mode, all regulators turn off. The $\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, and $\overline{\text{STATUS}}$ pins keep low.

APPLICATIONS INFORMATION

INPUT CAPACITOR SELECTION

Higher value input capacitors help reduce the input voltage ripple and improve transient response. To minimize supply noise, place the input capacitors as close as possible to the PVINx pins. The voltage rating of the input capacitors must be greater than the maximum input voltage.

Input Capacitor Selection for the Buck Regulators

The input capacitors reduce the input voltage ripple caused by the switch current on the power input pins. The loop composed of the input capacitor, the high-side MOSFET, and the low-side MOSFET must be kept as small as possible. A ceramic capacitor with low ESR from 10 µF to 47 µF is recommended. Ensure that the rms current rating of the input capacitor is larger than the value calculated from the following equation:

$$I_{CIN\_RMS\_BUCK} = I_{OUT\_BUCK} \times \sqrt{D_{BUCK} \times (1 - D_{BUCK})}$$

where

$I_{CIN\_RMS\_BUCK}$ is the rms current through the buck input capacitor.
I_{OUT_BUCK} is the output current of the buck.
D_{BUCK} is the duty cycle of buck regulator ($D_{BUCK} = V_{OUT\_BUCK}/V_{IN\_BUCK}$).

Input Capacitor Selection for the Boost Regulator

Because the input current of the boost regulator is continuous, and the switch current on the power input pin is low, there are no strict constraints on the input capacitor for the boost regulator. A typical 10 µF ceramic capacitor with a voltage rating higher than the input voltage is recommended.

Input Capacitor Selection for the LDO Regulators

Connect at least a 1 µF ceramic capacitor with low ESR from PVINx pins to GND to reduce the circuit sensitivity to the PCB layout, especially when long input traces or high source impedance are encountered. If an output capacitance greater than 1 µF is required, increase the input capacitor to match the capacitance.

INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage, output voltage, and inductor ripple current. Using a small inductor value leads to a faster transient response but degrades efficiency because of a larger inductor ripple current. Using a large inductor value leads to smaller ripple current and better efficiency but results in a slower transient response.

Inductor Selection for the Buck Regulators

An inductor ranging from 0.33 µH to 1 µH is recommended for the best balance between transient and efficiency performance. The inductor ripple current, ΔI_{L_BUCK}, is typically set to one-third of the maximum load current.

Use the following equation to calculate the inductor value:

$$L_{BUCK} = \frac{(V_{IN\_BUCK} - V_{OUT\_BUCK}) \times D_{BUCK}}{\Delta I_{L\_BUCK} \times f_{SW}}$$

where:
V_{IN_BUCK} is the input voltage of buck regulator.
V_{OUT_BUCK} is the output voltage of buck regulator.
ΔI_{L_BUCK} is the inductor current ripple of buck regulator.
f_{SW} is the switching frequency.

Use the following equation to calculate the peak inductor current:

$$I_{PEAK\_BUCK} = I_{OUT\_BUCK} + \frac{\Delta I_{L\_BUCK}}{2}$$

where:
I_{PEAK_BUCK} is the peak inductor current of the buck.

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a quick saturation characteristic, the saturation current rating of the inductor must be higher than the current-limit threshold of the buck regulator to prevent the inductor from reaching saturation.

Use the following equation to calculate the rms current of the inductor (I_{RMS_BUCK}):

$$I_{RMS\_BUCK} = \sqrt{I_{OUT\_BUCK}^{2} + \frac{\Delta I_{L\_BUCK}^{2}}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low EMI.

Inductor Selection for the Boost Regulator

An inductor from 2.2 µH to 10 µH is recommended for optimal balance between transient and efficiency performance. The inductor ripple current, ΔI_{L_BOOST}, is typically set to 1/3 of the average inductor current, I_{AVE_BOOST} as follows:

$$I_{AVE\_BOOST} = \frac{I_{OUT\_BOOST}}{1 - D_{BOOST}}$$

where:
I_{OUT_BOOST} is the output current of the boost regulator.
D_{BOOST} is the duty cycle of the boost regulator.

$$D_{BOOST} = \frac{V_{OUT\_BOOST} - V_{IN\_BOOST}}{V_{OUT\_BOOST}}$$

Use the following equation to calculate the inductor value:

$$L_{BOOST} = \frac{V_{IN\_BOOST} \times D_{BOOST}}{\Delta I_{L\_BOOST} \times f_{SW}}$$

where:
V_{IN_BOOST} is the input voltage of boost regulator.

As the boost ratio increases (higher duty cycle), the average inductor current increases dramatically. Ensure that the

selected inductor is large enough to avoid the current limit throughout the entire input voltage range. Use the following equation to calculate the peak inductor current:

$$I_{PEAK\_BOOST} = \left(\frac{I_{OUT\_BOOST}}{1 - D_{BOOST}} \right) + \frac{I_{PP\_BOOST}}{2}$$

where

I_{PEAK_BOOST} is the peak inductor current of the boost.
I_{PP_BOOST} is the peak-to-peak inductor ripple current.

$$I_{PP\_BOOST} = \frac{V_{IN\_BOOST} \times D_{BOOST}}{L_{BOOST} \times f_{SW}}$$

where L_{BOOST} is the inductor value of the boost.

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a quick saturation characteristic, the saturation current rating of the inductor must be higher than the current-limit threshold of the boost regulator to prevent the inductor from reaching saturation.

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects both the output voltage ripple and the loop dynamics of the regulators in the ADP5140. The ADP5140 functions with small ceramic capacitors that have low equivalent series resistance (ESR) and low equivalent series inductance (ESL) and can, therefore, easily meet the output voltage ripple specifications. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. X5R or X7R dielectrics are recommended for best performance because of the low ESR and small temperature coefficients.

Output Capacitor Selection for the Buck Regulators

During a load step transient where the load suddenly increases, the output capacitor supplies the load until the control loop can ramp up the inductor current. The delay caused by the control loop causes output to undershoot. To calculate the output capacitance that is required to satisfy the voltage drop requirement, use the following equation:

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}{}^2 \times L_{BUCK}}{2 \times (V_{IN\_BUCK} - V_{OUT\_BUCK}) \times \Delta V_{OUT\_UV}}$$

where:

K_{UV} is a factor, with a typical setting of $K_{UV} = 2$.
ΔI_{STEP} is the load step.
ΔV_{OUT_UV} is the allowable undershoot on the output voltage of buck regulator.

Another example occurs when a load is suddenly removed from the output, and the energy stored in the inductor rushes into the output capacitor, causing the output to overshoot.

To calculate the output capacitance that is required to meet the overshoot requirement, use the following equation:

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}{}^2 \times L_{BUCK}}{(V_{OUT\_BUCK} + \Delta V_{OUT\_OV})^2 - V_{OUT\_BUCK}{}^2}$$

where:

K_{OV} is a factor, with a typical setting of $K_{OV} = 2$.
L_{BUCK} is the inductor current ripple
ΔV_{OUT_OV} is the allowable overshoot on the output voltage of buck regulator. When the buck regulator operates in continuous conduction mode, the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by the charging and discharging of the output capacitor, as follows:

$$\Delta V_{RIPPLE\_BUCK} = \Delta I_{L\_BUCK} \times \left(\frac{1}{8 \times f_{SW} \times C_{OUT\_RIPPLE\_BUCK}} + ESR_{BUCK} \right)$$

where:

ΔV_{RIPPLE_BUCK} is the allowable output ripple voltage of the buck regulator.
$C_{OUT\_RIPPLE\_BUCK}$ is the output capacitance to meet the voltage ripple requirement.
ESR_{BUCK} is the equivalent series resistance of the output capacitor of buck regulator in ohms (Ω).

Capacitors with lower ESR are preferable to guarantee low output voltage ripple, as shown in the following equation:

$$ESR_{BUCK} \leq \frac{\Delta V_{RIPPLE\_BUCK}}{\Delta I_{L\_BUCK}}$$

Select the largest output capacitance given by C_{OUT_UV}, C_{OUT_OV}, and $C_{OUT\_RIPPLE\_BUCK}$ to meet both load transient and output ripple performance.

Output Capacitor Selection for the Boost Regulator

In the boost regulator, the output capacitor supplies the load current while the inductor current ramps up. Therefore, the output ripple usually determines the output capacitance required, as follows:

$$\Delta V_{RIPPLE\_BOOST} = \frac{I_{OUT\_BOOST} \times D_{BOOST}}{C_{OUT\_RIPPLE\_BOOST} \times f_{SW}} + \left(ESR_{BOOST} \times I_{PEAK\_BOOST} \right)$$

where:

ΔV_{RIPPLE_BOOST} is the allowable output ripple voltage of the boost regulator.
ESR_{BOOST} is the equivalent series resistance of the output capacitor of boost regulator in Ω.

The output voltage of the boost regulator in the ADP5140 is fixed. A ceramic capacitor with a typical value of 10 µF or greater and low ESR is recommended. Larger capacitance values lower the output ripple and improve transient response and loop stability.

Output Capacitor Selection for the LDO Regulators

The output capacitance of the LDO regulators depends mainly on the load current. Generally, a large load current requires a large output capacitance to achieve a stable output voltage. A higher capacitor value improves the transient response of the LDO regulators to large changes in the load current.

Ceramic capacitors with a typical value of 1 µF to 10 µF are recommended as the output capacitors of the LDO regulators in the ADP5140.

LOW OUTPUT NOISE DESIGN OF BUCK4

In typical system application of the ADP5140, BUCK4 provides power for the power amplifier, which requires low noise input. BUCK4 in the ADP5140 optimizes the internal analog blocks and uses low noise reference architecture to achieve lower output noise. When the system design requires BUCK4 of the ADP5140 to power the power amplifier directly without the LDO regulator, it is highly recommended to add an additional secondary LC filter after the primary LC filter to filter the fundamental switching ripple further and achieve lower output noise in the noise sensitive frequency range of the power amplifier.

Because the secondary LC filter generates voltage drop when the load increases, an inductor with a small dc current resistance (DCR) is recommended to minimize the voltage drop, especially for a high current application.

There is a hybrid feedback method, as shown in Figure 95, which provides an adequate stability margin and maintains the output accuracy over all load conditions in the application where the secondary LC filter of BUCK4 is added.

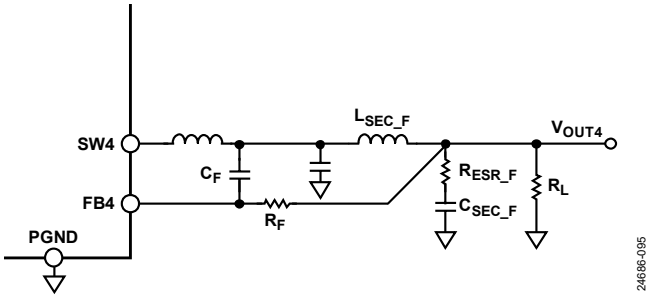

Figure 95. Hybrid Feedback Method of BUCK4 With Secondary LC Filter

To maintain the loop stability of BUCK4 when using the hybrid feedback method, the value constrains of the components shown in the following equation must be met:

$$R_F \times C_F > \frac{L_{SEC\_F} \times C_{SEC\_F}}{\frac{L_{SEC\_F}}{R_L} + R_{ESR\_F} \times C_{SEC\_F}}$$

where:
R_F is the feedback resistor.
C_F is the feedback capacitor.
L_{SEC_F} is the inductor of the secondary LC filter.
C_{SEC_F} is the capacitor of the secondary LC filter.
R_{ESR_F} is the equivalent series resistance of C_{SEC_F}.
R_L is the load resistance.

Note that larger R_F and C_F values degrade the load transient performance of BUCK4 because R_F and C_F work as an RC filter of the output voltage during load transient. It is recommended that $R_F \times C_F$ be 20% to 30% larger than the minimum limitation value shown in the previous equation to balance the loop stability and load transient performance.

VOLTAGE CONVERSION LIMITATIONS

There is a minimum on time and a minimum off time for each switching regulator. The voltage conversion between the input voltage and output voltage of each switching regulator has limitations.

Buck Regulator

The minimum output voltage of a buck regulator for a given input voltage and switching frequency is constrained by the minimum on time of the buck regulator and can be calculated using the following equation:

$$V_{OUT\_MIN} = V_{IN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MIN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_LS} + R_L) \times I_{OUT\_MIN}$$

where:
V_{OUT_MIN} is the minimum output voltage.
V_{IN} is the input voltage.
t_{MIN_ON} is the minimum on time.
R_{DSON_HS} is the high-side MOSFET on resistance.
R_{DSON_LS} is the low-side MOSFET on resistance.
I_{OUT_MIN} is the minimum output current.
R_L is the series resistance of output inductor.

The maximum output voltage of a buck regulator for a given input voltage and switching frequency is constrained by the minimum off time of the buck regulator and can be calculated using the following equation:

$$V_{OUT\_MAX} = V_{IN} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MAX} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_LS} + R_L) \times I_{OUT\_MAX}$$

where:
V_{OUT_MAX} is the maximum output voltage.
t_{MIN_OFF} is the minimum off time.
I_{OUT_MAX} is the maximum output current.

Boost Regulator

The maximum input voltage of the boost regulator for a given output voltage and switching frequency is constrained by the minimum on time of the boost regulator and can be calculated using the following equation:

$$V_{IN\_MAX} = V_{OUT} \times (1 - t_{MIN\_ON} \times f_{SW}) + I_{OUT\_MIN} \times (R_{DSON\_MAIN} \times (1 - t_{MIN\_ON} \times f_{SW}) + R_L + t_{MIN\_ON} \times f_{SW} \times R_{DSON\_SYNC}) / (1 - t_{MIN\_ON} \times f_{SW})$$

where:
V_{IN_MAX} is the maximum input voltage.
V_{OUT} is the output voltage.
t_{MIN_ON} is the minimum on time.
I_{OUT_MIN} is the minimum output current.
R_{DSON_MAIN} is the main MOSFET on resistance.

R_{DSON_SYNC} is the sync MOSFET on resistance.
R_L is the series resistance of output inductor.

The minimum input voltage of the boost regulator for a given output voltage and switching frequency is constrained by the minimum off time of the boost regulator and can be calculated using the following equation:

$$V_{IN\_MIN} = V_{OUT} \times t_{MIN\_OFF} \times f_{SW} + I_{OUT\_MAX} \times (R_{DSON\_MAIN} \times t_{MIN\_OFF} \times f_{SW} + R_L + (1 - t_{MIN\_OFF} \times f_{SW}) \times R_{DSON\_SYNC})/(t_{MIN\_OFF} \times f_{SW})$$

where:
V_{IN_MIN} is the minimum input voltage.
t_{MIN_OFF} is the minimum off time.
I_{OUT_MAX} is the maximum output current.

PCB LAYOUT RECOMMENDATIONS

In any switching power supply, there are some circuit paths that carry high dI/dt, which create spikes and noise. Some circuit paths are sensitive to noise, such as feedback traces, which must be devoid of spikes and noise. The key to proper PCB layout is to identify these critical paths and arrange the components and the copper area accordingly.

When designing PCB layouts, keep high current loops small. In addition, keep sensitive traces and components away from the switching nodes and the associated components.

Figure 96 shows a recommended PCB layout for the ADP5140. The following layout rules are recommended for the ADP5140:

- Place the input capacitor, output capacitor, and inductor as close as possible to the IC and use short traces.
- Use separate analog ground planes (GND) and power ground planes. Connect the ground reference of sensitive analog circuitry, such as output voltage divider components, reference capacitors, and output capacitors of the LDO regulators to analog ground. In addition, connect the ground reference of the power components, such as input and output capacitors of the buck and boost regulators, to power ground. Use the internal ground planes to connect the analog ground plane and power ground plane together.
- Connect the exposed pads of the ADP5140 to the internal ground plane.
- Separate the input power trace of each switching regulator. Using BUCK1 and BUCK2 as an example, although PVIN1 and PVIN2 are adjacent pins and are usually connected to the same input power, do not connect them directly near the IC pins. Use a separated input trace to connect each PVIN pin to its input capacitor.
- Ensure that the high current loop traces are as short and as wide as possible. Using a BUCKx regulator as an example, ensure that the high current path from the input capacitor through the inductor, the output capacitor, and the power ground plane back to the input capacitor is as short as possible by making sure that the input and output capacitors share a common power ground plane.
- Place the feedback resistor dividers as close as possible to the FBx pins to prevent noise pickup. Minimize the length of the feedback traces away from the high current traces and the switching nodes to avoid noise pickup.

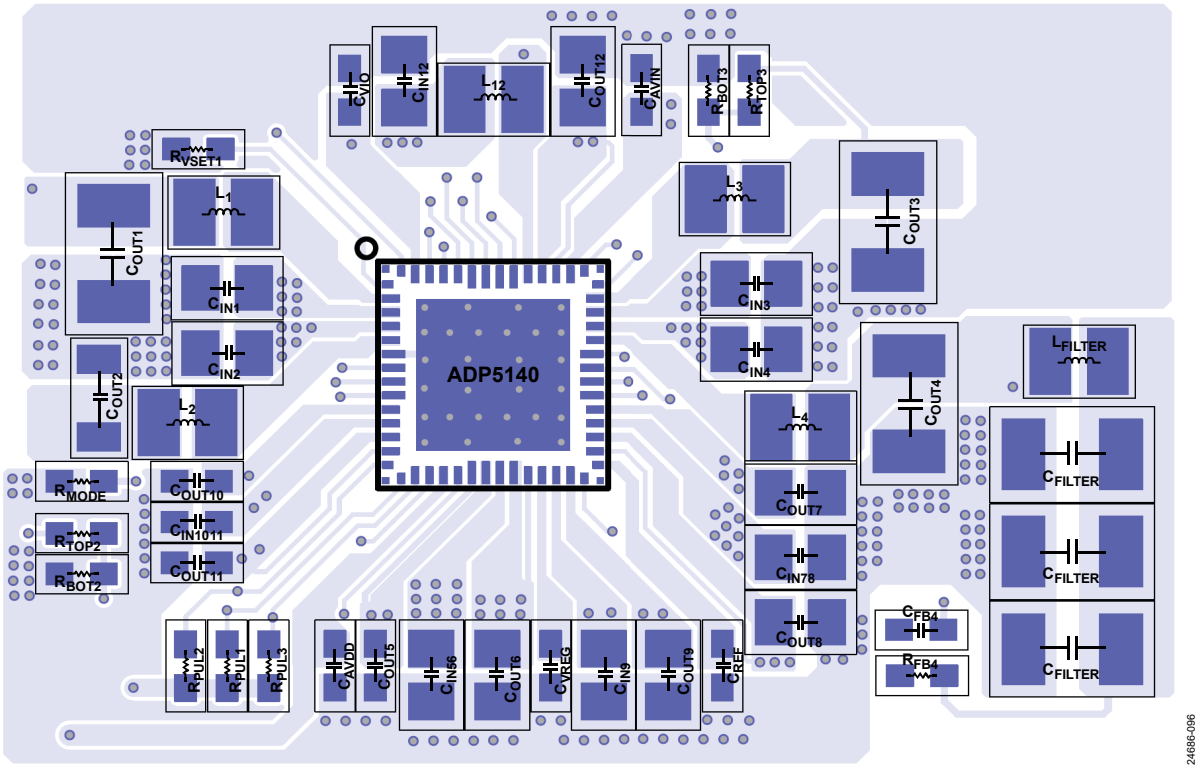

Figure 96. Recommended PCB Layout

SPI REGISTER MAP

SPI REGISTER SUMMARY

Table 33. SPI Register Summary Table

Register Address	Register Name	Reset	Table Reference
0x0000	IF_CFGA	0xC3000000	Table 34
0x0004	CLR_SPI_CNT	0x0	Table 35
0x0008	CHIP_INFO1	0xC035140	Table 36
0x000C	CHIP_INFO2	0x45600	Table 37
0x0010	SPI_CRC_PARAM	0x555590D9	Table 38
0x0014	SPI_CNT	0x0	Table 39
0x001C	PMIC_PSWD	0x0	Table 40
0x0020	QA_WD_ANSWER	0x0	Table 41
0x0024	QA_WD_TOKEN	0x0	Table 42
0x002C	SCRATCH_PAD	0x0	Table 43
0x2000	FAIL_SAFE_PIN_TIMEOUT	0x0	Table 44
0x2004	UV_STATUS	0x0	Table 45
0x2008	OV_STATUS	0x0	Table 46
0x200C	WARN_STATUS	0x0	Table 47
0x2010	OT_STATUS	0x0	Table 48
0x2014	OTHER_STATUS	0x0	Table 49
0x2018	OTHER1_STATUS	0x0	Table 50
0x201C	UV_LATCH	0x0	Table 51
0x2020	OV_LATCH	0x0	Table 52
0x2024	WARN_LATCH	0x0	Table 53
0x2028	OT_LATCH	0x0	Table 54
0x202C	OTHER_LATCH	0x0	Table 55
0x2030	OTHER1_LATCH	0x0	Table 56
0x2034	UV_RST_MASK	0x4C27	Table 57
0x2038	OV_RST_MASK	0xC27	Table 58
0x203C	WARN_RST_MASK	0x0	Table 59
0x2040	OT_RST_MASK	0x0	Table 60
0x2044	OTHER_RST_MASK	0x4	Table 61
0x2048	OTHER1_RST_MASK	0x0	Table 62
0x204C	UV_FAULT_MASK	0x4FFF	Table 63
0x2050	OV_FAULT_MASK	0xFFF	Table 64
0x2054	WARN_FAULT_MASK	0x0	Table 65
0x2058	OT_FAULT_MASK	0x0	Table 66
0x205C	OTHER_FAULT_MASK	0x3801FF	Table 67
0x2060	OTHER1_FAULT_MASK	0xC0	Table 68
0x2064	UV_INT_MASK	0x7FFF	Table 69
0x2068	OV_INT_MASK	0x3FFF	Table 70
0x206C	WARN_INT_MASK	0x3FFF	Table 71
0x2070	OT_INT_MASK	0xFFF	Table 72
0x2074	OTHER_INT_MASK	0x1F801FF	Table 73
0x2078	OTHER1_INT_MASK	0xC0	Table 74
0x207C	TRANSITION_MASK	0x0	Table 75
0x8004	MODE_PIN_STATUS	0x0	Table 76
0x8008	FREQ_CONFG	0x0	Table 77
0x800C	BUCK1_VOUT_SETTING	0x2F	Table 78
0x8010	BUCK1_VOUT	0x0	Table 79
0x8014	BUCK4_VOUT_SETTING	0x2	Table 80
0x8018	BUCK_DVS_INTERVAL	0x0	Table 81
0x801C	LDO1_VOUT_SETTING	0x1	Table 82

Register Address	Register Name	Reset	Table Reference
0x8020	LDO2_VOUT_SETTING	0x1	Table 83
0x8024	LDO3_VOUT_SETTING	0x1	Table 84
0x8028	LDO4_VOUT_SETTING	0x1	Table 85
0x802C	LDO5_VOUT_SETTING	0x1	Table 86
0x8030	LDO6_VOUT_SETTING	0x1	Table 87
0x8034	LDO7_VOUT_SETTING	0x1	Table 88
0x8038	WARN_WINDOW	0x5555555	Table 89
0x803C	FAULT_WINDOW	0xFAAAAAA	Table 90
0x8040	ERROR_COUNT	0x3F	Table 91
0x8044	SM_BIST_TRG	0x0	Table 92
0x8048	SM_BIST_STATUS	0x0	Table 93
0x804C	WDI0_PULSE_CTRL	0x0	Table 94
0x8050	WDI0_PULSE_HIGH	0x47E	Table 95
0x8054	WDI0_PULSE_LOW	0x352	Table 96
0x8058	WDI0_PULSE_WIN_WIDTH	0x898	Table 97
0x805C	WDI1_PULSE_CTRL	0x0	Table 98
0x8060	WDI1_PULSE_HIGH	0x47E	Table 99
0x8064	WDI1_PULSE_LOW	0x352	Table 100
0x8068	WDI1_PULSE_WIN_WIDTH	0x898	Table 101
0x806C	WDT0_CTRL	0x2C00A	Table 102
0x8070	WDT0_WINDOW	0xEA63A98	Table 103
0x8074	WDT0_CLEAR_VALUE	0x0	Table 104
0x8078	WDT0_STATUS	0x0	Table 105
0x807C	WDT0_CURRENT_VALUE	0x0	Table 106
0x8080	WDT1_CTRL	0x2C00A	Table 107
0x8084	WDT1_WINDOW	0x EA63A98	Table 108
0x8088	WDT1_CURRENT_VALUE	0x0	Table 109
0x808C	WDT1_CLEAR_VALUE	0x0	Table 110
0x8090	WDT1_STATUS	0x0	Table 111
0x8094	QA_WD_CTRL	0x35	Table 112
0x8098	QA_WD_WINDOW	0x1E85	Table 113
0x809C	QA_WD_CURRENT_VALUE	0x0	Table 114
0x80A0	QA_WD_CLEAR_VALUE	0x0	Table 115
0x80A4	QA_WD_STATUS	0x0	Table 116
0x80A8	QA_WD_TOKEN_SEED	0x0	Table 117
0x80AC	STANDBY_RAIL_ACTIVE	0x1F	Table 118
0x80B0	SPI_CRC_CHECKSUM	0x0	Table 119
0x80B4	SPI_CMD	0x0	Table 120
0x80B8	VOLTAGE_BLANK_TIME0	0x2222222	Table 121
0x80BC	VOLTAGE_BLANK_TIME1	0x2222222	Table 122
0x80C0	SYSREG_CRC_CHECKSUM	0x0	Table 123
0x80C4	SYSREG_CRC_GOLDEN	0x0	Table 124
0x80C8	SYSREG_CRC_POLYSEED	0x555590D9	Table 125
0x80CC	WAKEPIN_EVT	0x0	Table 126
0x80D0	SYSCRC_EN	0x0	Table 127
0x80D4	VM_TYP_CONFIGURATION	0x0	Table 128
0x80D8	FUSE_PERIOD_CHK_TIMER	0x96	Table 129
0x80F0	SPI_PIN_CTRL	0x0	Table 130

REGISTER BIT DESCRIPTIONS

Table 34. IF_CFGA, Register Address: 0x0000

Bits	Bit Name	Description	Reset	Access
[31:30]	COMM_MODE30_31	COMM_MODE30_31, COMM_MODE24_25, COMM_MODE6_7, and COMM_MODE0_1 are combined to set the SPI communication mode. Mode 0 (Little Endian and MSB): COMM_MODE30_31 = 00, COMM_MODE24_25 = 00, COMM_MODE6_7 = 00, and COMM_MODE0_1 = 00. Mode 1 (Little Endian and LSB): COMM_MODE30_31 = 00, COMM_MODE24_25 = 00, COMM_MODE6_7 = 11, and COMM_MODE0_1 = 11. Mode 2 (Big Endian and MSB): COMM_MODE30_31 = 11, COMM_MODE24_25 = 11, COMM_MODE6_7 = 00, and COMM_MODE0_1 = 00. Mode 3 (Big Endian and LSB): COMM_MODE30_31 = 11, COMM_MODE24_25 = 11, COMM_MODE6_7 = 11, and COMM_MODE0_1 = 11.	0x3	R/W
[29:26]	RESERVED	Reserved.	0x0	R
[25:24]	COMM_MODE24_25	COMM_MODE30_31, COMM_MODE24_25, COMM_MODE6_7, and COMM_MODE0_1 are combined to set the SPI communication mode. Mode 0 (Little Endian and MSB): COMM_MODE30_31 = 00, COMM_MODE24_25 = 00, COMM_MODE6_7 = 00, and COMM_MODE0_1 = 00. Mode 1 (Little Endian and LSB): COMM_MODE30_31 = 00, COMM_MODE24_25 = 00,COMM_MODE6_7 = 11, and COMM_MODE0_1 = 11. Mode 2 (Big Endian and MSB): COMM_MODE30_31 = 11,COMM_MODE24_25 = 11, COMM_MODE6_7 = 00, and COMM_MODE0_1 = 00. Mode 3 (Big Endian and LSB): COMM_MODE30_31 = 11, COMM_MODE24_25 = 11, COMM_MODE6_7 = 11, and COMM_MODE0_1 = 11.	0x3	R/W
[23:8]	RESERVED	Reserved.	0x0	R
[7:6]	COMM_MODE6_7	COMM_MODE30_31, COMM_MODE24_25, COMM_MODE6_7, and COMM_MODE0_1 are combined to set the SPI communication mode. Mode 0 (Little Endian and MSB): COMM_MODE30_31 = 00, COMM_MODE24_25 = 00, COMM_MODE6_7 = 00, and COMM_MODE0_1 = 00. Mode 1 (Little Endian and LSB): COMM_MODE30_31 = 00, COMM_MODE24_25 = 00, COMM_MODE6_7 = 11, and COMM_MODE0_1 = 11. Mode 2 (Big Endian and MSB): COMM_MODE30_31 = 11, COMM_MODE24_25 = 11, COMM_MODE6_7 = 00, and COMM_MODE0_1 = 00. Mode 3 (Big Endian and LSB): COMM_MODE30_31 = 11, COMM_MODE24_25 = 11, COMM_MODE6_7 = 11, and COMM_MODE0_1 = 11.	0x0	R/W
[5:2]	RESERVED	Reserved.	0x0	R

Bits	Bit Name	Description	Reset	Access
[1:0]	COMM_MODE0_1	COMM_MODE30_31, COMM_MODE24_25, COMM_MODE6_7, and COMM_MODE0_1 are combined to setting the SPI communication mode. Mode 0 (Little Endian and MSB): COMM_MODE30_31 = 00, COMM_MODE24_25 = 00, COMM_MODE6_7 = 00, and COMM_MODE0_1 = 00. Mode 1 (Little Endian and LSB): COMM_MODE30_31 = 00, COMM_MODE24_25 = 00, COMM_MODE6_7 = 11, and COMM_MODE0_1 = 11. Mode 2 (Big Endian and MSB): COMM_MODE30_31 = 11, COMM_MODE24_25 = 11, COMM_MODE6_7 = 00, and COMM_MODE0_1 = 00. Mode 3 (Big Endian and LSB): COMM_MODE30_31 = 11, COMM_MODE24_25 = 11, COMM_MODE6_7 = 11, and COMM_MODE0_1 = 11.	0x0	R/W

Table 35. CLR_SPI_CNT, Register Address: 0x0004

Bits	Bit Name	Description	Reset	Access
[32:2]	RESERVED	Reserved.	0x0	R
1	SPI_WRCNT_CLR	Write 1 to this bit to clear the SPI write counter.	0x0	R/W
0	SPI_RDCNT_CLR	Write 1 to this bit to clear the SPI read counter.	0x0	R/W

Table 36. CHIP_INFO1, Register Address: 0x0008

Bits	Bit Name	Description	Reset	Access
[31:24]	CHIP_TYPE	These bits are used to determine the chip type of the ADP5140. The default value is 0xC.	0xC	R
[23:20]	PRODUCT_GRADE	These bits are used to determine the product grade of the ADP5140. The default value is 0x0.	0x0	R
[19:16]	DEVICE_REVISION	These bits are used to determine the device revision of the ADP5140. The default value is 0x3.	0x3	R
[15:8]	PRODUCE_ID_UPBYTE	These bits are combined with PRODUCT_ID_LOWBYTE to determine the product ID value. The default value is 0x51.	0x51	R
[7:0]	PRODUCE_ID_LOWBYTE	These bits are combined with PRODUCT_ID_UPBYTE to determine the product ID value. The default value is 0x40.	0x40	R

Table 37. CHIP_INFO2, Register Address: 0x000C

Bits	Bit Name	Description	Reset	Access
[31:24]	RESERVED	Reserved.	0x0	R
[23:16]	VENDOR_ID_HI	These bits record the high byte of the vendor ID.	0x4	R
[15:8]	VENDOR_ID_LO	These bits record the low byte of the vendor ID.	0x56	R
[7:0]	SPI_REVISION	These bits record the revision number of the SPI.	0x0	R

Table 38. SPI_CRC_PARAM, Register Address: 0x0010

Bits	Bit Name	Description	Reset	Access
[31:16]	SPI_CRC_SEED	SPI Initial Seed Value for the CRC Calculation.	0x5555	R/W
[15:0]	SPI_CRC_POLY	Polynomial Value for the CRC Calculation.	0x90D9	R/W

Table 39. SPI_CNT, Register Address: 0x0014

Bits	Bit Name	Description	Reset	Access
[31:16]	WRITE_CNT	SPI Write Counter.	0x0	R
[15:0]	READ_CNT	SPI Read Counter.	0x0	R

Table 40. PMIC_PSWD, Register Address: 0x001C

Bits	Bit Name	Description	Default	Access
[31:0]	PMIC_PSWD	SPI register access is valid only after writing the correct password. However, IF_CFGA, CLR_SPI_CNT, CHIP_INFO1, CHIP_INFO2, SPI_CRC_PARAM, SPI_CNT, PMIC_PSWD, QA_WD_ANSWER, QA_WD_TOKEN, and SCRATCH_PAD are not protected by this password. 0x5F6A8C3D: unlock the register access. Other settings: lock the register access.	0x0	R/W

Table 41. QA_WD_ANSWER, Register Address: 0x0020

Bits	Bit Name	Description	Reset	Access
[31:0]	QA_WD_ANSWER	Write the correct answer to this register to feed the QA watchdog.	0x0	R/W

Table 42. QA_WD_TOKEN, Register Address: 0x0024

Bits	Bit Name	Description	Reset	Access
[31:4]	RESERVED	Reserved.	0x0	R
[3:0]	QA_WD_TOKEN	These bits are the token to generate the answer for the QA watchdog.	0x0	R

Table 43. SCRATCH_PAD, Register Address: 0x002C

Bits	Bit Name	Description	Reset	Access
[31:0]	SCRATCH_PAD	Only use this register for read and write register tests.	0x0	R/W

Table 44. FAIL_SAFE_PIN_TIMEOUT, Register Address: 0x2000

Bits	Bit Name	Description	Reset	Access
[31:15]	RESERVED	Reserved.	0x0	R
[14:10]	STATUS_TIMEOUT[4:0]	Set the Timeout for the $\overline{\text{STATUS}}$ Pin. The range is from 5 µs to 160 µs with 5 µs step. Timeout (µs) = 5 µs + STATUS_TIMEOUT[4:0] × 5 µs.	0x0	R/W
[9:5]	FAULT_TIMEOUT[4:0]	Set the Timeout for the $\overline{\text{FAULT}}$ Pin. The range is from 5 µs to 160 µs with 5 µs step. Timeout (µs) = 5 µs + FAULT_TIMEOUT[4:0] × 5 µs.	0x0	R/W
[4:0]	RESET_TIMEOUT[4:0]	Set the Timeout for the $\overline{\text{RESET}}$ Pin. The range is from 5 µs to 160 µs with 5 µs step. Timeout (µs) = 5 µs + RESET_TIMEOUT[4:0] × 5 µs.	0x0	R/W

Table 45. UV_STATUS, Register Address: 0x2004

Bits	Bit Name	Description	Reset	Access
[31:15]	RESERVED	Reserved.	0x0	R
14	VIO_UVLO_STATUS	Status for the Undervoltage on VIO. 0: no undervoltage fault on VIO. 1: undervoltage fault on VIO.	0x0	R
13	VM1_UV_STATUS	Status for the Undervoltage on VM1. 0: no undervoltage on VM1. 1: undervoltage on VM1.	0x0	R

Bits	Bit Name	Description	Reset	Access
12	VM0_UV_STATUS	Status for the Undervoltage on VM0. 0: no undervoltage on VM0. 1: undervoltage on VM0.	0x0	R
11	VOUT11_UV_STATUS	Status for the Undervoltage on Regulator 11. 0: no undervoltage on Regulator 11. 1: undervoltage on Regulator 11.	0x0	R
10	VOUT10_UV_STATUS	Status for the Undervoltage on Regulator 10. 0: no undervoltage on Regulator 10. 1: undervoltage on Regulator 10.	0x0	R
9	VOUT9_UV_STATUS	Status for the Undervoltage on Regulator 9. 0: no undervoltage on Regulator 9. 1: undervoltage on Regulator 9.	0x0	R
8	VOUT8_UV_STATUS	Status for the Undervoltage on Regulator 8. 0: no undervoltage on Regulator 8. 1: undervoltage on Regulator 8.	0x0	R
7	VOUT7_UV_STATUS	Status for the Undervoltage on Regulator 7. 0: no undervoltage on Regulator 7. 1: undervoltage on Regulator 7.	0x0	R
6	VOUT6_UV_STATUS	Status for the Undervoltage on Regulator 6. 0: no undervoltage on Regulator 6. 1: undervoltage on Regulator 6.	0x0	R
5	VOUT5_UV_STATUS	Status for the Undervoltage on Regulator 5. 0: no undervoltage on Regulator 5. 1: undervoltage on Regulator 5.	0x0	R
4	VOUT4_UV_STATUS	Status for the Undervoltage on Regulator 4. 0: no undervoltage on Regulator 4. 1: undervoltage on Regulator 4.	0x0	R
3	VOUT3_UV_STATUS	Status for the Undervoltage on Regulator 3. 0: no undervoltage on Regulator 3. 1: undervoltage on Regulator 3.	0x0	R
2	VOUT2_UV_STATUS	Status for the Undervoltage on Regulator 2. 0: no undervoltage on Regulator 2. 1: undervoltage on Regulator 2.	0x0	R
1	VOUT1_UV_STATUS	Status for the Undervoltage on Regulator 1. 0: no undervoltage on Regulator 1. 1: undervoltage on Regulator 1.	0x0	R
0	VOUT12_UV_STATUS	Status for the Undervoltage on Regulator 12. 0: no undervoltage on Regulator 12. 1: undervoltage on Regulator 12.	0x0	R

Table 46. OV_STATUS, Register Address: 0x2008

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
13	VM1_OV_STATUS	Status for the Overvoltage on VM1. 0: no overvoltage on VM1. 1: overvoltage on VM1.	0x0	R
12	VM0_OV_STATUS	Status for the Overvoltage on VM0. 0: no overvoltage on VM0. 1: overvoltage on VM0.	0x0	R
11	VOUT11_OV_STATUS	Status for the Overvoltage on Regulator 11. 0: no overvoltage on Regulator 11. 1: overvoltage on Regulator 11.	0x0	R
10	VOUT10_OV_STATUS	Status for the Overvoltage on Regulator 10. 0: no overvoltage on Regulator 10. 1: overvoltage on Regulator 10.	0x0	R
9	VOUT9_OV_STATUS	Status for the Overvoltage on Regulator 9. 0: no overvoltage on Regulator 9. 1: overvoltage on Regulator 9.	0x0	R
8	VOUT8_OV_STATUS	Status for the Overvoltage on Regulator 8. 0: no overvoltage on Regulator 8. 1: overvoltage on Regulator 8.	0x0	R
7	VOUT7_OV_STATUS	Status for the Overvoltage on Regulator 7. 0: no overvoltage on Regulator 7. 1: overvoltage on Regulator 7.	0x0	R
6	VOUT6_OV_STATUS	Status for the Overvoltage on Regulator 6. 0: no overvoltage on Regulator 6. 1: overvoltage on Regulator 6.	0x0	R
5	VOUT5_OV_STATUS	Status for the Overvoltage on Regulator 5. 0: no overvoltage on Regulator 5. 1: overvoltage on Regulator 5.	0x0	R
4	VOUT4_OV_STATUS	Status for the Overvoltage on Regulator 4. 0: no overvoltage on Regulator 4. 1: overvoltage on Regulator 4.	0x0	R
3	VOUT3_OV_STATUS	Status for the Overvoltage on Regulator 3. 0: no overvoltage on Regulator 3. 1: overvoltage on Regulator 3.	0x0	R
2	VOUT2_OV_STATUS	Status for the Overvoltage on Regulator 2. 0: no overvoltage on Regulator 2. 1: overvoltage on Regulator 2.	0x0	R
1	VOUT1_OV_STATUS	Status for the Overvoltage on Regulator 1. 0: no overvoltage on Regulator 1. 1: overvoltage on Regulator 1.	0x0	R
0	VOUT12_OV_STATUS	Status for the Overvoltage on Regulator 12. 0: no overvoltage on Regulator 12. 1: overvoltage on Regulator 12.	0x0	R

Table 47. WARN_STATUS, Register Address: 0x200C

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
13	VM1_WARN_STATUS	Warning Status on VM1. 0: no warning on VM1. 1: voltage on VM1 exceeds the warning threshold.	0x0	R
12	VM0_WARN_STATUS	Warning Status on VM0. 0: no warning on VM0. 1: voltage on VM0 exceeds the warning threshold.	0x0	R
11	VOUT11_WARN_STATUS	Warning Status on Regulator 11. 0: no warning on Regulator 11. 1: voltage on Regulator 11 exceeds the warning threshold.	0x0	R
10	VOUT10_WARN_STATUS	Warning Status on Regulator 10. 0: no warning on Regulator 10. 1: voltage on Regulator 10 exceeds the warning threshold.	0x0	R
9	VOUT9_WARN_STATUS	Warning Status on Regulator 9. 0: no warning on Regulator 9. 1: voltage on Regulator 9 exceeds the warning threshold.	0x0	R
8	VOUT8_WARN_STATUS	Warning Status on Regulator 8. 0: no warning on Regulator 8. 1: voltage on Regulator 8 exceeds the warning threshold.	0x0	R
7	VOUT7_WARN_STATUS	Warning Status on Regulator 7. 0: no warning on Regulator 7. 1: voltage on Regulator 7 exceeds the warning threshold.	0x0	R
6	VOUT6_WARN_STATUS	Warning Status on Regulator 6. 0: no warning on Regulator 6. 1: voltage on Regulator 6 exceeds the warning threshold.	0x0	R
5	VOUT5_WARN_STATUS	Warning Status on Regulator 5. 0: no warning on Regulator 5. 1: voltage on Regulator 5 exceeds the warning threshold.	0x0	R
4	VOUT4_WARN_STATUS	Warning Status on Regulator 4. 0: no warning on Regulator 4. 1: voltage on Regulator 4 exceeds the warning threshold.	0x0	R
3	VOUT3_WARN_STATUS	Warning Status on Regulator 3. 0: no warning on Regulator 3. 1: voltage on Regulator 3 exceeds the warning threshold.	0x0	R
2	VOUT2_WARN_STATUS	Warning Status on Regulator 2. 0: no warning on Regulator 2. 1: voltage on Regulator 2 exceeds the warning threshold.	0x0	R
1	VOUT1_WARN_STATUS	Warning Status on Regulator 1. 0: no warning on Regulator 1. 1: voltage on Regulator 1 exceeds the warning threshold.	0x0	R
0	VOUT12_WARN_STATUS	Warning Status on Regulator 12. 0: no warning on Regulator 12. 1: voltage on Regulator 12 exceeds the warning threshold.	0x0	R

Table 48. OT_STATUS, Register Address: 0x2010

Bits	Bit Name	Description	Reset	Access
[31:12]	RESERVED	Reserved.	0x0	R
11	VOUT12_OT_STATUS	Overtemperature Status on Regulator 12. 0: no overtemperature on Regulator 12. 1: overtemperature on Regulator 12.	0x0	R
10	VOUT4_OT_STATUS	Overtemperature Status on Regulator 4. 0: no overtemperature on Regulator 4. 1: overtemperature on Regulator 4.	0x0	R
9	VOUT3_OT_STATUS	Overtemperature Status on Regulator 3. 0: no overtemperature on Regulator 3. 1: overtemperature on Regulator 3.	0x0	R
8	VOUT2_OT_STATUS	Overtemperature Status on Regulator 2. 0: no overtemperature on Regulator 2. 1: overtemperature on Regulator 2.	0x0	R
7	VOUT1_OT_STATUS	Overtemperature Status on Regulator 1. 0: no overtemperature on Regulator 1. 1: over temperature on Regulator 1.	0x0	R
6	VOUT11_OT_STATUS	Overtemperature Status on Regulator 11. 0: no overtemperature on Regulator 11. 1: overtemperature on Regulator 11.	0x0	R
5	VOUT10_OT_STATUS	Overtemperature Status on Regulator 10. 0: no overtemperature on Regulator 10. 1: overtemperature on Regulator 10.	0x0	R
4	VOUT9_OT_STATUS	Overtemperature Status on Regulator 9. 0: no overtemperature on Regulator 9. 1: overtemperature on Regulator 9.	0x0	R
3	VOUT8_OT_STATUS	Overtemperature Status on Regulator 8. 0: no overtemperature on Regulator 8. 1: overtemperature on Regulator 8.	0x0	R
2	VOUT7_OT_STATUS	Overtemperature Status on Regulator 7. 0: no overtemperature on Regulator 7. 1: overtemperature on Regulator 7.	0x0	R
1	VOUT6_OT_STATUS	Overtemperature Status on Regulator 6. 0: no overtemperature on Regulator 6. 1: overtemperature on Regulator 6.	0x0	R
0	VOUT5_OT_STATUS	Overtemperature Status on Regulator 5. 0: no overtemperature on Regulator 5. 1: overtemperature on Regulator 5.	0x0	R

Table 49. OTHER_STATUS, Register Address: 0x2014

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved.	0x0	R
28	WDI1_EXT_STATUS	Falling Edge Detection on WDI1 when WD1 is Disabled. 0: no falling edge detected on WDI1. 1: falling edge detected on WDI1.	0x0	R
27	WDI0_EXT_STATUS	Falling Edge Detection on WDI0 when WD0 is Disabled. 0: no falling edge detected on WDI0. 1: falling edge detected on WDI0.	0x0	R
26	VSET1_DETECTION_STATUS	VSET1 Pin Detection Status. 0: VSET1 pin detection pass. 1: VSET1 pin detection fail.	0x0	R
25	MODE_DETECTION_STATUS	MODE Pin Detection Status. 0: MODE pin detection pass. 1: MODE pin detection fail.	0x0	R
24	SYNC_STATUS	Synchronization Status when Configured as Sync In. 0: synchronization complete. 1: synchronization fail.	0x0	R
23	WDI1_PULSE_STATUS	Pulse Monitor Status on the WDI1 pin. 0: pulse on WDI1 is within range. 1: pulse on WDI1 is out of range.	0x0	R
22	WDI0_PULSE_STATUS	Pulse Monitor Status on the WDI0 Pin. 0: pulse on WDI0 is within range. 1: pulse on WDI0 is out of range.	0x0	R
21	CLKM_FAIL_STATUS	Clock Monitor Fail Status. 0: no clock drift occurs. 1: clock drift occurs.	0x0	R
20	SHR_CRC_STATUS	CRC Error Status in the Shadow Register. 0: no CRC error. 1: CRC error.	0x0	R
19	SHR_ECC_STATUS	ECC Two-Bit Error Status in Shadow Register. 0: no two bits ECC error. 1: two bits ECC error.	0x0	R
18	$\overline{\text{STATUS}}$_EXT_STATUS	External Fail on the $\overline{\text{STATUS}}$ Pin. 0: no output pin fail on the $\overline{\text{STATUS}}$ pin. 1: output pin fail on the $\overline{\text{STATUS}}$ pin.	0x0	R
17	$\overline{\text{FAULT}}$_EXT_STATUS	External Fail on the $\overline{\text{FAULT}}$ Pin. 0: no output pin fail on the $\overline{\text{FAULT}}$ pin. 1: output pin fail on the $\overline{\text{FAULT}}$ pin.	0x0	R
16	$\overline{\text{RESET}}$_EXT_STATUS	External Fail on the $\overline{\text{RESET}}$ Pin. 0: no output pin fail on the $\overline{\text{RESET}}$ pin. 1: output pin fail on the $\overline{\text{RESET}}$ pin.	0x0	R
[15:9]	RESERVED	Reserved	0x0	R

Bits	Bit Name	Description	Reset	Access
8	SPI_FMT_ERR_STATUS	SPI Format Error Status. 0: no error. 1: error.	0x0	R
7	SPI_RDD_ERR_STATUS	SPI Redundant Error Status. 0: no error. 1: error.	0x0	R
6	SPI_CLK_ERR_STATUS	SPI Clock Error Status. 0: no error. 1: error.	0x0	R
5	SPI_ACCESS_FAIL	SPI Accessed Unlocked Register Fail 0: no fail. 1: SPI access unlocked register.	0x0	R
4	SPI_ADDR_FAIL	SPI Accessed Address Fail. 0: no address fail. 1: SPI accessed wrong address.	0x0	R
3	SPI_CRC_FAIL	SPI CRC Status. 0: no CRC fail on SPI. 1: CRC fail on SPI.	0x0	R
2	QA_WD_FAIL	QA Watchdog Fail. 0: no fail on QA watchdog. 1: QA watchdog fail.	0x0	R
1	WD1_FAIL	WD1 Fail. 0: no fail on WD1 1: WD1 fail.	0x0	R
0	WD0_FAIL	WD0 Fail. 0: no fail on WD0. 1: WD0 fail.	0x0	R

Table 50. OTHER1_STATUS, Register Address: 0x2018

Bits	Bit Name	Description	Reset	Access
[31:19]	RESERVED	Reserved.	0x0	R
18	FB8_RECAP_SHORT_STATUS	Status for FB8 and RECAP Short Event. 0: FB8 and RECAP are not short. 1: FB8 and RECAP are short.	0x0	R
17	VREG_GOOD_STATUS	VREG Good Status. 0: VREG is not good. 1: VREG is good.	0x0	R
16	PIN_OPEN_FAULT_LDO7_STATUS	LDO7 Pin Open Fault Status. 0: no open fault. 1: open fault.	0x0	R
15	PIN_OPEN_FAULT_LDO6_STATUS	LDO6 Pin Open Fault Status. 0: no open fault. 1: open fault.	0x0	R

Bits	Bit Name	Description	Reset	Access
14	PIN_OPEN_FAULT_LDO5_STATUS	LDO5 Pin Open Fault Status. 0: no open fault. 1: open fault.	0x0	R
13	PIN_OPEN_FAULT_LDO4_STATUS	LDO4 Pin Open Fault Status. 0: no open fault. 1: open fault.	0x0	R
12	PIN_OPEN_FAULT_LDO3_STATUS	LDO3 Pin Open Fault Status. 0: no open fault. 1: open fault.	0x0	R
11	PIN_OPEN_FAULT_LDO2_STATUS	LDO2 Pin Open Fault Status. 0: no open fault. 1: open fault.	0x0	R
10	PIN_OPEN_FAULT_LDO1_STATUS	LDO1 Pin Open Fault Status. 0: no open fault. 1: open fault.	0x0	R
9	PIN_OPEN_FAULT_BOOST_STATUS	BOOST Pin Open Fault Status. 0: no open fault. 1: open fault.	0x0	R
8	WAKE_FALLING_EVT_STATUS	Status for Falling Event on the WAKE Pin. 0: no falling event occurs on the WAKE pin. 1: falling event occurs on the WAKE pin.	0x0	R
7	SYS_REG_CRC_ERR_STATUS	System Register CRC Error Status. 0: no error. 1: error.	0x0	R
6	TSD_STATUS	Status for TSD 0: no TSD occurs. 1: TSD occurs.	0x0	R
5	LDO5_INPUT_OVLO_STATUS	Status for the LDO5 Input Overvoltage. 0: no overvoltage. 1: overvoltage.	0x0	R
4	LDO3_INPUT_OVLO_STATUS	Status for the LDO3 Input Overvoltage. 0: no overvoltage. 1: overvoltage.	0x0	R
3	LDO1_INPUT_OVLO_STATUS	Status for the LDO1 Input Overvoltage. 0: no overvoltage. 1: overvoltage.	0x0	R
2	LDO5_INPUT_UVLO_STATUS	Status for the LDO5 Input Undervoltage 0: no undervoltage. 1: undervoltage.	0x0	R
1	LDO3_INPUT_UVLO_STATUS	Status for the LDO3 Input Undervoltage 0: no undervoltage. 1: undervoltage.	0x0	R

Bits	Bit Name	Description	Reset	Access
0	LDO1_INPUT_UVLO_STATUS	Status for the LDO1 Input Undervoltage. 0: no undervoltage. 1: undervoltage.	0x0	R

Table 51. UV_LATCH[1], Register Address: 0x201C

Bits	Bit Name	Description	Reset	Access
[31:15]	RESERVED	Reserved.	0x0	R
14	VIO_UVLO_LATCH	Latch the Undervoltage Event on VIO. 0: no undervoltage occurred on VIO. 1: undervoltage occurred on VIO.	0x0	R
13	VM1_UV_LATCH	Latch the Undervoltage Event on VM1. 0: no undervoltage occurred on VM10, no undervoltage occurred on VM1. 1: undervoltage occurred on VM1.	0x0	R
12	VM0_UV_LATCH	Latch the Undervoltage Event on VM0. 0: no undervoltage occurred on VM0. 1: undervoltage occurred on VM0.	0x0	R
11	VOUT11_UV_LATCH	Latch the Undervoltage Event on Regulator 11. 0: no undervoltage occurred on Regulator 11. 1: undervoltage occurred on Regulator 11.	0x0	R
10	VOUT10_UV_LATCH	Latch the Undervoltage Event on Regulator 10. 0: no undervoltage occurred on Regulator 10. 1: undervoltage occurred on Regulator 10.	0x0	R
9	VOUT9_UV_LATCH	Latch the Undervoltage Event on Regulator 9. 0: no undervoltage occurred on Regulator 9. 1: undervoltage occurred on Regulator 9.	0x0	R
8	VOUT8_UV_LATCH	Latch the Undervoltage Event on Regulator 8. 0: no undervoltage occurred on Regulator 8. 1: undervoltage occurred on Regulator 8.	0x0	R
7	VOUT7_UV_LATCH	Latch the Undervoltage Event on Regulator 7. 0: no undervoltage occurred on Regulator 7. 1: undervoltage occurred on Regulator 7.	0x0	R
6	VOUT6_UV_LATCH	Latch the Undervoltage Event on Regulator 6. 0: no undervoltage occurred on Regulator 6. 1: undervoltage occurred on Regulator 6.	0x0	R
5	VOUT5_UV_LATCH	Latch the Undervoltage Event on Regulator 5. 0: no undervoltage occurred on Regulator 5. 1: undervoltage occurred on Regulator 5.	0x0	R
4	VOUT4_UV_LATCH	Latch the Undervoltage Event on Regulator 4. 0: no undervoltage occurred on Regulator 4. 1: undervoltage occurred on Regulator 4.	0x0	R
3	VOUT3_UV_LATCH	Latch the Undervoltage Event on Regulator 3. 0: no undervoltage occurred on Regulator 3. 1: undervoltage occurred on Regulator 3.	0x0	R

Bits	Bit Name	Description	Reset	Access
2	VOUT2_UV_LATCH	Latch the Undervoltage Event on Regulator 2. 0: no undervoltage occurred on Regulator 2. 1: undervoltage occurred on Regulator 2.	0x0	R
1	VOUT1_UV_LATCH	Latch the Undervoltage Event on Regulator 1. 0: no undervoltage occurred on Regulator 1. 1: undervoltage occurred on Regulator 1.	0x0	R
0	VOUT12_UV_LATCH	Latch the Undervoltage Event on Regulator 12. 0: no undervoltage occurred on Regulator 12. 1: undervoltage occurred on Regulator 12.	0x0	R

[1] Write 1 to clear.

Table 52. OV_LATCH[1], Register Address: 0x2020

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
13	VM1_OV_LATCH	Latch the Overvoltage Event on VM1. 0: no overvoltage occurred on VM1. 1: overvoltage occurred on VM1.	0x0	R
12	VM0_OV_LATCH	Latch the Overvoltage Event on VM0. 0: no overvoltage occurred on VM0. 1: overvoltage occurred on VM0.	0x0	R
11	VOUT11_OV_LATCH	Latch the Overvoltage Event on Regulator 11. 0: no overvoltage occurred on Regulator 11. 1: overvoltage occurred on Regulator 11.	0x0	R
10	VOUT10_OV_LATCH	Latch the Overvoltage Event on Regulator 10. 0: no overvoltage occurred on Regulator 10. 1: overvoltage occurred on Regulator 10.	0x0	R
9	VOUT9_OV_LATCH	Latch the Overvoltage Event on Regulator 9. 0: no overvoltage occurred on Regulator 9. 1: overvoltage occurred on Regulator 9.	0x0	R
8	VOUT8_OV_LATCH	Latch the Overvoltage Event on Regulator 8. 0: no overvoltage occurred on Regulator 8. 1: overvoltage occurred on Regulator 8.	0x0	R
7	VOUT7_OV_LATCH	Latch the Overvoltage Event on Regulator 7. 0: no overvoltage occurred on Regulator 7. 1: overvoltage occurred on Regulator 7.	0x0	R
6	VOUT6_OV_LATCH	Latch the Overvoltage Event on Regulator 6. 0: no overvoltage occurred on Regulator 6. 1: overvoltage occurred on Regulator 6.	0x0	R
5	VOUT5_OV_LATCH	Latch the Overvoltage Event on Regulator 5. 0: no overvoltage occurred on Regulator 5. 1: overvoltage occurred on Regulator 5.	0x0	R

Bits	Bit Name	Description	Reset	Access
4	VOUT4_OV_LATCH	Latch the Overvoltage Event on Regulator 4. 0: no overvoltage occurred on Regulator 4. 1: overvoltage occurred on Regulator 4.	0x0	R
3	VOUT3_OV_LATCH	Latch the Overvoltage Event on Regulator 3. 0: no overvoltage occurred on Regulator 3. 1: overvoltage occurred on Regulator 3.	0x0	R
2	VOUT2_OV_LATCH	Latch the Overvoltage Event on Regulator 2. 0: no overvoltage occurred on Regulator 2. 1: overvoltage occurred on Regulator 2.	0x0	R
1	VOUT1_OV_LATCH	Latch the Overvoltage Event on Regulator 1. 0: no overvoltage occurred on Regulator 1. 1: overvoltage occurred on Regulator 1.	0x0	R
0	VOUT12_OV_LATCH	Latch the Overvoltage Event on Regulator 12. 0: no overvoltage occurred on Regulator 12. 1: overvoltage occurred on Regulator 12.	0x0	R

[1] Write 1 to clear.

Table 53. WARN_LATCH[1], Register Address: 0x2024

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
13	VM1_WARN_LATCH	Latch the Warning Event on VM1. 0: no warning occurred on VM1. 1: warning occurred on VM1.	0x0	R
12	VM0_WARN_LATCH	Latch the Warning Event on VM0. 0: no warning occurred on VM0. 1: warning occurred on VM0.	0x0	R
11	VOUT11_WARN_LATCH	Latch the Warning Event on Regulator 11. 0: no warning occurred on Regulator 11. 1: warning occurred on Regulator 11.	0x0	R
10	VOUT10_WARN_LATCH	Latch the Warning Event on Regulator 10. 0: no warning occurred on Regulator 10. 1: warning occurred on Regulator 10.	0x0	R
9	VOUT9_WARN_LATCH	Latch the Warning Event on Regulator 9. 0: no warning occurred on Regulator 9. 1: warning occurred on Regulator 9.	0x0	R
8	VOUT8_WARN_LATCH	Latch the Warning Event on Regulator 8. 0: no warning occurred on Regulator 8. 1: warning occurred on Regulator 8.	0x0	R
7	VOUT7_WARN_LATCH	Latch the Warning Event on Regulator 7. 0: no warning occurred on Regulator 7. 1: warning occurred on Regulator 7.	0x0	R

Bits	Bit Name	Description	Reset	Access
6	VOUT6_WARN_LATCH	Latch the Warning Event on Regulator 6. 0: no warning occurred on Regulator 6. 1: warning occurred on Regulator 6.	0x0	R
5	VOUT5_WARN_LATCH	Latch the Warning Event on Regulator 5. 0: no warning occurred on Regulator 5. 1: warning occurred on Regulator 5.	0x0	R
4	VOUT4_WARN_LATCH	Latch the Warning Event on Regulator 4. 0: no warning occurred on Regulator 4. 1: warning occurred on Regulator 4.	0x0	R
3	VOUT3_WARN_LATCH	Latch the Warning Event on Regulator 3. 0: no warning occurred on Regulator 3. 1: warning occurred on Regulator 3.	0x0	R
2	VOUT2_WARN_LATCH	Latch the Warning Event on Regulator 2. 0: no warning occurred on Regulator 2. 1: warning occurred on Regulator 2.	0x0	R
1	VOUT1_WARN_LATCH	Latch the Warning Event on Regulator 1. 0: no warning occurred on Regulator 1. 1: warning occurred on Regulator 1.	0x0	R
0	VOUT12_WARN_LATCH	Latch the Warning Event on Regulator 12. 0: no warning occurred on Regulator 12. 1: warning occurred on Regulator 12.	0x0	R

[1] Write 1 to clear.

Table 54. OT_LATCH[1], Register Address: 0x2028

Bits	Bit Name	Description	Reset	Access
[31:12]	RESERVED	Reserved.	0x0	R
11	VOUT12_OT_LATCH	Latch the Overtemperature Event on Regulator 12. 0: no overtemperature occurred on Regulator 12. 1: overtemperature occurred on Regulator 12.	0x0	R
10	VOUT4_OT_LATCH	Latch the Overtemperature Event on Regulator 4. 0: no overtemperature occurred on Regulator 4. 1: overtemperature occurred on Regulator 4.	0x0	R
9	VOUT3_OT_LATCH	Latch the Overtemperature Event on Regulator 3. 0: no overtemperature occurred on Regulator 3. 1: overtemperature occurred on Regulator 3.	0x0	R
8	VOUT2_OT_LATCH	Latch the Overtemperature Event on Regulator 2. 0: no overtemperature occurred on Regulator 2. 1: overtemperature occurred on Regulator 2.	0x0	R
7	VOUT1_OT_LATCH	Latch the Overtemperature Event on Regulator 1. 0: no overtemperature occurred on Regulator 1. 1: overtemperature occurred on Regulator 1.	0x0	R

Bits	Bit Name	Description	Reset	Access
6	VOUT11_OT_LATCH	Latch the Overtemperature Event on Regulator 11. 0: no overtemperature occurred on Regulator 11. 1: overtemperature occurred on Regulator 11.	0x0	R
5	VOUT10_OT_LATCH	Latch the Overtemperature Event on Regulator 10. 0: no overtemperature occurred on Regulator 10. 1: overtemperature occurred on Regulator 10.	0x0	R
4	VOUT9_OT_LATCH	Latch the Overtemperature Event on Regulator 9. 0: no overtemperature occurred on Regulator 9. 1: overtemperature occurred on Regulator 9.	0x0	R
3	VOUT8_OT_LATCH	Latch the Overtemperature Event on Regulator 8. 0: no overtemperature occurred on Regulator 8. 1: overtemperature occurred on Regulator 8.	0x0	R
2	VOUT7_OT_LATCH	Latch the Overtemperature Event on Regulator 7. 0: no overtemperature occurred on Regulator 7. 1: overtemperature occurred on Regulator 7.	0x0	R
1	VOUT6_OT_LATCH	Latch the Overtemperature Event on Regulator 6. 0: no overtemperature occurred on Regulator 6. 1: overtemperature occurred on Regulator 6.	0x0	R
0	VOUT5_OT_LATCH	Latch the Overtemperature Event on Regulator 5. 0: no overtemperature occurred on Regulator 5. 1: overtemperature occurred on Regulator 5.	0x0	R

[1] Write 1 to clear.

Table 55. OTHER_LATCH[1], Register Address: 0x202C

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved.	0x0	R
28	WDI1_EXT_LATCH	Latch the Falling Edge Event on the WDI1 Pin when WD1 is Disabled. 0: no falling edge occurred on the WDI1 Pin. 1: falling edge occurred on the WDI1 Pin.	0x0	R
27	WDI0_EXT_LATCH	Latch the Falling Edge Event on the WDI0 Pin when WD0 is Disabled. 0: no falling edge occurred on the WDI0 Pin. 1: falling edge occurred on the WDI0 Pin.	0x0	R
26	VSET1_DETECTION_LATCH	Latch the VSET1 Pin Fault Event. 0: no fault occurred on the VSET1 pin. 1: fault occurred on the VSET1 pin.	0x0	R
25	MODE_DETECTION_LATCH	Latch the MODE Pin Fault Event. 0: no fault occurred on the MODE pin. 1: fault occurred on the MODE pin.	0x0	R
24	SYNC_FAIL_LATCH	Latch the Synchronization Fail Event. 0: no synchronization fail occurred. 1: synchronization fail occurred.	0x0	R

Bits	Bit Name	Description	Reset	Access
23	WDI1_PULSE_FAIL_LATCH	Latch the Pulse Monitor Fail Event on the WDI1 Pin. 0: no pulse fail occurred on the WDI1 pin. 1: pulse fail occurred on the WDI1 pin.	0x0	R
22	WDI0_PULSE_FAIL_LATCH	Latch the Pulse Monitor Fail Event on the WDI0 Pin. 0: no pulse fail occurred on the WDI0 pin. 1: pulse fail occurred on the WDI0 pin.	0x0	R
21	CLKM_FAIL_LATCH	Latch the Clock Fail Event. 0: no clock fail occurred. 1: clock failed occurred.	0x0	R
20	SHR_CRC_FAIL_LATCH	Latch the CRC Error Event in the Shadow Register. 0: no CRC error occurred. 1: CRC error occurred.	0x0	R
19	SHR_ECC_FAIL_LATCH	Latch the ECC Two Bits Error Event in the Shadow Register. 0: no two bits ECC error occurred. 1: two bits ECC error occurred.	0x0	R
18	$\overline{\text{STATUS}}$_EXT_FAIL_LATCH	Latch the External Fail Event on the $\overline{\text{STATUS}}$ Pin. 0: no output pin fail occurred on the $\overline{\text{STATUS}}$ Pin. 1: output pin fail occurred on the $\overline{\text{STATUS}}$ Pin.	0x0	R
17	$\overline{\text{FAULT}}$_EXT_FAIL_LATCH	Latch the External Fail Event on the $\overline{\text{FAULT}}$ Pin. 0: no output pin fail occurred on the $\overline{\text{FAULT}}$ Pin. 1: pin fail occurred on the $\overline{\text{FAULT}}$ Pin.	0x0	R
16	$\overline{\text{RESET}}$_EXT_FAIL_LATCH	Latch the External Fail Event on the $\overline{\text{RESET}}$ Pin. 0: no output pin fail occurred on the $\overline{\text{RESET}}$ Pin. 1: output pin fail occurred on the $\overline{\text{RESET}}$ Pin.	0x0	R
[15:9]	RESERVED	Reserved.	0x0	R
8	SPI_FMT_ERR_LATCH	Latch the SPI Format Error. 0: no format error occurred. 1: format error occurred.	0x0	R
7	SPI_RDD_ERR_LATCH	Latch the SPI Redundant Error. 0: no redundant error occurred. 1: redundant error occurred.	0x0	R
6	SPI_CLK_ERR_LATCH	Latch the SPI Clock Error. 0: no clock error occurred. 1: clock error occurred.	0x0	R
5	SPI_ACCESS_FAIL_LATCH	Latch the SPI Accessed Unlocked Register Fail. 0: no accessed fail occurred. 1: SPI access unlocked register fail occurred.	0x0	R
4	SPI_ADDR_FAIL_LATCH	Latch the SPI Accessed Address Fail Event. 0: no address fail occurred. 1: SPI accessed wrong address occurred.	0x0	R

Bits	Bit Name	Description	Reset	Access
3	SPI_CRC_FAIL_LATCH	Latch the SPI CRC Error Event. 0: no CRC fail occurred on the SPI. 1: CRC fail occurred on the SPI.	0x0	R
2	QA_WD_FAIL_LATCH	Latch QA Watchdog Fail. 0: no QA watchdog fail occurred. 1: QA watchdog fail occurred.	0x0	R
1	WD1_FAIL_LATCH	Latch WD1 Fail. 0: no WD1 fail occurred. 1: WD1 fail occurred.	0x0	R
0	WD0_FAIL_LATCH	Latch WD0 Fail. 0: no WD0 fail occurred. 1: WD0 fail occurred.	0x0	R

[1] Write 1 to clear.

Table 56. OTHER1_LATCH[1], Register Address: 0x2030

Bits	Bit Name	Description	Reset	Access
[31:19]	RESERVED	Reserved.	0x0	R
18	FB8_RECAP_SHORT_LATCH	Latch the FB8 and RECAP Short Event. 0: no FB8 and RECAP short occurred. 1: FB8 and RECAP short occurred.	0x0	R
17	VREG_GOOD_LATCH	VREG Good Latch. 0: no VREG good event occurred. 1: VREG good event occurred.	0x0	R
16	PIN_OPEN_FAULT_LDO7_LATCH	LDO7 Pin Open Fault Latch. 0: no open fault occurred. 1: open fault occurred.	0x0	R
15	PIN_OPEN_FAULT_LDO6_LATCH	LDO6 Pin Open Fault Latch. 0: no open fault occurred. 1: open fault occurred.	0x0	R
14	PIN_OPEN_FAULT_LDO5_LATCH	LDO5 Pin Open Fault Latch. 0: no open fault occurred. 1: open fault occurred.	0x0	R
13	PIN_OPEN_FAULT_LDO4_LATCH	LDO4 Pin Open Fault Latch. 0: no open fault occurred. 1: open fault occurred.	0x0	R
12	PIN_OPEN_FAULT_LDO3_LATCH	LDO3 Pin Open Fault Latch. 0: no open fault occurred. 1: open fault occurred.	0x0	R
11	PIN_OPEN_FAULT_LDO2_LATCH	LDO2 Pin Open Fault Latch. 0: no open fault occurred. 1: open fault occurred.	0x0	R

Bits	Bit Name	Description	Reset	Access
10	PIN_OPEN_FAULT_LDO1_LATCH	LDO1 Pin Open Fault Latch. 0: no open fault occurred. 1: open fault occurred.	0x0	R
9	PIN_OPEN_FAULT_BOOST_LATCH	BOOST Pin Open Fault Latch. 0: no open fault occurred. 1: open fault occurred.	0x0	R
8	WAKE_FALLING_EVT_LATCH	Latch the Falling Event on the WAKE Pin. 0: no falling event occurred on the WAKE pin. 1: falling event occurred on the WAKE pin.	0x0	R
7	SYS_REG_CRC_ERR_LATCH	Latch the System Register CRC Error. 0: no system register CRC error occurred. 1: system register CRC occurred.	0x0	R
6	TSD_LATCH	Latch the TSD Event. 0: no TSD event occurred. 1: TSD event occurred.	0x0	R
5	LDO5_INPUT_OVLO_LATCH	Latch the LDO5 Input Overvoltage Event. 0: no overvoltage occurred. 1: overvoltage occurred.	0x0	R
4	LDO3_INPUT_OVLO_LATCH	Latch the LDO3 Input Overvoltage Event. 0: no overvoltage occurred. 1: overvoltage occurred.	0x0	R
3	LDO1_INPUT_OVLO_LATCH	Latch the LDO1 Input Overvoltage Event. 0: no overvoltage occurred. 1: overvoltage occurred.	0x0	R
2	LDO5_INPUT_UVLO_LATCH	Latch the LDO5 Input Undervoltage Event. 0: no undervoltage occurred. 1: undervoltage occurred.	0x0	R
1	LDO3_INPUT_UVLO_LATCH	Latch the LDO3 Input Undervoltage Event. 0: no undervoltage occurred. 1: undervoltage occurred.	0x0	R
0	LDO1_INPUT_UVLO_LATCH	Latch the LDO1 Input Undervoltage Event. 0: no undervoltage occurred. 1: undervoltage occurred.	0x0	R

[1] Write 1 to clear.

Table 57. UV_RST_MASK, Register Address: 0x2034

Bits	Bit Name	Description	Reset	Access
[31:15]	RESERVED	Reserved.	0x0	R
14	VIO_UVLO_RST_MASK	Mask the VIO_UVLO_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
13	VM1_UV_RST_MASK	Mask the VM1_UV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
12	VM0_UV_RST_MASK	Mask the VM0_UV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
11	VOUT11_UV_RST_MASK	Mask the VOUT11_UV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
10	VOUT10_UV_RST_MASK	Mask the VOUT10_UV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
9	VOUT9_UV_RST_MASK	Mask the VOUT9_UV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
8	VOUT8_UV_RST_MASK	Mask the VOUT8_UV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
7	VOUT7_UV_RST_MASK	Mask the VOUT7_UV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
6	VOUT6_UV_RST_MASK	Mask the VOUT6_UV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
5	VOUT5_UV_RST_MASK	Mask the VOUT5_UV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
4	VOUT4_UV_RST_MASK	Mask the VOUT4_UV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
3	VOUT3_UV_RST_MASK	Mask the VOUT3_UV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
2	VOUT2_UV_RST_MASK	Mask the VOUT2_UV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
1	VOUT1_UV_RST_MASK	Mask the VOUT1_UV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
0	VOUT12_UV_RST_MASK	Mask the VOUT12_UV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Table 58. OV_RST_MASK, Register Address: 0x2038

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
13	VM1_OV_RST_MASK	Mask the VM1_OV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
12	VM0_OV_RST_MASK	Mask the VM0_OV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
11	VOUT11_OV_RST_MASK	Mask the VOUT11_OV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
10	VOUT10_OV_RST_MASK	Mask the VOUT10_OV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
9	VOUT9_OV_RST_MASK	Mask the VOUT9_OV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
8	VOUT8_OV_RST_MASK	Mask the VOUT8_OV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
7	VOUT7_OV_RST_MASK	Mask the VOUT7_OV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
6	VOUT6_OV_RST_MASK	Mask the VOUT6_OV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
5	VOUT5_OV_RST_MASK	Mask the VOUT5_OV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
4	VOUT4_OV_RST_MASK	Mask the VOUT4_OV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
3	VOUT3_OV_RST_MASK	Mask the VOUT3_OV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
2	VOUT2_OV_RST_MASK	Mask the VOUT2_OV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
1	VOUT1_OV_RST_MASK	Mask the VOUT1_OV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
0	VOUT12_OV_RST_MASK	Mask the VOUT12_OV_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Table 59. WARN_RST_MASK, Register Address: 0x203C

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
13	VM1_WARN_RST_MASK	Mask the VM1_WARN_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
12	VM0_WARN_RST_MASK	Mask the VM0_WARN_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
11	VOUT11_WARN_RST_MASK	Mask the VOUT11_WARN_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
10	VOUT10_WARN_RST_MASK	Mask the VOUT10_WARN_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
9	VOUT9_WARN_RST_MASK	Mask the VOUT9_WARN_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
8	VOUT8_WARN_RST_MASK	Mask the VOUT8_WARN_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
7	VOUT7_WARN_RST_MASK	Mask the VOUT7_WARN_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
6	VOUT6_WARN_RST_MASK	Mask the VOUT6_WARN_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
5	VOUT5_WARN_RST_MASK	Mask the VOUT5_WARN_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
4	VOUT4_WARN_RST_MASK	Mask the VOUT4_WARN_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
3	VOUT3_WARN_RST_MASK	Mask the VOUT3_WARN_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
2	VOUT2_WARN_RST_MASK	Mask the VOUT2_WARN_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
1	VOUT1_WARN_RST_MASK	Mask the VOUT1_WARN_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
0	VOUT12_WARN_RST_MASK	Mask the VOUT12_WARN_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Table 60. OT_RST_MASK, Register Address: 0x2040

Bits	Bit Name	Description	Reset	Access
[31:12]	RESERVED	Reserved.	0x0	R
11	VOUT12_OT_RST_MASK	Mask the VOUT12_OT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
10	VOUT4_OT_RST_MASK	Mask the VOUT4_OT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
9	VOUT3_OT_RST_MASK	Mask the VOUT3_OT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
8	VOUT2_OT_RST_MASK	Mask the VOUT2_OT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
7	VOUT1_OT_RST_MASK	Mask the VOUT1_OT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
6	VOUT11_OT_RST_MASK	Mask the VOUT11_OT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
5	VOUT10_OT_RST_MASK	Mask the VOUT10_OT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
4	VOUT9_OT_RST_MASK	Mask the VOUT9_OT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
3	VOUT8_OT_RST_MASK	Mask the VOUT8_OT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
2	VOUT7_OT_RST_MASK	Mask the VOUT7_OT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
1	VOUT6_OT_RST_MASK	Mask the VOUT6_OT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
0	VOUT5_OT_RST_MASK	Mask the VOUT5_OT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Table 61. OTHER_RST_MASK, Register Address: 0x2044

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved.	0x0	R
28	WDI1_EXT_RST_MASK	Mask the WDI1_EXT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
27	WDI0_EXT_RST_MASK	Mask the WDI0_EXT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
26	VSET1_DETECTION_RST_MASK	Mask the VSET1_DETECTION_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
25	MODE_DETECTION_RST_MASK	Mask the MODE_DETECTION_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
24	SYNC_FAIL_RST_MASK	Mask the SYNC_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
23	WDI1_PULSE_FAIL_RST_MASK	Mask the WDI1_PULSE_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
22	WDI0_PULSE_FAIL_RST_MASK	Mask the WDI0_PULSE_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
21	CLKM_FAIL_RST_MASK	Mask the CLKM_FAIL_STATUS on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
20	SHR_CRC_FAIL_RST_MASK	Mask the SHR_CRC_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
19	SHR_ECC_FAIL_RST_MASK	Mask the SHR_ECC_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
18	$\overline{\text{STATUS}}$_EXT_FAIL_RST_MASK	Mask the $\overline{\text{STATUS}}$_EXT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
17	$\overline{\text{FAULT}}$_EXT_FAIL_RST_MASK	Mask the $\overline{\text{FAULT}}$_EXT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
16	$\overline{\text{RESET}}$_EXT_FAIL_RST_MASK	Mask the $\overline{\text{RESET}}$_EXT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
[15:9]	RESERVED	Reserved.	0x0	R/W
8	SPI_FMT_ERR_RST_MASK	Mask the SPI_FMT_ERR_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
7	SPI_RDD_ERR_RST_MASK	Mask the SPI_RDD_ERR_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
6	SPI_CLK_ERR_RST_MASK	Mask the SPI_CLK_ERR_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
5	SPI_ACCESS_FAIL_RST_MASK	Mask the SPI_ACCESS_FAIL Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
4	SPI_ADDR_FAIL_RST_MASK	Mask the SPI_ADDR_FAIL Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
3	SPI_CRC_FAIL_RST_MASK	Mask the SPI_CRC_FAIL Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
2	QA_WD_FAIL_RST_MASK	Mask the QA_WD_FAIL Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
1	WD1_FAIL_RST_MASK	Mask the WD1_FAIL Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
0	WD0_FAIL_RST_MASK	Mask the WD0_FAIL Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Table 62. OTHER1_RST_MASK, Register Address: 0x2048

Bits	Bit Name	Description	Reset	Access
[31:19]	RESERVED	Reserved.	0x0	R
18	FB8_RECAP_SHORT_RST_MASK	Mask FB8_RECAP_SHORT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
17	VREG_GOOD_RST_MASK	Mask VREG_GOOD_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
16	PIN_OPEN_FAULT_LDO7_RST_MASK	Mask PIN_OPEN_FAULT_LDO7_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask	0x0	R/W
15	PIN_OPEN_FAULT_LDO6_RST_MASK	Mask PIN_OPEN_FAULT_LDO6_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
14	PIN_OPEN_FAULT_LDO5_RST_MASK	Mask PIN_OPEN_FAULT_LDO5_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
13	PIN_OPEN_FAULT_LDO4_RST_MASK	Mask PIN_OPEN_FAULT_LDO4_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
12	PIN_OPEN_FAULT_LDO3_RST_MASK	Mask PIN_OPEN_FAULT_LDO3_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
11	PIN_OPEN_FAULT_LDO2_RST_MASK	Mask PIN_OPEN_FAULT_LDO2_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
10	PIN_OPEN_FAULT_LDO1_RST_MASK	Mask PIN_OPEN_FAULT_LDO1_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
9	PIN_OPEN_FAULT_BOOST_RST_MASK	Mask PIN_OPEN_FAULT_BOOST_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
8	WAKE_FALLING_EVT_RST_MASK	Mask the WAKE_FALLING_EVT_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
7	SYS_REG_CRC_ERR_RST_MASK	Mask the SYS_REG_CRC_ERR_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
6	TSD_RST_MASK	Mask the TSD_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
5	LDO5_INPUT_OVLO_RST_MASK	Mask the LDO5_INPUT_OVLO_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
4	LDO3_INPUT_OVLO_RST_MASK	Mask the LDO3_INPUT_OVLO_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
3	LDO1_INPUT_OVLO_RST_MASK	Mask the LDO1_INPUT_OVLO_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
2	LDO5_INPUT_UVLO_RST_MASK	Mask the LDO5_INPUT_UVLO_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
1	LDO3_INPUT_UVLO_RST_MASK	Mask the LDO3_INPUT_UVLO_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
0	LDO1_INPUT_UVLO_RST_MASK	Mask the LDO1_INPUT_UVLO_STATUS Bit on the $\overline{\text{RESET}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Table 63. UV_FAULT_MASK, Register Address: 0x204C

Bits	Bit Name	Description	Reset	Access
[31:15]	RESERVED	Reserved.	0x0	R
14	VIO_UVLO_FAULT_MASK	Mask the VIO_UVLO_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
13	VM1_UV_FAULT_MASK	Mask the VM1_UV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
12	VM0_UV_FAULT_MASK	Mask the VM0_UV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
11	VOUT11_UV_FAULT_MASK	Mask the VOUT11_UV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
10	VOUT10_UV_FAULT_MASK	Mask the VOUT10_UV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
9	VOUT9_UV_FAULT_MASK	Mask the VOUT9_UV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
8	VOUT8_UV_FAULT_MASK	Mask the VOUT8_UV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
7	VOUT7_UV_FAULT_MASK	Mask the VOUT7_UV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask	0x1	R/W
6	VOUT6_UV_FAULT_MASK	Mask the VOUT6_UV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
5	VOUT5_UV_FAULT_MASK	Mask the VOUT5_UV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
4	VOUT4_UV_FAULT_MASK	Mask the VOUT4_UV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
3	VOUT3_UV_FAULT_MASK	Mask the VOUT3_UV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
2	VOUT2_UV_FAULT_MASK	Mask the VOUT2_UV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
1	VOUT1_UV_FAULT_MASK	Mask the VOUT1_UV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
0	VOUT12_UV_FAULT_MASK	Mask the VOUT12_UV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Table 64. OV_FAULT_MASK, Register Address: 0x2050

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
13	VM1_OV_FAULT_MASK	Mask the VM1_OV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
12	VM0_OV_FAULT_MASK	Mask the VM0_OV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
11	VOUT11_OV_FAULT_MASK	Mask the VOUT11_OV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
10	VOUT10_OV_FAULT_MASK	Mask the VOUT10_OV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
9	VOUT9_OV_FAULT_MASK	Mask the VOUT9_OV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
8	VOUT8_OV_FAULT_MASK	Mask the VOUT8_OV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
7	VOUT7_OV_FAULT_MASK	Mask the VOUT7_OV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
6	VOUT6_OV_FAULT_MASK	Mask the VOUT6_OV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
5	VOUT5_OV_FAULT_MASK	Mask the VOUT5_OV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
4	VOUT4_OV_FAULT_MASK	Mask the VOUT4_OV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
3	VOUT3_OV_FAULT_MASK	Mask the VOUT3_OV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
2	VOUT2_OV_FAULT_MASK	Mask the VOUT2_OV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
1	VOUT1_OV_FAULT_MASK	Mask the VOUT1_OV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
0	VOUT12_OV_FAULT_MASK	Mask the VOUT12_OV_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Table 65. WARN_FAULT_MASK, Register Address: 0x2054

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
13	VM1_WARN_FAULT_MASK	Mask the VM1_WARN_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
12	VM0_WARN_FAULT_MASK	Mask the VM0_WARN_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
11	VOUT11_WARN_FAULT_MASK	Mask the VOUT11_WARN_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
10	VOUT10_WARN_FAULT_MASK	Mask the VOUT10_WARN_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
9	VOUT9_WARN_FAULT_MASK	Mask the VOUT9_WARN_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
8	VOUT8_WARN_FAULT_MASK	Mask the VOUT8_WARN_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
7	VOUT7_WARN_FAULT_MASK	Mask the VOUT7_WARN_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
6	VOUT6_WARN_FAULT_MASK	Mask the VOUT6_WARN_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
5	VOUT5_WARN_FAULT_MASK	Mask the VOUT5_WARN_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
4	VOUT4_WARN_FAULT_MASK	Mask the VOUT4_WARN_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
3	VOUT3_WARN_FAULT_MASK	Mask the VOUT3_WARN_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
2	VOUT2_WARN_FAULT_MASK	Mask the VOUT2_WARN_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
1	VOUT1_WARN_FAULT_MASK	Mask the VOUT1_WARN_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
0	VOUT12_WARN_FAULT_MASK	Mask the VOUT12_WARN_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Table 66. OT_FAULT_MASK, Register Address: 0x2058

Bits	Bit Name	Description	Reset	Access
[31:12]	RESERVED	Reserved.	0x0	R
11	VOUT12_OT_FAULT_MASK	Mask the VOUT12_OT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
10	VOUT4_OT_FAULT_MASK	Mask the VOUT4_OT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
9	VOUT3_OT_FAULT_MASK	Mask the VOUT3_OT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
8	VOUT2_OT_FAULT_MASK	Mask the VOUT2_OT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
7	VOUT1_OT_FAULT_MASK	Mask the VOUT1_OT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
6	VOUT11_OT_FAULT_MASK	Mask the VOUT11_OT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
5	VOUT10_OT_FAULT_MASK	Mask the VOUT10_OT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
4	VOUT9_OT_FAULT_MASK	Mask the VOUT9_OT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
3	VOUT8_OT_FAULT_MASK	Mask the VOUT8_OT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
2	VOUT7_OT_FAULT_MASK	Mask the VOUT7_OT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
1	VOUT6_OT_FAULT_MASK	Mask the VOUT6_OT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
0	VOUT5_OT_FAULT_MASK	Mask the VOUT5_OT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Table 67. OTHER_FAULT_MASK, Register Address: 0x205C

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved.	0x0	R
28	WDI1_EXT_FAULT_MASK	Mask the WDI1_EXT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
27	WDI0_EXT_FAULT_MASK	Mask the WDI0_EXT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
26	VSET1_DETECTION_FAULT_MASK	Mask the VSET1_DETECTION_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
25	MODE_DETECTION_FAULT_MASK	Mask the MODE_DETECTION_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
24	SYNC_FAIL_FAULT_MASK	Mask the SYNC_FAIL_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
23	WDI1_PULSE_FAIL_FAULT_MASK	Mask the WDI1_PULSE_FAIL_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
22	WDI0_PULSE_FAIL_FAULT_MASK	Mask the WDI0_PULSE_FAIL_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
21	CLKM_FAIL_FAULT_MASK	Mask the CLKM_FAIL_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
20	SHR_CRC_FAIL_FAULT_MASK	Mask the SHR_CRC_FAIL_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
19	SHR_ECC_FAIL_FAULT_MASK	Mask the SHR_ECC_FAIL_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
18	$\overline{\text{STATUS}}$_EXT_FAIL_FAULT_MASK	Mask the $\overline{\text{STATUS}}$_EXT_FAIL_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
17	$\overline{\text{FAULT}}$_EXT_FAIL_FAULT_MASK	Mask the $\overline{\text{FAULT}}$_EXT_FAIL_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
16	$\overline{\text{RESET}}$_EXT_FAIL_FAULT_MASK	Mask the $\overline{\text{RESET}}$_EXT_FAIL_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
[15:9]	RESERVED	Reserved.	0x0	R
8	SPI_FMT_ERR_FAULT_MASK	Mask the SPI_FMT_ERR_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
7	SPI_RDD_ERR_FAULT_MASK	Mask the SPI_RDD_ERR_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
6	SPI_CLK_ERR_FAULT_MASK	Mask the SPI_CLK_ERR_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
5	SPI_ACCESS_FAIL_FAULT_MASK	Mask the SPI_ACCESS_FAIL_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
4	SPI_ADDR_FAIL_FAULT_MASK	Mask the SPI_ADDR_FAIL_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
3	SPI_CRC_FAIL_FAULT_MASK	Mask the SPI_CRC_FAIL_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1:not mask.	0x1	R/W
2	QA_WD_FAIL_FAULT_MASK	Mask the QA_WD_FAIL_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
1	WD1_FAIL_FAULT_MASK	Mask the WD1_FAIL_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
0	WD0_FAIL_FAULT_MASK	Mask the WD0_FAIL_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Table 68. OTHER1_FAULT_MASK, Register Address: 0x2060

Bits	Bit Name	Description	Reset	Access
[31:19]	RESERVED	Reserved.	0x0	R
18	FB8_RECAP_SHORT_FAULT_MASK	Mask the FB8_RECAP_SHORT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
17	VREG_GOOD_FAULT_MASK	Mask the VREG_GOOD_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
16	PIN_OPEN_FAULT_LDO7_FAULT_MASK	Mask the PIN_OPEN_FAULT_LDO7_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
15	PIN_OPEN_FAULT_LDO6_FAULT_MASK	Mask the PIN_OPEN_FAULT_LDO6_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
14	PIN_OPEN_FAULT_LDO5_FAULT_MASK	Mask the PIN_OPEN_FAULT_LDO5_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
13	PIN_OPEN_FAULT_LDO4_FAULT_MASK	Mask the PIN_OPEN_FAULT_LDO4_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
12	PIN_OPEN_FAULT_LDO3_FAULT_MASK	Mask the PIN_OPEN_FAULT_LDO3_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
11	PIN_OPEN_FAULT_LDO2_FAULT_MASK	Mask the PIN_OPEN_FAULT_LDO2_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
10	PIN_OPEN_FAULT_LDO1_FAULT_MASK	Mask the PIN_OPEN_FAULT_LDO1_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
9	PIN_OPEN_FAULT_BOOST_FAULT_MASK	Mask the PIN_OPEN_FAULT_BOOST_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
8	WAKE_FALLING_EVT_FAULT_MASK	Mask the WAKE_FALLING_EVT_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
7	SYS_REG_CRC_ERR_FAULT_MASK	Mask the SYS_REG_CRC_ERR_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
6	TSD_FAULT_MASK	Mask the TSD_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
5	LDO5_INPUT_OVLO_ FAULT_MASK	Mask the LDO5_INPUT_OVLO_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
4	LDO3_INPUT_OVLO_ FAULT_MASK	Mask the LDO3_INPUT_OVLO_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
3	LDO1_INPUT_OVLO_ FAULT_MASK	Mask the LDO1_INPUT_OVLO_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
2	LDO5_INPUT_UVLO_ FAULT_MASK	Mask the LDO5_INPUT_UVLO_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
1	LDO3_INPUT_UVLO_ FAULT_MASK	Mask the LDO3_INPUT_UVLO_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
0	LDO1_INPUT_UVLO_ FAULT_MASK	Mask the LDO1_INPUT_UVLO_LATCH Bit on the $\overline{\text{FAULT}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Table 69. UV_INT_MASK, Register Address: 0x2064

Bits	Bit Name	Description	Reset	Access
[31:15]	RESERVED	Reserved.	0x0	R
14	VIO_UVLO_INT_MASK	Mask the VIO_UVLO_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
13	VM1_UV_INT_MASK	Mask the VM1_UV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
12	VM0_UV_INT_MASK	Mask the VM0_UV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
11	VOUT11_UV_INT_MASK	Mask the VOUT11_UV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
10	VOUT10_UV_INT_MASK	Mask the VOUT10_UV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
9	VOUT9_UV_INT_MASK	Mask the VOUT9_UV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
8	VOUT8_UV_INT_MASK	Mask the VOUT8_UV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
7	VOUT7_UV_INT_MASK	Mask the VOUT7_UV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
6	VOUT6_UV_INT_MASK	Mask the VOUT6_UV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
5	VOUT5_UV_INT_MASK	Mask the VOUT5_UV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
4	VOUT4_UV_INT_MASK	Mask the VOUT4_UV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
3	VOUT3_UV_INT_MASK	Mask the VOUT3_UV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
2	VOUT2_UV_INT_MASK	Mask the VOUT2_UV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
1	VOUT1_UV_INT_MASK	Mask the VOUT1_UV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
0	VOUT12_UV_INT_MASK	Mask the VOUT12_UV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Table 70. OV_INT_MASK, Register Address: 0x2068

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
13	VM1_OV_INT_MASK	Mask the VM1_OV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
12	VM0_OV_INT_MASK	Mask the VM0_OV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
11	VOUT11_OV_INT_MASK	Mask the VOUT11_OV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
10	VOUT10_OV_INT_MASK	Mask the VOUT10_OV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
9	VOUT9_OV_INT_MASK	Mask the VOUT9_OV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
8	VOUT8_OV_INT_MASK	Mask the VOUT8_OV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
7	VOUT7_OV_INT_MASK	Mask the VOUT7_OV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
6	VOUT6_OV_INT_MASK	Mask the VOUT6_OV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
5	VOUT5_OV_INT_MASK	Mask the VOUT5_OV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
4	VOUT4_OV_INT_MASK	Mask the VOUT4_OV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
3	VOUT3_OV_INT_MASK	Mask the VOUT3_OV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
2	VOUT2_OV_INT_MASK	Mask the VOUT2_OV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
1	VOUT1_OV_INT_MASK	Mask the VOUT1_OV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
0	VOUT12_OV_INT_MASK	Mask the VOUT12_OV_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Table 71. WARN_INT_MASK, Register Address: 0x206C

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
13	VM1_WARN_INT_MASK	Mask the VM1_WARN_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
12	VM0_WARN_INT_MASK	Mask the VM0_WARN_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
11	VOUT11_WARN_INT_MASK	Mask the VOUT11_WARN_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
10	VOUT10_WARN_INT_MASK	Mask the VOUT10_WARN_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
9	VOUT9_WARN_INT_MASK	Mask the VOUT9_WARN_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
8	VOUT8_WARN_INT_MASK	Mask the VOUT8_WARN_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
7	VOUT7_WARN_INT_MASK	Mask the VOUT7_WARN_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
6	VOUT6_WARN_INT_MASK	Mask the VOUT6_WARN_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
5	VOUT5_WARN_INT_MASK	Mask the VOUT5_WARN_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
4	VOUT4_WARN_INT_MASK	Mask the VOUT4_WARN_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
3	VOUT3_WARN_INT_MASK	Mask the VOUT3_WARN_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
2	VOUT2_WARN_INT_MASK	Mask the VOUT2_WARN_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
1	VOUT1_WARN_INT_MASK	Mask the VOUT1_WARN_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 1: not mask. 0: mask.	0x1	R/W
0	VOUT12_WARN_INT_MASK	Mask the VOUT12_WARN_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Table 72. OT_INT_MASK, Register Address: 0x2070

Bits	Bit Name	Description	Reset	Access
[31:12]	RESERVED	Reserved.	0x0	R
11	VOUT12_OT_INT_MASK	Mask the VOUT12_OT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
10	VOUT4_OT_INT_MASK	Mask the VOUT4_OT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
9	VOUT3_OT_INT_MASK	Mask the VOUT3_OT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
8	VOUT2_OT_INT_MASK	Mask the VOUT2_OT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
7	VOUT1_OT_INT_MASK	Mask the VOUT1_OT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
6	VOUT11_OT_INT_MASK	Mask the VOUT11_OT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
5	VOUT10_OT_INT_MASK	Mask the VOUT10_OT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
4	VOUT9_OT_INT_MASK	Mask the VOUT9_OT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
3	VOUT8_OT_INT_MASK	Mask the VOUT8_OT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
2	VOUT7_OT_INT_MASK	Mask the VOUT7_OT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
1	VOUT6_OT_INT_MASK	Mask the VOUT6_OT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
0	VOUT5_OT_INT_MASK	Mask the VOUT5_OT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Table 73. OTHER_INT_MASK, Register Address: 0x2074

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved.	0x0	R
28	WDI1_EXT_INT_MASK	Mask the WDI1_EXT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
27	WDI0_EXT_INT_MASK	Mask the WDI0_EXT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
26	VSET1_DETECTION_INT_MASK	Mask the VSET1_DETECTION_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
25	MODE_DETECTION_INT_MASK	Mask the MODE_DETECTION_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
24	SYNC_FAIL_INT_MASK	Mask the SYNC_FAIL_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
23	WDI1_PULSE_FAIL_INT_MASK	Mask the WDI1_PULSE_FAIL_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
22	WDI0_PULSE_FAIL_INT_MASK	Mask the WDI0_PULSE_FAIL_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
21	CLKM_FAIL_INT_MASK	Mask the CLKM_FAIL_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
20	SHR_CRC_FAIL_INT_MASK	Mask the SHR_CRC_FAIL_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
19	SHR_ECC_FAIL_INT_MASK	Mask the SHR_ECC_FAIL_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
18	$\overline{\text{STATUS}}$_EXT_FAIL_INT_MASK	Mask the $\overline{\text{STATUS}}$_EXT_FAIL_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
17	$\overline{\text{FAULT}}$_EXT_FAIL_INT_MASK	Mask the $\overline{\text{FAULT}}$_EXT_FAIL_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
16	$\overline{\text{RESET}}$_EXT_FAIL_INT_MASK	Mask the $\overline{\text{RESET}}$_EXT_FAIL_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
[15:9]	RESERVED	Reserved.	0x0	R

Bits	Bit Name	Description	Reset	Access
8	SPI_FMT_ERR_INT_MASK	Mask the SPI_FMT_ERR_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
7	SPI_RDD_ERR_INT_MASK	Mask the SPI_RDD_ERR_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
6	SPI_CLK_ERR_INT_MASK	Mask the SPI_CLK_ERR_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
5	SPI_ACCESS_FAIL_INT_MASK	Mask the SPI_ACCESS_FAIL_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
4	SPI_ADDR_FAIL_INT_MASK	Mask the SPI_ADDR_FAIL_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask 1: not mask.	0x1	R/W
3	SPI_CRC_FAIL_INT_MASK	Mask the SPI_CRC_FAIL_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
2	QA_WD_FAIL_INT_MASK	Mask the QA_WD_FAIL_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
1	WD1_FAIL_INT_MASK	Mask the WD1_FAIL_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
0	WD0_FAIL_INT_MASK	Mask the WD0_FAIL_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W

Table 74. OTHER1_INT_MASK, Register Address: 0x2078

Bits	Bit Name	Description	Reset	Access
[31:19]	RESERVED	Reserved.	0x0	R
18	FB8_RECAP_SHORT_INT_MASK	Mask the FB8_RECAP_SHORT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
17	VREG_GOOD_INT_MASK	Mask the VREG_GOOD_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
16	PIN_OPEN_FAULT_LDO7_INT_MASK	Mask the PIN_OPEN_FAULT_LDO7_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
15	PIN_OPEN_FAULT_LDO6_INT_MASK	Mask the PIN_OPEN_FAULT_LDO6_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
14	PIN_OPEN_FAULT_LDO5_INT_MASK	Mask the PIN_OPEN_FAULT_LDO5_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
13	PIN_OPEN_FAULT_LDO4_INT_MASK	Mask the PIN_OPEN_FAULT_LDO4_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
12	PIN_OPEN_FAULT_LDO3_INT_MASK	Mask the PIN_OPEN_FAULT_LDO3_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
11	PIN_OPEN_FAULT_LDO2_INT_MASK	Mask the PIN_OPEN_FAULT_LDO2_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
10	PIN_OPEN_FAULT_LDO1_INT_MASK	Mask the PIN_OPEN_FAULT_LDO1_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
9	PIN_OPEN_FAULT_BOOST_INT_MASK	Mask the PIN_OPEN_FAULT_BOOST_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
8	WAKE_FALLING_EVT_INT_MASK	Mask the WAKE_FALLING_EVT_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
7	SYS_REG_CRC_ERR_INT_MASK	Mask the SYS_REG_CRC_ERR_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
6	TSD_INT_MASK	Mask the TSD_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x1	R/W
5	LDO5_INPUT_OVLO_INT_MASK	Mask the LDO5_INPUT_OVLO_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
4	LDO3_INPUT_OVLO_INT_MASK	Mask the LDO3_INPUT_OVLO_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
3	LDO1_INPUT_OVLO_INT_MASK	Mask the LDO1_INPUT_OVLO_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
2	LDO5_INPUT_UVLO_INT_MASK	Mask the LDO5_INPUT_UVLO_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
1	LDO3_INPUT_UVLO_INT_MASK	Mask the LDO3_INPUT_UVLO_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W
0	LDO1_INPUT_UVLO_INT_MASK	Mask the LDO1_INPUT_UVLO_LATCH Bit on the $\overline{\text{STATUS}}$ Pin. 0: mask. 1: not mask.	0x0	R/W

Table 75. TRANSITION_MASK, Register Address: 0x207C

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved.	0x0	R
5	WDQA_COND5_FAIL_MASK	Mask the QA Watchdog Fail in Condition 5. 0: mask. 1: not mask.	0x0	R/W
4	WD1_COND5_FAIL_MASK	Mask the WD1 Fail in Condition 5. 0: mask. 1: not mask.	0x0	R/W
3	WD0_COND5_FAIL_MASK	Mask the WD0 Fail in Condition 5. 0: mask. 1: not mask.	0x0	R/W
2	WDQA_COND3_FAIL_MASK	Mask the QA watchdog Fail in Condition 3. 0: mask. 1: not mask.	0x0	R/W
1	WD1_COND3_FAIL_MASK	Mask the WD1 Fail in Condition 3. 0: mask. 1: not mask.	0x0	R/W
0	WD0_COND3_FAIL_MASK	Mask the WD0 Fail in Condition 3. 0: mask. 1: not mask.	0x0	R/W

Table 76. MODE_PIN_STATUS, Register Address: 0x8004

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved.	0x0	R
5	DEBUG	Record the Debug Mode Configuration Information by the MODE Pin. 0: debug mode disabled. 1: debug mode enabled.	0x0	R
[4:1]	ADDRESS	Record the Device Index Configuration Information the MODE Pin. 0001: Address 0. 0010: Address 1. 0100: Address 2.	0x0	R

Bits	Bit Name	Description	Reset	Access
		1000: Address 3. Other settings: invalid.		
0	VIO	Record the I/O Voltage Configuration Information by the MODE Pin. 0: 1.8 V. 1: 3.3 V.	0x0	R

Table 77. FREQ_CONFG, Register Address: 0x8008

Bits	Bit Name	Description	Reset	Access
[31:10]	RESERVED	Reserved.	0x0	R
9	SP_EN	Enable Frequency Spread Spectrum. 0: disable the frequency spread spectrum. 1: enable the frequency spread spectrum.	0x0	R/W
[8:6]	SD	Setting the Sweep Depth of the Frequency Spread Spectrum. 000: 2%. 001: 4%. 010: 6%. 011: 8%. 100: 10%. Other settings: not supported.	0x0	R/W
[5:3]	SF	Setting the Sweep Frequency of the Frequency Spread Spectrum. 000: 5 kHz. 001: 10.42 kHz. 010: 15.63 kHz. 011: 20.83 kHz. 100: 25 kHz. 101: 31.25 kHz. 110: 41.67 kHz. 111: 62.5 kHz.	0x0	R/W
2	SYNC_EN	Enable Sync Function. 0: the SYNC pin is high impedance, and the synchronization function disabled. 1: the synchronization function is enabled, and the SYNC pin direction is determined by the SYNC_DIR bit.	0x0	R/W
1	SYNC_DIV	Setting Frequency on the SYNC Pin when Configured as an Output. 0: f_{SW}. 1: $f_{SW}/5$.	0x0	R/W
0	SYNC_DIR	Setting the SYNC Pin Direction. 0: configure as input. 1: configure as output.	0x0	R/W

Table 78. BUCK1_VOUT_SETTING, Register Address: 0x800C

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved.	0x0	R
[5:0]	BUCK1_VOUTSET	Setting the Output Voltage of BUCK1. The range is from 0.8 V to 1.4 V, and the default is 1.27 V. V_{OUT1} = 800 mV + BUCK1_VOUTSET[5:0] × 10 mV.	0x2F	R/W

Table 79. BUCK1_VOUT, Register Address: 0x8010

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved.	0x0	R
[5:0]	BUCK1_VOUT_CODE	Before the SPI writes to the BUCK1_VOUT_SETTING register, the BUCK1_VOUT_CODE bits map with the resistor on the VSET1 pin. When the SPI writes to the BUCK1_VOUT_SETTING register, BUCK1_VOUT_CODE matches with the value of the BUCK1_VOUTSET bits in the BUCK1_VOUT_SETTING register. Otherwise, the wrong code occurs. 000000: 5.62 kΩ. 000101: 7.87 kΩ. 001010: 11 kΩ. 001111: 15.4 kΩ. 010100: 21.5 kΩ. 011001: 30.1 kΩ. 011110: 42.2 kΩ. 100011: 59 kΩ. 101000: 84.5 kΩ. 101101: 115 kΩ. 101111: 162 kΩ. 110010: 232 kΩ. 110111: 316 kΩ. 111100: 475 kΩ. Other setting: wrong code.	0x0	R

Table 80. BUCK4_VOUT_SETTING, Register Address: 0x8014

Bits	Bit Name	Description	Reset	Access
[31:4]	RESERVED	Reserved.	0x0	R
[3:0]	BUCK4_VOUTSET	Set the Output Voltage of BUCK4 (V_{OUT4}). 0000: 0.55 V. 0001: 0.60 V. 0010: 0.65 V. 0011: 0.70 V. 0100: 0.75 V. 0101: 0.80 V. 0110: 0.85 V. 0111: 0.90 V. 1000: 0.95 V. 1001: 1.00 V. 1010: 1.05 V. 1011: 1.10 V.	0x2	R/W

Bits	Bit Name	Description	Reset	Access
		1100: 1.15 V. 1101: 1.20 V. Other settings: not support.		

Table 81. BUCK_DVS_INTERVAL, Register Address: 0x8018

Bits	Bit Name	Description	Reset	Access
[31:4]	RESERVED	Reserved.	0x0	R
[3:2]	BUCK1_INTERVAL	Set the Interval for BUCK1 During DVS. 00: 10 µs. 01: 20 µs. 10: 30 µs. 11: 40 µs.	0x0	R/W
[1:0]	BUCK4_INTERVAL	Set the Interval for BUCK4 During DVS. 00: 10 µs. 01: 20 µs. 10: 30 µs. 11: 40 µs.	0x0	R/W

Table 82. LDO1_VOUT_SETTING, Register Address: 0x801C

Bits	Bit Name	Description	Reset	Access
[31:3]	RESERVED	Reserved.	0x0	R
[2:0]	LDO1_VOUTSET	Set the Output Voltage of LDO1 (Regulator 5). 000: 1.76 V. 001: 1.8 V. 010: 1.85 V. 011: 1.89 V. 100: 1.94 V. 101: 1.98 V. 110: 2.03 V. 111: 2.07 V.	0x1	R/W

Table 83. LDO2_VOUT_SETTING, Register Address: 0x8020

Bits	Bit Name	Description	Reset	Access
[31:3]	RESERVED	Reserved.	0x0	R
[2:0]	LDO2_VOUTSET	Set the Output Voltage of LDO2 (Regulator 6). 000: 1.76 V. 001: 1.8 V. 010: 1.85 V. 011: 1.89 V. 100: 1.94 V. 101: 1.98 V. 110: 2.03 V. 111: 2.07 V.	0x1	R/W

Table 84. LDO3_VOUT_SETTING, Register Address: 0x8024

Bits	Bit Name	Description	Reset	Access
[31:3]	RESERVED	Reserved.	0x0	R
[2:0]	LDO3_VOUTSET	Set the Output Voltage of LDO3 (Regulator 7). 000: 0.86 V. 001: 0.9 V. 010: 0.94 V. 011: 0.97 V. 100: 1.01 V. 101: 1.04 V. 110: 1.08 V. 111: 1.12 V.	0x1	R/W

Table 85. LDO4_VOUT_SETTING, Register Address: 0x8028

Bits	Bit Name	Description	Reset	Access
[31:3]	RESERVED	Reserved.	0x0	R
[2:0]	LDO4_VOUTSET	Set the Output Voltage of LDO4 (Regulator 8). 000: 0.86 V. 001: 0.9 V. 010: 0.94 V. 011: 0.97 V. 100: 1.01 V. 101: 1.04 V. 110: 1.08 V. 111: 1.12 V.	0x1	R/W

Table 86. LDO5_VOUT_SETTING, Register Address: 0x802C

Bits	Bit Name	Description	Reset	Access
[31:3]	RESERVED	Reserved.	0x0	R
[2:0]	LDO5_VOUTSET	Set the Output Voltage of LDO5 (Regulator 9). 000: 0.86 V. 001: 0.9 V. 010: 0.94 V. 011: 0.97 V. 100: 1.01 V. 101: 1.04 V. 110: 1.08 V. 111: 1.12 V.	0x1	R/W

Table 87. LDO6_VOUT_SETTING, Register Address: 0x8030

Bits	Bit Name	Description	Reset	Access
[31:2]	RESERVED	Reserved.	0x0	R
[1:0]	LDO6_VOUTSET	Set the Output Voltage of LDO6 (Regulator 10). 00: 3.2 V. 01: 3.3 V. 10: 3.35 V. 11: 3.4 V.	0x1	R/W

Table 88. LDO7_VOUT_SETTING, Register Address: 0x8034

Bits	Bit Name	Description	Reset	Access
[31:2]	RESERVED	Reserved.	0x0	R
[1:0]	LDO7_VOUTSET	Set the Output Voltage of LDO7 (Regulator 11). 00: 3.2 V. 01: 3.3 V. 10: 3.35 V. 11: 3.4 V.	0x1	R/W

Table 89. WARN_WINDOW, Register Address: 0x8038

Bits	Bit Name	Description	Reset	Access
[31:28]	RESERVED	Reserved.	0x0	R
[27:26]	VM1_WARN_WINDOW	Set the Warning Window for the VM1 Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x1	R/W
[25:24]	VM0_WARN_WINDOW	Set the Warning Window for the VM0 Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x1	R/W
[23:22]	FB12_WARN_WINDOW	Set the Warning Window for the FB12 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x1	R/W
[21:20]	FB11_WARN_WINDOW	Set the Warning Window for the FB11 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x1	R/W
[19:18]	FB10_WARN_WINDOW	Set the Warning Window for the FB10 Voltage Monitor. 00: 4%. 01: 5%.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
		10: 6%. 11: 8%.		
[17:16]	FB9_WARN_WINDOW	Set the Warning Window for the FB9 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x1	R/W
[15:14]	FB8_WARN_WINDOW	Set the Warning Window for the FB8 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x1	R/W
[13:12]	FB7_WARN_WINDOW	Set the Warning Window for the FB7 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x1	R/W
[11:10]	FB6_WARN_WINDOW	Set the Warning Window for the FB6 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x1	R/W
[9:8]	FB5_WARN_WINDOW	Set the Warning Window for the FB5 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x1	R/W
[7:6]	FB4_WARN_WINDOW	Set the Warning Window for the FB4 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x1	R/W
[5:4]	FB3_WARN_WINDOW	Set the Warning Window for the FB3 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x1	R/W
[3:2]	FB2_WARN_WINDOW	Set the Warning Window for the FB2 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
[1:0]	FB1_WARN_WINDOW	Set the Warning Window for the FB1 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x1	R/W

Table 90. FAULT_WINDOW, Register Address: 0x803C

Bits	Bit Name	Description	Reset	Access
[31:28]	RESERVED	Reserved.	0x0	R
[27:26]	VM1_FAULT_WINDOW	Set the Fault Window for the VM1 Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x3	R/W
[25:24]	VM0_FAULT_WINDOW	Set the Fault Window for the VM0 Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x3	R/W
[23:22]	FB12_FAULT_WINDOW	Set the Fault Window of the FB12 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x2	R/W
[21:20]	FB11_FAULT_WINDOW	Set the Fault Window of the FB11 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x2	R/W
[19:18]	FB10_FAULT_WINDOW	Set the Fault Window of the FB10 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x2	R/W
[17:16]	FB9_FAULT_WINDOW	Set the Fault Window of the FB9 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x2	R/W
[15:14]	FB8_FAULT_WINDOW	Set the Fault Window of the FB8 Voltage Monitor. 00: 4%. 01: 5%.	0x2	R/W

Bits	Bit Name	Description	Reset	Access
		10: 6%. 11: 8%.		
[13:12]	FB7_FAULT_WINDOW	Set the Fault Window of the FB7 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x2	R/W
[11:10]	FB6_FAULT_WINDOW	Set the Fault Window of the FB6 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x2	R/W
[9:8]	FB5_FAULT_WINDOW	Set the Fault Window of the FB5 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x2	R/W
[7:6]	FB4_FAULT_WINDOW	Set the Fault Window of the FB4 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x2	R/W
[5:4]	FB3_FAULT_WINDOW	Set the Fault Window of the FB3 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x2	R/W
[3:2]	FB2_FAULT_WINDOW	Set the Fault Window of the FB2 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x2	R/W
[1:0]	FB1_FAULT_WINDOW	Set the Fault Window of the FB1 Voltage Monitor. 00: 4%. 01: 5%. 10: 6%. 11: 8%.	0x2	R/W

Table 91. ERROR_COUNT, Register Address: 0x8040

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved.	0x0	R
[5:3]	NEC_PER	Set the Peripheral Error Counter Threshold (N_{EC_P}). 000: 1. 001: 2. 010: 3. 011: 4. 100: 5. 101: 6. 110: 7. 111: 8.	0x7	R/W
[2:0]	NEC_SYS	Set the System Error Counter Threshold (N_{EC_S}). 000: 1. 001: 2. 010: 3. 011: 4. 100: 5. 101: 6. 110: 7. 111: 8.	0x7	R/W

Table 92. SM_BIST_TRG, Register Address: 0x8044

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved.	0x0	R
0	BIST_TRIG	Diagnose Control Block SPI Trigger. Write 1 to trigger the BIST.	0x0	R/W

Table 93. SM_BIST_STATUS, Register Address: 0x8048

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
15	CLK_MON_PASS	Clock Monitor Check During Self Check Process. 0: fail. 1: pass.	0x0	R
14	CRC_PASS	CRC Check During Self Check Process. 0: fail. 1: pass.	0x0	R
13	ECC_PASS	Error Correction Code (ECC) Check During Self Check Process. 0: fail. 1: pass.	0x0	R
12	OV_FAILURE_PASS	Overvoltage Failure Check During Self Check Process. 0: fail. 1: pass.	0x0	R

Bits	Bit Name	Description	Reset	Access
11	OV_WARN_PASS	Overvoltage Warning Check During Self Check Process. 0: fail. 1: pass.	0x0	R
10	UV_FAILURE_PASS	Undervoltage Failure Check During Self Check Process. 0: fail. 1: pass.	0x0	R
9	UV_WARN_PASS	Undervoltage Warning Check During Self Check Process. 0: fail. 1: pass.	0x0	R
8	SM_BIST_ALL_PASS	SM BIST All Pass. 0: fail. 1: pass.	0x0	R
7	CLK_MON_DONE	Clock Monitor Check Done. 0: not done. 1: done.	0x0	R
6	CRC_DONE	CRC Check Done. 0: not done. 1: done.	0x0	R
5	ECC_DONE	ECC Check Done. 0: not done. 1: done.	0x0	R
4	OV_FAILURE_DONE	Overvoltage Failure Check Done. 0: not done. 1: done.	0x0	R
3	OV_WARN_DONE	Overvoltage Warning Check Done. 0: not done. 1: done.	0x0	R
2	UV_FAILURE_DONE	Undervoltage Failure Check Done. 0: not done. 1: done.	0x0	R
1	UV_WARN_DONE	Undervoltage Warning Check Done. 0: not done. 1: done.	0x0	R
0	SM_BIST_ALL_DONE	SM BIST All Done. 0: not done. 1: done.	0x0	R

Table 94. WDI0_PULSE_CTRL, Register Address: 0x804C

Bits	Bit Name	Description	Reset	Access
[31:3]	RESERVED	Reserved.	0x0	R
2	WDI0_PULSE_UPPER_MASK	WDI0 Pulse Width Monitor Upper Threshold Fault Mask. 0: when the WDI0 pulse width is greater than the high threshold, the fault generates. 1: when the WDI0 pulse width is greater than the high threshold, the fault does not generate.	0x0	R/W
1	WDI0_PULSE_LOWER_MASK	WDI0 Pulse Width Monitor Lower Threshold Fault Mask. 0: when the WDI0 pulse width is less than the lower threshold, the fault generates. 1: when the WDI0 pulse width is less than the lower threshold, the fault does not generate.	0x0	R/W
0	WDI0_PULSE_EN	WDI0 Pulse Width Monitor Enable. 0: disable. 1: enable.	0x0	R/W

Table 95. WDI0_PULSE_HIGH, Register Address: 0x8050

Bits	Bit Name	Description	Reset	Access
[31:18]	RESERVED	Reserved.	0x0	R
[17:0]	WDI0_PULSE_HIGH	Set the WDI0 Pulse Width Monitor Upper Limitation Threshold. WDI0 slow pulse width time ($t_{WDI0\_PULSE\_SLOW}$) = WDI0_PULSE_HIGH × 500 ns.	0x47E	R/W

Table 96. WDI0_PULSE_LOW, Register Address: 0x8054

Bits	Bit Name	Description	Reset	Access
[31:18]	RESERVED	Reserved.	0x0	R
[17:0]	WDI0_PULSE_LOW	Set the WDI0 Pulse Width Monitor Lower Limitation Threshold. WDI0 fast pulse width time ($t_{WDI0\_PULSE\_FAST}$) = WDI0_PULSE_LOW × 500 ns.	0x352	R/W

Table 97. WDI0_PULSE_WIN_WIDTH, Register Address: 0x8058

Bits	Bit Name	Description	Reset	Access
[31:18]	RESERVED	Reserved.	0x0	R
[17:0]	WDI0_WIN_WIDTH	Record WDI0 Built-In Self Test (BIST) Clock Pulse Width During Self Check Process.	0x898	R/W

Table 98. WDI1_PULSE_CTRL, Register Address: 0x805C

Bits	Bit Name	Description	Reset	Access
[31:3]	RESERVED	Reserved.	0x0	R
2	WDI1_PULSE_UPPER_MASK	WDI1 Pulse Width Monitor Upper Threshold Fault Mask. 0: when the WDI1 pulse width is greater than the high threshold, the fault generates. 1: when the WDI1 pulse width is greater than the high threshold, the fault does not generate.	0x0	R/W
1	WDI1_PULSE_LOWER_MASK	WDI1 Pulse Width Monitor Lower Threshold Fault Mask. 0: when the WDI1 pulse width is less than the lower threshold, the fault generates. 1: when the WDI1 pulse width is less than the lower threshold, the fault does not generate.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
0	WDI1_PULSE_EN	WDI1Pulse Width Monitor Enable. 0: disable 1: enable	0x0	R/W

Table 99. WDI1_PULSE_HIGH, Register Address: 0x8060

Bits	Bit Name	Description	Reset	Access
[31:18]	RESERVED	Reserved.	0x0	R
[17:0]	WDI1_PULSE_HIGH	Set the WDI1 Pulse Width Monitor Upper Limitation Threshold. WDI1 slow pulse width time ($t_{WDI1\_PULSE\_SLOW}$) = WDI1_PULSE_HIGH × 500 ns.	0x47E	R/W

Table 100. WDI1_PULSE_LOW, Register Address: 0x8064

Bits	Bit Name	Description	Reset	Access
[31:18]	RESERVED	Reserved.	0x0	R
[17:0]	WDI1_PULSE_LOW	Set the WDI1 Pulse Width Monitor Lower Limitation Threshold. WDI1 fast pulse width time ($t_{WDI1\_PULSE\_FAST}$) = WDI1_PULSE_LOW × 500 ns.	0x352	R/W

Table 101. WDI1_PULSE_WIN_WIDTH, Register Address: 0x8068

Bits	Bit Name	Description	Reset	Access
[31:18]	RESERVED	Reserved.	0x0	R
[17:0]	WDI1_WIN_WIDTH	Record WDI1 BIST Clock Pulse Width During Self Check Process.	0x898	R/W

Table 102. WDT0_CTRL, Register Address: 0x806C

Bits	Bit Name	Description	Reset	Access
[31:18]	RESERVED	Reserved.	0x0	R
17	WDT0_LOCK	Lock All WD0 Registers. 1: lock. 0: unlock.	0x1	R/W
[16:13]	WDT0_FAULT_THRESHOLD	Set the Fault Threshold of WD0 to Produce Watchdog Fault.	0x6	R/W
[12:5]	WDT0_SPI_FEED	Software Feed WD0. Write 0x51 to feed WD0.	0x0	R/W
[4:3]	WDT0_PRE_SCALE	Set the Scale Factor for WD0. 00: 1. 01: 16. 10: 256. 11: 4096.	0x1	R/W
[2:1]	WDT0_TRIG_EDGE_SEL	Trigger Edge Configuration for WD0. 00: both edges. 01: rising edge. 10: falling edge. 11: both edges.	0x1	R/W
0	WDT0_EN_CTRL	WD0 Enable Bit. 0: disable the WD0. 1: enable the WD0.	0x0	R/W

Table 103. WDT0_WINDOW, Register Address: 0x8070

Bits	Bit Name	Description	Reset	Access
[31:16]	WDT0_FAST_WINDOW	Set the Fast Window for WD0.	0xEA6	R/W
[15:0]	WDT0_SLOW_WINDOW	Set the Slow Window for WD0.	0x3A98	R/W

Table 104. WDT0_CLEAR_VALUE, Register Address: 0x8074

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	WDT0_CLEAR_VALUE	These bits contain the value of the time counter when a feed comes in to reset the time counter of WD0.	0x0	R

Table 105. WDT0_STATUS, Register Address: 0x8078

Bits	Bit Name	Description	Reset	Access
[31:4]	RESERVED	Reserved.	0x0	R
[3:1]	WDT0_FAULT_COUNTER	Fault Counter Number of WD0.	0x0	R
0	WDT0_SINGLE_FAIL	Bad Watchdog Feed to WD0 Indicator Flag. 0: good watchdog feed. 1: bad watchdog feed.	0x0	R

Table 106. WDT0_CURRENT_VALUE, Register Address: 0x807C

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	WDT0_CURRENT_VALUE	These bits contain the current value of the time counter for WD0.	0x0	R

Table 107. WDT1_CTRL, Register Address: 0x8080

Bits	Bit Name	Description	Reset	Access
[31:18]	RESERVED	Reserved.	0x0	R
17	WDT1_LOCK	Lock All WD1 Registers. 1: lock. 0: unlock.	0x1	R/W
[16:13]	WDT1_FAULT_THRESHOLD	Set the WD1 Fault Threshold.	0x6	R/W
[12:5]	WDT1_SPI_FEED	Software Feed WD1. Write 0x52 to feed WD1.	0x0	R/W
[4:3]	WDT1_PRE_SCALE	Set the WD1 Scale Factor. 00: 1. 01: 16. 10: 256. 11: 4096.	0x1	R/W
[2:1]	WDT1_TRIG_EDGE_SEL	Trigger Edge Configuration for WD1. 00: both edges. 01: rising edge. 10: falling edge. 11: both edges.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
0	WDT1_EN_CTRL	WD1 Enable Bit. 0: disable the WD1. 1: enable the WD1.	0x0	R/W

Table 108. WDT1_WINDOW, Register Address: 0x8084

Bits	Bit Name	Description	Reset	Access
[31:16]	WDT1_FAST_WINDOW	Set the WD1 Fast Window.	0xEA6	R/W
[15:0]	WDT1_SLOW_WINDOW	Set the WD1 Slow Window.	0x3A98	R/W

Table 109. WDT1_CURRENT_VALUE, Register Address: 0x8088

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	WDT1_CURRENT_VALUE	These bits contain the current value of the time counter for WD1.	0x0	R

Table 110. WDT1_CLEAR_VALUE, Register Address: 0x808C

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	WDT1_CLEAR_VALUE	These bits contain the value of the time counter when a feed comes in to reset the time counter for WD1.	0x0	R

Table 111. WDT1_STATUS, Register Address: 0x8090

Bits	Bit Name	Description	Reset	Access
[31:4]	RESERVED	Reserved.	0x0	R
[3:1]	WDT1_FAULT_COUNTER	Fault Counter Number of WD1.	0x0	R
0	WDT1_SINGLE_FAIL	Bad Watchdog Feed to WD1 Indicator Flag. 0: good watchdog feed. 1: bad watchdog feed.	0x0	R

Table 112. QA_WD_CTRL, Register Address: 0x8094

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved.	0x0	R
7	QA_WD_LOCK	Lock all QA watchdog registers except for the QA_WD_ANSWER register and QA_WD_TOKEN register. 1: lock. 0: unlock.	0x0	R/W
6	RESERVED	Reserved.	0x0	R
[5:3]	QA_WD_FAULT_THRESHOLD	Set the QA Watchdog Fault Threshold.	0x6	R/W
[2:1]	QA_WD_PRE_SCALE	Set the QA Watchdog Scale Factor. 00: 1. 01: 16.	0x2	R/W

Bits	Bit Name	Description	Reset	Access
		10: 256. 11: 4096.		
0	QA_WD_EN_CTRL	QA Watchdog Enable Bit. 0: disable the QA watchdog. 1: enable the QA watchdog.	0x1	R/W

Table 113. QA_WD_WINDOW, Register Address: 0x8098

Bits	Bit Name	Description	Reset	Access
[31:16]	QA_WD_FAST_WINDOW	Set the QA Watchdog Fast Window.	0x0	R/W
[15:0]	QA_WD_SLOW_WINDOW	Set the QA Watchdog Slow Window.	0x1E85	R/W

Table 114. QA_WD_CURRENT_VALUE, Register Address: 0x809C

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	QA_WD_CURRENT_VALUE	These bits contain the current value of the time counter for the QA watchdog.	0x0	R

Table 115. QA_WD_CLEAR_VALUE, Register Address: 0x80A0

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	QA_WD_CLEAR_VALUE	These bits contain the value of the time counter when a feed comes in to reset the time counter of the QA watchdog.	0x0	R

Table 116. QA_WD_STATUS, Register Address: 0x80A4

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved.	0x0	R
[4:2]	QA_WD_FAULT_COUNTER	Current Number of the QA Watchdog Fault Counter.	0x0	R
1	RESERVED	Reserved.	0x0	R
0	QA_WD_SINGLE_FAIL	Bad Watchdog Feed to the QA_WD Indicator Flag. 0: good watchdog feed. 1: bad watchdog feed.	0x0	R

Table 117. QA_WD_TOKEN_SEED, Register Address: 0x80A8

Bits	Bit Name	Description	Reset	Access
[31:4]	RESERVED	Reserved.	0x0	R
[3:0]	QA_WD_TOKEN_SEED	Feed value for the linear feedback shift register that generates a 4-bit, pseudo random number that generates the answer for the QA watchdog.	0x0	R/W

Table 118. STANDBY_RAIL_ACTIVE, Register Address: 0x80AC

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved.	0x0	R
4	STANDBY_BOOST	Boost Activity in Standby Mode. 0: off. 1: on.	0x1	R/W
3	STANDBY_LDO7	LDO7 Activity in Standby Mode. 0: off. 1: on.	0x1	R/W
2	STANDBY_LDO1	LDO1 Activity in Standby Mode. 0: off. 1: on.	0x1	R/W
1	STANDBY_BUCK3	BUCK3 Activity in Standby Mode. 0: off. 1: on.	0x1	R/W
0	STANDBY_BUCK2	BUCK2 Activity in Standby Mode. 0: off. 1: on.	0x1	R/W

Table 119. SPI_CRC_CHECKSUM, Register Address: 0x80B0

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	SPI_CRC_CHECKSUM	SPI Write/Read CRC Checksum Result Calculated by SPI Block.	0x0	R

Table 120. SPI_CMD, Register Address: 0x80B4

Bits	Bit Name	Description	Reset	Access
[31:4]	RESERVED	Reserved.	0x0	R
[3:0]	SPI_CMD	SPI Command to Transition Between Different Modes. 0x1: enters self check mode from any mode (SPI_CMD_RST). 0x2: enters to power-down mode (SPI_CMD1). 0x4: enters standby mode (SPI_CMD2). 0x8: enters peripheral ramp-up mode (SPI_CMD3).	0x0	R/W

Table 121. VOLTAGE_BLANK_TIME0, Register Address: 0x80B8

Bits	Bit Name	Description	Reset	Access
[31:28]	RESERVED	Reserved.	0x0	R
[27:24]	VM1_BLANK_TIME	Set the Blank Time for the VM1 Voltage Monitor. 0000: 16 µs. 0001: 32 µs. 0010: 48 µs. 0011: 64 µs. 0100: 80 µs.	0x2	R/W

Bits	Bit Name	Description	Reset	Access
		0101: 96 µs. 0110: 112 µs. 0111: 128 µs. 1000: 144 µs. 1001: 160 µs. 1010: 176 µs. 1011: 192 µs. 1100: 208 µs. 1101: 240 µs. 1110: 288 µs. 1111: 352 µs.		
[23:20]	VM0_BLANK_TIME	Set the Blank Time for the VM0 Voltage Monitor. 0000: 16 µs. 0001: 32 µs. 0010: 48 µs. 0011: 64 µs. 0100: 80 µs. 0101: 96 µs. 0110: 112 µs. 0111: 128 µs. 1000: 144 µs. 1001: 160 µs. 1010: 176 µs. 1011: 192 µs. 1100: 208 µs. 1101: 240 µs. 1110: 288 µs. 1111: 352 µs.	0x2	R/W
[19:16]	FB12_BLANK_TIME	Set the Blank Time for the FB12 Voltage Monitor. 0000: 16 µs. 0001: 32 µs. 0010: 48 µs. 0011: 64 µs. 0100: 80 µs. 0101: 96 µs. 0110: 112 µs. 0111: 128 µs. 1000: 144 µs. 1001: 160 µs. 1010: 176 µs. 1011: 192 µs. 1100: 208 µs.	0x2	R/W

Bits	Bit Name	Description	Reset	Access
		1101: 240 µs. 1110: 288 µs. 1111: 352 µs.		
[15:12]	FB4_BLANK_TIME	Set the Blank Time for the FB4 Voltage Monitor. 0000: 16 µs. 0001: 32 µs. 0010: 48 µs. 0011: 64 µs. 0100: 80 µs. 0101: 96 µs. 0110: 112 µs. 0111: 128 µs. 1000: 144 µs. 1001: 160 µs. 1010: 176 µs. 1011: 192 µs. 1100: 208 µs. 1101: 240 µs. 1110: 288 µs. 1111: 352 µs.	0x2	R/W
[11:8]	FB3_BLANK_TIME	Set the Blank Time for the FB3 Voltage Monitor. 0000: 16 µs. 0001: 32 µs. 0010: 48 µs. 0011: 64 µs. 0100: 80 µs. 0101: 96 µs. 0110: 112 µs. 0111: 128 µs. 1000: 144 µs. 1001: 160 µs. 1010: 176 µs. 1011: 192 µs. 1100: 208 µs. 1101: 240 µs. 1110: 288 µs. 1111: 352 µs.	0x2	R/W
[7:4]	FB2_BLANK_TIME	Set the Blank Time for the FB2 Voltage Monitor. 0000: 16 µs. 0001: 32 µs. 0010: 48 µs. 0011: 64 µs.	0x2	R/W

Bits	Bit Name	Description	Reset	Access
		0100: 80 µs. 0101: 96 µs. 0110: 112 µs. 0111: 128 µs. 1000: 144 µs. 1001: 160 µs. 1010: 176 µs. 1011: 192 µs. 1100: 208 µs. 1101: 240 µs. 1110: 288 µs. 1111: 352 µs.		
[3:0]	FB1_BLANK_TIME	Set the Blank Time for the FB1 Voltage Monitor. 0000: 16 µs. 0001: 32 µs. 0010: 48 µs. 0011: 64 µs. 0100: 80 µs. 0101: 96 µs. 0110: 112 µs. 0111: 128 µs. 1000: 144 µs. 1001: 160 µs. 1010: 176 µs. 1011: 192 µs. 1100: 208 µs. 1101: 240 µs. 1110: 288 µs. 1111: 352 µs.	0x2	R/W

Table 122. VOLTAGE_BLANK_TIME1, Register Address: 0x80BC

Bits	Bit Name	Description	Reset	Access
[31:28]	RESERVED	Reserved.	0x0	R
[27:24]	FB11_BLANK_TIME	Set the Blank Time for the FB11 Voltage Monitor. 0000: 16 µs. 0001: 32 µs. 0010: 48 µs. 0011: 64 µs. 0100: 80 µs. 0101: 96 µs. 0110: 112 µs. 0111: 128 µs.	0x2	R/W

Bits	Bit Name	Description	Reset	Access
		1000: 144 µs. 1001: 160 µs. 1010: 176 µs. 1011: 192 µs. 1100: 208 µs. 1101: 240 µs. 1110: 288 µs. 1111: 352 µs.		
[23:20]	FB10_BLANK_TIME	Set the Blank Time for the FB10 Voltage Monitor. 0000: 16 µs. 0001: 32 µs. 0010: 48 µs. 0011: 64 µs. 0100: 80 µs. 0101: 96 µs. 0110: 112 µs. 0111: 128 µs. 1000: 144 µs. 1001: 160 µs. 1010: 176 µs. 1011: 192 µs. 1100: 208 µs. 1101: 240 µs. 1110: 288 µs. 1111: 352 µs.	0x2	R/W
[19:16]	FB9_BLANK_TIME	Set the Blank Time for the FB9 Voltage Monitor. 0000: 16 µs. 0001: 32 µs. 0010: 48 µs. 0011: 64 µs. 0100: 80 µs. 0101: 96 µs. 0110: 112 µs. 0111: 128 µs. 1000: 144 µs. 1001: 160 µs. 1010: 176 µs. 1011: 192 µs. 1100: 208 µs. 1101: 240 µs. 1110: 288 µs. 1111: 352 µs.	0x2	R/W

Bits	Bit Name	Description	Reset	Access
[15:12]	FB8_BLANK_TIME	Set the Blank Time for the FB8 Voltage Monitor. 0000: 16 µs. 0001: 32 µs. 0010: 48 µs. 0011: 64 µs. 0100: 80 µs. 0101: 96 µs. 0110: 112 µs. 0111: 128 µs. 1000: 144 µs. 1001: 160 µs. 1010: 176 µs. 1011: 192 µs. 1100: 208 µs. 1101: 240 µs. 1110: 288 µs. 1111: 352 µs.	0x2	R/W
[11:8]	FB7_BLANK_TIME	Set the Blank Time for the FB7 Voltage Monitor. 0000: 16 µs. 0001: 32 µs. 0010: 48 µs. 0011: 64 µs. 0100: 80 µs. 0101: 96 µs. 0110: 112 µs. 0111: 128 µs. 1000: 144 µs. 1001: 160 µs. 1010: 176 µs. 1011: 192 µs. 1100: 208 µs. 1101: 240 µs. 1110: 288 µs. 1111: 352 µs.	0x2	R/W
[7:4]	FB6_BLANK_TIME	Set the Blank Time for the FB6 Voltage Monitor. 0000: 16 µs. 0001: 32 µs. 0010: 48 µs. 0011: 64 µs. 0100: 80 µs. 0101: 96 µs. 0110: 112 µs.	0x2	R/W

Bits	Bit Name	Description	Reset	Access
		0111: 128 µs. 1000: 144 µs. 1001: 160 µs. 1010: 176 µs. 1011: 192 µs. 1100: 208 µs. 1101: 240 µs. 1110: 288 µs. 1111: 352 µs.		
[3:0]	FB5_BLANK_TIME	Set the Blank Time for the FB5 Voltage Monitor. 0000: 16 µs. 0001: 32 µs. 0010: 48 µs. 0011: 64 µs. 0100: 80 µs. 0101: 96 µs. 0110: 112 µs. 0111: 128 µs. 1000: 144 µs. 1001: 160 µs. 1010: 176 µs. 1011: 192 µs. 1100: 208 µs. 1101: 240 µs. 1110: 288 µs. 1111: 352 µs.	0x2	R/W

Table 123. SYSREG_CRC_CHECKSUM, Register Address: 0x80C0

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	SYS_REG_CRC_CHECKSUM	CRC Result Calculated in Power Management IC (PMIC).	0x0	R

Table 124. SYSREG_CRC_GOLDEN, Register Address: 0x80C4

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	SYS_REG_CRCGOLDEN	CRC Golden Result from Processor.	0x0	R/W

Table 125. SYSREG_CRC_POLYSEED, Register Address: 0x80C8

Bits	Bit Name	Description	Reset	Access
[31:16]	SYS_REG_CRC_SEED	System Register CRC Seed.	0x5555	R/W
[15:0]	SYS_REG_CRC_POLY	System Register CRC Polynomial.	0x90D9	R/W

Table 126. WAKEPIN_EVT, Register Address: 0x80CC

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved.	0x0	R
0	CFG_WAKEPIN_EVT_DET	Configure the WAKE Pin Function. 0: the WAKE pin is configured as the normal wake function. 1: the WAKE pin is configured as the event detector.	0x0	R/W

Table 127. SYSCRC_EN, Register Address: 0x80D0

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved.	0x0	R
0	SYSCRC_EN	System Register CRC Enable Control. 0: disable the system register CRC periodic check. 1: enable the system register CRC periodic check.	0x0	R/W

Table 128. VM_TYP_CONFIGURATION, Register Address: 0x80D4

Bits	Bit Name	Description	Reset	Access
[31:4]	RESERVED	Reserved.	0x0	R
[3:2]	VM1_TYP	VM1 Typical Configuration. 00: neither the undervoltage nor the overvoltage thresholds are effective on VM1. 01: only the undervoltage threshold is effective on VM1. 10: only the overvoltage threshold is effective on VM1. 11: both the undervoltage and the overvoltage thresholds are effective on VM1 and act as window monitors.	0x0	R/W
[1:0]	VM0_TYP	VM0 Typical Configuration. 00: neither the undervoltage nor the overvoltage thresholds are effective on VM0. 01: only the undervoltage threshold is effective on VM0. 10: only the overvoltage threshold is effective on VM0. 11: both the undervoltage and the overvoltage thresholds are effective on VM0 and act as window monitor.	0x0	R/W

Table 129. FUSE_PERIOD_CHK_TIMER, Register Address: 0x80D8

Bits	Bit Name	Description	Reset	Access
[31:10]	RESERVED	Reserved.	0x0	R
[9:0]	FUSE_PERIOD_CHK_TIMER	Diagnose Control Block ECC/CRC Periodical Check Timer Counter (ms).	0x96	R/W

Table 130. SPI_PIN_CTRL, Register Address: 0x80F0

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved.	0x0	R
3	$\overline{\text{STATUS}}$_SPI_CTRL_DATA	Control $\overline{\text{STATUS}}$ Pin Status. 1: high. 0: low.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
2	$\overline{\text{STATUS}}$_SPI_CTRL_EN	Enable or Disable $\overline{\text{STATUS}}$ Pin SPI Control Function. 1: enable. 0: disable.	0x0	R/W
1	$\overline{\text{FAULT}}$_SPI_CTRL_DATA	Control $\overline{\text{FAULT}}$ Pin Status. 1: high. 0: low.	0x0	R/W
0	$\overline{\text{FAULT}}$_SPI_CTRL_EN	Enable or Disable $\overline{\text{FAULT}}$ Pin SPI Control Function. 1: enable. 0: disable.	0x0	R/W

OUTLINE DIMENSIONS

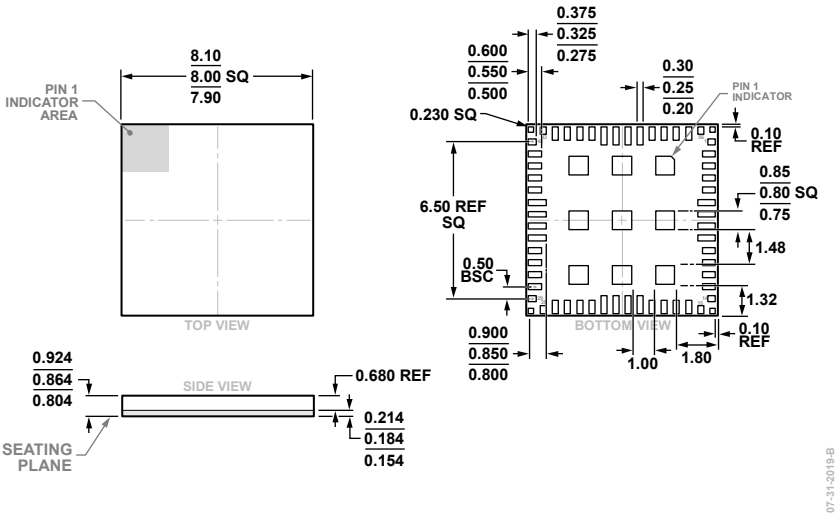

Figure 97. 56-Terminal Land Grid Array [LGA]
(CC-56-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option	Package Quantity
ADP5140WACCZ-R7	−40°C to +150°C	56-Terminal Land Grid Array [LGA]	CC-56-2	750
ADP5140-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADP5140W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.