Fully Integrated 24V/12A Switched Capacitor DC/DC Converter with Overvoltage and Overcurrent Protections

FEATURES

- **Wide V_{HIGH}/V_{LOW} Voltage from 0V/0V to 24V/12V**
- **Wide V_{CC} Supply Range from 4.5V to 38V**
- **Very High Efficiency: 97% at 10A Load**
- **Input Overvoltage Protection with External Overvoltage Protection MOSFET**
- **Input and Output Short-Circuit Protection**
- **Soft Start-Up into Steady-State Operation**
- **$EXTV_{CC}$ Capable of 5V to 14V Input for High Efficiency**
- Inrush Current Limit and Protection
- Integrated Bootstrap Diodes
- Programmable Operating Frequency from 100kHz to 1.4MHz
- Available in a 4mm × 5mm LGA (LQFN) Package

APPLICATIONS

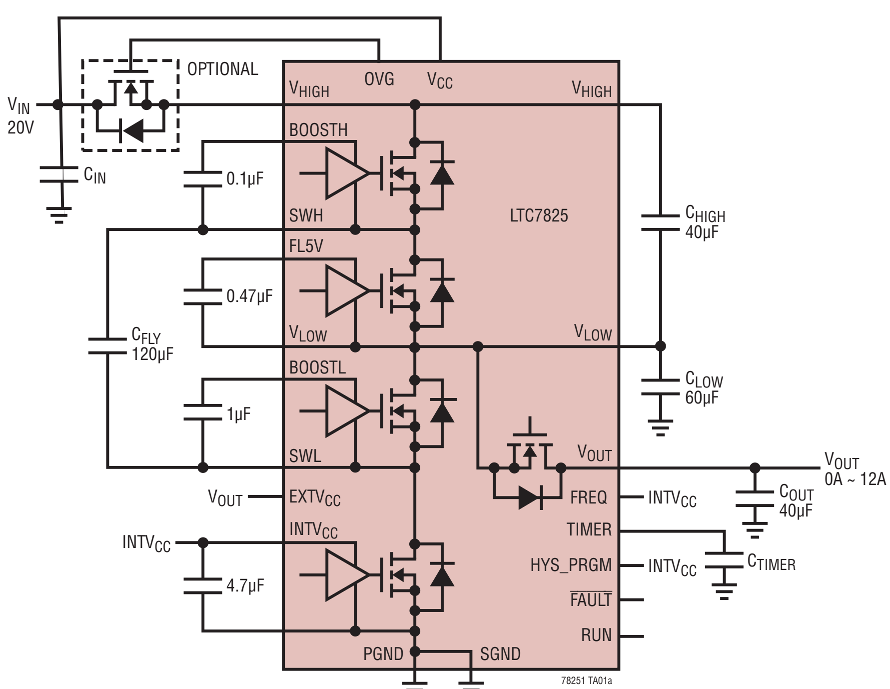
- Consumer Electronics
- Industrial Applications
- Battery Applications

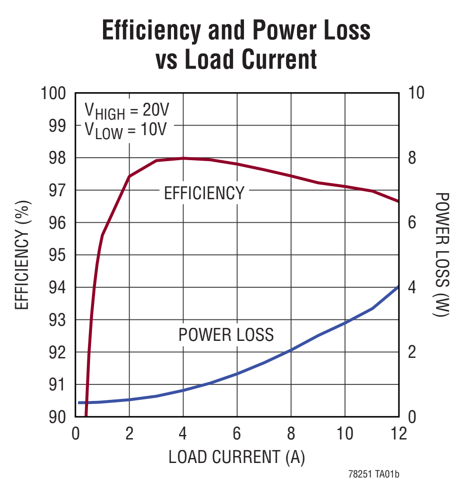
DESCRIPTION

The LTC®7825 is a fully integrated monolithic DC/DC converter. It achieves very high efficiency with a switched capacitor architecture in applications with 2:1 input to output voltage ratio. The LTC7825 input can survive voltage transient up to 40V when protected by an optional MOSFET between V_{IN} and V_{HIGH}. The input and output are fully disconnected during short-circuit conditions. The LTC7825 features integrated bootstrap diodes and provides a compact and cost-effective solution for high power intermediate bus applications requiring current limit protections.

The LTC7825 operating switching frequency can be linearly programmed from 100kHz to 1.4MHz. The part is available in a 4mm × 5mm LGA (LQFN) package.

TYPICAL APPLICATION





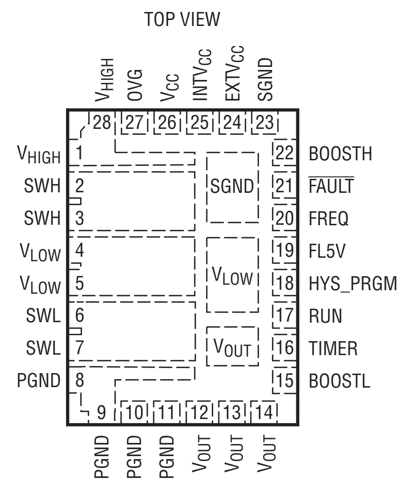
Rev. A

ABSOLUTE MAXIMUM RATINGS

(All the voltage is referred to the SGND pin unless otherwise specified) (Note 1)

V_{CC} .... –0.3V to 40V
V_{LOW}, V_{OUT} .... –0.3V to 13V
V_{HIGH} .... 0.3V to 26V
(BOOSTH – SWH), (BOOSTL – SWL)........ –0.3V to 5.5V
(FL5V – VLOW) (OVG – V_{HIGH}) .... –0.3V to 5.5V
$INTV_{CC}$, RUN .... –0.3V to 6V
$EXTV_{CC}$ .... –0.3V to 13V
HYS_PRGM, FREQ, TIMER .... –0.3V to $INTV_{CC}$
$\overline{\text{FAULT}}$, OVG .... –0.3V to 29V
Operating Junction Temperature Range. –40°C to 125°C
Storage Temperature Range .... –40°C to 150°C

PIN CONFIGURATION



LGA PACKAGE
28-LEAD (4mm x 5mm) PLASTIC LQFN
T_{JMAX} = 125°C, θ_{JA} = 29.7°C/W

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7825AV#PBF	7825	28-Lead (4mm × 5mm) Plastic LQFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 12V, V_{RUN} = 5V, unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT/OUTPUT VOLTAGE							
V_{CC}	IC Bias Voltage Range			4.5		40	V
V_{VHIGH}	V_{HIGH} Voltage Range			0		25	V
V_{VLOW}	V_{LOW} Voltage Range			0		12.5	V
I_Q	V_{CC} Supply Current Normal Operation	V_{RUN} = 0V V_{RUN} = 5V, No Switching			20 3		µA mA
V_{UVLO}	Undervoltage Lockout Threshold	V_{INTVCC} Falling V_{INTVCC} Rising			3.9 4.2		V V
Gate Drivers							
$R_{DS(ON)1,2}$	Top Two MOSFETs On-Resistance				8		mΩ
$R_{DS(ON)}3,4$	Bottom Two MOSFETs On-Resistance				6		mΩ
$R_{DS(ON)}5$	V_{OUT} MOSFETs On-Resistance				2.5		mΩ
RUN Pin							
V_{RUN}	RUN Pin on Threshold	V_{RUN} Rising		1.1	1.22	1.35	V
$V_{RUN,HYS}$	RUN Pin on Hysteresis				80		mV
$INTV_{CC}$ Regulator							
V_{INTVCC_VCC}	V_{CC} LDO Voltage No Load	V_{CC} = 12V, V_{EXTVCC} = 0V		4.25	4.5	4.75	V
V_{INTVCC_EXT}	$EXTV_{CC}$ LDO Voltage No Load	V_{EXTVCC} = 8V, V_{CC} = 12V (Note 5)		4.25	4.5	4.75	V
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	V_{EXTVCC} Ramping Positive (Note 6)			5.1		V
V_{LDOHYS}	$EXTV_{CC}$ Hysteresis				300		mV
V_{HIGH} and V_{LOW} Resistance							
R_{VHIGH}	V_{HIGH} to GND Resistance				1.2		MegΩ
R_{VLOW}	V_{LOW} to GND Resistance				0.6		MegΩ
V_{LOW} Balance Current							
I_{SOURCE}	Source Current to V_{LOW} Pin	V_{HIGH} = 12V, V_{LOW} = 5V, TIMER = 0.8V			200		mA
I_{SINK} (LTC7825)	Sink Current from V_{LOW} Pin	V_{HIGH} = 12V, V_{LOW} = 7V, TIMER = 0.8V			50		mA
Oscillator							
f_S	Oscillator Frequency Range			100		1200	kHz
f_{NOM}	Nominal Frequency	V_{FREQ} = 0V V_{FREQ} = 1.02V V_{FREQ} = $INTV_{CC}$			300 400 600		kHz kHz kHz
I_{FREQ}	FREQ Setting Current			9	10	11	µA
$\overline{FAULT}$ and HYS_PRGM							
$R_{\overline{FAULT}}$	$\overline{FAULT}$ Open-Drain Pull-Down Resistance				180		Ω
$I_{\overline{FAULT}\_LEAK}$	$\overline{FAULT}$ Leakage Current	$V_{\overline{FAULT}}$ = 29V				±1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 12V, V_{RUN} = 5V, unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{HYS_PRGM}	HYS_PRGM Setting Current			9	10	11	µA
V_{VLOW_FAULT} (LTC7825)	V_{LOW} Voltage Fault Level	V_{VHIGH} = 12V, V_{HYS_PRGM} = 1V V_{VLOW} Ramping Up V_{VLOW} Ramping Down			 6.2 5.8		 V V
		V_{VHIGH} = 16V, V_{HYS_PRGM} = $INTV_{CC}$ V_{VLOW} Ramping Up V_{LOW} Ramping Down			 8.4 7.6		 V V
		V_{VHIGH} = 8V, V_{HYS_PRGM} = 0V V_{VLOW} Ramping Up V_{VLOW} Ramping Down			 4.24 3.76		 V V
OVG							
V_{OVG_VHIGH}	OVG to V_{HIGH}	OVG On			4		V
V_{OV}	V_{HIGH} Overvoltage Threshold	V_{HIGH} Rising			26		V
V_{OV_HYS}	V_{HIGH} Overvoltage Hysteresis	Hysteresis			3.2		V
TIMER Current	I_{TIMER}	V_{TIMER} < 0.5V or V_{TIMER} > 1V			4		µA
		0.5V < V_{TIMER} < 1V			8		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7825A is specified over the –40C to 125C operating junction temperature range. High junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D \bullet J_A)$.

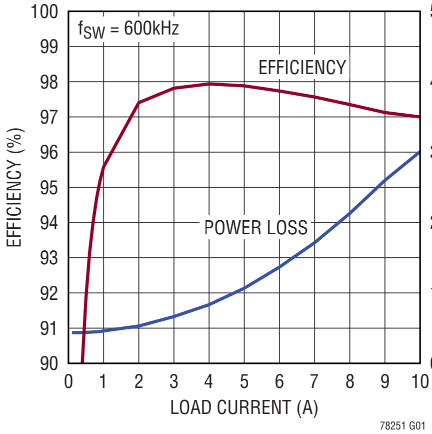
Note 4: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 5: When V_{CC} > 6V, $EXTV_{CC}$ is recommended to reduce IC Temperature.

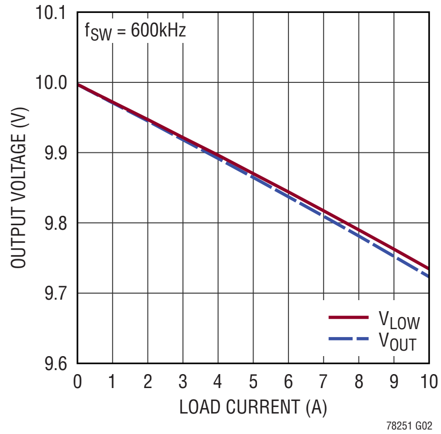
Note 6: $EXTV_{CC}$ is enabled only if V_{CC} is higher than 6V.

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

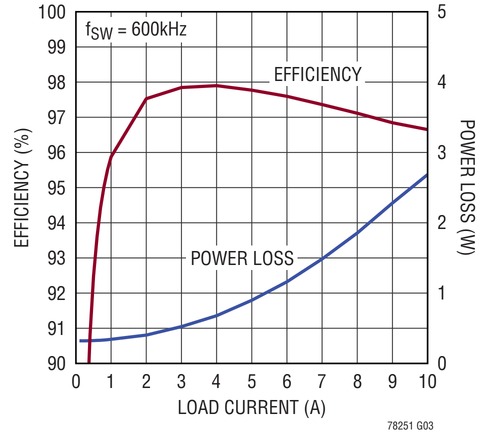
Efficiency and Power Loss vs Load $20V_{IN}$ Voltage Divider in Figure 3



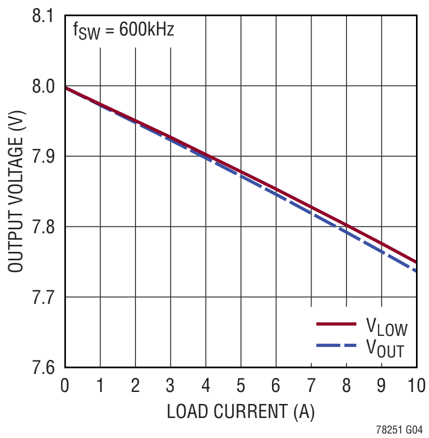
V_{LOW} and V_{OUT} Load Regulation $20V_{IN}$ Voltage Divider in Figure 3



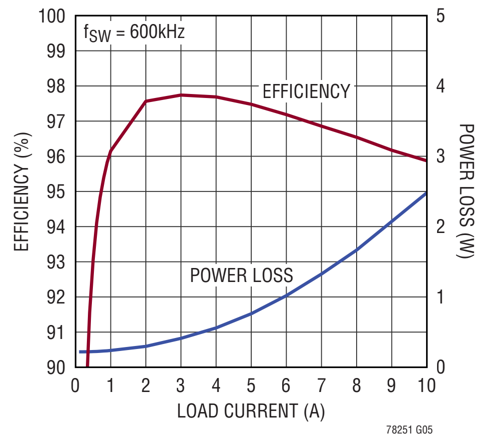
Efficiency and Power Loss vs Load $16V_{IN}$ Voltage Divider in Figure 3



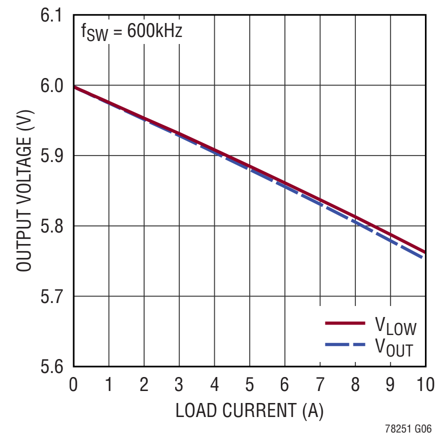
V_{LOW} and V_{OUT} Load Regulation $16V_{IN}$ Voltage Divider in Figure 3



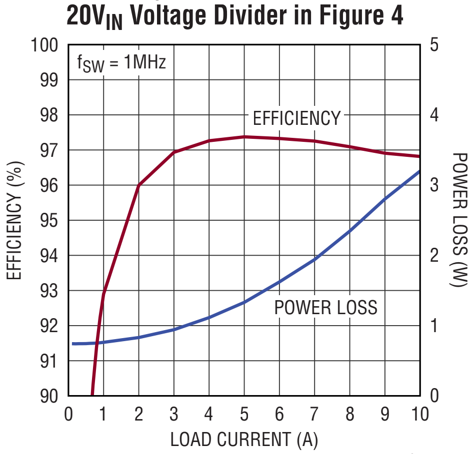
Efficiency and Power Loss vs Load $12V_{IN}$ Voltage Divider in Figure 3



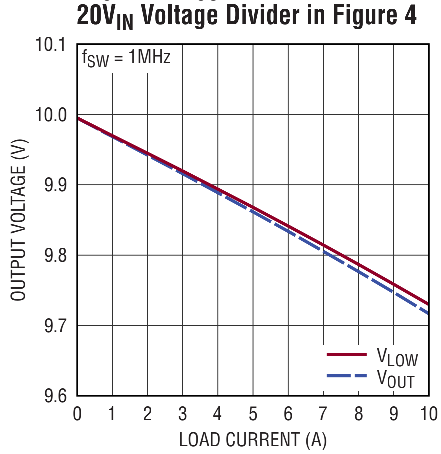
V_{LOW} and V_{OUT} Load Regulation $12V_{IN}$ Voltage Divider in Figure 3



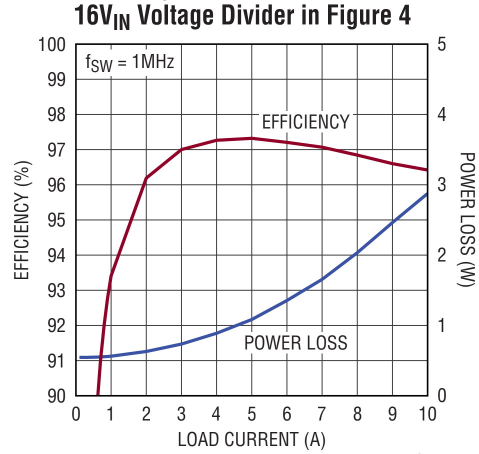
Efficiency and Power Loss vs Load $20V_{IN}$ Voltage Divider in Figure 4



V_{LOW} and V_{OUT} Load Regulation $20V_{IN}$ Voltage Divider in Figure 4

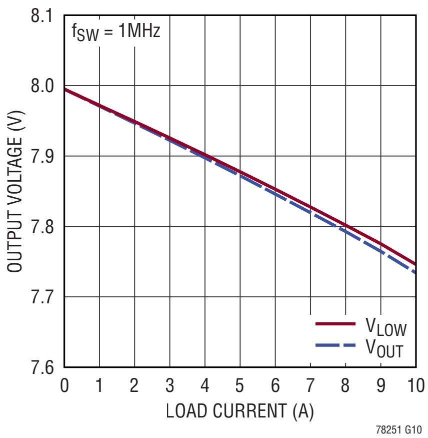


Efficiency and Power Loss vs Load $16V_{IN}$ Voltage Divider in Figure 4

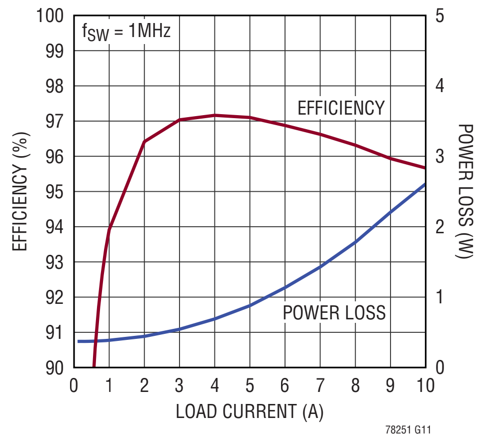


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

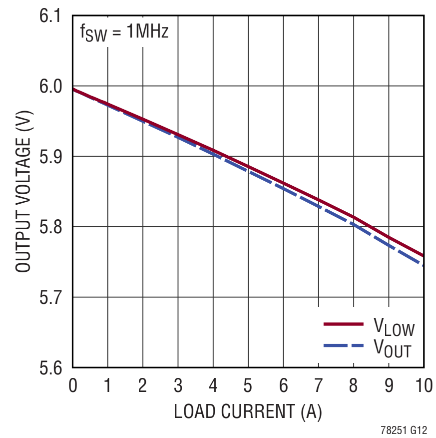
V_{LOW} and V_{OUT} Load Regulation 16V_{IN} Voltage Divider in Figure 4



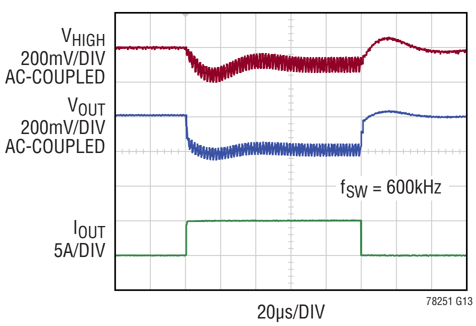
Efficiency and Power Loss vs Load 12V_{IN} Voltage Divider in Figure 4



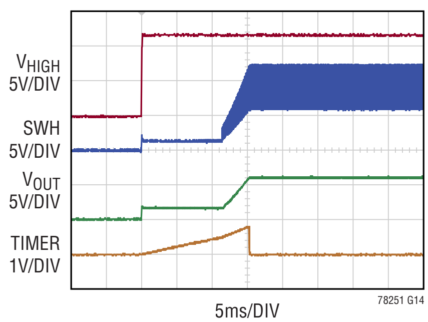
V_{LOW} and V_{OUT} Load Regulation 12V_{IN} Voltage Divider in Figure 4



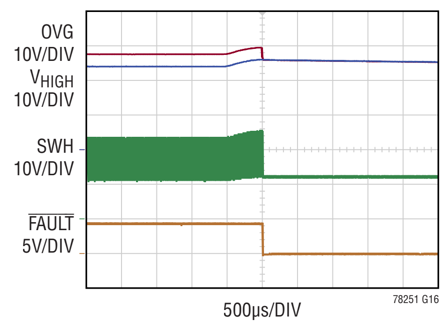
Load Transient 0A–5A–0A 12V to 6V Divider in Figure 3



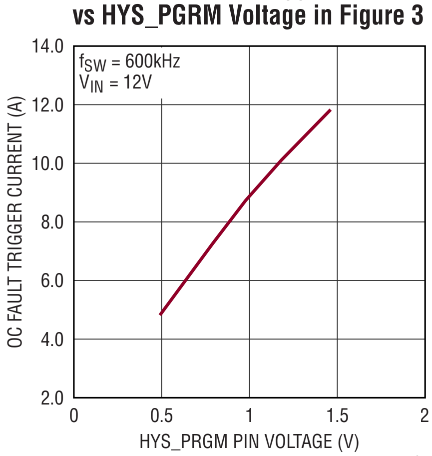
Soft Start-Up 12V to 6V Divider RUN Pin Float



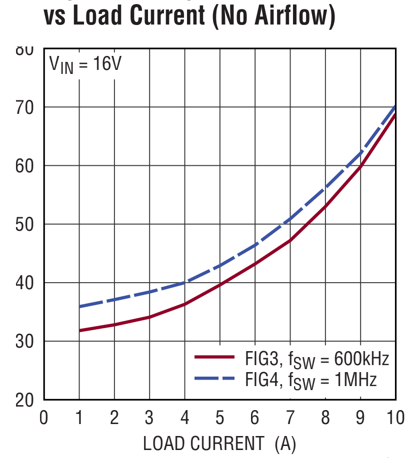
Input Overvoltage Protection with the External MOSFET and OVG Control



Overcurrent Fault Trigger Current vs HYS_PRGM Voltage in Figure 3



Top Case Temperature vs Load Current (No Airflow)



Rev. A

PIN FUNCTIONS

V_{HIGH} (Pins 1, 28): Switched Capacitor Converter High Side Voltage Input. Connect capacitors from V_{HIGH} to GND and to V_{LOW} for high efficiency operation.

SWH (Pins 2, 3): High Side Switching Node. Connect to the flying capacitors.

V_{LOW} (Pins 4, 5): Switched Capacitor Converter Low Side Voltage Input. Connect capacitors from V_{LOW} to GND.

SWL (Pins 6, 7): Low Side Switching Node. Connect to the flying capacitors.

PGND (Pins 8, 9, 10, 11): Power Ground.

V_{OUT} (Pins 12, 13, 14): Output of the Internal Disconnect MOSFET Connected to V_{LOW}. The input short protection is achieved by turning off the internal disconnect MOSFET. If internal disconnect is not needed, V_{OUT} may be short to V_{LOW} externally for higher efficiency.

BOOSTL, BOOSTH (Pins 15, 22): Bootstrapped Supplies to the floating Drivers. Capacitors are connected between the BOOSTH to SWH and BOOSTL to SWL pins.

TIMER (Pin 16): Connecting a capacitor between this pin and ground sets the amount of time of soft start-up. It also sets the short-circuit retry time. See the Applications Information section for details.

RUN (Pin 17): Digital Run Control Input. Forcing RUN below 1.2V shuts down the controller. When RUN pin is higher than 1.2V, internal circuitry starts up. A 1µA pull-up current flows out of RUN pin when RUN is below 1.2V and an additional 4.5µA current flowing out of RUN pin when RUN is above 1.2V.

HYS_PRGM (Pin 18): A resistor connected between this pin and ground will set the window threshold of the window comparator that monitors the voltage difference across $V_{HIGH}/2$ and V_{LOW}. Tying this pin to GND or $INTV_{CC}$ sets the window to 240mV or 400mV, respectively. There is a 10µA current flowing throughout this pin.

FL5V (Pin 19): Floating 5V power for the internal driver and control circuit. A 0.1µF ~ 1µF ceramic capacitor or other low ESR capacitor is required from this pin to the V_{LOW} pin.

FREQ (Pin 20): Frequency Set Pin. There is a precision 10µA current flowing out of this pin. A resistor to ground sets a voltage which in turn programs the frequency. Tying this pin to GND or $INTV_{CC}$ sets the default 300kHz/600kHz switching frequency. See the Applications Information section for the detailed information.

$\overline{\text{FAULT}}$ (Pin 21): This is an open-drain output. $\overline{\text{FAULT}}$ is pulled to ground when the V_{LOW} voltage is out of the $V_{HIGH}/2$ window threshold.

SGND (Pin 23): Signal Ground. All small-signal components should connect to this ground. Connect this pin with PGND pins on the PCB.

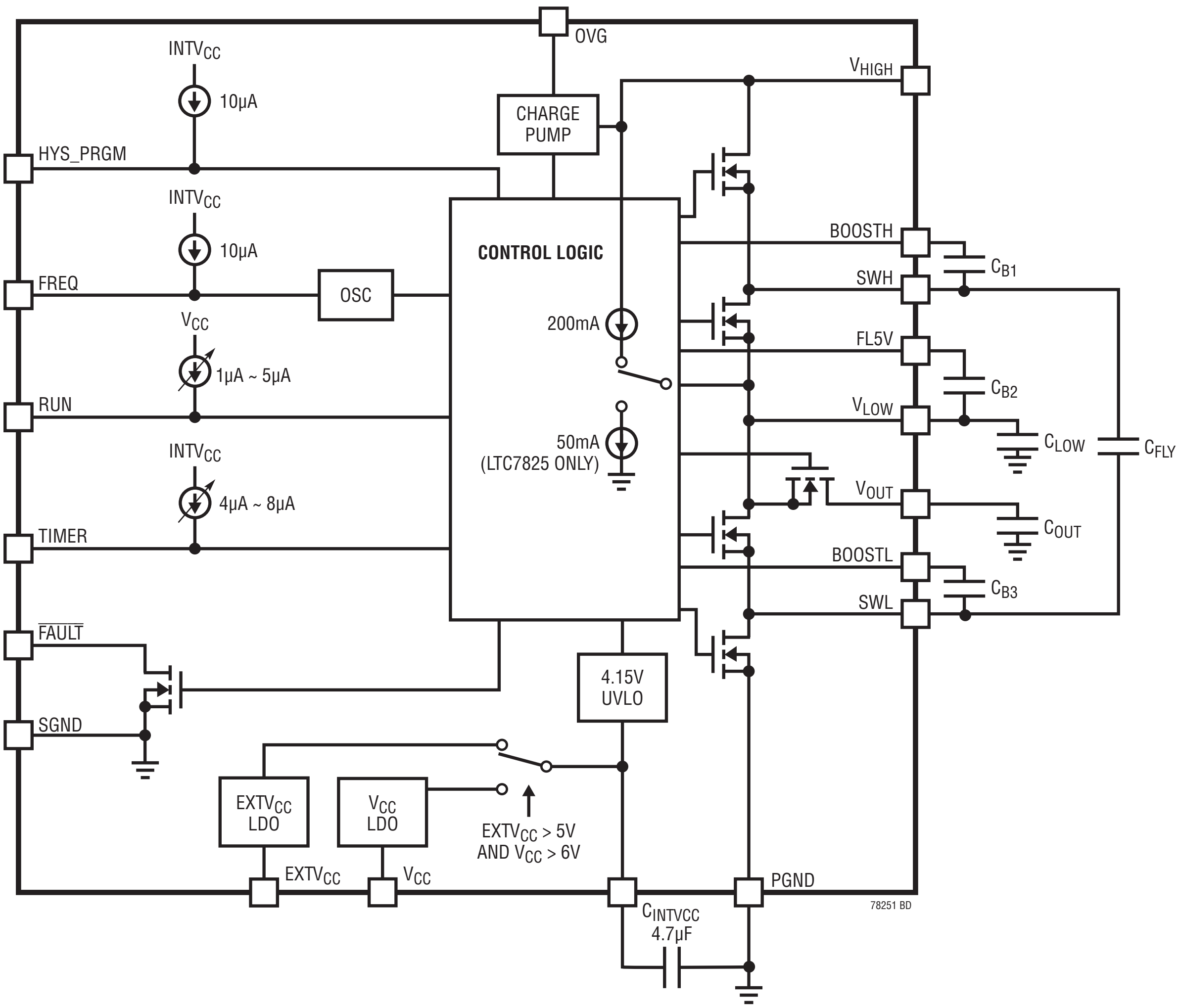
$EXTV_{CC}$ (Pin 24): External Power Input to an Internal LDO Connected to the $INTV_{CC}$. This LDO supplies $INTV_{CC}$ power, bypassing the internal LDO powered from V_{CC} whenever $EXTV_{CC}$ is higher than 5V and V_{CC} is higher than 6V. Do not float or exceed 14V on this pin.

$INTV_{CC}$ (Pin 25): Output of the Internal Linear Low Dropout Regulator. The driver and control circuits are powered from this voltage source. Must be bypassed to power ground with a minimum of 4.7µF ceramic or other low ESR capacitor. Do not use the $INTV_{CC}$ pin for any other ICs.

V_{CC} (Pin 26): Power supply for drivers and internal charging circuit. A bypass capacitor should be tied between this pin and the GND pin.

OVG (Pin 27): Optional input over voltage protection pin. connect this pin to the gate of the external N-channel MOSFET. If the V_{HIGH} voltage is higher than 26V, the OVG turns off the external MOSFET. If not used, leave this pin floating.

BLOCK DIAGRAM



OPERATION

MAIN CONTROL

The LTC7825 is a constant-frequency, open loop switched capacitor/charge pump converter for high power and high voltage applications. In the steady-state operation, the internal switches are turned on and off to force the flying capacitor between SWH and SWL either parallel with the capacitor at V_{LOW} or serial with the capacitor at V_{LOW}. When the flying capacitors and V_{LOW} capacitors are paralleled, the voltages on the flying capacitor and V_{LOW} capacitor are the same. When the flying capacitors and V_{LOW} capacitors are serial to V_{HIGH}, the voltage on the flying capacitor plus the voltage on the V_{LOW} capacitor equals the voltage on V_{HIGH}. So the V_{LOW} pin voltage is always close to half of the V_{HIGH} voltage in the steady state and it is not sensitive to the variable loads due to the very low output impedance operating at a high switching frequency. The LTC7825 does not regulate the output voltage with a closed-loop feedback system. However, it stops switching when fault conditions occur, such as a V_{LOW} pin short to GND, an overcurrent event, and overtemperature conditions.

$INTV_{CC}$/$EXTV_{CC}$ POWER

Power for the internal quad N-channel MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. Normally an internal 4.5V linear regulator supplies $INTV_{CC}$ power from V_{CC}. If V_{CC} is connected to a high input voltage, an optional external voltage source may be connected to the $EXTV_{CC}$ pin, enabling the second 4.5V linear regulator and supplying $INTV_{CC}$ power from the $EXTV_{CC}$ pin. To enable the linear regulator under the $EXTV_{CC}$ pin, V_{CC} has to be higher than 6V and the $EXTV_{CC}$ pin voltage has to be higher than 5V. Do not exceed 13V on the $EXTV_{CC}$ pin. Each top MOSFET driver is biased from the floating bootstrap capacitors C_B, which normally recharge during each off cycle through an internal diode when the respective top MOSFET turns off.

START-UP AND SHUTDOWN (RUN)

The LTC7825 is in the shutdown mode when the RUN pin is pulled down. In shutdown mode, most internal circuitry is turned off including the $INTV_{CC}$ regulator and the LTC7825 consumes less than 30µA current. All internal N-channel MOSFETs are actively turned off. Releasing RUN allows an internal 1µA current to pull-up this pin and enable the converter. Alternately, the RUN pin may be externally pulled up or driven directly by logic. Do not exceed the absolute maximum rating of 6V on this pin.

After RUN is released and the $INTV_{CC}$ voltage passes UVLO, the LTC7825 starts up and monitors the V_{HIGH} and V_{LOW} voltage continuously. The LTC7825 starts switching and provides full power only if V_{LOW} voltage is close to half of V_{HIGH} voltage or both V_{LOW} and V_{HIGH} voltages are close to ground. In voltage divider applications, V_{LOW} is pre-balanced to half the V_{HIGH} voltage and the LTC7825 may start-up with V_{LOW} at different initial conditions.

FAULT PROTECTION AND THERMAL SHUTDOWN

The LTC7825 monitors system voltage, current and temperature for fault protections. It will stop switching and pull the $\overline{\text{FAULT}}$ pin down when fault conditions occur. To clear V_{LOW} voltage faults, the V_{LOW} pin voltage has to be within the programmed window around $V_{HIGH}/2$ or the V_{HIGH}/V_{LOW} voltages must be lower than 1V/0.5V. To clear V_{HIGH} over voltage fault, the V_{HIGH} voltage must be lower than 26V and OVG must be 4V higher than V_{HIGH}. To clear temperature faults, the IC temperature has to be lower than 165°C.

The $\overline{\text{FAULT}}$ pin is allowed to be pulled up by an external resistor to sources of up to 25V. It can be used to control external disconnect MOSFETs, which isolate the input and output during fault conditions.

OPERATION

OVERCURRENT PROTECTION

During the steady-state operation, the V_{LOW} voltage drops linearly as load current increases. The overcurrent protection can be set by choosing different V_{LOW} to $V_{HIGH}/2$ windows controlled by HYS_PRGM pin. If overcurrent fault is triggered, the LTC7825 stops switching and will retry to start up.

In practice, the V_{LOW} voltage valley is impacted by switching frequency and C_{FLY}/C_{OUT}. To set the correct hysteresis window, measure the V_{LOW} voltage at full load and maximum switching ripple. Although the LTC7825 is designed to optimize efficiency around 10A load, there is no strict limit on the output current. As long as the hysteresis window on the V_{LOW} is large enough, the LTC7825 can supply more than 12A load current with heat sinks or forced air flow. Refer to the Typical Performance Characteristics section for an example of HYS_PRGM setting.

FREQUENCY SELECTION (FREQ PIN)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses but requires larger capacitance to maintain low output ripple voltage and low output impedance. The FREQ pin can be used to program the converter's operating frequency from 100kHz to 1.4MHz. There is a precision 10µA current flowing out of the FREQ pin, so the user can program the converter's switching frequency with a single resistor to SGND. The voltage on the FREQ pin is equal to the resistance multiplied by 10µA current (e.g., the voltage is 1V with a 100k resistor from the FREQ pin to GND). A curve is provided in Figure 1 showing the relationship between the voltage on the FREQ pin and switching frequency. Tie FREQ pin to SGND/$INTV_{CC}$ enables the default switching frequency of 300kHz/600kHz.

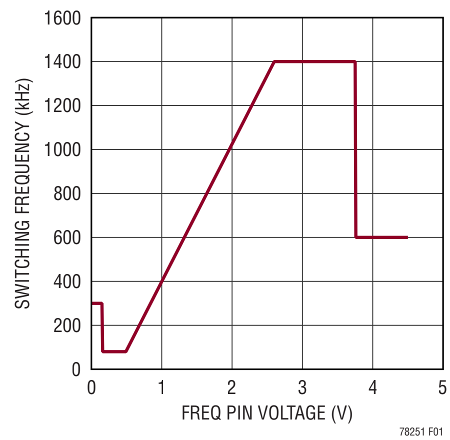


Figure 1. Relationship Between Switching Frequency and Voltage at FREQ Pin

APPLICATIONS INFORMATION

The Typical Application on the first page of this data sheet is a LTC7825 voltage divider circuit. The converter can convert V_{HIGH} voltage to V_{LOW} voltage with a 2:1 step-down ratio and supply 12A load current in steady-state operation. In overcurrent or start-up conditions, the converter automatically limits the V_{HIGH} supply peak current to 200mA for thermal protection.

VOLTAGE DIVIDER PRE-BALANCE BEFORE SWITCHING

In voltage divider applications, the LTC7825 can achieve soft start-up to minimize the inrush current at all initial conditions. The voltages on the flying capacitors and V_{LOW} capacitors are pre-charged to half of the V_{HIGH} voltage internally. The pre-charge current during start-up is around 200mA. To further minimize the thermal stress, the TIMER pin can be used to control the pre-charge timing. The pre-charge is only enabled at $0.5 < V_{TIMER} < 1.0V$.

WINDOW COMPARATOR PROGRAMMING

In steady-state operation, V_{LOW} voltage should be always close to $V_{HIGH}/2$. A floating window comparator monitors the voltage on the V_{LOW} pin and compares it with $V_{HIGH}/2$. The window hysteresis voltage can be programmed and is equal to one fifth of the voltage at the HYS_PRGM pin. There is a precision 10µA current flowing out of the HYS_PRGM pin. A single resistor from the HYS_PRGM pin to GND sets the HYS_PRGM pin voltage, which equals the resistor value multiplied by 10µA current (e.g., the voltage is 1V with a 100k resistor from the HYS_PRGM pin to GND). With a 100k resistor on the HYS_PRGM pin, the $V_{HIGH}/2$ voltage has to be within (V_{LOW} ± 200mV) window during the normal operation, otherwise a fault is triggered and the LTC7825 stops switching.

The window hysteresis voltage can be linearly programmed from 100mV to 480mV with different resistor values on the HYS_PRGM pin. If the HYS_PRGM pin is tied to SGND/$INTV_{CC}$, a default 240mV/400mV hysteresis window is applied internally. The hysteresis window voltage must be programmed large enough to tolerate the V_{LOW} pin voltage ripple and voltage drop at maximum load conditions.

EFFECTIVE OPEN-LOOP OUTPUT RESISTANCE AND LOAD REGULATION

The LTC7825 does not regulate the output voltage through a feedback closed loop system. The V_{LOW} voltage is very close to half the V_{HIGH} voltage in steady-state operation. The output resistance is very low because $R_{DS(ON)}$ resistance from V_{HIGH} to V_{LOW} is just 20mΩ to 30mΩ depending on the switching frequency and the capacitance of C_{FLY} and C_{LOW}. If the output disconnect MOSFET is used, the output resistance from V_{LOW} to V_{OUT} is around 2mΩ.

In many applications, multi-layer ceramic capacitors (MLCC) are selected as flying capacitors. The voltage coefficients of MLCC capacitors strongly depend on the type and size of capacitors. Normally larger size X7R MLCC capacitors are better than X5R in terms of voltage coefficient. The MLCCs still drop 20% to 30% capacitance with high DC bias voltage. Capacitance derating needs to considered when estimating the output resistance of the switched capacitor circuits.

$INTV_{CC}$ REGULATORS AND $EXTV_{CC}$

The LTC7825 features a PMOS LDO that supplies power to $INTV_{CC}$ from the V_{CC} supply. $INTV_{CC}$ powers the gate drivers and most of the LTC7825's internal circuitry. The linear regulator regulates the voltage at the $INTV_{CC}$ pin to 4.5V. $EXTV_{CC}$ connects to $INTV_{CC}$ through another PMOS LDO and can supply the needed power when $EXTV_{CC}$ voltage is higher than 5V and V_{CC} is higher than 6V. Both LDOs can supply the driver current and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor or low ESR electrolytic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers.

In high input voltage applications, the LDO loss may cause the IC die temperature to rise. A low voltage supply on the $EXTV_{CC}$ pin may be used to reduce the IC temperature rise. When the voltage on the $EXTV_{CC}$ pin is higher than 5V, the linear regulator from $EXTV_{CC}$ is enabled. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. Using the

APPLICATIONS INFORMATION

$EXTV_{CC}$ allows the MOSFET driver and control power to be derived from other high efficiency sources such as V_{LOW} pin of a 20V to 10V voltage divider or other voltage rails in the system. Using $EXTV_{CC}$ can significantly reduce the IC temperature rise and improve the system efficiency in high V_{IN} applications. Do not apply more than 13V to the $EXTV_{CC}$ pin.

FLOAT MOSFET DRIVER SUPPLY (CB)

External bootstrap capacitors $C_{B1}/C_{B2}/C_{B3}$, connected to the BOOST pins, supply the gate drive voltages for the internal power MOSFETs. Capacitors in the Functional Diagram are charged though internal diodes from $INTV_{CC}$. Typically, 0.1μF X7R is adequate for the bootstrap capacitor.

UNDERVOLTAGE LOCKOUT

The LTC7825 has a precision UVLO comparator constantly monitoring the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action when $INTV_{CC}$ is below 3.9V. To prevent oscillation when there is a disturbance on the $INTV_{CC}$, the UVLO comparator has 300mV hysteresis.

INPUT DISCONNECT MOSFET AND OVG CONTROL

The LTC7825 features the optional input disconnect protection. This feature uses an external N-channel MOSFET, the gate of which is connected to the OVG pin. The OVG pin turns the MOSFET on and off. In normal operation, the OVG pin voltage is 4V higher than the V_{HIGH} pin regulated by an internal charge pump. If the V_{HIGH} pin voltage is higher than 26V, the OVG pin is pulled down to V_{HIGH} to turn off the external MOSFET, and switching stops. The LTC7825 can survive at an input transient voltage as high as 40V which is limited by the V_{CC} pin maximum voltage rating. Refer to the Typical Performance Characteristics section for the example of input overvoltage protection. If the input voltage is always below 24V and the input disconnect feature is not needed, let the OVG pin float.

OUTPUT DISCONNECT MOSFET AND SHORT-CIRCUIT PROTECTIONS

The output disconnect MOSFET is integrated internally and designed to protect the output voltage during the input short-circuit conditions. The output disconnect MOSFET behaves like an ideal diode from the V_{LOW} to the V_{OUT} pin and it is turned off when the V_{HIGH} voltage is lower than the V_{OUT} voltage. During V_{HIGH} short-circuit conditions, the V_{LOW} voltage will be pulled down due to the internal body diodes from V_{LOW} to V_{HIGH}; the V_{OUT} voltage will not be pulled down. If the output disconnect function is not needed, users may short the V_{LOW} and V_{OUT} pins together on the PCB to achieve better efficiency and thermal performances.

FAULT RESPONSE AND TIMER PIN

The LTC7825 stops switching and pulls the $\overline{FAULT}$ pin low during fault conditions. A capacitor connected from the TIMER pin to GND sets the time for retry and start-up if fault conditions are removed. A typical waveform on the TIMER pin, during a fault condition, is shown in Figure 2.

After the $\overline{FAULT}$ pin is pulled low, a 4μA pull-up current flows out of TIMER pin and starts to charge the TIMER capacitor. The pull-up current increases to 8μA when the TIMER pin voltage is higher than 0.5V and back to 4μA when the TIMER pin voltage is higher than 1.0V. The TIMER pin will be strongly pulled down whenever the fault conditions are removed or the TIMER pin voltage is higher than 3V. When the TIMER pin voltage is between 0.5V and 1.0V, the internal pre-balance circuit will source or sink current to the V_{LOW} pin and regulate the V_{LOW} pin to $V_{HIGH}/2$ with around 200mA/50mA capability. The pre-balance time can be calculated based on the value of capacitor C_{TIMER} on the TIMER pin.

For voltage divider applications, if the flying capacitor C_{FLY} and the V_{LOW} capacitor are very large and input voltage is high, it may take several pre-balance time periods to pre-balance the V_{LOW} pin to $V_{HIGH}/2$ with a fixed C_{TIMER}. A longer start-up time is expected.

APPLICATIONS INFORMATION

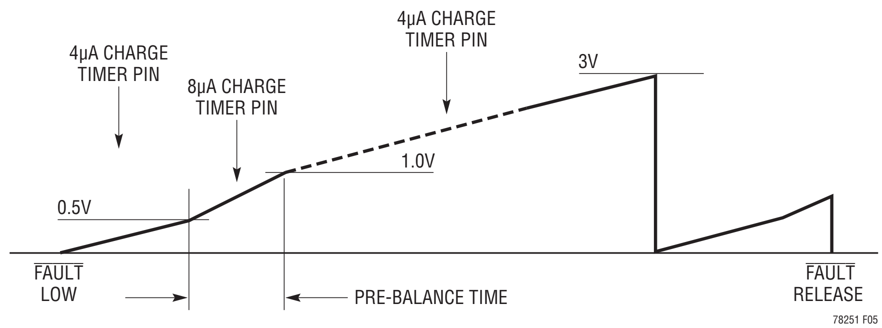


Figure 2. Timer Behavior During Fault or Start-Up

VOLTAGE DOUBLER AND INVERTER APPLICATIONS

The LTC7825 may be used as a voltage doubler or voltage inverter. In voltage doubler applications, V_{LOW} is the input and V_{HIGH} is the output. In voltage inverter applications, V_{HIGH} is the input, V_{LOW} is the ground and PGND is the negative output. In the doubler and inverter applications, the LTC7825 can start-up without capacitor inrush charging current if the input voltage is ramping slowly up from zero. As long as the input voltage ramps up slowly (in milliseconds), the output voltage can track the input voltage and the voltage difference between capacitors is always small, minimizing inrush current. Slew rate control of the input voltage can be achieved by using a disconnect MOSFET at the input or using Hot Swap controllers. Unlike voltage dividers, the voltage doubler and inverter applications have to start up from zero input voltage every time, but they can start up with heavy initial load currents.

INPUT/OUTPUT CAPACITOR AND FLYING CAPACITOR SELECTION

In high power switched capacitor applications, large AC currents flow through the flying capacitors and input/output capacitors. Low ESR ceramic capacitors are highly recommended for high power switched capacitor applications. Make sure the maximum RMS capacitor current is within the spec or higher rated capacitors are preferred. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose capacitors rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design.

The input capacitor RMS current is approximately half of the load current. The input capacitor has to be selected to accommodate the maximum load conditions.

PC BOARD LAYOUT CHECKLIST

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1. Are the exposed pad SGND/V_{LOW}/V_{OUT} solidly connected to the corresponding pins on the PCB?
2. Are all the capacitors C_{FLY}/C_{LOW}/C_{OUT} close to the IC? The PCB trace to those capacitors should be wide enough to handle large load currents.
3. Is the $INTV_{CC}$ bypassing capacitor connected close to the IC, between the $INTV_{CC}$ and ground plane?
4. Are the PCB traces to V_{HIGH}/V_{LOW}/PGND wide enough to handle large load currents?
5. In the cases of a multilayer board, are there enough thermal vias on the V_{HIGH}/V_{OUT}/PGND plane?

Refer to the standard demo board design on here for the PCB layout examples.

APPLICATIONS INFORMATION

DESIGN EXAMPLE

As a design example using LTC7825 in a voltage divider application, assumes V_{IN} = 12V ~ 20V, V_{OUT} = 6V ~ 10V, I_{OUT} = 10A.

The switching frequency selection is a trade-off between switching losses and solution size. High switching frequency generates high switching losses but may require fewer flying capacitors and output capacitors. In most applications, the best switching frequency is around 300kHz to 600kHz, therefore 500kHz is a good starting point. Select the flying capacitors so that the ripple voltage at the flying capacitor is around 100mV at the full-load condition (see Equation 1).

$$C_{FLY} = \frac{I_{OUT}}{2 \bullet f_{SW} \bullet C_{FLY\_RIPPLE}} = \frac{10A}{2 \bullet 500kHz \bullet 100mV} = 100\mu F \quad (1)$$

Considering the ceramic capacitance derating at 10V DC bias voltage, twelve 10µF/X7R capacitors are paralleled as the flying capacitors. The worst-case RMS current may be 40% higher than the maximum output current. The worst-case RMS current on each capacitor is 10A • 140%/12 = 1.17A. Double check and make sure the RMS current on each capacitor is below the ripple current ratings and temperature rise is below the limits.

The input/output capacitor selection is similar to the flying capacitor selection. More output capacitors result in smaller output voltage ripple and higher efficiency. Because of the lower RMS current, the output capacitor value can be much less than the flying capacitor. In general, start with half the number of the flying capacitors as the input/output capacitors. The input capacitors can be placed from V_{HIGH} to PGND or may be connected between V_{HIGH} and V_{LOW} to serve as input/output capacitors at the same time. However, the voltage rating of those capacitors must be selected based on the input voltage instead of the output voltage.

The design example is shown in Figure 3 in the Typical Applications section. By running experimental tests, the full-load efficiency is almost the same at 500kHz and 600kHz switching frequency. Tie FREQ pin to $INTV_{CC}$ for 600kHz operation. At 10A load, the V_{LOW} is 250mV to 300mV lower than $V_{HIGH}/2$, taking into account the ripple on the V_{LOW}, the HYS_PGRM pin is connected to $INTV_{CC}$ to program a 400mV hysteresis window.

TYPICAL APPLICATIONS

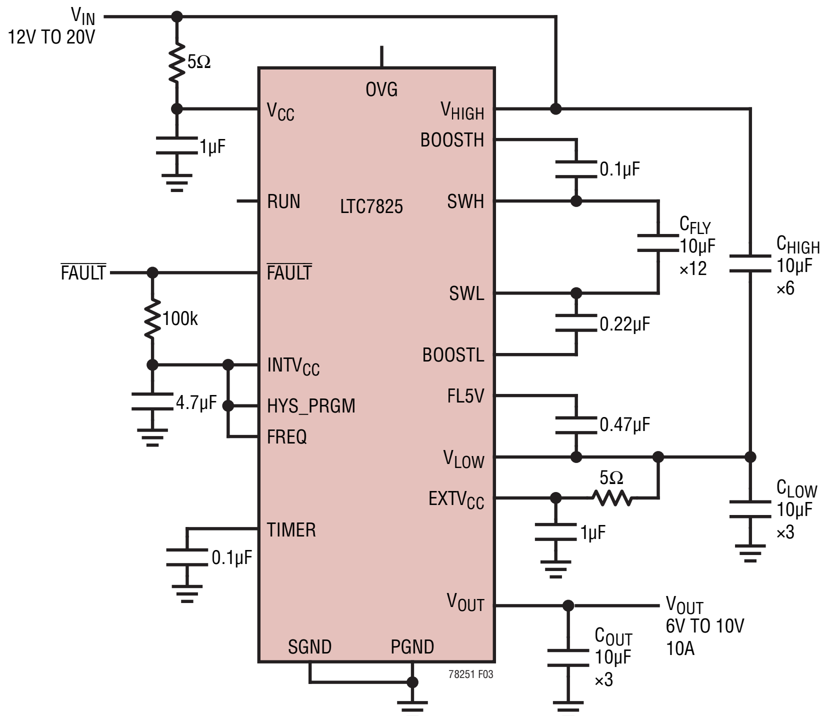


Figure 3. High Efficiency 20V/10A Voltage Divider at 600kHz Switching Frequency

TYPICAL APPLICATIONS

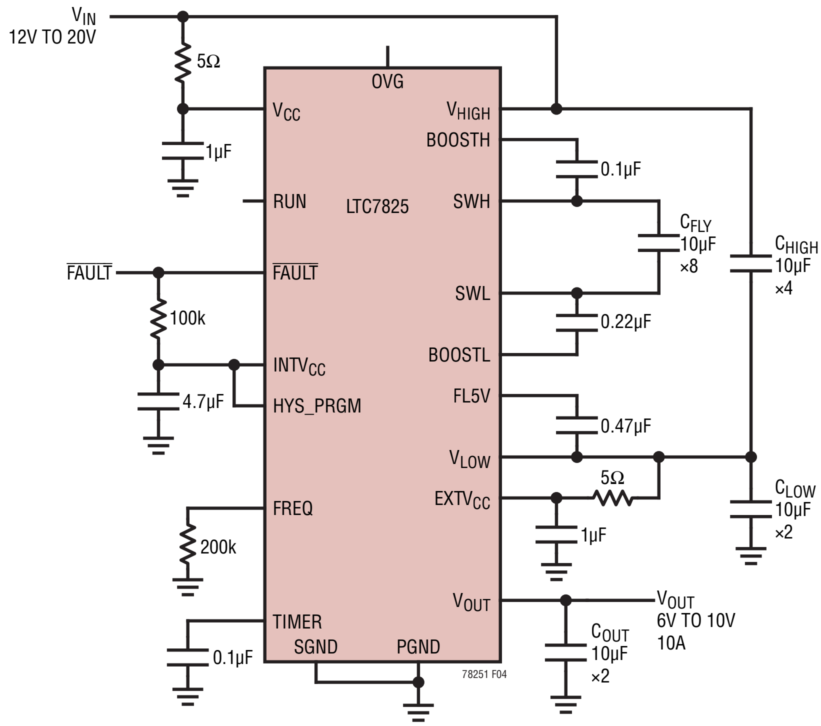
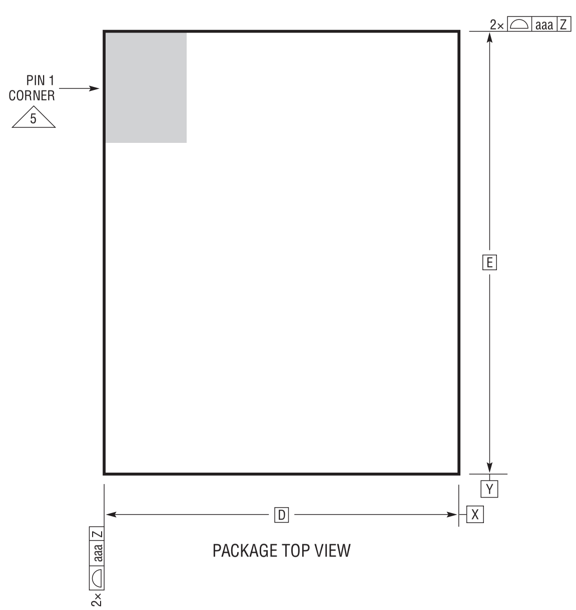
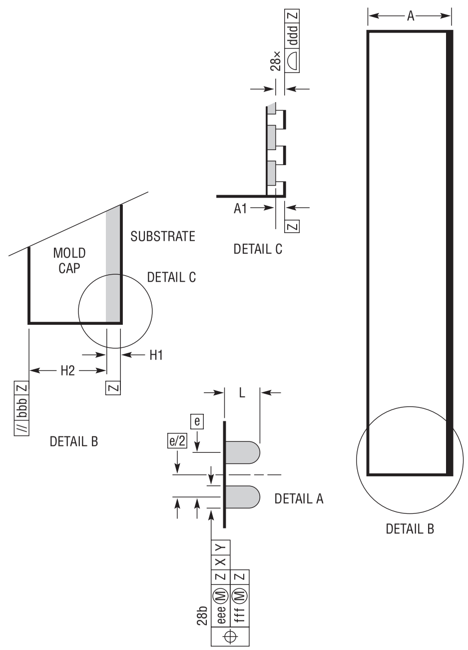


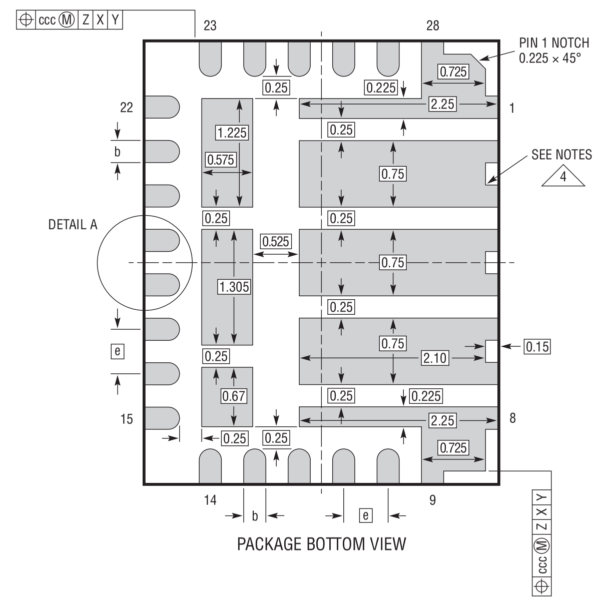
Figure 4. High Power Density 20V/10A Voltage Divider at 1MHz Switching Frequency

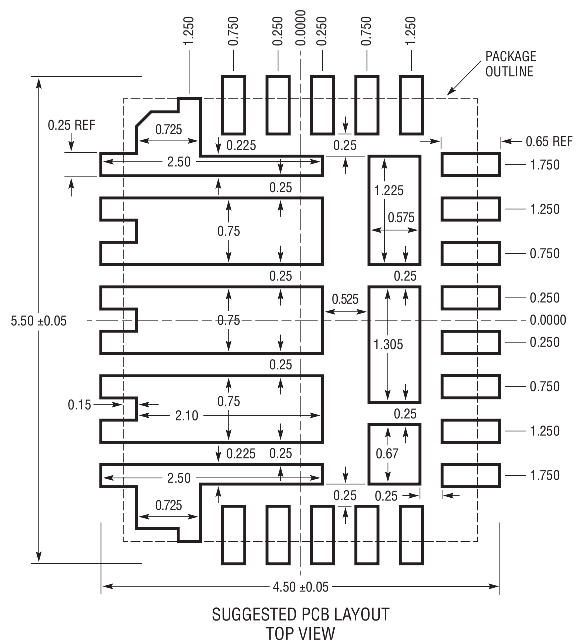
PACKAGE DESCRIPTION

LQFN Package
28-Lead (4mm × 5mm × 0.95mm)
(Reference LTC DWG # 05-08-7007 Rev Ø)



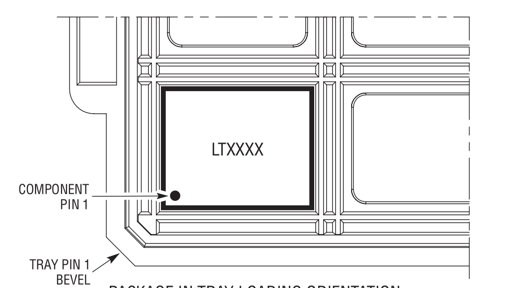






	DIMENSIONS			
SYMBOL	**MIN**	**NOM**	**MAX**	**NOTES**
A	0.85	0.95	1.05	
A1			0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		4.00		
E		5.00		
e		0.50		
H1		0.25 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE IS SEGMENTED AND ARRANGED IN A MATRIX FORMAT. IT MAY HAVE OPTIONAL CORNER RADII ON EACH SEGMENT



PACKAGE IN TRAY LOADING ORIENTATION

LQFN 28 0819 REV Ø

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/23	Updated Absolute Maximum Ratings (Operating Junction Temperature Range)	2

TYPICAL APPLICATION

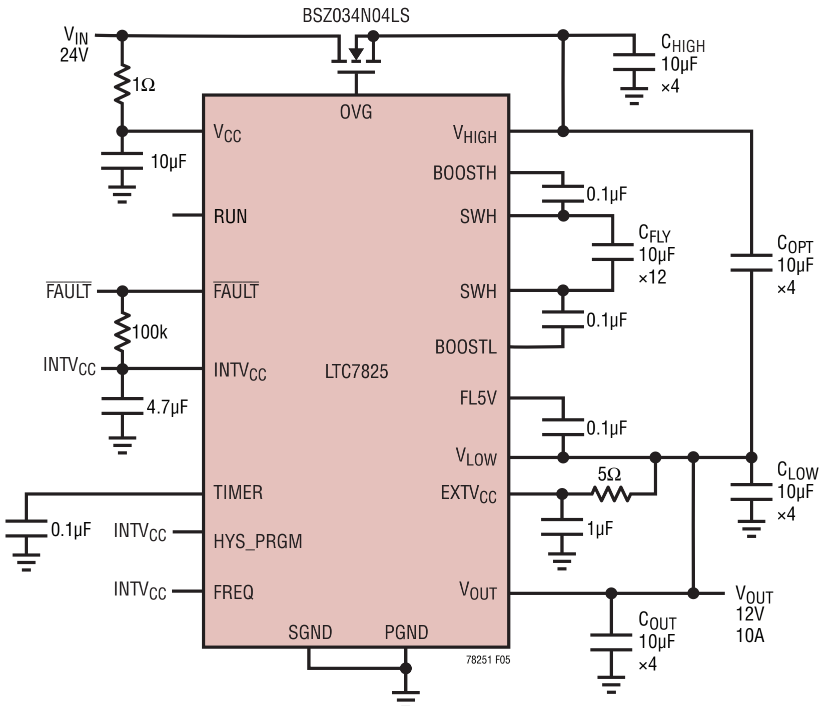


Figure 5. High Efficiency 24V to 12V, 10A Voltage Divider with Overvoltage MOSFET at Input

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7820	Fixed Ratio High Power Inductorless (Charge Pump)	$6V < V_{IN} \le 72V$, Fixed 50% Duty Cycle, 100kHz to 1MHz Switching Frequency, 4mm × 5mm UFD Package
LTC7821	80V, Hybrid Step-Down Synchronous Controller	$10V < V_{IN} \le 72V$, $0.8V < V_{OUT} \le V_{IN}/2$, 50kHz to 1.7MHz Switching Frequency, 5mm × 5mm UH Package
LTC3890/LTC3890-1/ LTC3890-2/LTC3890-3	60V Dual 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	$4V \le V_{IN} \le 60V$, $0.8V \le V_{OUT} \le 24V$, $I_Q = 50µA$, PLL Fixed Frequency 50kHz to 900kHz
LTC7801	150V Synchronous Step-Down DC/DC Controller	$4.5V \le V_{IN} \le 140V$, $150V_{P-P}$, $0.8V \le V_{OUT} \le 60V$, $I_Q = 40µA$, PLL Fixed Frequency 50kHz to 900kHz, 24-Lead 4mm × 5mm QFN or TSSOP
LTC3255	48V Fault Protected 50mA Step-Down Charge Pump	$4V \le V_{IN} \le 48V$, $2.4V \le V_{OUT} \le 12.5V$, $I_Q = 20µA$, 3mm × 3mm DFN-10, MSOP-10
LTC7802	40V Dual 3MHz 2-Phase Synchronous Step-Down Controller with Spread Spectrum	$4.5V \le V_{IN} \le 40V$, V_{OUT} Up to 40V, $I_Q = 12µA$, Fixed Frequency 100kHz to 3MHz, 16-Pin 3mm × 3mm QFN and MSOP
LTC7803	40V 3MHz Synchronous Step-Down Controller with Spread Spectrum	$4.5V \le V_{IN} \le 40V$, V_{OUT} Up to 40V, $I_Q = 12µA$, Fixed Frequency 100kHz to 3MHz, 4mm × 5mm QFN-28

10/23
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