

## Silicon Digital Attenuator, 1-Bit, 100 MHz to 30 GHz

### FEATURES

- ▶ Ultrawideband frequency range: 100 MHz to 30 GHz
- ▶ 16 dB single attenuation step
- ▶ Low insertion loss
  - ▶ 0.7 dB at 8 GHz
  - ▶ 0.9 dB at 18 GHz
  - ▶ 1.3 dB at 30 GHz
- ▶ Attenuation accuracy:  $\pm 0.20$  dB typical at up to 30 GHz
- ▶ High input linearity
  - ▶ P0.1dB insertion loss state: 33 dBm typical
  - ▶ P0.1dB 16 dB attenuation state: 30 dBm typical
  - ▶ IP3 insertion loss state: 51 dBm typical
  - ▶ IP3 16 dB attenuation state: 49 dBm typical
- ▶ High RF power handling
  - ▶ 30 dBm typical steady state average
  - ▶ 33 dBm typical steady state peak
- ▶ RF amplitude settling time (0.1 dB of final  $RF_{OUT}$ ): 110 ns typical
- ▶ Single-supply operation supported
- ▶ Tight distribution in relative phase
- ▶ No low frequency spurious signals
- ▶ CMOS-/LVTTTL-compatible
- ▶ 12-terminal, 2.25 mm x 2.25 mm, land grid array [LGA] package

### APPLICATIONS

- ▶ Industrial scanners
- ▶ Test and instrumentation
- ▶ Cellular infrastructure: 5G millimeter wave
- ▶ Military radios, radars, electronic counter measures (ECMs)
- ▶ Microwave radios and very small aperture terminals (VSATs)

### FUNCTIONAL BLOCK DIAGRAM

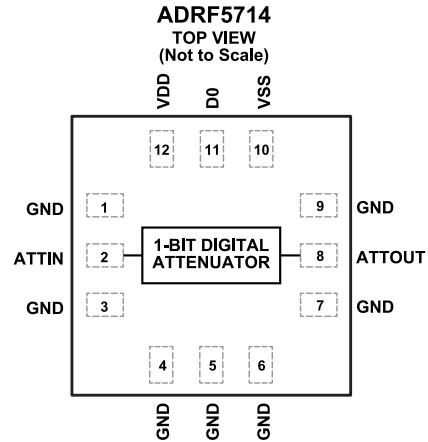


Figure 1. Functional Block Diagram

### GENERAL DESCRIPTION

The ADRF5714 is a silicon, 1-bit digital attenuator with 16 dB attenuation, which supports glitch-free operation.

This device operates from 100 MHz to 30 GHz with better than 1.3 dB of insertion loss and excellent attenuation accuracy. The ATTIN and ATTOUT port of the ADRF5714 has an RF input power handling capability of 30 dBm average and 33 dBm peak.

The ADRF5714 requires a dual-supply voltage of +3.3 V and -3.3 V. The device features CMOS-/low voltage transistor to transistor logic (LVTTTL)-compatible control.

The ADRF5714 can also operate with a single positive supply voltage ( $V_{DD}$ ) applied while the negative supply voltage ( $V_{SS}$ ) is tied to ground. See the [Theory of Operation](#) section for more details.

The ADRF5714 RF ports are designed to match a characteristic impedance of 50  $\Omega$ . The ADRF5714 comes in a [12-terminal, 2.25 mm x 2.25 mm, RoHS compliant, LGA package](#) and operates from -40°C to +105°C.

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**REVISION HISTORY****12/2023—Revision 0: Initial Version**

## SPECIFICATIONS

Positive supply voltage ( $V_{DD}$ ) = 3.3 V, negative supply voltage ( $V_{SS}$ ) = -3.3 V, control voltage ( $V_{CTRL}$ ) = 0 V or  $V_{DD}$ , and case temperature ( $T_{CASE}$ ) = 25°C with a 50  $\Omega$  system, unless otherwise noted.  $V_{CTRL}$  refers to the control voltage on the D0 pin.

Table 1. Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit	
FREQUENCY RANGE	f		100		30,000	MHz	
INSERTION LOSS		100 MHz to 8 GHz		0.7		dB	
		8 GHz to 18 GHz		0.9		dB	
		18 GHz to 30 GHz		1.3		dB	
RETURN LOSS		ATTIN and ATTOUT pins, attenuation state					
		100 MHz to 8 GHz		25		dB	
		8 GHz to 18 GHz		22		dB	
		18 GHz to 30 GHz		17		dB	
ATTENUATION		Between minimum and maximum attenuation states		16		dB	
		Between any successive attenuation states		16		dB	
		Referenced to insertion loss					
		100 MHz to 8 GHz		±0.10		dB	
		8 GHz to 18 GHz		±0.15		dB	
		18 GHz to 30 GHz		±0.20		dB	
RELATIVE PHASE		Referenced to insertion loss					
		100 MHz to 8 GHz		12		Degrees	
		8 GHz to 18 GHz		25		Degrees	
		18 GHz to 30 GHz		45		Degrees	
SWITCHING		All attenuation states at input power ( $P_{IN}$ ) = 10 dBm					
		Rise Time and Fall Time	$t_{RISE}, t_{FALL}$	10% to 90% of RF output ( $RF_{OUT}$ )	20		ns
		On Time and Off Time	$t_{ON}, t_{OFF}$	50% triggered control to 90% of $RF_{OUT}$	50		ns
		RF Amplitude Settling Time					
		0.1 dB		50% triggered control to 0.1 dB of final $RF_{OUT}$	110		ns
0.05 dB		50% triggered control to 0.05 dB of final $RF_{OUT}$	140		ns		
RF Phase Settling Time		f = 1 GHz					
1°		50% triggered control to 1° of final $RF_{OUT}$	65			ns	
INPUT LINEARITY <sup>1</sup>	P0.1dB	100 MHz to 30 GHz					
		0.1 dB Power Compression					
		Insertion Loss State			33		dBm
		16 dB Attenuation State			30		dBm
		Third-Order Intercept	IP3	Two-tone $P_{IN}$ = 20 dBm per tone, $\Delta f$ = 1 MHz, all attenuation states			
Insertion Loss State				51		dBm	
16 dB Attenuation State				49		dBm	
DIGITAL CONTROL INPUT		D0 pin					
		Voltage					
		Low	$V_{INL}$		0	0.8	V
		High	$V_{INH}$		1.2	3.3	V
		Current					
		Low	$I_{INL}$			-33	$\mu A$
High	$I_{INH}$			<1	$\mu A$		

## SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>SUPPLY CURRENT</b>						
Positive Supply Current		VDD and VSS pins				
D0 = 0 V				150		μA
D0 = 3.3 V				120		μA
Negative Supply Current				500		μA
<b>RECOMMENDED OPERATING CONDITIONS</b>						
Supply Voltage						
Positive	V <sub>DD</sub>		3.15		3.45	V
Negative	V <sub>SS</sub>		-3.45		-3.15	V
Digital Control Voltage			0		V <sub>DD</sub>	V
RF Power Handling <sup>2</sup>		f = 100 MHz to 30 GHz, T <sub>CASE</sub> = 85°C <sup>3</sup>				
Input at ATTIN or ATTOUT		Steady state average		30		dBm
		Steady state peak		33		dBm
		Hot switching		30		dBm
Case Temperature	T <sub>CASE</sub>		-40		+105	°C

<sup>1</sup> Input linearity performance degrades over frequency, see [Figure 15](#) to [Figure 18](#).

<sup>2</sup> For power derating over frequency, see [Figure 2](#) and [Figure 3](#). Applicable for all ATTIN and ATTOUT power specifications.

<sup>3</sup> For 105°C operation, the power handling degrades from the T<sub>CASE</sub> = 85°C specifications by 3 dB.

## SPECIFICATIONS

## SINGLE-SUPPLY OPERATION

$V_{DD} = 3.3\text{ V}$ ,  $V_{SS} = -3.3\text{ V}$ ,  $V_{CTRL} = 0\text{ V}$  or  $V_{DD}$ , and  $T_{CASE} = 25^\circ\text{C}$  with a  $50\ \Omega$  system, unless otherwise noted. The small signal and bias characteristics are maintained for the single-supply operation.

Table 2. Single-Supply Operation Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		100		30,000	MHz
SWITCHING		All attenuation states at $P_{IN} = 10\text{ dBm}$				
Rise Time and Fall Time	$t_{RISE}, t_{FALL}$	10% to 90% of $RF_{OUT}$		130		ns
On Time and Off Time	$t_{ON}, t_{OFF}$	50% triggered control to 90% of $RF_{OUT}$		150		ns
RF Amplitude Settling Time						
0.1 dB		50% triggered control to 0.1 dB of final $RF_{OUT}$		350		ns
0.05 dB		50% triggered control to 0.05 dB of final $RF_{OUT}$		400		ns
RF Phase Settling Time		f = 1 GHz				
1°		50% triggered control to 1° of final $RF_{OUT}$		165		ns
INPUT LINEARITY		100 MHz to 30 GHz				
0.1 dB Power Compression	P0.1dB			21		dBm
Insertion Loss State				19		dBm
16 dB Attenuation State						
Third-Order Intercept	IP3	Two-tone $P_{IN} = 20\text{ dBm}$ per tone, $\Delta f = 1\text{ MHz}$ , all attenuation states				
Insertion Loss State				37		dBm
16 dB Attenuation State				42		dBm
RECOMMENDED OPERATING CONDITIONS						
RF Power Handling		f = 100 MHz to 30 GHz, $T_{CASE} = 85^\circ\text{C}$				
Input at ATTIN and ATTOUT						
Average				19		dBm
Peak				19		dBm
Hot Switching				19		dBm
Case Temperature	$T_{CASE}$		-40		+105	°C

**ABSOLUTE MAXIMUM RATINGS**

For recommended operating conditions, see [Table 1](#) and [Table 2](#).

**Table 3. Absolute Maximum Ratings**

Parameter	Rating
V <sub>DD</sub>	-0.3 V to +3.6 V
V <sub>SS</sub>	-3.6 V to +0.3 V
Digital Control Inputs	
Voltage	-0.3 V to V <sub>DD</sub> + 0.3 V
Current	3 mA
RF Input Power <sup>1</sup>	
Dual Supply (V <sub>DD</sub> = 3.3 V, V <sub>SS</sub> = -3.3 V, f = 100 MHz to 30 GHz, T <sub>CASE</sub> = 85°C <sup>2</sup> )	
Average	31 dBm
Peak	34 dBm
Hot Switching	31 dBm
Single Supply (V <sub>DD</sub> = 3.3 V, V <sub>SS</sub> = 0 V, f = 100 MHz to 30 GHz, T <sub>CASE</sub> = 85°C <sup>2</sup> )	
Average	20 dBm
Peak	20 dBm
Hot Switching	20 dBm
Unbiased Condition (V <sub>DD</sub> , V <sub>SS</sub> = 0 V)	15 dBm
Temperature	
Junction (T <sub>J</sub> )	135°C
Storage	-65°C to +150°C
Reflow	260°C

- <sup>1</sup> For power derating over frequency, see [Figure 2](#) and [Figure 3](#). Applicable for all ATTIN and ATTOUT power specifications.
- <sup>2</sup> For 105°C operation, the power handling degrades from the T<sub>CASE</sub> = 85°C specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

**THERMAL RESISTANCE**

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

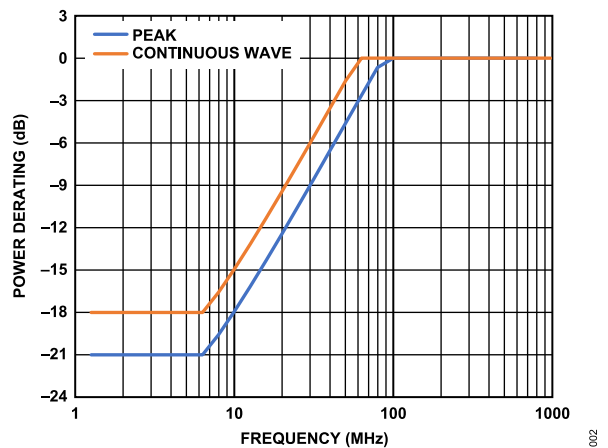
θ<sub>JC</sub> is the junction to case bottom (channel to package bottom) thermal resistance.

**Table 4. Thermal Resistance**

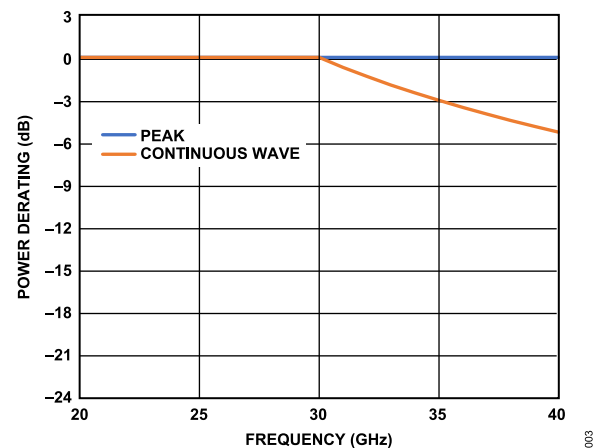
Package Type	θ <sub>JC</sub> <sup>1</sup>	Unit
CC-12-6	50	°C/W

- <sup>1</sup> θ<sub>JC</sub> was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

**POWER DERATING CURVES**



**Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T<sub>CASE</sub> = 85°C**



**Figure 3. Power Derating vs. Frequency, High Frequency Detail, T<sub>CASE</sub> = 85°C**

**ABSOLUTE MAXIMUM RATINGS****ELECTROSTATIC DISCHARGE (ESD) RATINGS**

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

**ESD Ratings for ADRF5714**

*Table 5. ADRF5714, 12-Terminal LGA*

ESD Model	Withstand Threshold (V)	Class
HBM		
ATTIN and ATTOUT Pins	1000	1C
Supply and Control Pins	2000	2
CDM	500	C2A

**ESD CAUTION**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

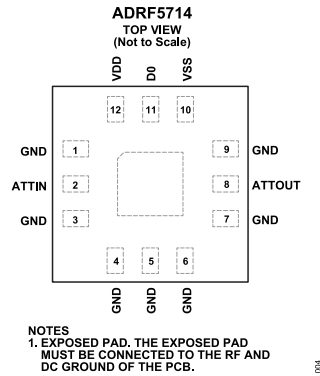


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3 to 7, 9	GND	Ground. The GND pins must be connected to the RF and DC ground of the PCB.
2	ATTIN	Attenuator Input. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See <a href="#">Figure 5</a> for the interface schematic.
8	ATTOUT	Attenuator Output. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See <a href="#">Figure 5</a> for the interface schematic.
10	VSS	Negative Supply Input. See <a href="#">Figure 8</a> for the interface schematic.
11	D0	Control Input for 16 dB Attenuation Bit. See the <a href="#">Theory of Operation</a> section for more information. See <a href="#">Figure 6</a> for the interface schematic.
12	VDD	Positive Supply Input. See <a href="#">Figure 7</a> for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and DC ground of the PCB.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

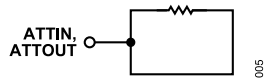


Figure 5. ATTIN and ATTOU Interface Schematic

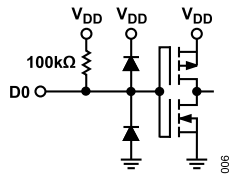


Figure 6. D0 Interface Schematic

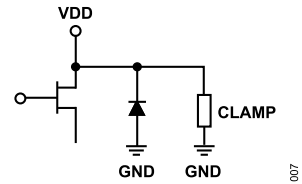


Figure 7. VDD Interface Schematic

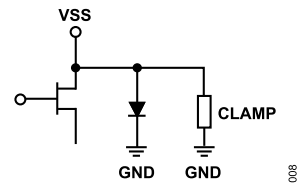


Figure 8. VSS Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

$V_{DD} = 3.3\text{ V}$ ,  $V_{SS} = -3.3\text{ V}$ ,  $V_{CTRL} = 0\text{ V}$  or  $V_{DD}$ , and  $T_{CASE} = 25^\circ\text{C}$ , with a  $50\ \Omega$  system, unless otherwise noted.

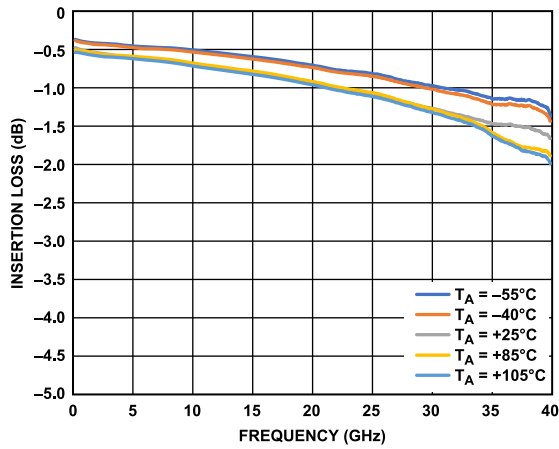


Figure 9. Insertion Loss vs. Frequency over Temperature

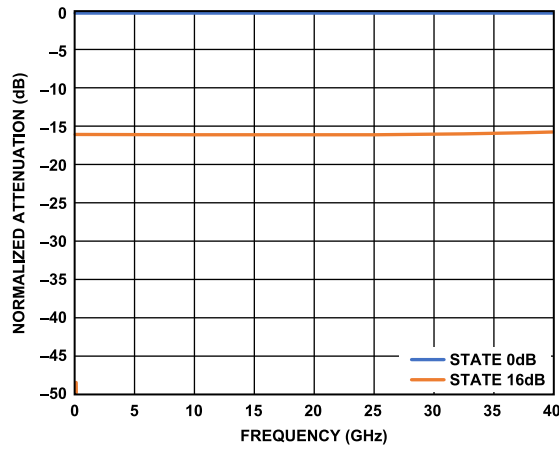


Figure 12. Normalized Attenuation vs. Frequency for All States

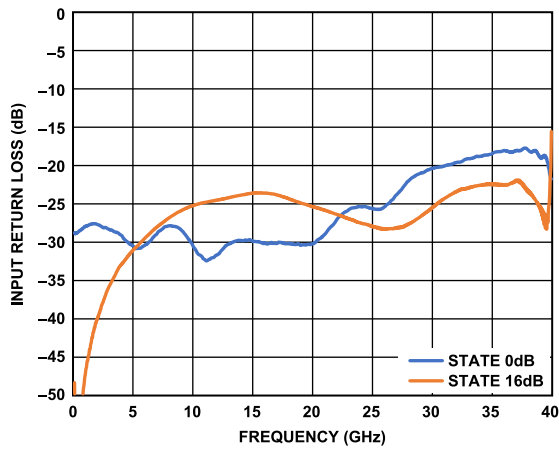


Figure 10. Input Return Loss vs. Frequency

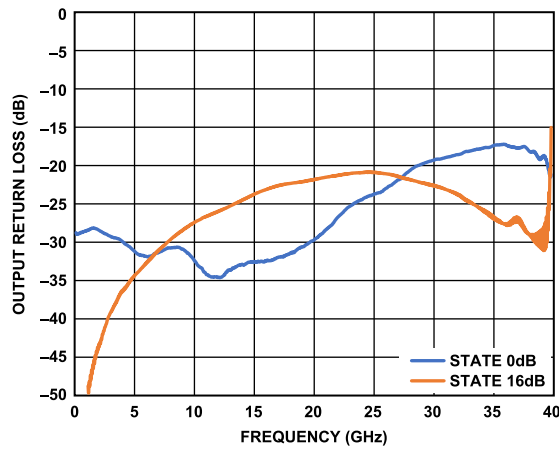


Figure 13. Output Return Loss vs. Frequency

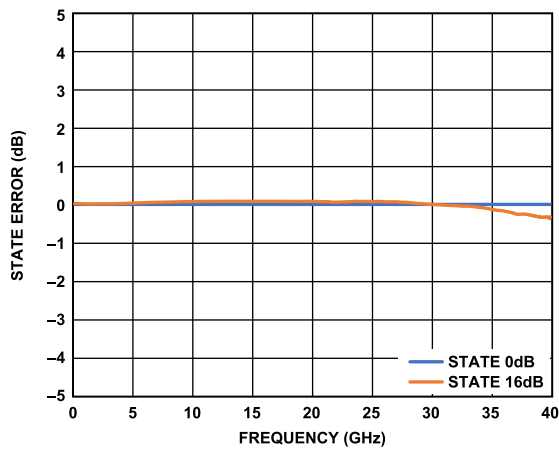


Figure 11. State Error vs. Frequency

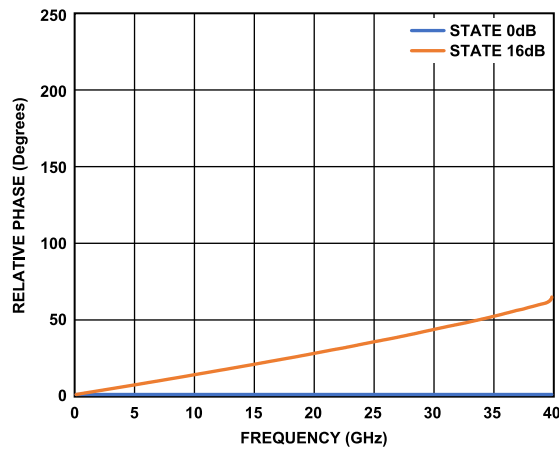


Figure 14. Relative Phase vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

$V_{DD} = 3.3\text{ V}$ ,  $V_{SS} = -3.3\text{ V}$ ,  $V_{CTRL} = 0\text{ V}$  or  $V_{DD}$ , and  $T_{CASE} = 25^\circ\text{C}$  with a  $50\ \Omega$  system, unless otherwise noted.

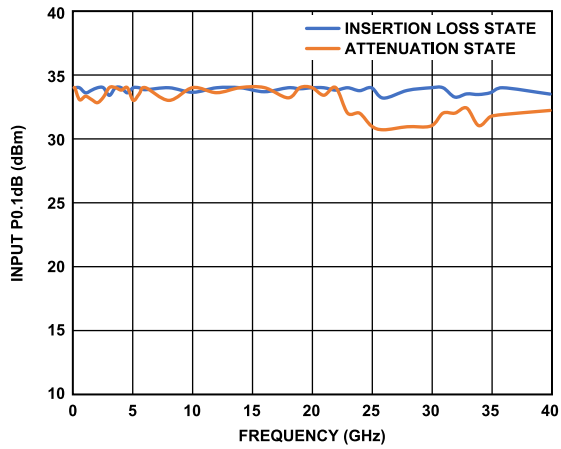


Figure 15. Input P0.1dB vs. Frequency

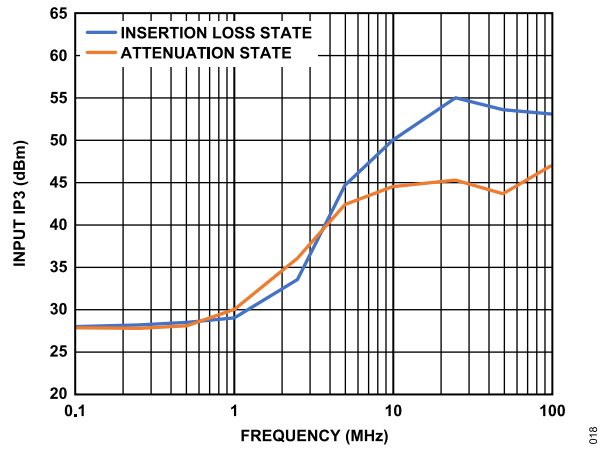


Figure 18. Input IP3 vs. Frequency, Low Frequency Detail

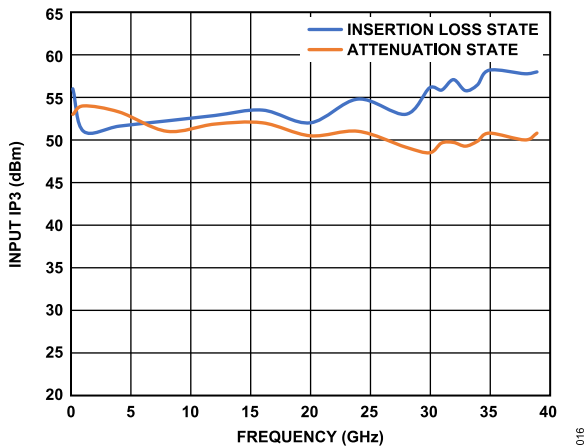


Figure 16. Input IP3 vs. Frequency

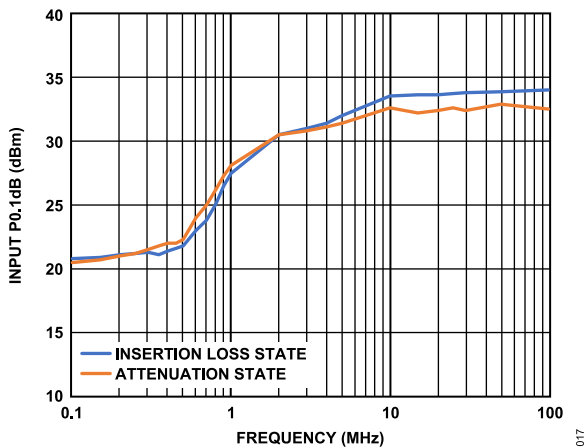


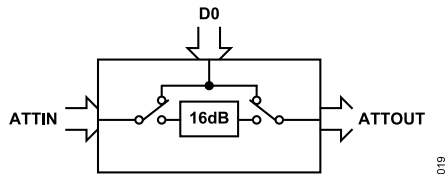
Figure 17. Input P0.1dB vs. Frequency, Low Frequency Detail

## THEORY OF OPERATION

The ADRF5714 incorporates a 1-bit attenuator that offers an attenuation range of 16 dB. The ADRF5714 has a digital control input, D0, to select the desired state, as shown in Figure 19. See Table 7 for the truth table.

**Table 7. Truth Table**

Digital Control Input (D0)	Attenuation State (dB)
Low	0 (reference)
High	16



**Figure 19. Simplified Circuit Diagram**

## RF INPUT AND OUTPUT

Both RF ports (ATTIN and ATTOUT) are DC-coupled to 0 V. No DC blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50  $\Omega$ . Therefore, external matching components are not required.

The ADRF5714 supports bidirectional operation at the same power level. The power handling of the ATTIN and ATTOUT ports are the same. Refer to the RF input power specifications in Table 1.

The ADRF5714 can operate with a single positive supply voltage applied to the VDD pin, and the VSS pin connected to ground. However, some performance degradations can occur in the input compression and input third-order intercept (see Table 2).

## POWER SUPPLY

The ADRF5714 requires a positive supply voltage applied to the VDD pin, and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Apply the digital control input. However, powering the digital control input before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 k $\Omega$  resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller output is in a high impedance state after VDD is powered up and the control pin is not driven to a valid logic state.
4. Apply an RF input signal to ATTIN or ATTOUT.

The ideal power-down sequence is the reverse order of the power-up sequence.

**APPLICATIONS INFORMATION**

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a trace width of 16 mil and ground clearance of 6 mil to have a characteristic impedance of 50 Ω. For optimal RF and thermal grounding, as many through vias as possible are arranged around transmission lines and under the exposed pad of the package.

The RF input and output ports (ATTIN and ATTOUT) are connected through 50 Ω transmission lines. On the VDD and VSS supply traces, a 100 pF bypass capacitor filters high frequency noise.

Figure 20 shows the simplified application circuit for the ADRF5714.

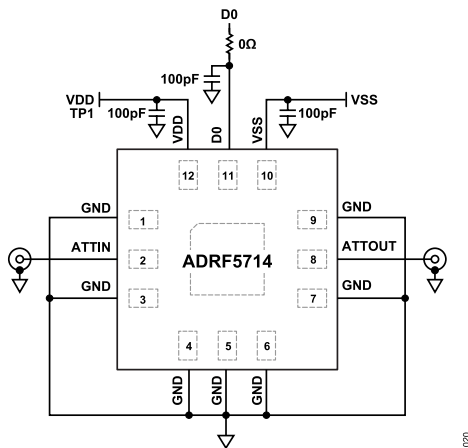


Figure 20. Simplified Application Circuit

**RECOMMENDATIONS FOR PCB DESIGN**

The RF ports are matched to 50 Ω internally, and the pinout is designed to mate a CPWG with a 50 Ω characteristic impedance on the PCB. Figure 21 shows the referenced CPWG RF trace design for an RF substrate with 12 mil thick Rogers RO4003 dielectric material. The RF trace with a 16 mil width and a 6 mil clearance is recommended for 2.2 mil finished copper thickness.

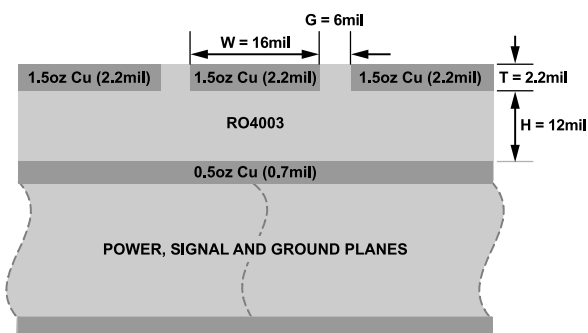


Figure 21. Example PCB Stackup

Figure 22 shows the routing of the RF traces, supply, and control signals from the ADRF5714. The ground planes are connected with as many filled through vias as allowed for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

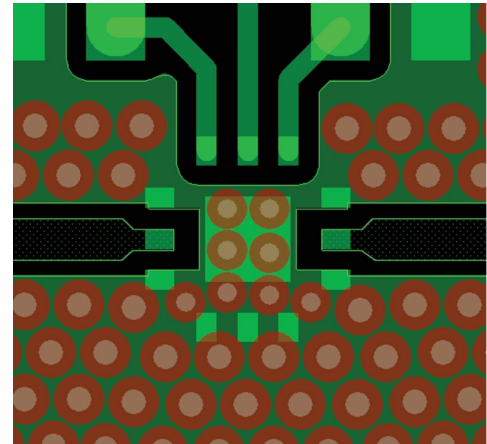


Figure 22. PCB Routs

Figure 23 shows the recommended layout from the ATTIN and ATTOUT pins of the ADRF5714 to the 50 Ω CPWG on the referenced stackup. PCB pads are drawn 1:1 to device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same 2 mil width and tapered with a 90° angle. The paste mask is also designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

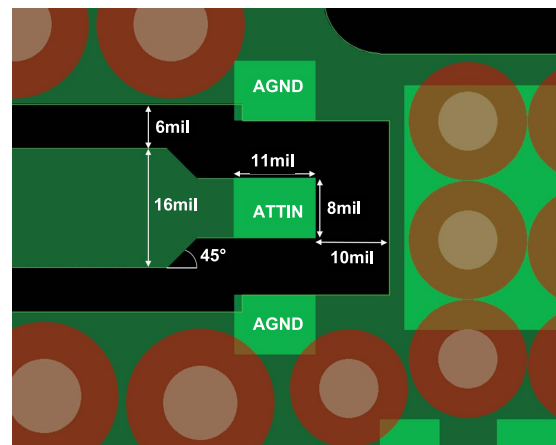


Figure 23. Recommended ATTIN Pin and ATTOUT Pin Transitions

For alternate PCB stackups with different dielectric thickness and CPWG design, contact [Analog Devices, Inc., Technical Support Request](http://analog.com) for further recommendations.

OUTLINE DIMENSIONS

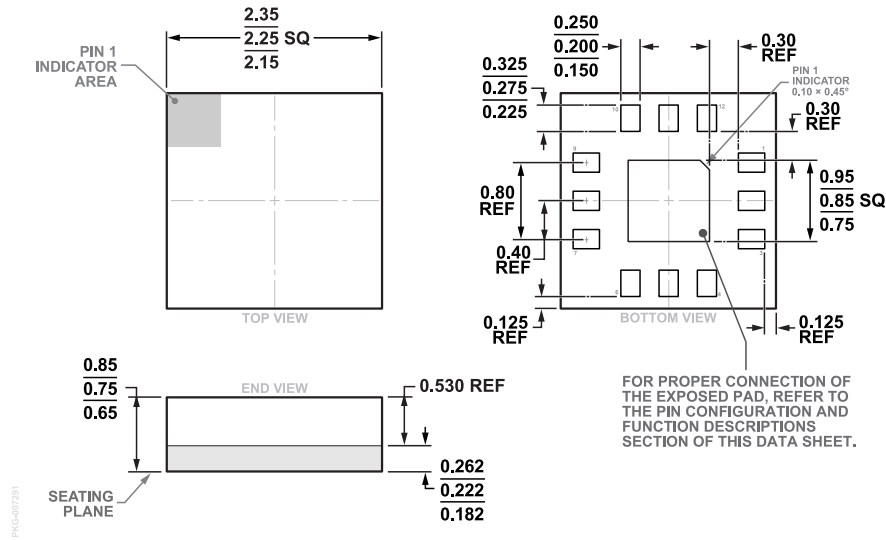


Figure 24. 12-Terminal Land Grid Array [LGA]  
(CC-12-6)  
Dimensions shown in millimeters

Updated: September 15, 2023

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Packing Quantity	Package Option
ADRF5714BCCZN	-40°C to +105°C	12-Terminal Land Grid Array [LGA]	Reel, 500	CC-12-6
ADRF5714BCCZN-R7	-40°C to +105°C	12-Terminal Land Grid Array [LGA]	Reel, 500	CC-12-6

<sup>1</sup> Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 8. Evaluation Boards

Model <sup>1</sup>	Description
ADRF5714-EVALZ	Evaluation Board

<sup>1</sup> Z = RoHS-Compliant Part.