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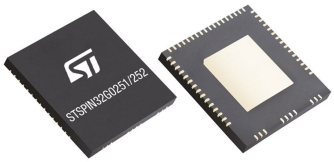
# STSPIN32G0252

Datasheet

## 250 V three-phase BLDC controller with embedded STM32 MCU



QFN 10x10 72L pitch 0.5

STSPIN

| Product status link |
| --- |
| STSPIN32G0252 |

| Product label |
| --- |
| SUSTAINABLE TECHNOLOGY |

## Features

- Three-phase gate drivers
  - High-voltage rail up to 250 V
  - dV/dt transient immunity ±50 V/ns
  - Gate driving voltage range from 9 V to 20 V
- Driver current capability:
  - 1.00/0.85 A source/sink current @ 25 °C
- 32-bit ARM® Cortex®-M0+ MCU core:
  - Up to 64 MHz clock frequency
  - 8-Kbyte SRAM with hardware parity check
  - 64-Kbyte flash memory with protection and securable area
  - CRC calculation unit
- Up to 32 general-purpose I/O ports (GPIO)
- 1 advanced timer for motor control, 16-bit with up to 6 x PWM channels
- 5 general-purpose timers (1x 32-bit)
- 2 low-power timers
- 12-bit ADC converter (up to 15 channels) with 2 MSps conversion rate
- 5-channel DMA controller with flexible mapping
- Internal high precision voltage reference
- Full set of interfaces: 2x $I^2C$, 2x SPI, 3x UART and 1x low-power UART
- Matched propagation delay for all channels
- Integrated bootstrap diodes
- Comparator for fast overcurrent protection
- UVLO, interlocking, and deadtime functions
- Smart shutdown (smartSD) function
- Standby mode for low power consumption
- On-chip debug support via SWD
- Extended temperature range: -40 to +125 °C
- QFN 10x10 72L pitch 0.5 creepage 1.8 mm package

## Applications

- Three-phase motor drivers
- Inverters
- Industrial appliances and fans

# 1 Description

The STSPIN32G0252 is a system-in-package providing an integrated solution suitable for driving three-phase applications.

It embeds an MCU (STM32G031x8x3) featuring an Arm 32-bit Cortex®-M0+ CPU and a 250 V triple half-bridge gate driver, able to drive N-channel power MOSFETs or IGBTs.

A comparator featuring an advanced smartSD function is integrated in the device, ensuring fast and effective protection against overload and overcurrent.

The high-voltage bootstrap diodes are also integrated, as well as anti cross-conduction (interlocking), deadtime, and UVLO protection on both the lower and upper driving sections, which prevents the power switches from operating in low efficiency or dangerous conditions. Matched delays between low and high-side sections guarantee no cycle distortion.

The integrated MCU is based on the high-performance 32-bit Arm Cortex®-M0+ core, operating at a frequency up to 64 MHz and featuring a memory protection unit (MPU), which enhances the application's security.

This microcontroller represents the perfect choice for advanced motor control applications thanks to the comprehensive set of features such as the 12-bit ADC, an internal voltage reference buffer, one general-purpose 32-bit timer, one 16-bit PWM timer dedicated to motor control, four general-purpose 16-bit timers, two 16-bit low-power timers, a 5-channel DMA that performs data transfers between memory-mapped peripherals and/or memories to offload the CPU.

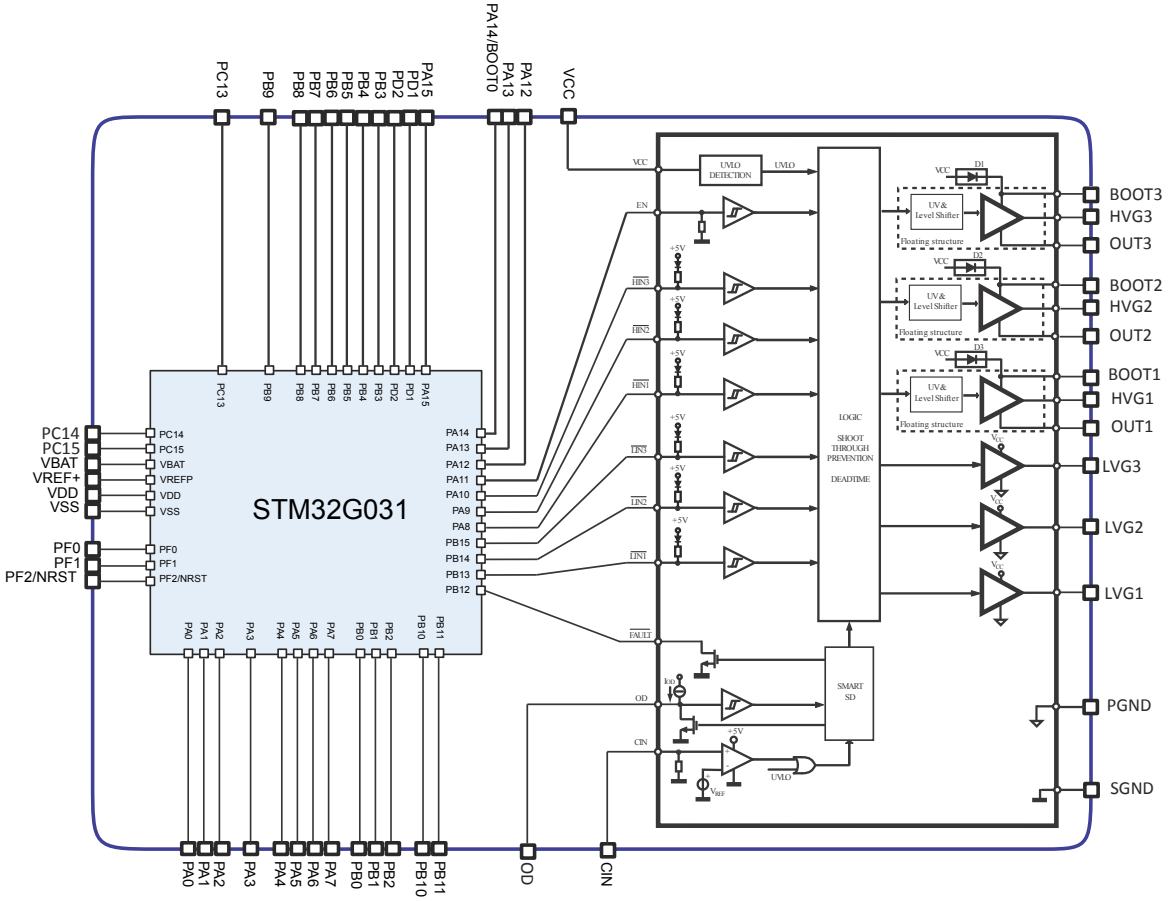
It also embeds high-speed memories (64 KB of flash memory, and 8 KB of SRAM) with several protection mechanisms, up to 32 available GPIOs, main interfaces ($I^2C$, SPI, and UART), a comprehensive set of power-saving modes, and an analog independent supply input for ADC.

Such a feature-rich microcontroller allows running sensorless or sensored Field Oriented Control (FOC) with one, two or three shunts or a more traditional six-step control mode.

The STSPIN32G0252 also features a full set of protections and an extended temperature range (-40 °C to +125 °C), guaranteeing stable operation even in the most demanding industrial applications. An SWD interface is provided for microcontroller firmware programming and debugging.

# 2 Block diagram

Figure 1. **STSPIN32G0252 SiP block diagram**



# 3 Pin description and connection diagram

Figure 2. **STSPIN32G0252 pin connection (top view)**

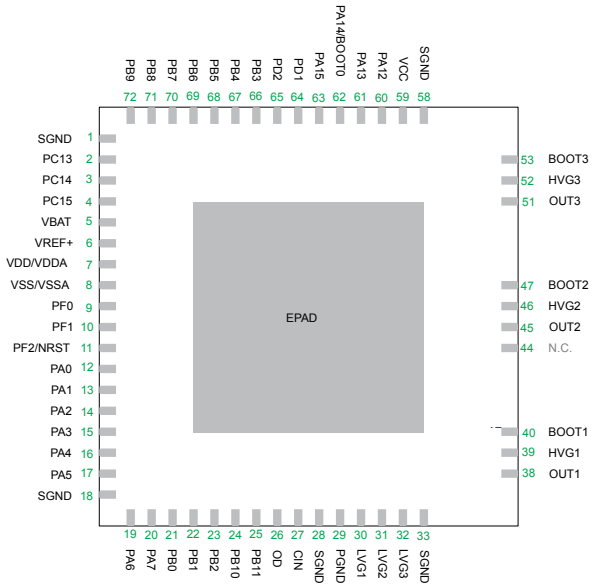



Table 1. **Legend/abbreviations used in the pin description table**

| Name | | Symbol | Definition |
|---|---|---|---|
| Pin name | | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | | AO | Gate driver analog output |
| | | P | Gate driver supply\GND pin |
| | | S | Supply pin |
| | | I | Input-only pin |
| | | I/O | Input / output pin |
| I/O structure | | FT | 5 V-tolerant I/O |
| | | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| | | FT_a | I/O, with analog switch function |
| | | FT_f | I/O, Fm+ capable |
| | | FT_e | I/O, with switchable diode to VDD |
| Notes | | Unless otherwise specified, all I/Os are set as floating inputs during and after reset | |
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers | |
| | Additional functions | Functions directly selected/enabled through peripheral registers | |

**Table 2. Pin description**

| Pin N. | Name | Type | MCU | Driver | Function |
|---|---|---|---|---|---|
| 1 | SGND | P | | Y | Driver signal ground |
| 2 | PC13 | I/O - FT | Y | | TIM1_BK, TAMP_IN1, RTC_TS, RTC_OUT1, WKUP2 |
| 3 | PC14 | I/O - FT | Y | | TIM1_BK2, OSC32_IN |
| 4 | PC15 | I/O - FT | Y | | OSC32_EN, OSC_EN, OSC32_OUT |
| 5 | VBAT | S | Y | | VBAT |
| 6 | VREF+ | S | Y | | VREF_OUT |
| 7 | VDD/VDDA | S | Y | | |
| 8 | VSS/VSSA | S | Y | | |
| 9 | PF0 | I/O - FT | Y | | TIM14_CH1, OSC_IN |
| 10 | PF1 | I/O - FT | Y | | OSC_EN, OSC_OUT |
| 11 | PF2/NRST | I/O | Y | | MCO, NRST (default functionality) |
| 12 | PA0 | I/O - FT_a | Y | | SPI2_SCK, USART2_CTS, TIM2_CH1_ETR, LPTIM1_OUT, ADC_IN0, TAMP_IN2, WKUP1 |
| 13 | PA1 | I/O - FT_ea | Y | | SPI1_SCK/I2S1_CK, USART2_RTS_DE_CK, TIM2_CH2, I2C1_SMBA, EVENTOUT, ADC_IN1 |
| 14 | PA2 | I/O - FT_a | Y | | SPI1_MOSI/I2S1_SD, USART2_TX, TIM2_CH3, LPUART1_TX, ADC_IN2, WKUP4, LSCO |
| 15 | PA3 | I/O - FT_ea | Y | | SPI2_MISO, USART2_RX, TIM2_CH4, LPUART1_RX, EVENTOUT, ADC_IN3 |
| 16 | PA4 | I/O - FT_a | Y | | SPI1_NSS/I2S1_WS, SPI2_MOSI, TIM14_CH1, LPTIM2_OUT, EVENTOUT, ADC_IN4, RTC_OUT2 |
| 17 | PA5 | I/O - FT_ea | Y | | SPI1_SCK/I2S1_CK, TIM2_CH1_ETR, LPTIM2_ETR, EVENTOUT, ADC_IN5 |
| 18 | SGND | P | | Y | Driver signal ground |
| 19 | PA6 | I/O - FT_ea | Y | | SPI1_MISO/I2S1_MCK, TIM3_CH1, TIM1_BK, TIM16_CH1, LPUART1_CTS, ADC_IN6 |
| 20 | PA7 | I/O - FT_a | Y | | SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM1_CH1N, TIM14_CH1, TIM17_CH1, ADC_IN7 |
| 21 | PB0 | I/O - FT_ea | Y | | SPI1_NSS/I2S1_WS, TIM3_CH3, TIM1_CH2N, LPTIM1_OUT, ADC_IN8 |
| 22 | PB1 | I/O - FT_ea | Y | | TIM14_CH1, TIM3_CH4, TIM1_CH3N, LPTIM2_IN1, LPUART1_RTS_DE, EVENTOUT, ADC_IN9 |
| 23 | PB2 | I/O - FT_ea | Y | | SPI2_MISO, LPTIM1_OUT, EVENTOUT, ADC_IN10 |
| 24 | PB10 | I/O - FT_fa | Y | | LPUART1_RX, TIM2_CH3, SPI2_SCK, I2C2_SCL, ADC_IN11 |
| 25 | PB11 | I/O - FT_fa | Y | | SPI2_MOSI, LPUART1_TX, TIM2_CH4, I2C2_SDA, ADC_IN15 |
| 26 | OD | AO | | Y | Open drain comparator output |
| 27 | CIN | I | | Y | Comparator positive input |
| 28 | SGND | P | | Y | Driver signal ground |
| 29 | PGND | P | | Y | Driver power ground |
| 30 | LVG1 (1) | AO | | Y | Phase 1 low-side driver output |
| 31 | LVG2 (1) | AO | | Y | Phase 2 low-side driver output |
| 32 | LVG3 (1) | AO | | Y | Phase 3 low-side driver output |
| 33 | SGND | P | | Y | Driver signal ground |
| 38 | OUT1 | P | | Y | Phase 1 high-side (floating) common voltage |

| Pin N. | Name | Type | MCU | Driver | Function |
|---|---|---|---|---|---|
| 39 | HVG1 (1) | AO | | Y | Phase 1 high-side driver output |
| 40 | BOOT1 | P | | Y | Phase 1 bootstrap supply voltage |
| 44 | NC | | | | Not connected |
| 45 | OUT2 | P | | Y | Phase 2 high-side (floating) common voltage |
| 46 | HVG2 (1) | AO | | Y | Phase 2 high-side driver output |
| 47 | BOOT2 | P | | Y | Phase 2 bootstrap supply voltage |
| 51 | OUT3 | P | | Y | Phase 3 high-side (floating) common voltage |
| 52 | HVG3 (1) | AO | | Y | Phase 3 high-side driver output |
| 53 | BOOT3 | P | | Y | Phase 3 bootstrap supply voltage |
| 58 | SGND | P | | Y | Driver signal ground |
| 59 | VCC | P | | Y | Driver power supply |
| 60 | PA12 | I/O - FT_f | Y | | SPI1_MOSI/I2S1_SD, USART1_RTS_DE_CK, TIM1_ETR, I2S_CKIN, I2C2_SDA |
| 61 | PA13 | I/O - FT_ea | Y | | SWDIO, IR_OUT, EVENTOUT, ADC_IN17 |
| 62 | PA14/BOOT0 | I/O - FT_a | Y | | SWCLK, USART2_TX, EVENTOUT, ADC_IN18, BOOT0 |
| 63 | PA15 | I/O - FT | Y | | SPI1_NSS/I2S1_WS, USART2_RX, TIM2_CH1_ETR, EVENTOUT |
| 64 | PD1 | I/O - FT | Y | | EVENTOUT, SPI2_SCK, TIM17_CH1 |
| 65 | PD2 | I/O - FT | Y | | TIM3_ETR, TIM1_CH1N |
| 66 | PB3 | I/O - FT | Y | | SPI1_SCK/I2S1_CK, TIM1_CH2, TIM2_CH2, USART1_RTS_DE_CK, EVENTOUT |
| 67 | PB4 | I/O - FT | Y | | SPI1_MISO/I2S1_MCK, TIM3_CH1, USART1_CTS, TIM17_BK, EVENTOUT |
| 68 | PB5 | I/O - FT | Y | | SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM16_BK, LPTIM1_IN1, I2C1_SMBA, WKUP6 |
| 69 | PB6 | I/O - FT_f | Y | | USART1_TX, TIM1_CH3, TIM16_CH1N, SPI2_MISO, LPTIM1_ETR, I2C1_SCL, EVENTOUT |
| 70 | PB7 | I/O - FT_f | Y | | USART1 _RX, SPI2_MOSI, TIM17_CH1N, LPTIM1_IN2, I2C1_SDA, EVENTOUT, PVD_IN |
| 71 | PB8 | I/O - FT_f | Y | | SPI2_SCK, TIM16_CH1, I2C1_SCL, EVENTOUT |
| 72 | PB9 | I/O - FT_f | Y | | IR_OUT, TIM17_CH1, SPI2_NSS, I2C1_SDA, EVENTOUT |
| - | EPAD | P | | Y | Exposed pad, internally connected to SGND |

1. *The circuit guarantees less than 1 V on the LVG and HVG pins (at $I_{sink}$ = 10 mA), with VCC > 3 V. This allows omitting the "bleeder" resistor connected between the gate and the source of the external MOSFETs normally used to hold the pin low. When the EN is set low, gate driver outputs are forced low and assure low impedance.*

**Table 3. STSPIN32G0252 MCU-Driver internal connections**

| MCU pad | Type | Controller pad | Function |
|---|---|---|---|
| PB12 | I/O - FT_a | $\overline{\text{FAULT}}$ | Gate driver fault output |
| PB13 | I/O - FT_f | $\overline{\text{LIN1}}$ | Gate driver low-side input driver 1 |
| PB14 | I/O - FT_f | $\overline{\text{LIN2}}$ | Gate driver low-side input driver 2 |
| PB15 | I/O - FT | $\overline{\text{LIN3}}$ | Gate driver low-side input driver 3 |
| PA8 | I/O - FT | $\overline{\text{HIN1}}$ | Gate driver high-side input driver 1 |
| PA9 | I/O - FT_f | $\overline{\text{HIN2}}$ | Gate driver high-side input driver 2 |
| PA10 | I/O - FT_f | $\overline{\text{HIN3}}$ | Gate driver high-side input driver 3 |
| PA11 | I/O - FT_f | EN | Gate driver shutdown input |

*Note: Each unused GPIO inside the system-in-package should be configured in OUTPUT mode low level after startup by the software.*

# 4 Electrical data

## 4.1 Absolute maximum ratings

Each voltage referred to SGND unless otherwise specified.

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Test condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| VCC | Power supply voltage | | -0.3 | 21 | V |
| $V_{PGND}$ | Low-side driver ground | | VCC – 21 | VCC + 0.3 | V |
| $V_{PS}$ (1) | Low-side driver ground | | -21 | 21 | V |
| $V_{OUT}$ | Output voltage | | $V_{BOOT}$ – 21 | $V_{BOOT}$ + 0.3 | V |
| $V_{BOOT}$ | Bootstrap voltage | | -0.3 | 270 | V |
| $V_{HVG}$ | High-side gate output voltage | | $V_{OUT}$ – 0.3 | $V_{BOOT}$ + 0.3 | V |
| $V_{LVG}$ | Low-side gate output voltage | | $V_{PGND}$ – 0.3 | VCC + 0.3 | V |
| $V_{CIN}$ | Comparator input voltage | | -0.3 | 20 | V |
| $V_{OD}$ | Open-drain voltage (OD, FAULT) | | -0.3 | 21 | V |
| $dV_{OUT}/dt$ | Common-mode transient immunity | | | 50 | V/ns |
| $V_{IN}$ | MCU logic input voltage (2) | Input voltage on FT_xx | -0.3 | VDD + 4.0 (3) | V |
| | | Input voltage on any other pin | -0.3 | 4 | V |
| $I_{IO}$ | MCU I/O output current (2) | 2 | -25 | 15 | mA |
| $\Sigma I_{IO}$ | MCU I/O total output current (2) | | -80 | 80 | mA |
| $V_{DD}$, $V_{DDA}$, $V_{BAT}$ | MCU main supply voltages | | -0.3 | 4 | V |
| $V_{REF+}$ | | | -0.3 | Min($V_{DD}$+0.4, 4.0) | V |
| $T_{STG}$ | Storage temperature | | -55 | 150 | °C |
| $T_J$ | Junction temperature | | -40 | 150 | °C |
| $P_{TOT}$ | Total power dissipation | | | 4.5 | W |
| ESD | Human Body Model | | 2 (4) | | kV |

1. *$V_{PS} = V_{PGND} - V_{SGND}$*
2. *For details refer to the Absolute maximum ratings section in the STM32G031x8x3 datasheet; all voltages are defined with respect to VSS.*
3. *To sustain a voltage higher than 4 V, the internal pull-up/pull-down resistors must be disabled.*
4. *Pins 40, 47 and 53 have HBM ESD rating 1C conforming to ANSI/ESDA/JEDEC JS-001-2017.*

## 4.2 Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VCC | Power supply voltage | | $(V_{CCthON})_{MAX}$ | | 20 | V |
| $V_{LS}$ (1) | Low-side driver supply voltage | | 4 | | 20 | V |
| $V_{PS}$ (2) | Low-side driver ground | | -5 | | 5 | V |
| $V_{BO}$ (3) | Floating supply voltage | | $(V_{BOthON})_{MAX}$ | | 20 | V |
| $V_{CIN}$ | Comparator input voltage | | 0 | | 15 | V |
| $V_{OUT}$ | DC output voltage | | -10 (4) | | 230 | V |
| $F_{SW}$ | Maximum switching frequency (5) | | | | 800 | kHz |
| $V_{DD}$ | Standard MCU operating voltage | | 1.7 (6) | | 3.6 | V |
| $V_{DDA}$ | Analog supply voltage | For ADC operation | 1.62 | | 3.6 | V |
| | | For VREFBUF operation | 2.4 | | 3.6 | V |
| $V_{BAT}$ | Backup operating voltage | | 1.55 | | 3.6 | V |
| $V_{REF+}$ | ADC positive reference voltage | $V_{DDA} \geq 2$ V | 2 | | $V_{DDA}$ | V |
| | | $V_{DDA} < 2$ V | $V_{DDA}$ | | | V |
| $T_J$ | Operating junction temperature | | -40 | | 125 | °C |

1. *$V_{LS}$ = VCC - $V_{PGND}$*
2. *$V_{PS}$ = $V_{PGND}$ - $V_{SGND}$*
3. *$V_{BO}$ = $V_{BOOT}$ - $V_{OUT}$*
4. *LVG off. VCC = 9 V. Logic is operational if $V_{BOOT}$ > 5 V*
5. *Actual maximum $F_{SW}$ depends on power dissipation.*
6. *When RESET is released, functionality is guaranteed down to $V_{PDR}$ min.*

## 4.3 Thermal data

**Table 6. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th(JA)}$ | Thermal resistance junction to ambient (1) | 22.4 | °C/W |

1. *JEDEC 2s2p PCB in still air.*

# 5 Electrical characteristics

**Table 7. Electrical characteristics**

(VCC = 15 V; VDD = 3.3 V; PGND = SGND; $T_J$ = +25 °C, unless otherwise specified)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Power supply and standby mode** | | | | | | |
| $I_{QCCU}$ | VCC undervoltage quiescent supply current | VCC = 7 V;<br>EN = 5 V; CIN = SGND | | 430 | 744 | µA |
| $I_{QCC}$ | VCC quiescent supply current | EN = 5 V;<br>CIN = SGND<br>LVG & HVG: OFF | | 950 | 1450 | µA |
| $VCC_{thON}$ | VCC UVLO turn-on threshold | | 8 | 8.5 | 9 | V |
| $VCC_{thOFF}$ | VCC UVLO turn-off threshold | | 7.5 | 8 | 8.5 | V |
| $VCC_{hys}$ | VCC UVLO threshold hysteresis | | 0.4 | 0.5 | 0.6 | V |
| $I_{DD}$ (1) | $V_{DD}$ current consumption (Supply current in run mode, code executing from flash memory; all I/O pins are in analog input mode, all peripherals are disabled) | Range 1; PLL enabled;<br>$f_{HCLK} = f_{PLLRCLK}$ = 64 MHz (2) | | 5.2 | | mA |
| | | Range 2; PLL enabled;<br>$f_{HCLK} = f_{PLLRCLK}$ = 16 MHz (2) | | 1.2 | | |
| $I_{DDA}$ (1) (5) | $V_{DDA}$ current consumption | ADC consumption<br>$f_S$ = 2.5 MSps | | 410 | | µA |
| | | VREFBUF consumption<br>$I_{load}$ = 4 mA | | 35 | | |
| $V_{BOR1}$ | Brownout reset threshold 1 | $V_{DD}$ rising edge | 2.05 | 2.1 | 2.18 | V |
| | | $V_{DD}$ falling edge | 1.95 | 2.0 | 2.08 | V |
| $V_{hyst\_BORH1}$ | $V_{BOR1}$ hysteresis voltage | | | 100 | | mV |
| **High-side floating section supply** | | | | | | |
| $I_{QBOU}$ | VBO undervoltage quiescent supply current | VCC = $V_{BO}$ = 6.5 V;<br>EN = 5 V; CIN = SGND | | 25 | 62 | µA |
| $I_{QBO}$ | $V_{BO}$ quiescent supply current | $V_{BO}$ = 15 V<br>EN = 5 V; CIN = SGND<br>LVG OFF; HVG = ON | | 84 | 150 | µA |
| $V_{BOthON}$ | $V_{BO}$ UVLO turn-on threshold | | 7.5 | 8 | 8.5 | V |
| $V_{BOthOff}$ | $V_{BO}$ UVLO turn-off threshold | | 7 | 7.5 | 8 | V |
| $V_{BOhys}$ | $V_{BO}$ UVLO threshold hysteresis | | 0.4 | 0.5 | 0.6 | V |
| $I_{LK}$ | High-voltage leakage current | BOOT = HVG = OUT = 620 V | | | 15 | µA |
| $R_{Dboot}$ | Bootstrap diode on-resistance | $T_J$ = 25 °C, LVG ON | | 215 | 240 | Ω |

| Symbol | Parameter | Test condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Output driving buffers** | | | | | | | |
| $I_{SO}$ | Source peak current | $T_J$ = 25 °C | | 0.8 | 1.0 | 1.2 | A |
| | | Full temperature range (3) | | 0.7 | | 1.5 | A |
| $I_{SI}$ | Sink peak current | $T_J$ = 25 °C | | 0.75 | 0.9 | 1.1 | A |
| | | Full temperature range (3) | | 0.55 | | 1.2 | A |
| $R_{DSonON}$ | Source $R_{DSon}$ | I = 10 mA, $T_J$ = 25 °C | | 5.0 | 7.3 | 9.7 | Ω |
| | | I = 10 mA, Full temperature range (3) | | 4.1 | | 12.4 | Ω |
| $R_{DSonOFF}$ | Sink $R_{DSon}$ | I = 10 mA, $T_J$ = 25 °C | | 5.0 | 6.7 | 8.7 | Ω |
| | | I = 10 mA, Full temperature range (3) | | 4.1 | | 11.6 | Ω |
| **Logic inputs** | | | | | | | |
| $V_{il}$ | Low level logic threshold voltage | 1.62 V < $V_{DD}$ < 3.6 V | | | | 0.3 · $V_{DD}$ (4) | V |
| | | | | | | 0.39 · $V_{DD}$–0.06 (5) | V |
| $V_{ih}$ | High level logic threshold voltage | 1.62 V < $V_{DD}$ < 3.6 V | | 0.7 · $V_{DD}$ (4) | | | V |
| | | | | 0.49 · $V_{DD}$+0.26 (5) | | | V |
| $V_{hyst}$ (5) | Input hysteresis | FT_xx, NRST, 1.62 V < VDD < 3.6 V | | | 200 | | mV |
| $I_{lkg}$ (5) | Input leakage current | All except FT_e | 0 < $V_{IN}$ ≤ $V_{DD}$ | | | ± 70 | nA |
| | | | $V_{DD}$ ≤ $V_{IN}$ ≤ $V_{DD}$+1 V | | | 600 (6) | |
| | | | $V_{DD}$+1 V < $V_{IN}$ ≤ 5.5 V | | | 150 (6) | |
| | | FT_e (7) | 0 < $V_{IN}$ ≤ $V_{DD}$ | | | 10 | |
| $V_{SSDh}$ | SmartSD restart threshold | | | 3.5 | 4 | 4.3 | V |
| $V_{SSDl}$ | SmartSD unlatch threshold | | | | 0.56 | 0.75 | V |
| **Sense comparator and FAULT (8)** | | | | | | | |
| $V_{REF}$ | Internal voltage reference | | | 410 | 460 | 510 | mV |
| $CIN_{hyst}$ | Comparator input hysteresis | | | 40 | 70 | | mV |
| $CIN_{PD}$ | Comparator input pull-down current | $V_{CIN}$ = 1 V | | 7 | 10 | 13 | µA |
| $I_{OD}$ | OD internal current source | | | 2.5 | 5 | 7.5 | µA |
| $R_{ON\_OD}$ | OD on-resistance | $I_{OD}$ = 16 mA | | 19 | 25 | 36 | W |
| $I_{SAT\_OD}$ | OD saturation current | $V_{OD}$ = 5 V | | | 95 | | mA |

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{FLOAT\_OD}$ | OD floating voltage level | OD connected only to an external capacitance | 4.4 | 4.8 | 5.2 | V |
| $I_{OL\_OD}$ | OD low level sink current | $V_{OD}$ = 400 mV | 11 | 16 | 21 | mA |
| $R_{ON\_F}$ | FAULT on-resistance | $I_{FAULT}$ = 8 mA | | 50 | 100 | Ω |
| $I_{OL\_F}$ | FAULT low level sink current | $V_{FAULT}$ = 400 mV | 4 | 8 | 12 | mA |
| $t_{OD}$ | Comparator propagation delay | $R_{pu}$ = 100 kΩ to 5 V;<br>0 to 3.3 V voltage step on CIN<br>50% CIN to 90% OD | | 350 | 500 | ns |
| $t_{CIN-F}$ | Comparator triggering to FAULT | 0 to 3.3 V voltage step on CIN;<br>50% CIN to 90% FAULT | | 350 | 500 | ns |
| $t_{CINoff}$ | Comparator triggering to high/low-side driver propagation delay | 0 to 3.3 V voltage step on CIN 50% CIN to 90% LVG/HVG | | 360 | 510 | ns |
| $t_{FCIN}$ | Comparator input filter time | | 200 | 300 | 400 | ns |
| SR | Slew rate | $C_L$ = 1 nF; $R_{pu}$ = 1 kΩ to 5 V;<br>90% to 10% OD | 4 | 7.7 | 10.3 | V/µs |
| **Driver dynamic characteristics** | | | | | | |
| $t_{on}$ (3) | High/low-side driver turn-on propagation delay | OUT = 0 V<br>BOOT = VCC<br>$C_L$ = 1 nF<br>$V_{in}$ = 0 to 3.3 V<br>see Figure 3 | | 85 | | ns |
| $t_{off}$ (3) | High/low-side driver turn-off propagation delay | | | 85 | | ns |
| $t_{EN}$ (3) | Enable to high/low-side driver propagation delay | | | 345 | | ns |
| $t_r$ | Rise time | $C_L$ = 1 nF | | 19 | | ns |
| $t_f$ | Fall time | $C_L$ = 1 nF | | 17 | | ns |

1. *The current consumption depends on the firmware loaded in the microcontroller. See STM32G031x8x3 datasheet.www.st.com*
2. *$V_{DD}$ = 3.0 V for values in Typ. columns, all peripherals disabled, cache enabled, prefetch disabled for code. Prefetch and cache enabled when fetching from Flash memory.*
3. *Values provided by characterization, not tested.*
4. *Data tested in production.*
5. *Data guaranteed by design - not tested in production.*
6. *This value represents the pad leakage of the I/O itself. The total product pad leakage is provided by this formula: $I_{Total\_Ileak\_max}$ = 10 µA + [number of I/Os where $V_{IN}$ is applied on the pad] x $I_{lkg}$(Max).*
7. *FT_e with diode enabled. Input leakage current of FT_e I/Os with the diode disabled is the same as standard I/Os.*
8. *The comparator is disabled when VCC is in UVLO condition.*

Figure 3. **Propagation delay timing definition**

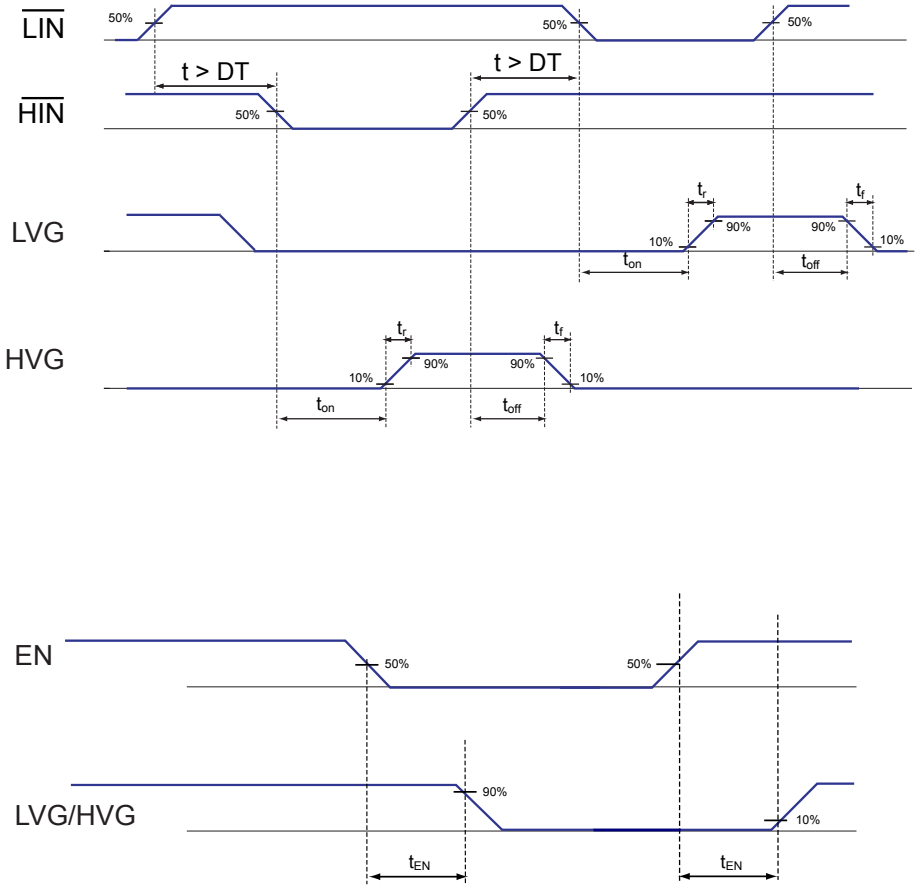



Figure 4. **Deadtime timing definitions**

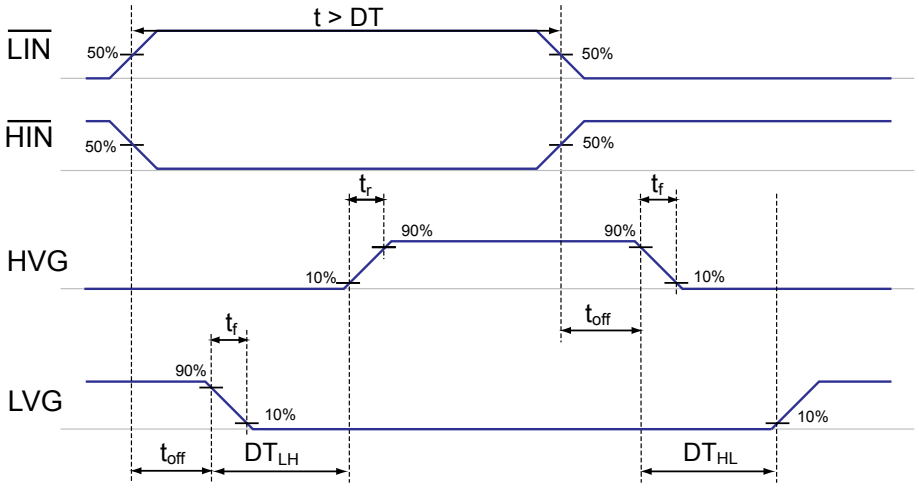
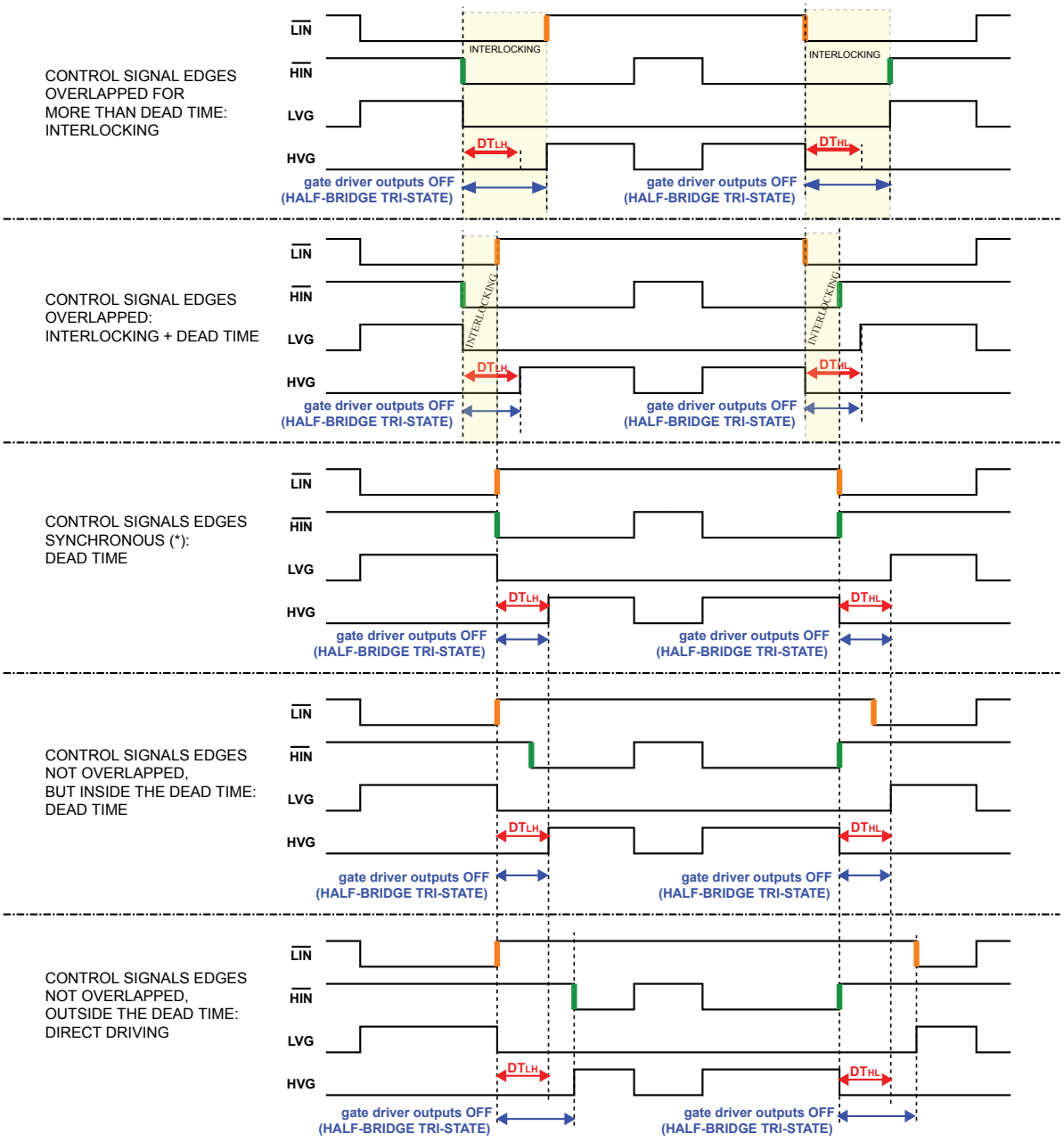


Figure 5. **Deadtime and interlocking waveforms definition**



# 6 Device description

The STSPIN32G0252 is a system-in-package providing an integrated solution suitable for driving high-voltage three-phase applications.

## 6.1 Gate driver

The STSPIN32G0252 integrates a triple half-bridge gate driver able to drive N-channel power MOSFETs or IGBTs. The high-side section is supplied by a bootstrapped voltage technique with an integrated bootstrap diode.

All the input lines are connected to a pull-down resistor with a typical value of 100 kΩ.

The high- and low-side outputs of the same half-bridge cannot be simultaneously driven high thanks to an integrated interlocking function.

### 6.1.1 Inputs and outputs

The device is controlled through the following logic inputs:

- EN: enable input, active high;
- LIN: low-side driver inputs, active low;
- HIN: high-side driver inputs, active low.

**Table 8. Inputs truth table (applicable when the device is not in UVLO or SmartSD protection)**

| | Input pins | | | Output pins | |
|---|---|---|---|---|---|
| | **EN** | **$\overline{\text{LIN}}$** | **$\overline{\text{HIN}}$** | **LVG** | **HVG** |
| | L | X | X | Low | Low |
| | H | H | H | Low | Low |
| | H | L | H | **HIGH** | Low |
| | H | H | L | Low | **HIGH** |
| *Interlocking* | H | L | L | Low | Low |

*Note: X : Do not care.*

The FAULT and OD pins are open-drain outputs. The FAULT signal is set low in case VCC UVLO is detected, or in case the SmartShutDown comparator triggers an event. It is only used to signal a UVLO or SmartSD activation to external circuits, and its state does not affect the behavior of other functions or circuits inside the driver. The OD behavior is explained in Comparator and Smart shutdown.

### 6.1.2 Deadtime

The deadtime feature, in companion with the interlocking feature, guarantees that driver outputs of the same channel are not high simultaneously and at least a DT time passes between the turn-off of one driver's output and the turn-on of the companion output of the same channel. If a deadtime longer than the internal DT is applied to the LIN and HIN inputs by the external controller, the internal DT is ignored and the outputs follow the deadtime determined by the inputs. Refer to Figure 3 for the deadtime and interlocking waveforms.

### 6.1.3 VCC UVLO protection

Undervoltage protection is available on VCC and BOOT supply pins. In order to avoid intermittent operation, a hysteresis sets the turn-off threshold with respect to the turn-on threshold.

When VCC voltage goes below the $V_{CCthOFF}$ threshold, all the outputs are switched off, both LVG and HVG. When VCC voltage reaches the $V_{CCthON}$ threshold, the driver returns to normal operation and sets the LVG outputs according to actual input pin status; HVG is also set according to input pin status if the corresponding $V_{BO}$ section is not in UVLO condition. The FAULT output is kept low when VCC is in UVLO condition. The following figures show some examples of typical operation conditions.

Figure 6. **VCC power ON and UVLO, LVG timing**

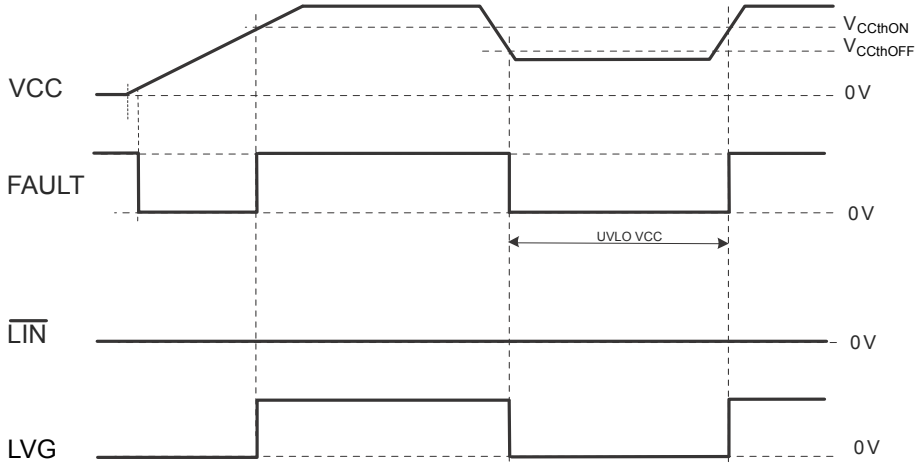
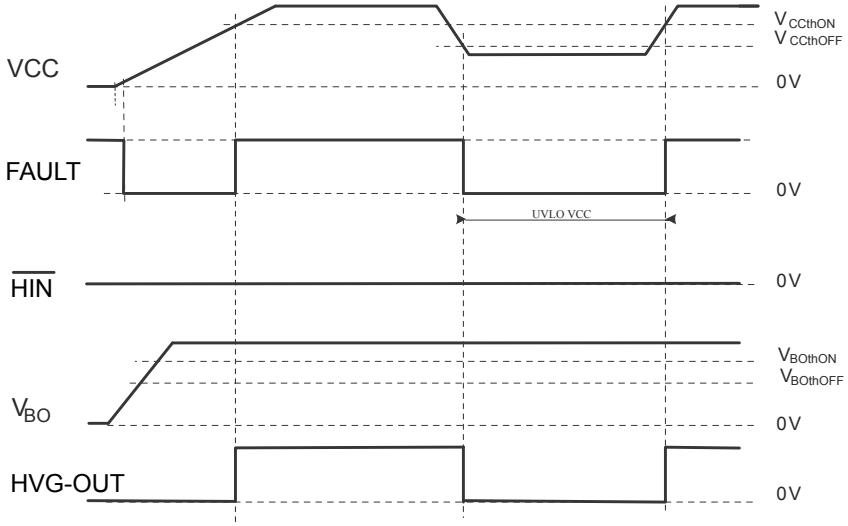



Figure 7. **VCC power ON and UVLO, HVG timing**

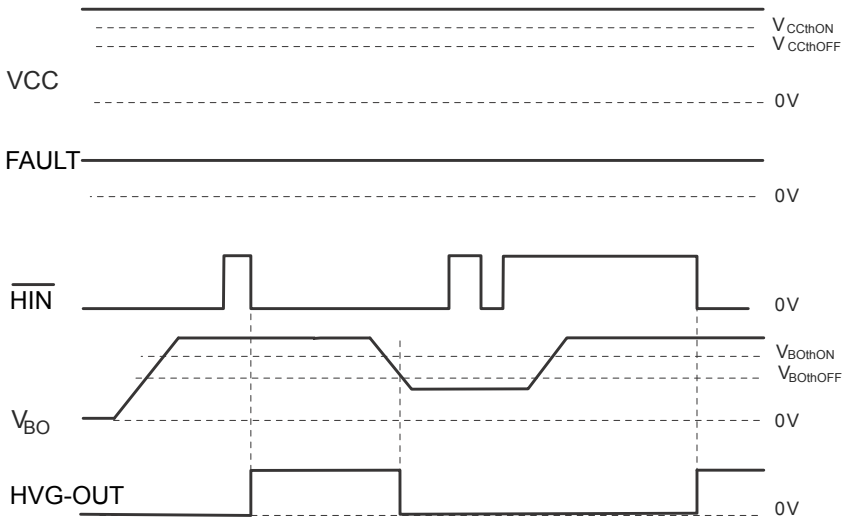


### 6.1.4 $V_{BO}$ UVLO protection

Dedicated undervoltage protection is available on each bootstrap section between BOOTx and OUTx supply pins. In order to avoid intermittent operation, a hysteresis sets the turn-off threshold with respect to the turn-on threshold.

When the $V_{BO}$ voltage goes below the $V_{BOthOFF}$ threshold, the HVG output of the corresponding bootstrap section is switched off. When the $V_{BO}$ voltage reaches the $V_{BOthON}$ threshold, the device returns to normal operation and the output remains off up to the next input pin transition that requests HVG to turn on.

**Figure 8. $V_{BO}$ power-ON and UVLO timing**




### 6.1.5 Comparator and Smart shutdown

The STSPIN32G0252 integrates a comparator committed to the fault protection function, thanks to the SmartShutDown (SmartSD) circuit.

The SmartSD architecture allows immediate turn-off of the gate driver outputs in the case of overload or overcurrent condition, by minimizing the propagation delay between the fault detection event and the actual output switch-off. In fact, the time delay between the fault detection and the output turn-off is not dependent on the value of the external components connected to the OD pin, which are only used to set the duration of disable time after the fault.

This provides the possibility to increase the duration of the output disable time after the fault event up to very large values without increasing the delay time of the protection. The duration of the disable time is determined by the values of the external capacitor $C_{OD}$ and of the optional pull-up resistor connected to the OD pin.

The comparator has an internal voltage reference $V_{REF}$ connected to the inverting input, while the non-inverting input is available on the CIN pin. The comparator's CIN input can be connected to an external shunt resistor in order to implement a fast and simple overcurrent protection function. The output signal of the comparator is filtered from glitches shorter than $t_{FCIN}$ and then fed to the SmartSD logic.

If the impulse on the CIN pin is higher than $V_{REF}$ and wider than $t_{FCIN}$, the SmartSD logic is triggered and immediately sets all of the driver outputs to low-level (OFF).

At the same time, FAULT is forced low to signal the event (for example to an MCU input) and OD starts to discharge the external $C_{OD}$ capacitor used to set the duration of the output disable time of the fault event.

The FAULT pin is released and driver outputs restart following the input pins as soon as the *output disable time* expires.

The overall disable time is composed of two phases:

- The OD *unlatch time* ($t_1$ in Figure 9), which is the time required to discharge the $C_{OD}$ capacitor down to the $V_{SSDl}$ threshold. The discharge starts as soon as the SSD comparator is triggered.
- The OD *Restart time* ($t_2$ in Figure 9), which is the time required to recharge the $C_{OD}$ capacitor up to the $V_{SSDh}$ threshold. The recharge of $C_{OD}$ starts when the OD internal MOSFET is turned-off, which happens when the fault condition has been removed (CIN < $V_{REF}$ - $C_{INhyst}$) and the voltage on OD reaches the $V_{SSDl}$ threshold. This time normally covers most of the overall output disable time.

If no external pull-up is connected to OD, the external $C_{OD}$ capacitor is discharged with a time constant defined by $C_{OD}$ and the internal MOSFET's characteristic (Equation 1), and the Restart time is determined by the internal current source $I_{OD}$ and by $C_{OD}$ (Equation 2 ).

**Equation 1**

(1)

$$t_1 \cong R_{ON\_OD} \cdot C_{OD} \cdot \ln\left(\frac{V_{OD}}{V_{SSDl}}\right)$$

**Equation 2**

(2)

$$t_2 \cong \frac{C_{OD} \cdot V_{SSDh}}{I_{OD}} \cdot \ln\left(\frac{V_{SSDl} - V_{OD}}{V_{SSDh} - V_{OD}}\right)$$

Where $V_{OD} = V_{FLOAT\_OD}$

In case the OD pin is connected to VCC by an external pull-up resistor $R_{OD\_ext}$, the OD discharge time is determined by the external network $R_{OD\_ext}$ $C_{OD}$ and by the internal MOSFET's $R_{ON\_OD}$ (Equation 3), while the Restart time is determined by current in $R_{OD\_ext}$ (Equation 4).

**Equation 3**

(3)

$$t_1 \cong C_{OD} \cdot \left(R_{OD\_ext} // R_{ON\_OD}\right) \cdot \ln\left(\frac{V_{OD} - V_{on}}{V_{SSDl} - V_{on}}\right)$$

**Equation 4**

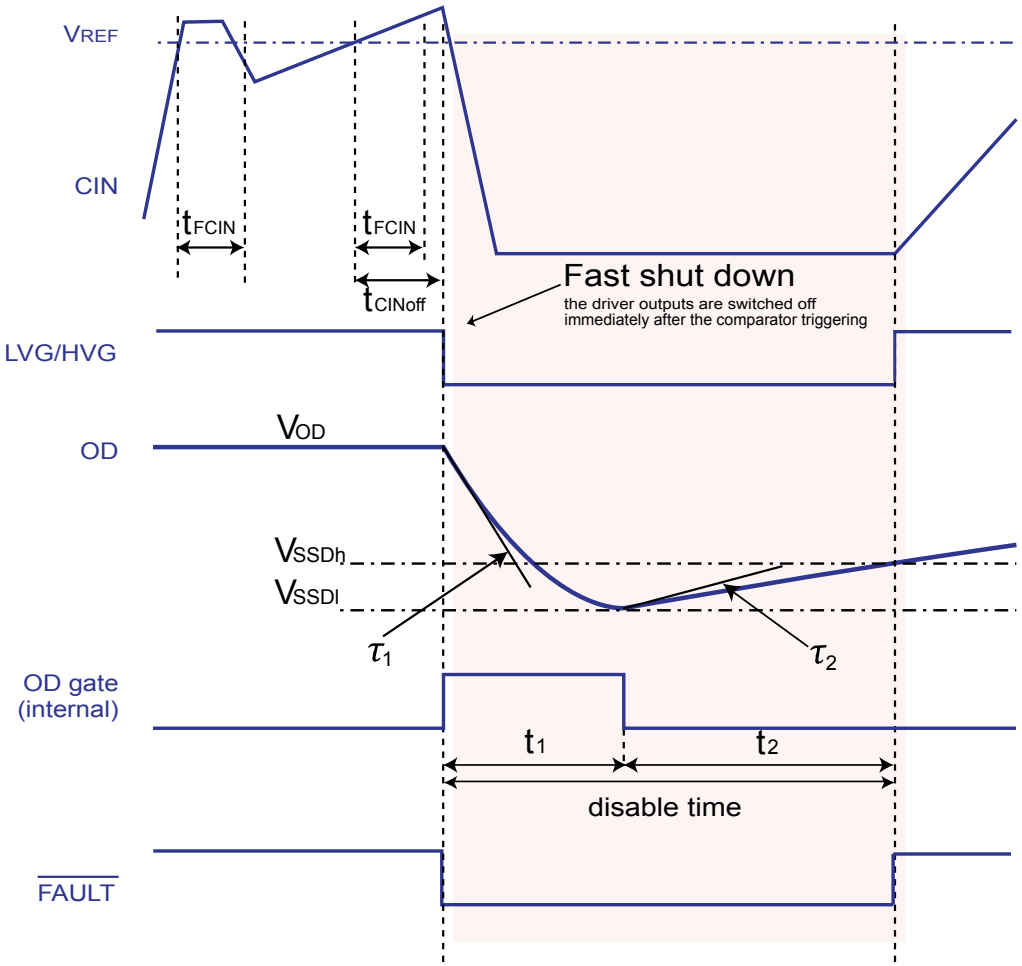
(4)

$$t_2 \cong C_{OD} \cdot R_{OD\_ext} \cdot \ln\left(\frac{V_{SSDl} - V_{OD}}{V_{SSDh} - V_{OD}}\right)$$

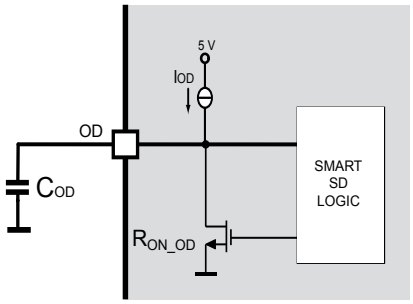
where

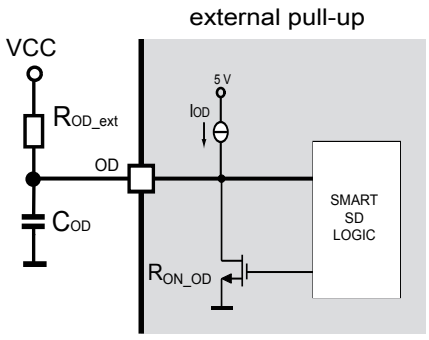
$$V_{on} = \frac{R_{ON\_OD}}{R_{OD\_ext} + R_{ON\_OD}} \cdot V_{cc} \quad ; \quad V_{OD} = V_{cc}$$

Figure 9. **Smart shutdown timing waveforms**




SMART SHUTDOWN CIRCUIT



## 6.2 Microcontroller unit

The integrated MCU is the STM32G031x8 with the following main characteristics:

- Core: ARM® Cortex® -M0+ 32-bit CPU, frequency up to 64 MHz
- Memories: 8 KB of SRAM, 64 KB of flash memory
- ADC 12-bit resolution and 0.4 µs sampling time
- 5-channel DMA controller with flexible mapping
- Full set of interfaces: UART, $I^2C$, SPI, LPUART

*Note: For more details, refer to the STM32G031x8 datasheet on www.st.com.*

### 6.2.1 Memories and boot mode

The device has the following features:

- 8 Kbytes of embedded SRAM
- The non-volatile memory is divided into two arrays:
  - 64 Kbytes of embedded flash memory for programs and data
  - Option bytes

The flash memory embeds the Error Correction Code (ECC) feature supporting:

- Single error detection and correction.
- Double error detection.
- The address of the ECC fail can be read from the ECC register.
- 1 Kbyte (128 double word) OTP (one-time programmable) bytes for user data. The OTP data cannot be erased and can be written only once.

Flexible protections can be configured thanks to the option bytes:

- Readout protection (RDP) to protect the whole memory with the following options:
  - Level 0: no readout protection.
  - Level 1: memory readout protection; the flash memory cannot be read from or written to if either the debug features are connected or the boot from RAM or bootloader are selected.
  - Level 2: chip readout protection; the debug features (serial wire), the boot from RAM and the bootloader selection are disabled. This selection is irreversible.
- Write protection (WRP): the protected area is protected against erasing and programming.
- Proprietary code readout protection (PCROP): a part of the flash memory can be protected against read and write from third parties.
- Securable memory area: a part of flash memory can be configured by option bytes to be securable.

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- Boot from User flash memory.
- Boot from System Memory.
- Boot from embedded SRAM.

The boot pin is shared with a standard GPIO and can be enabled through the boot selector option bit.

The bootloader is located in System Memory. It is used to reprogram the flash memory by one of the following interfaces:

- USART on pins PA9/PA10 or PA2/PA3.
- $I^2C$-bus on pins PB6/PB7 or PB10/PB11.

### 6.2.2 Power management

The VDD is the external power supply for the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD/VDDA pin.

The $V_{DDA}$ is the analog power supply for ADC and the voltage reference buffer. The $V_{DDA}$ voltage level is identical to the $V_{DD}$ voltage as it is provided externally through the VDD/VDDA pin.

The $V_{BAT}$ is the power supply (through a power switch) for RTC, TAMP, low-speed external 32.768 kHz oscillator, and backup registers when $V_{DD}$ is not present. $V_{BAT}$ is provided externally through the $V_{BAT}$ pin.

$V_{REF+}$ is the analog peripheral input reference voltage, or the output of the internal voltage reference buffer (when enabled).

- When $V_{DDA}$ < 2 V, $V_{REF+}$ must be equal to $V_{DDA}$.
- When $V_{DDA}$ ≥ 2 V, $V_{REF+}$ must be between 2 V and $V_{DDA}$. It can be grounded when the analog peripherals using $V_{REF+}$ are not active.

The device has an integrated power-on/power-down (POR/PDR) reset active in all power modes except shutdown and ensures proper operation upon power-on and power-down. It maintains the device in reset when the supply voltage is below the $V_{POR/PDR}$ threshold, without the need for an external reset circuit.

Brownout reset (BOR) function allows extra flexibility. It can be enabled and configured through option bytes, by selecting one of four thresholds for rising $V_{DD}$ and the other four for falling $V_{DD}$.

The device also features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}$ power supply and compares it to the $V_{PVD}$ threshold. It allows generating an interrupt when the $V_{DD}$ level crosses the $V_{PVD}$ threshold, selectively while falling, while rising, or while falling and rising. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

The MCU supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wake-up sources:

- **Sleep mode**

  In sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run mode**

  The low-power run mode is achieved with $V_{CORE}$ supplied by the low-power regulator to minimize the regulator's operating current.

- **Stop mode**

  In stop mode the device achieves low power consumption while retaining the content of SRAM and registers.

- **Standby mode**

  The standby mode is used to achieve a very low power consumption with POR/PDR always active in this mode.

  The device exits standby mode when an external reset (NRST pin), IWDG reset event, wake-up event (WKUP pin, configurable rising or falling edge) or RTC event (alarm, periodic wake-up, timestamp, tamper), or when a failure is detected on LSE (CSS on LSE).

- **Shutdown mode**

  The shutdown mode is used to achieve the lowest power consumption. The BOR is not available in shutdown mode. No power voltage monitoring is possible in this mode. Therefore, switching to an RTC domain is not supported.

  The device exits shutdown mode upon external reset event (NRST pin), IWDG reset event, wake-up event (WKUP pin, configurable rising or falling edge) or RTC event (alarm, periodic wake-up, timestamp, tamper).

### 6.2.3 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted deadtimes.

This timer is used to generate the PWM signal for the three half-bridge gate drivers as shown in Table 9.

**Table 9. TIM1 channel configuration**

| MCU I/O | Analog IC input/output | TIM1 channel |
|---|---|---|
| PB13 | LIN1 | TIM1_CH1N |
| PB14 | LIN2 | TIM1_CH2N |
| PB15 | LIN3 | TIM1_CH3N |
| PA8 | HIN1 | TIM1_CH1 |
| PA9 | HIN2 | TIM1_CH2 |
| PA10 | HIN3 | TIM1_CH3 |
| PB12 (1) | FAULT | TIM1_BKIN |

1. *The PB12 must be configured with internal pull-up since FAULT output is open-drain.*

# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 7.1 QFN 10x10 72L package information

**Figure 10. Package mechanical data**

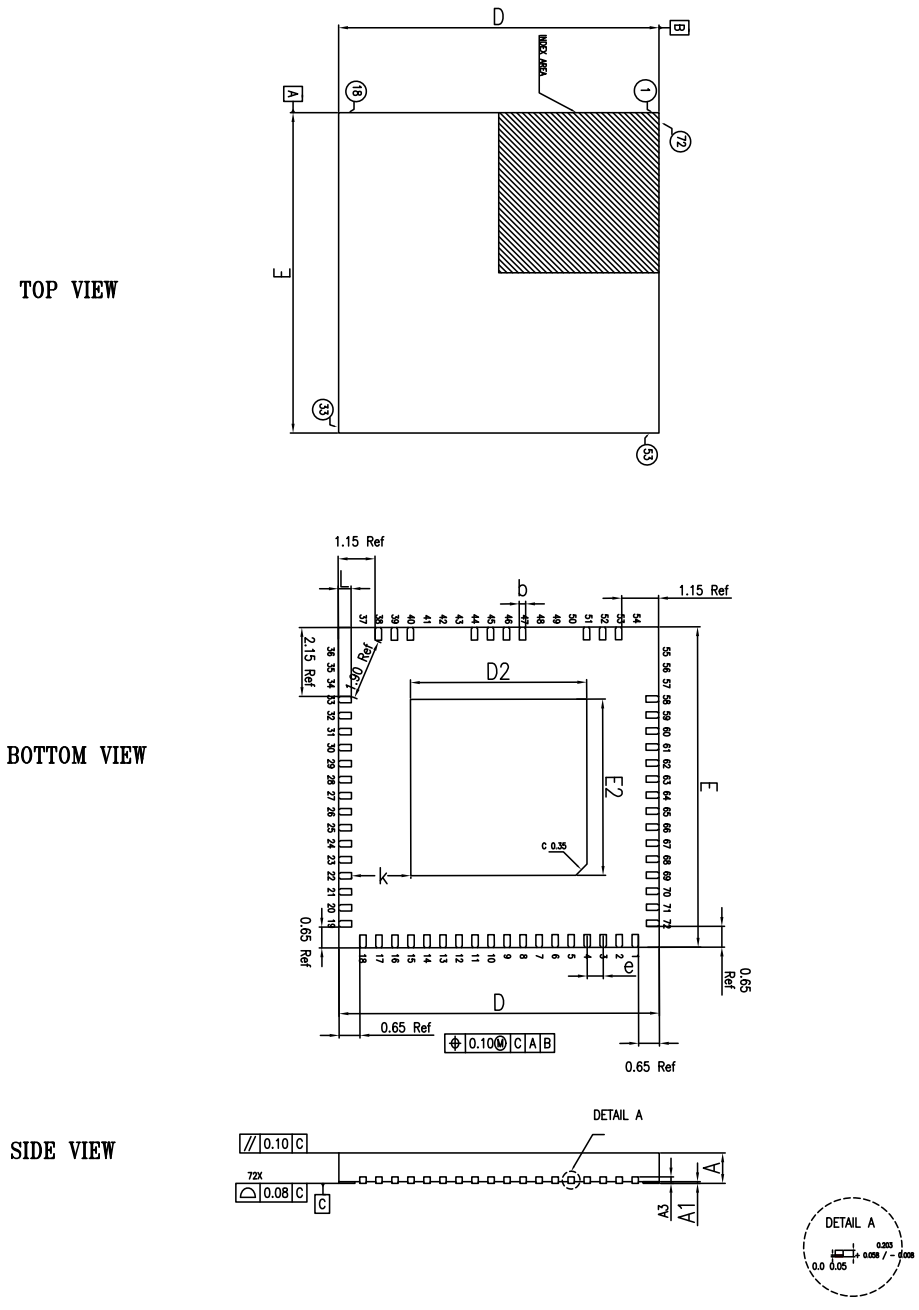


Table 10. **QFN package dimensions**

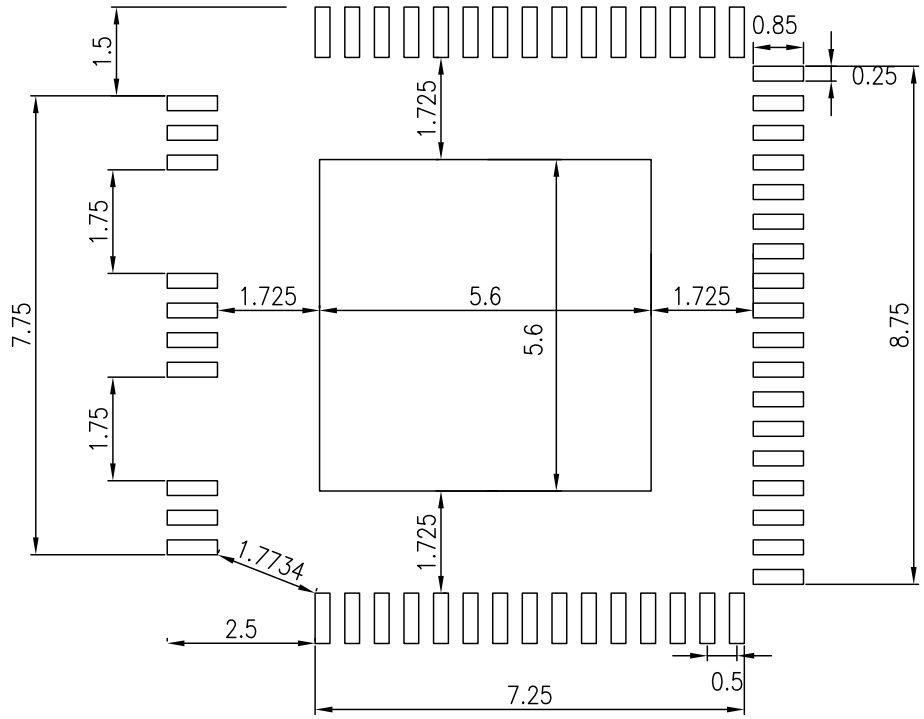
| Symbol | Min. | Nom. | Max. |
|---|---|---|---|
| A | 0.90 | 0.95 | 1.00 |
| A1 | 0 | | 0.05 |
| A3 | | 0.20 Ref. | |
| b | 0.15 | 0.20 | 0.25 |
| D | 9.90 | 10.00 | 10.10 |
| D2 | 5.40 | 5.50 | 5.60 |
| e | | 0.50 BSC | |
| E | 9.90 | 10.00 | 10.10 |
| E2 | 5.40 | 5.50 | 5.60 |
| L | 0.30 | 0.40 | 0.50 |
| K | | 1.85 Ref. | |
| **Tolerance** | | | |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |

*Note: All dimensions are mm unless otherwise specified.*

## 7.2 Suggested land pattern

*Note: All dimensions are mm unless otherwise specified.*

Figure 11. **QFN 10x10 72L suggested land pattern**



# 8 Ordering information

Table 11. **Order codes**

| Order code | Package | Package marking | Packaging |
|---|---|---|---|
| STSPIN32G0252Q | QFN 10 x 10 72L | SPING252Q | Tray |
| STSPIN32G0252QTR | QFN 10 x 10 72L | SPING252Q | Tape and Reel |

# Revision history

Table 12. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 13-Dec-2023 | 1 | Initial release. |

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