AS1170

Datasheet

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AS1170 High current LED/VCSEL driver

1 General description

The AS1170 is an inductive high efficient DCDC step up converter with two current sinks. The DCDC step up converter operates at a fixed frequency of 4 MHz and includes soft startup to allow easy integration into noise sensitive RF systems. The AS1170 includes flash timeout, overvoltage, over temperature, undervoltage and short circuit protection functions. The AS1170 is controlled by an I²C interface and has a hardware automatic shutdown if SCL=0 for 100 ms. Therefore no additional enable input is required for shutting down of the device once the system shuts down. The AS1170 is available in a space-saving WL-CSP package measuring only 2.25 mm x 1.5 mm x 0.6 mm.

1.1 Key benefits & features

The AS1170 module is specifically designed for:

Table 1: Added value overview

Features	Benefits
High efficiency 4 MHz fixed frequency DCDC Boost converter	Stable even in coil current limit
Independent channel control	Combine channels for higher current output
PWM operation for lower output current	31.25 kHz to avoid audible noise
WL-CSP package	Tiny footprint of 2.25 mm x 1.5 mm x 0.6 mm
Automatic current adjustment for low battery voltage	Long battery lifetime
High output current	Current adjustable up to 2000 mA

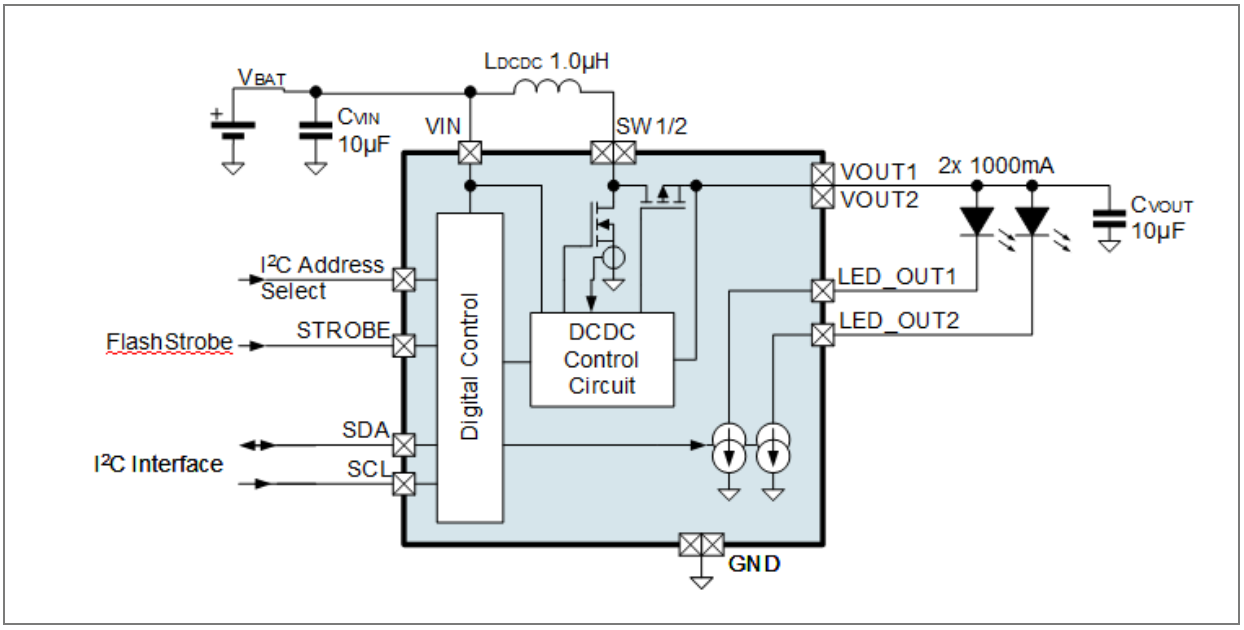
1.2 Applications

- Flash / torch / video light for smartphones, feature-phones
- 3D sensing – Active stereo vision / structured light
- Handheld scanners
- Safety signage

1.3 Block diagram

The functional block of this device is shown below:

Figure 1: Functional block of AS1170

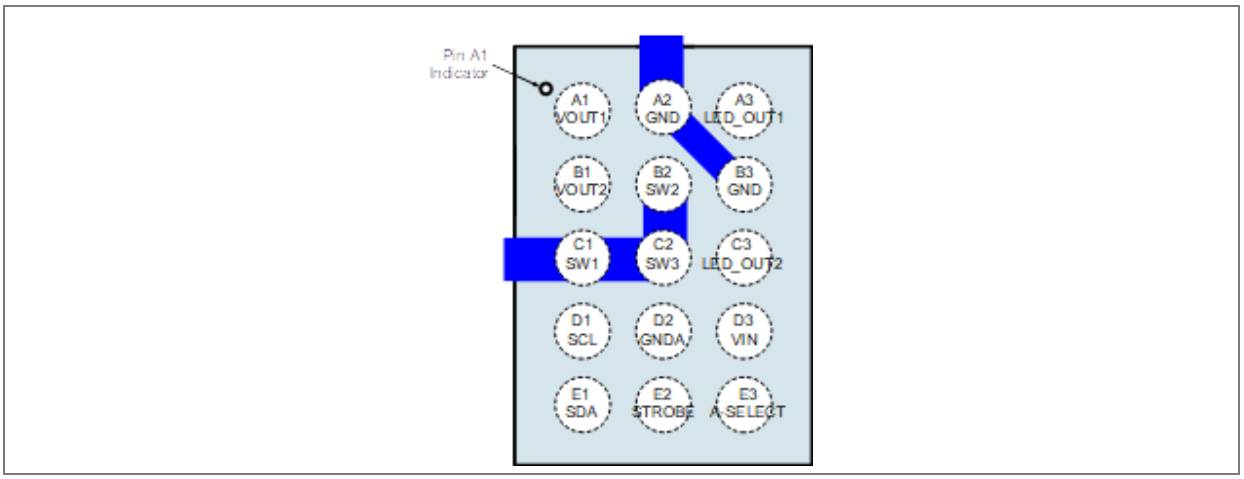


2 Ordering information

Product code	Q-Number	Package	Delivery form	Delivery quantity
AS1170	Q65113A7128	AS1170 WLP LF T&R	Tape and reel	10000 pcs
AS1170	Q65113A7129	AS1170 WLP LF T&R	Tape and reel	500 pcs

3 Pin assignment

Figure 2: Pin assignment



3.1.1 Pin description

Table 2: Pin description

Pin number	Pin name	Value
A1	VOUT1	DCDC converter output capacitor - make a short connection to C_{VOUT} / V_{OUT2}.
A2	GND	Power and analog ground; make a short connection between both balls.
A3	LED_OUT1	Flash LED current sink.
B1	SW1	DCDC converter switching node - make a short connection to SW2 / coil L_{DCDC}.
B2	GND	Power and analog ground; make a short connection between both balls.
C1	VOUT2	DCDC converter output capacitor - make a short connection to C_{VOUT} / V_{OUT1}.
C2	SW2	DCDC converter switching node - make a short connection to SW1 / coil L_{DCDC}.
C3	LED_OUT2	Flash led current sink.
D1	SCL	Serial clock input for I²C interface.
D2	VIN	Positive supply voltage input - connect to supply and make a short connection to input capacitor C_{VIN} and to coil L_{DCDC}.
E1	SDA	Serial data input/output for I²C interface (needs external pull-up resistor).
E2	STROBE	Digital input with pulldown to control strobe time for flash function.
E3	A-SELECT	Alternative I²C address pin.

4 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute maximum ratings of AS1170

Parameter	Min	Max	Unit	Comments
V_{IN} to GND	-0.3	+7.0	V	
Strobe, SCL, SDA to GND	-0.3	V_{IN} + 0.3	V	Max. +7 V
SW1/2, VOUT1/2, LED_OUT1/2 to GND	-0.3	+7.0	V	
VOUT1/2 to SW1/2	-0.3	0.0	V	**Note:** Diode between VOUT1/2 and SW1/2
Voltage between GND pins	0.0	0.0	V	Short connection recommended
Input pin current without causing latchup	-100	+100 + IIN	mA	EIA/JESD78
Continuous power dissipation (T_A = +70 °C)				
Continuous power dissipation		1230	mW	P_T @ 70 °C
Continuous power dissipation de-rating factor		16.7	mW/K	PDERATE2
Electrostatic discharge				
ESD_{HBM} Pins LED_OUT1/23		±8000	V	JEDEC JESD22-A114F
ESD_{HBM}		±2000	V	
ESD_{CDM}		±500	V	JS-002-2022
ESD_{MM}		±100	V	JESD22-A115C
Temperature ranges and storage conditions				
Junction to ambient thermal resistance		604	K/W	
Junction temperature		150	°C	Internally limited (over temperature protection), max. 20000s
Storage temperature range	-55	125	°C	
Humidity	5	85	%	Non condensing
Body temperature during soldering		260	°C	According to IPC/JEDEC J-STD-020

Parameter	Min	Max	Unit	Comments
Moisture sensitivity level (MSL)		MSL1		Represents a max. floor life time of unlimited

(1) Depending on actual PCB layout and PCB used measured on demoboard; for peak power dissipation during flashing see document AS1170 thermal measurements.
(2) PDERATE de-rating factor changes the total continuous power dissipation (P_T) if the ambient temperature is not 70 °C. Therefore for e.g. T_{AMB} = 85 °C, calculate P_T at 85 °C = P_T - PDERATE * (85 °C to 70 °C).
(3) Pins LED_OUT1 connected to LED_OUT2 and capacitor C_{VOUT} connected to VOUT1/2 and GND; both GND pins connected together.
(4) Measured on AS1170 demoboard.

5 Electrical characteristics

Table 4: Electrical characteristics of AS1170

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
General operating conditions						
V_{VIN}	Supply voltage	Pin V_{IN}	2.7	3.7	4.4	V
$V_{VINREDUCED\_FUNC}$	Supply voltage	AS1170 functionally working, but not all parameters fulfilled	2.5		2.7	V
			4.4		5.5	
$I_{SHUTDOWN}$	Shutdown current	SCL=SDA=0 V, V_{VIN}<3.7 V		0.6	2.0	µA
I_{STANBY}	Standby current	Interface active, V_{VIN}<3.7 V		1.0	10	µA
T_{AMB}	Operating temperature		-30	25	85	°C
E_{ta}	Application efficiency (DCDC and current sink)	L_{COIL} = 0.6 µH @ 3 A, L_{ESR}= 60 mΩ, LED_OUT1,2=1300 mA, t_{FLASH}<300 ms		84		%
DCDC step up converter						
V_{VOUT}	DCDC boost output voltage (pin VOUT1/2)		2.8		5.5	V
V_{VOUT5V}	DCDC boost output voltage (pin VOUT1/2)	Constant voltage mode operation const_v_mode=1 (see Page 49)		5.0		V
R_{PMOS}	On-resistance	DCDC internal PMOS switch		70		mΩ
R_{NMOS}	On-resistance	DCDC internal NMOS switch		70		mΩ
f_{CLK}	Operating frequency	All internal timings are derived from this oscillator	-7.5%	4.0	+7.5%	MHz

Symbol	Parameter	Condition		Min	Typ.	Max	Unit
Current sinks							
V_{LED}	LED forward voltage	Two flash LEDs at 1800 mA combined		2.8	3.5	3.95	V
		Single flash LED at 1600 mA		2.8		4.2	V
I_{LED_OUT}	LED_OUT1/2 current sinks output combined	Dual flash LED	current_boost=1	0		2000	mA
			current_boost=0	0		1800	
		Single flash LED				1600	mA
$I_{LED\_OUT\Delta}$	LED_OUT1/2 current sink accuracy	I_{LEDOUT}>=800 mA or I_{LEDOUT}<500 mA 0 °C < T_J < 100 °C		-7		+7	%
		500 mA<I_{LED_OUT}<800 mA, 0 °C < T_J < 100 °C		-5		+5	%
$I_{LED\_OUTRAMP}$	LED_OUT1/2 ramp time	Ramp-up during startup			250	1000	µs
		Ramp-down			500	1000	µs
$I_{LED\_OUTRIPPLE}$	LED_OUT current ripple	I_{LED_OUT} = 1000 mA, BW=20 MHz			20		mA_{PP}
V_{ILED_COMP}	LED_OUT current sink voltage compliance	Minimum voltage between pin LED_OUT1/2 and GND for operation of the current sink	current_boost=0		325		mV
			current_boost=1		360		
$V_{LED\_OUTCOMP\_HYST}$	Comparators hysteresis	Hysteresis for comparators between LED_OUT1 and LED_OUT2 reporting signals led_out1above2 and led_out2above1			30		mV
V_{HIGH_VDS}	Comparator high VDS	Low VDS and high VDS comparator – see Page 17			900		mV
V_{LOW_VDS}	Comparator low VDS				320		
$I_{LEAK\_LED\_OUT}$	LED_OUT1/2 leakage current	Pins LED_OUT1 and LED_OUT2		-1.0	0.0	+1.0	µA
Protection and fault detection functions (see Page 18)							
$V_{VOUTMAX}$	VVOUT overvoltage protection	DCDC converter overvoltage protection		5.0	5.3	5.6	V
I_{LIMIT}	Current limit for coil L_{DCDC} (Pin SW) measured at 40% PWM duty cycle maximum 40000s lifetime operation in overcurrent limit		coil_peak=00b	1.8	2.0	2.23	A
			coil_peak=01b	2.25	2.5	2.78	
		Default value	coil_peak (see Page 24 =10b	2.7	3.0	3.34	
			coil_peak=11b	3.15	3.5	3.9	

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
$V_{LEDSHORT}$	Flash LED short circuit detection voltage	Voltage measured between pins VOUT1,2 and LED_OUT1,2		1.0		V
T_{OVTEMP}	Overtemperature protection	Junction temperature		144		°C
$T_{OVTEMPHYST}$	Overtemperature hysteresis			5		°C
$t_{FLASHTIMEOUT}$	Flash timeout timer	Can be adjusted with register flash_timeout	2		1280	ms
		Accuracy	-7.5		+7.5	%
V_{UVLO}	Undervoltage lockout	Falling V_{VIN}	2.25	2.4	2.5	V
		Rising V_{VIN}	V_{UVLO}+ 0.05	V_{UVLO}+ 0.1	V_{UVLO}+ 0.15	V
Digital interface						
V_{IH}	High level input voltage	Pins SCL, SDA	1.26		V_{VIN}	V
V_{IL}	Low level input voltage		0.0		0.54	V
$V_{IHFLASH}$	High level input voltage	Pin STROBE	0.7		V_{VIN}	V
$V_{ILFLASH}$	Low level input voltage		0.0		0.54	V
V_{OL}	Low level output voltage	Pin SDA, I_{OL}=3 mA			0.3	V
I_{LEAK}	Leakage current	Pins SCL, SDA	-1.0	0.0	+1.0	µA
I_{PD}	Pulldown current to GND	Pins STROBE		36		µA
$t_{TIMEOUT}$	SCL timeout	In indicator, assist or flash mode, if SCL is low longer than this timeout, the AS1170 automatically enters shutdown mode	35		100	ms

(1) V_{VIN} = +2.7 V to +4.4 V, T_{AMB} = -30 °C to 85 °C, unless otherwise specified. Typical values are at V_{VIN} = +3.7 V, T_{AMB} = 25 °C, unless otherwise specified.

5.1 I²C specifications

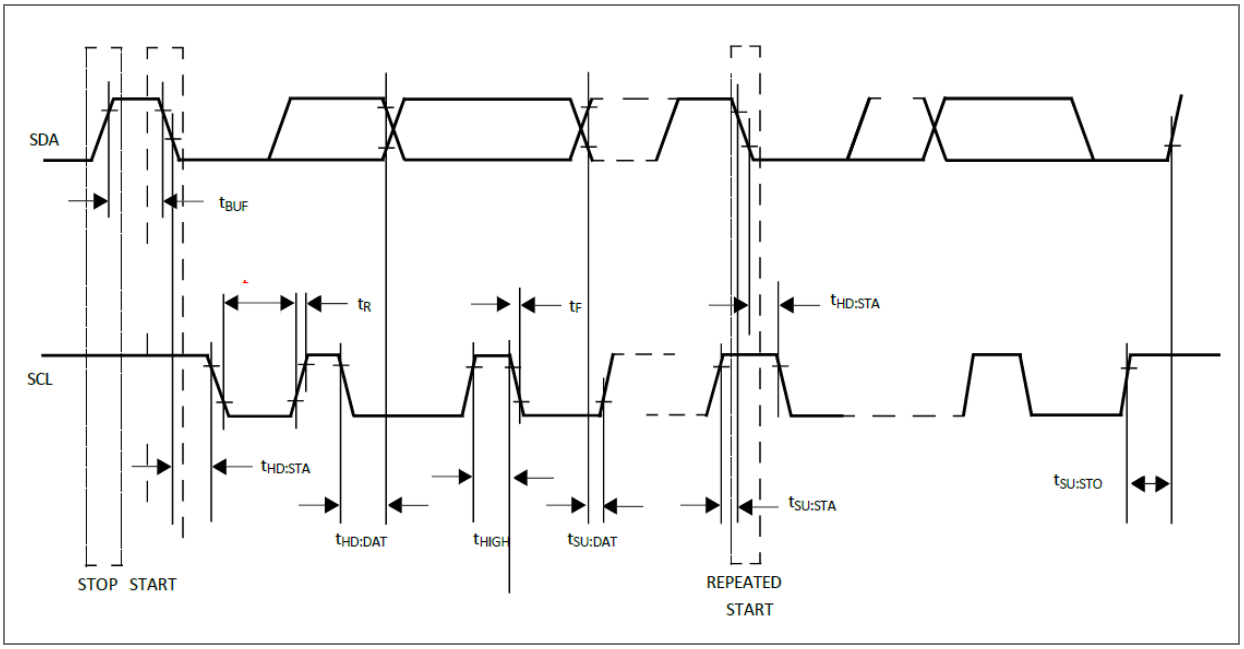
Table 5: I²C specifications

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
I²C mode timings – see Figure 3						
f_{SCLK}	SCL clock frequency		1 / $t_{TIMEOUT}$		400	kHz
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
$t_{HD:STA}$	Hold time (repeated) START Condition(7)		0.6			µs
t_{LOW}	LOW period of SCL clock		1.3			µs
t_{HIGH}	HIGH period of SCL clock		0.6			µs
$t_{SU:STA}$	Setup time for a repeated START condition		0.6			µs
$t_{HD:DAT}$	Data hold time(8)		0		0.9	µs
$t_{SU:DAT}$	Data setup time(9)		100			ns
t_R	Rise time of both SDA and SCL signals		20 + 0.1C_B		300	ns
t_F	Fall time of both SDA and SCL signals		20 + 0.1C_B		300	ns
$t_{SU:STO}$	Setup time for STOP condition		0.6			µs
C_B	Capacitive load for each bus line	C_B - total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O capacitance (SDA, SCL)				10	pF

(1) For V_{BAT}=4.5 V, SCL=1.8 V, SDA=1.8 V maximum I_{STANBY} is <16 µA.
(2) To improve efficiency at low output currents, the active part of the internal switching transistor PMOS is reduced in size to 1/5 its original size. This reduces the current required to drive the PMOS transistor and therefore improves overall efficiency at low output currents.
(3) The maximum current driving capability depends on supply voltage V_{VIN}, LED forward voltage and coil peak current limit.
(4) Due to slope compensation of the current limit, I_{LIMIT} changes with duty cycle – see Figure 17.
(5) The logic input levels V_{IH} and V_{IL} allow for 1.2 V or 1.8 V supplied driving circuit.
(6) A pulldown current of 36 µA is equal to a pulldown resistor of 42 kΩ at 1.5 V.
(7) After this period, the first clock pulse is generated.
(8) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(9) A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ = to 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\,max}$ + $t_{SU:DAT}$ = 1000 + 250 = 1250 ns before the SCL line is released.

5.2 Timing diagrams

Figure 3: I²C mode timing diagram



6 Typical operating characteristics

V_{VIN} = 3.7 V, T_A = 25 °C (unless otherwise specified), LED: ams OSRAM Phaser 2 (VF_{LED} = 3.8 V at 1 A).

Figure 4: DCDC efficiency vs. V_{VIN}

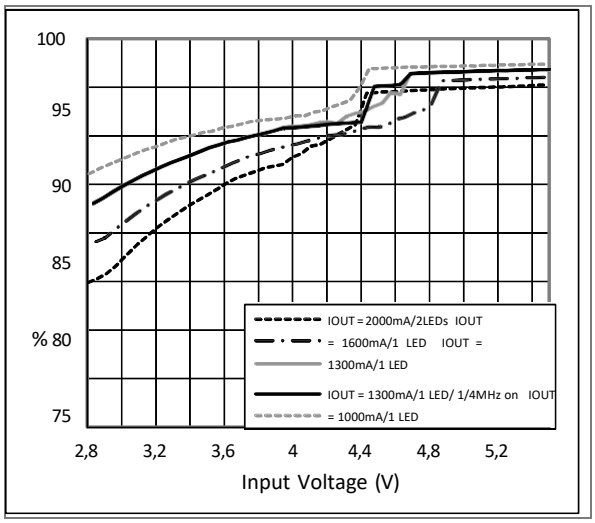


Figure 5: Application efficiency (P_{LED}/P_{VIN}) vs. V_{VIN}

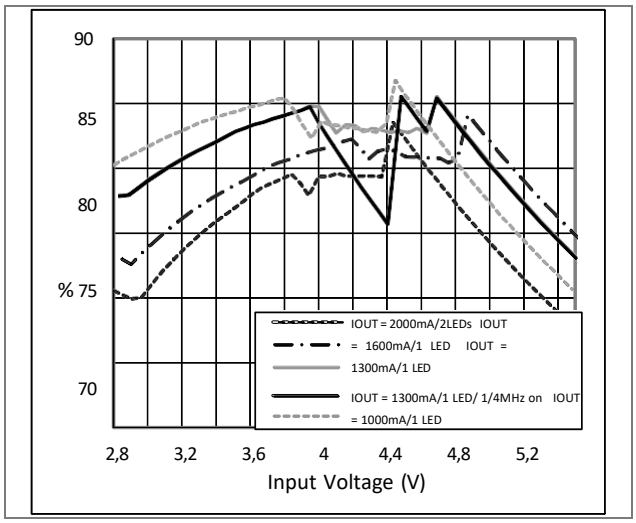


Figure 6: Battery current vs. V_{VIN}

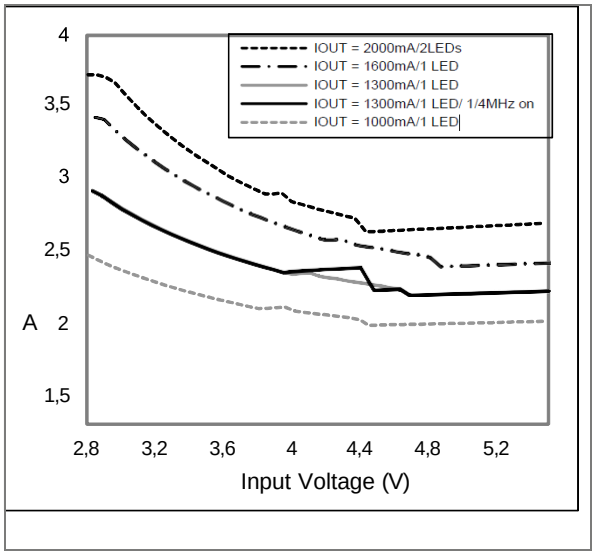


Figure 7: Efficiency at low currents (300 mA)

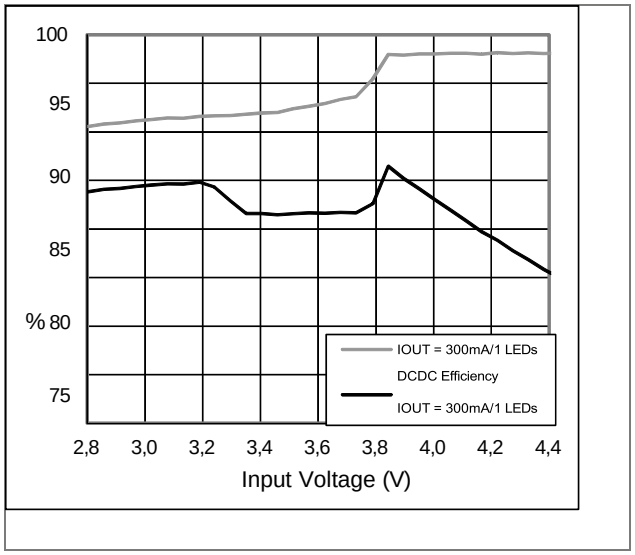


Figure 8: $I_{LED\ STARTUP}$ (I_{LED_OUT} = 1.0 A)

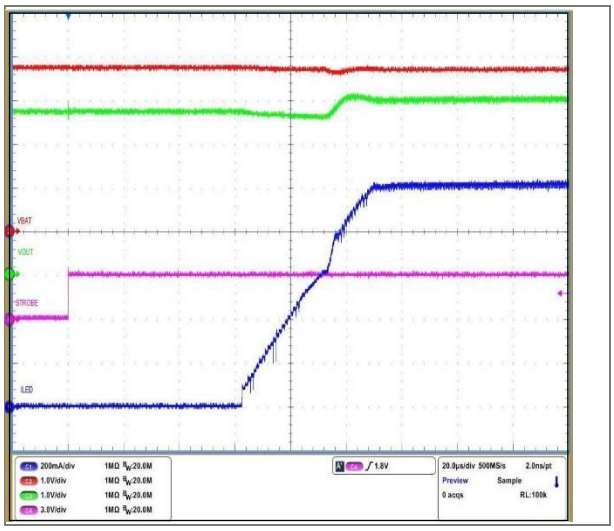


Figure 9: I_{VIN}, $I_{LED\ STARTUP}$ (I_{LED_OUT} = 800 mA)

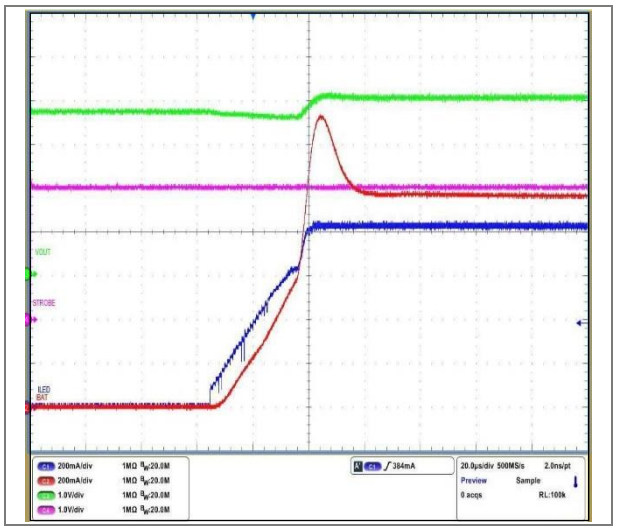


Figure 10: $I_{LED\ STARTUP}$ (I_{LED_OUT} = 60 mA)

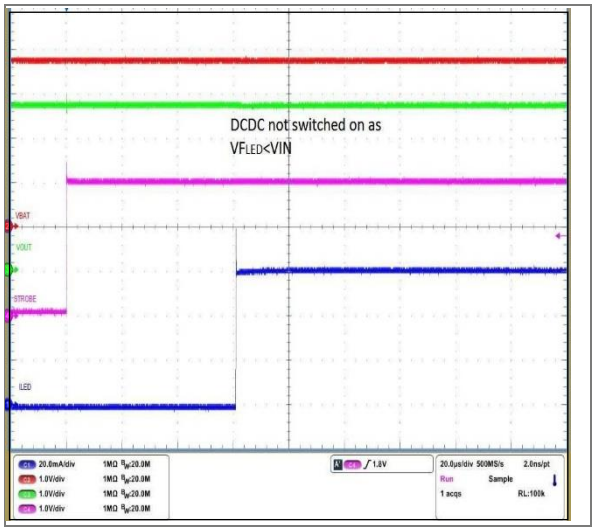


Figure 11: V_{OUT} / I_{LED_OUT} ripple, I_{LED_OUT} = 1.0 A

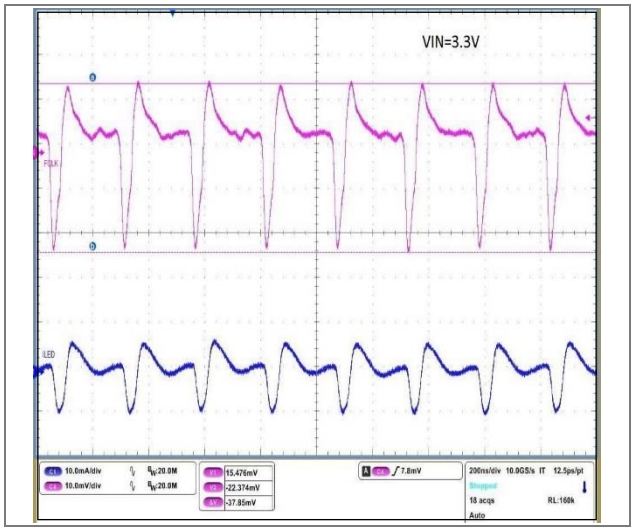


Figure 12: I_{LED} rampdown (ILED_OUT = 1.0 A)

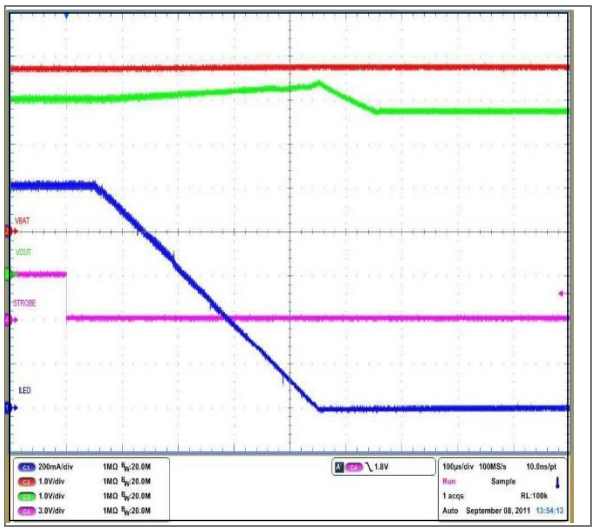


Figure 13: I_{LED_OUT} vs. T_{AMB}

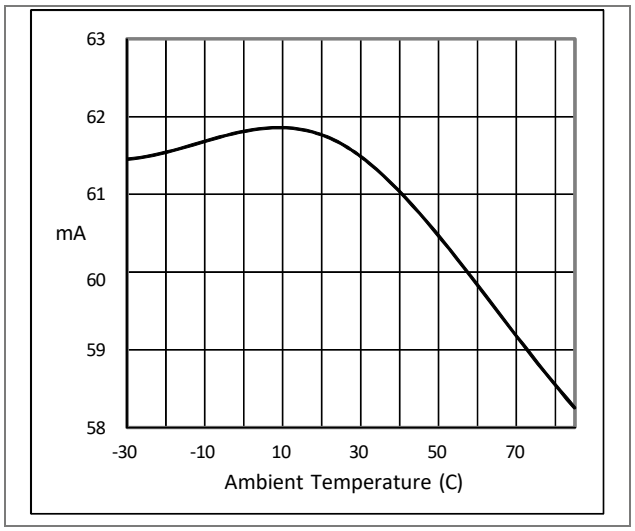


Figure 14: Oscillator frequency f_{CLK} vs. T_{AMB}

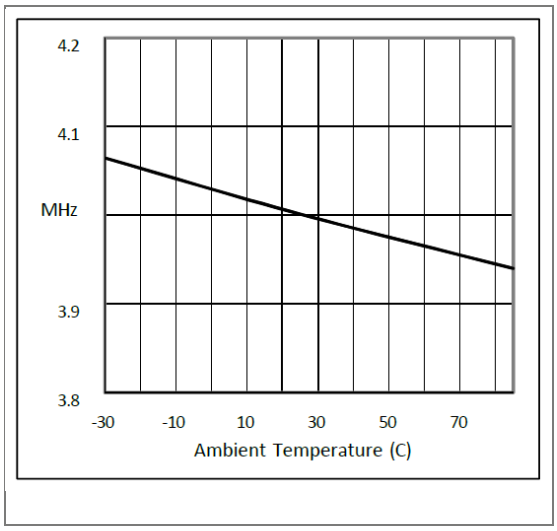
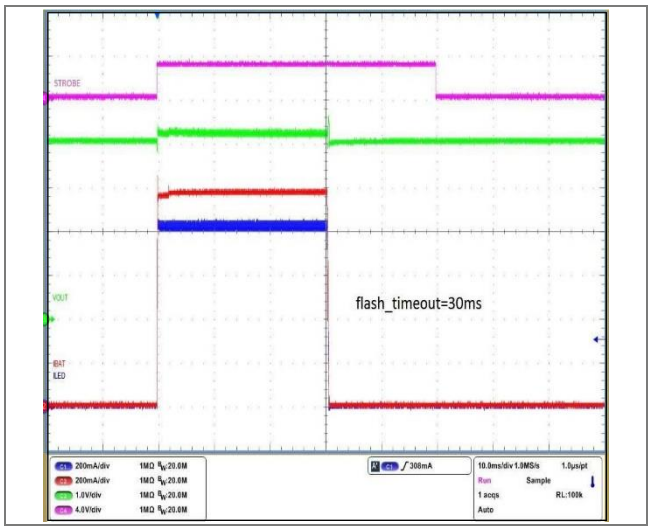


Figure 15: Flash timeout



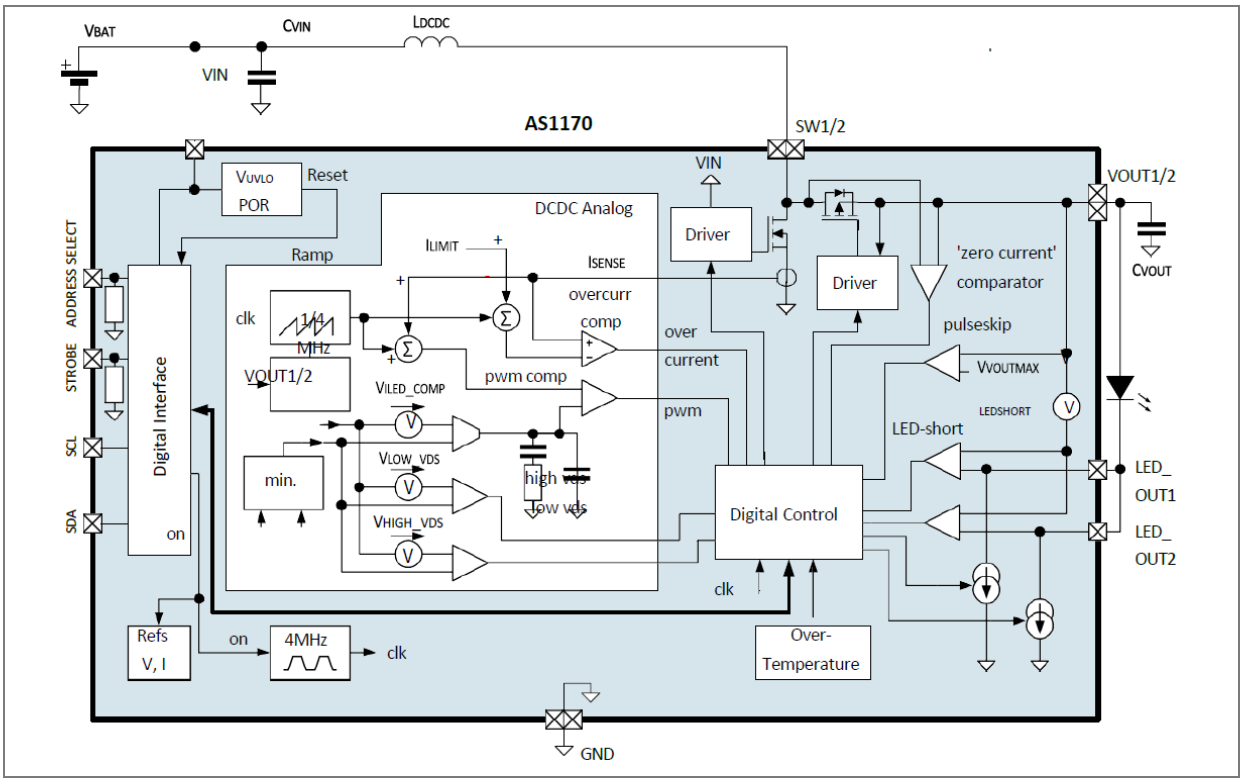
7 Detailed description

The AS1170 is a high performance DCDC step up converter with internal PMOS and NMOS switches. Its output is connected to one or two flash LEDs[1] with an internal current sink. The device is controlled by the pins SDA and SCL in I²C mode.

The actual operating mode like standby, assist light, indicator or flash mode, can then be chosen by the interface. If not in standby mode, the device automatically enters shutdown mode by keeping SCL low for more than t[2].

The AS1170 includes a fixed frequency DCDC step-up with accurate startup control. Together with the current sink (on LED_OUT1/2) it includes several protection and safety functions.

Figure 16: Internal circuit Diagram



[1] If two LEDs are connected, it is possible to operate each of the two LEDs individually as the LED current can be selected individually.
[2] Following registers are reset to their default value if the timeout expires: out_on=0, mode_setting=00, const_v_mode=0.

7.1 Softstart / soft ramp down

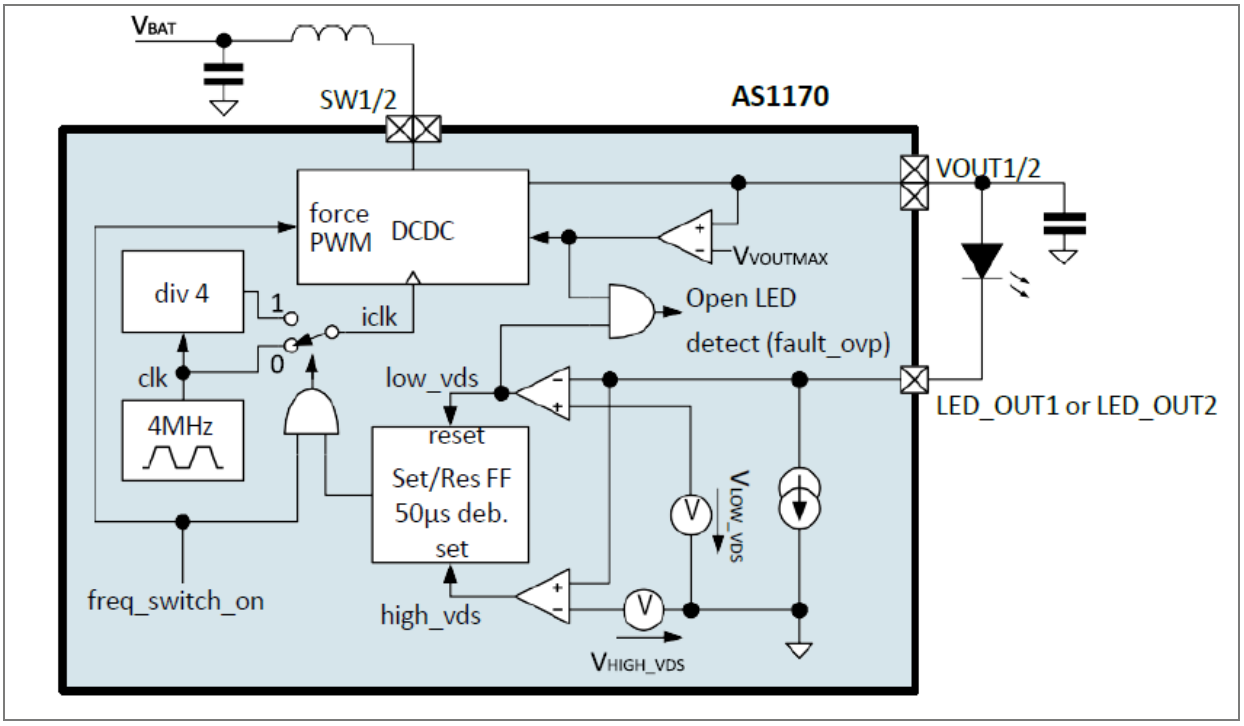
During startup and ramp down the LED current is smoothly ramped up and ramped down. If the DCDC converter goes out of regulation (measured by monitoring the voltage across the current sinks), the ramp up is temporarily stopped in order for the DCDC to return to regulation[3].

7.2 4 MHz / 1 MHz operating mode switching

If freq_switch_on=1 and in flash and assist light mode (indicator mode or low current mode using PWM mode -see mode_setting - always will use pulseskip) if led_current1>=40h and led_current2>=40h and current_boost=0, the DCDC converter always operates in PWM mode (exception: PFM mode is allowed during startup) to reduce EMI in EMI sensitive systems. For flash and assist light mode and high duty cycles close to 100% on-time (maximum duty cycle) of the PMOS, the DCDC converter can switch into a 1 MHz operating mode and maximum duty cycle to improve efficiency for this load condition[4]. The DCDC converter returns back to its normal 4 MHz operating frequency when load or supply conditions change. Due to this switching between two fixed frequencies the noise spectrum of the system is exactly defined and predictable. If improved efficiency is required, the fixed switching between 1 MHz / 4 MHz can be disabled by freq_switch_on=0. In this case pulseskip will be used.

[3] The actual value of the LED current setting can be readout by the register led_current_actual to allow the camera processor to adopt to the actual operating conditions.
[4] Efficiency compared to a 4 MHz only DCDC converter forced to operate with minimum duty cycle.

Figure 17: Internal circuit of 4 MHz / 1 MHz selection



(1) For simplicity Figure 17 shows only a single current sink.

7.3 Protection and fault detection functions

The protection functions protect the AS1170 and the LED(s) against physical damage. In most cases a fault register bit is set, which can be readout by the I²C interface. The fault bits are automatically cleared by an I²C readout of the fault register. Additionally the DCDC is stopped and the current sinks are disabled[5] by resetting out_on=0, mode_setting=00.

[5] Applies for all faults.

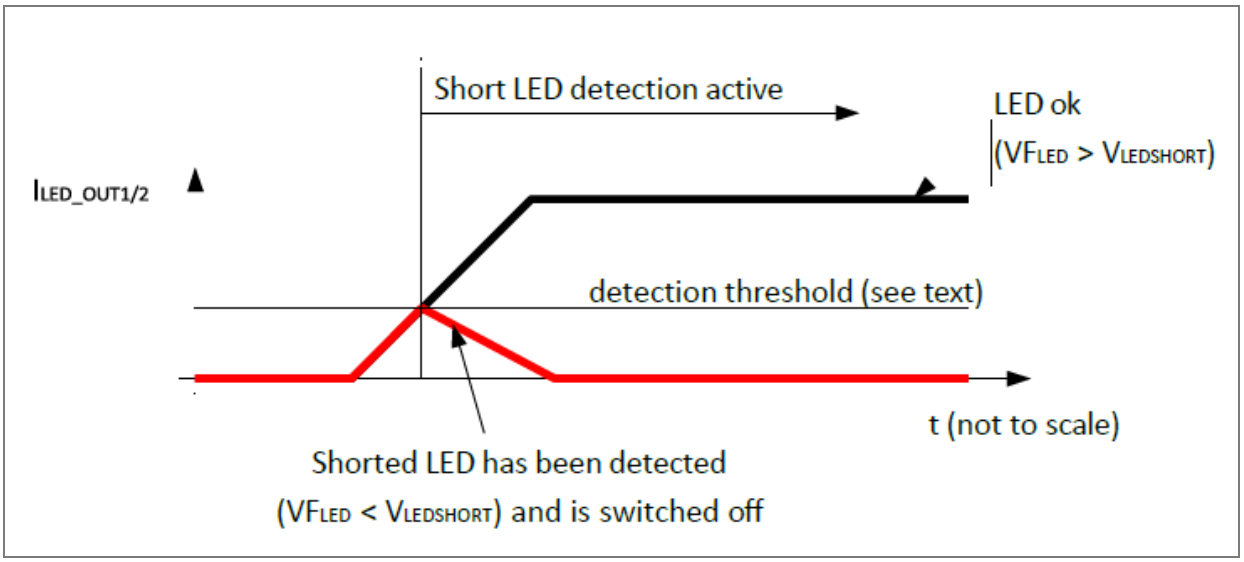
7.4 Overvoltage protection

In case of no or a broken LED(s) at the pin LED_OUT1/2 and an enabled DCDC converter, the voltage on VOUT1/2 rises until it reaches $V_{VOUTMAX}$ (overvoltage condition) and the voltage across the current source is below low_vds[6], the DCDC converter is stopped, the current sources are disabled and the bit fault_ovp is set[7].

7.5 Short circuit protection

After the startup of the DCDC converter, the voltage on LED_OUT1/2 is continuously monitored and compared against $V_{LEDSHORT}$ if the LED current is above 14 mA[8] (current_boost=0), 15.6 mA (current_boost=1)[9]. If the voltage across the LED (VF_{LED} = VOUT1/2-LED_OUT1/2) stays below $V_{LEDSHORT}$, the DCDC is stopped (as a shorted LED is assumed), the current sinks are disabled and the bit fault_led_short is set. In a dual LED configuration for the AS1170, if a single shorted LED is detected, this LED is disabled and the device continuous operation with the other LED.

Figure 18: Short LED detection



[6] If overvoltage is reached, but none of the low_vds comparator(s) triggers, VOUT1/2 is still regulated below $V_{VOUTMAX}$.
[7] In constant voltage mode (5V generation, register bit const_v_mode=1) this fault is disabled.
[8] Measured for each LED_OUT1/2 pin.
[9] To avoid errors in short LED detection for LEDs with a high leakage current.

7.5.1 Over temperature protection

The junction temperature of the AS1170 is continuously monitored. If the temperature exceeds T_{OVTEMP}, the DCDC is stopped, the current sinks are disabled (instantaneous) and the bit fault_overtemp is set. The driver is automatically re-enabled[10] once the junction temperature drops below T_{OVTEMP}-$T_{OVTEMPHYST}$.

7.5.2 Flash timeout

If the flash is started a timeout timer is started in parallel. If the flash duration defined by the STROBE input (strobe_on = 1 and strobe_type = 1) exceeds $t_{FLASHTIMEOUT}$ (adjustable by register), the DCDC is stopped and the flash current sinks (on pin LED_OUT1/2) are disabled and fault_timeout is set.

If the flash duration is defined by the timeout timer itself (strobe_on = 0, the register fault_timeout is set after the flash has been finished.

7.5.3 Supply undervoltage protection

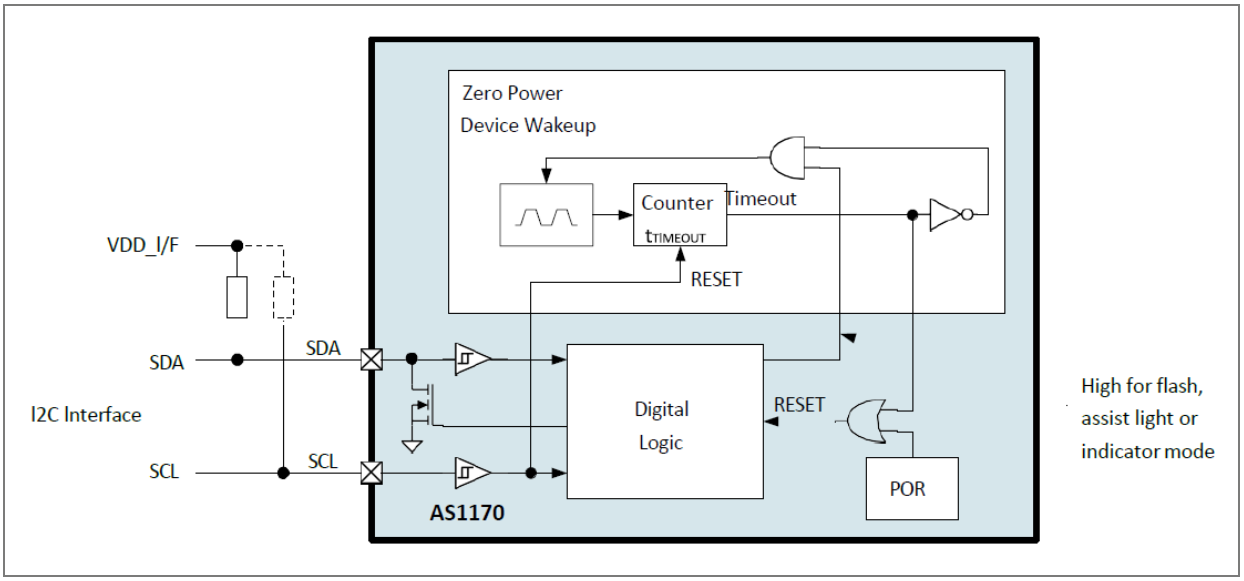
If the voltage on the pin V_{IN} (=battery voltage) is or falls below V_{UVLO}, the AS1170 is kept in shutdown state and all registers are set to their default state.

7.5.4 Wakeup circuit - power off detection

In flash, assist light and indicator mode (register mode_setting=01, 10 or 11) and out_on=1, if SCL is L for more than $t_{TIMEOUT}$, shutdown mode is automatically entered. This feature automatically detects a power-off of the controlling circuit driving SCL and SDA (VDD_I/F goes to 0 V e.g. due to a low power condition of the driving circuit).

[10] In constant voltage mode (const_v_mode=1) the DCDC will not be automatically re-enabled.

Figure 19: Device shutdown and wakeup



In shutdown mode once pin SCL goes high for the first time, the internal counter shown in Figure 20 is immediately reset thus releasing the internal RESET (assuming V_{IN} is above V_{UVLO}) signal and allows instant communication on the I²C bus. Therefore no additional action is required to leave the shutdown mode and start I²C communication.

Purpose of this circuit

The purpose of this circuit is an additional security mechanism.

Assume the user indicator operation (there is no timeout for these operating modes) and the battery slowly drops below the undervoltage limit of the system. The processor would get a reset by the PMIC and the LDO operating VDD_I/F is switched off, but the processor might not have been able to switch-off the indicator operation of the AS1170. Due to the implemented security mechanism the AS1170 detects a power off of VDD_I/F and automatically enters shutdown.

7.5.5 Current consumption in standby/shutdown mode

The AS1170 is designed to draw minimum current in standby and shutdown mode. There is a small difference in current consumption between these two operating modes (typ. 300 nA) only due to the internal level shifters (see the Schmitt trigger input buffers connected to SCL and SDA for shifting up the voltage on SCL/SDA (VDD_I/F e.g. 1.8 V) to the supply voltage on V_{IN} (e.g. 3.7 V). If the AS1170 is driven with digital levels close to 0 V/V_{IN}, the current consumption for standby mode is identical to shutdown mode.

7.5.6 Operating mode and currents

The output currents and operating mode are selected according to the following table:

Table 6: Operating mode and current settings

Operating mode and currents

SCL and SDA	STROBE	mode_setting	out_on	Condition	Mode	LED_OUT1/2 output current
SCL low for $t_{TIMEOUT}$ (1)	X	X	X	If previous operating mode was indicator, assist light or flash mode	Shutdown all registers are reset to their default values	0
I2C commands are accepted	X	10, 01 or 11	0		Standby	0
	X	01	1		Indicator mode or low current pwm mode(3)	LED current is defined by the 6LSB bits (bits 5...0) of led_current1 and led_current2 pwm modulated with 31.25 kHz defined by register inct_pwm (1/ 16...4/16)
	X	10	1		Assist light mode	LED current is defined by the 7LSB(2) bits (6...0) of led_current1 and led_current2
	X	11	1	strobe_on = 0	Flash mode; Flash duration defined by flash_timeout	LED current is defined by led_current1 and led_current2 - the current can be reduced during flash, see Flash current reductions below
	0->1			strobe_on = 1 and strobe_type = 0		
	1			strobe_on = 1 and strobe_type = 1	Flash mode; Flash duration defined by strobe input; timeout defined by flash_timeout	

(1) SCL low for $t_{TIMEOUT}$ and operating mode is indicator, assist or flash mode then shutdown mode is entered.

(2) The MSB bit of this register not used to protect the LED; therefore the maximum assist light current = half the maximum flash current.

(3) The low current mode is a general purpose PWM mode to drive less current through the LED in average, but keep the actual pulsed current in a range where the light output from the LED is still specified. As only the 6 LSBs of led_current1 and led_current2 are used the maximum current is limited to 1/4 of the maximum flash current.

7.5.7 Flash current reductions

Current reduction by V_{IN} measurements in flash mode

Due to the high load of the flash driver and the ESR of the battery (especially critical at low temperatures), the voltage on the battery drops. If the voltage drops below the reset threshold of the system would reset. To prevent this condition the AS1170 monitors the battery voltage and keeps it above vin_low_v_run as follows:

Before a flash is started the voltage on V_{IN} is measured. If the voltage is below the setting of vin_low_v the fault_uvlo is set and the flash is disabled (driver stays in shutdown) if vin_low_v_shutdown=1.

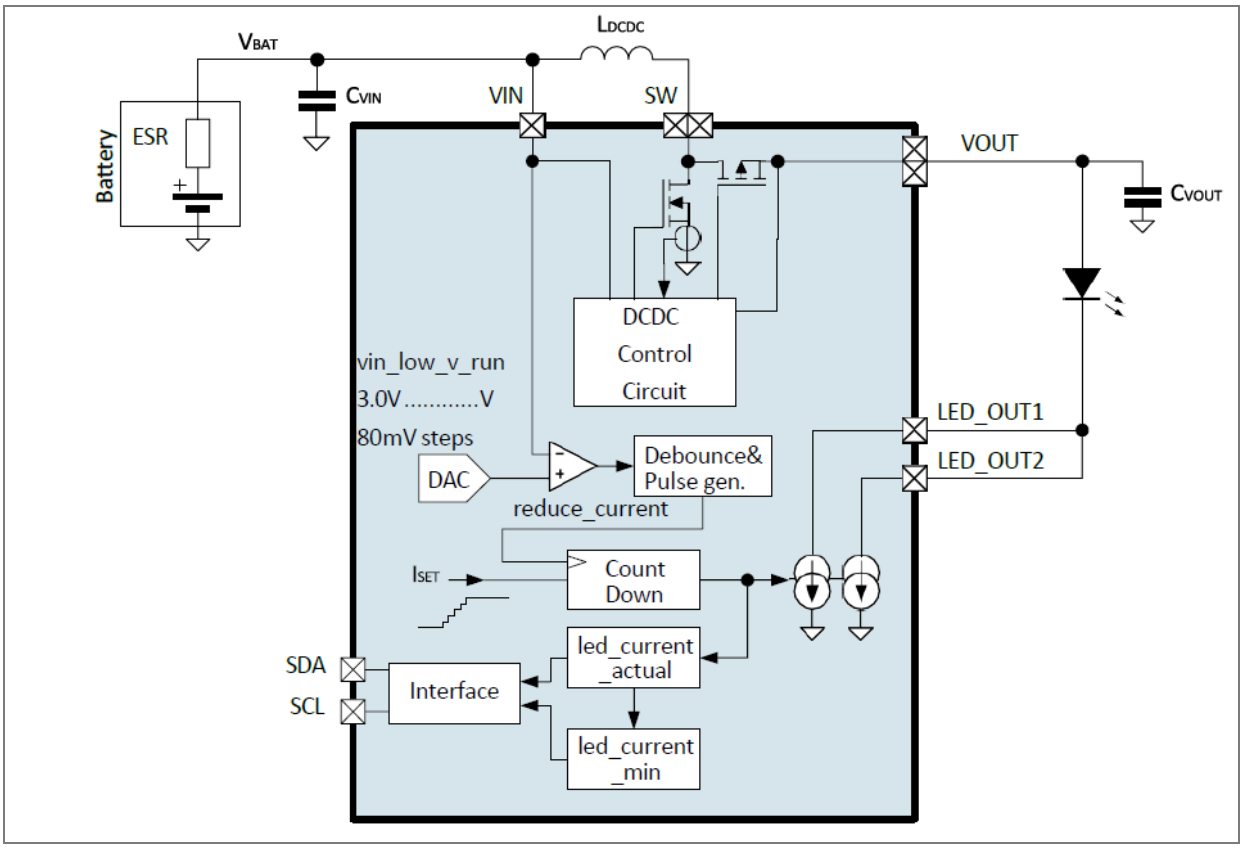
During flash, if the voltage on V_{IN} drops below the threshold defined by vin_low_v_run, the flash current is reduced (or ramping of the current is stopped during flash current startup) and fault_uvlo is set. The timing for the reduction of the current is 8 µs/LSB current change.

During the flash pulse the actual used current can be readout by the register led_current_actual.

After the flash pulse the minimum current can be readout by the register led_current_min - this allows to adjust the camera sensitivity (gain or iso-settings) for the subsequent flash pulse (e.g. when using a pre-flash and a main flash pulse).

The internal circuit for low voltage current reductions are shown in Figure 20.

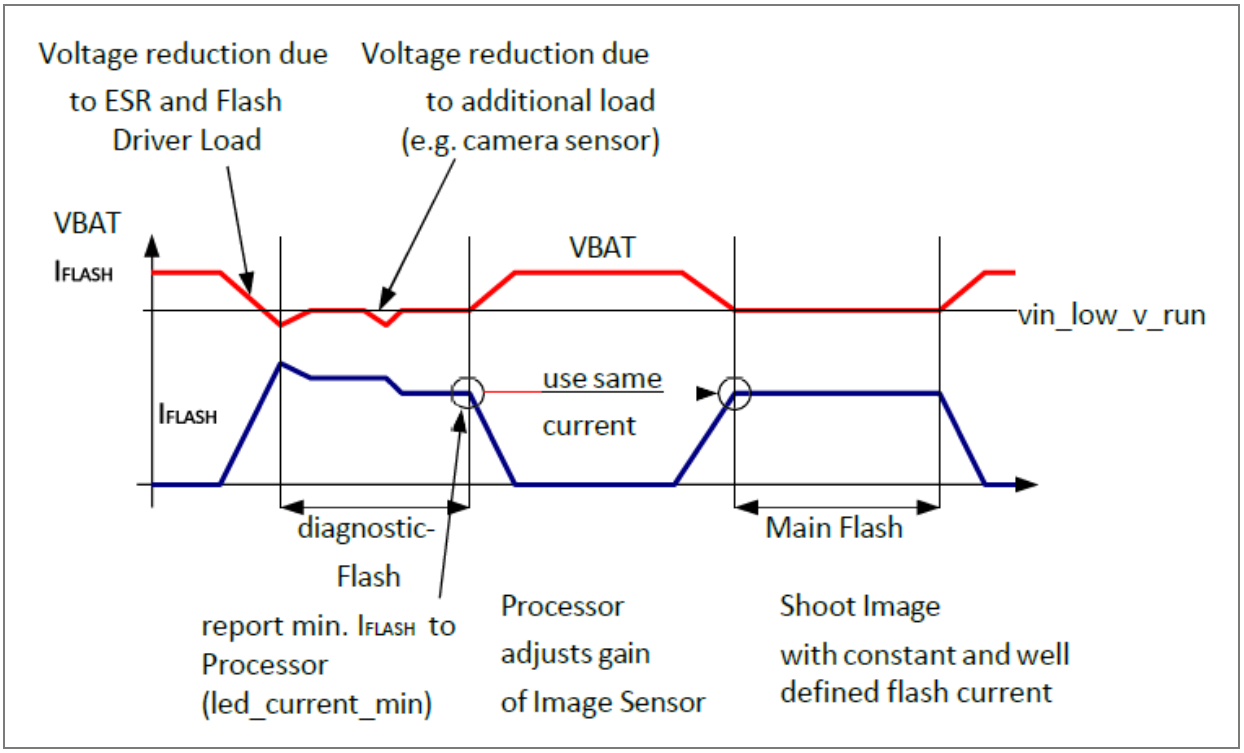
Figure 20: Low voltage current reduction internal circuit



A mobile phone camera flash system can trigger a diagnostic flash and a main-flash:

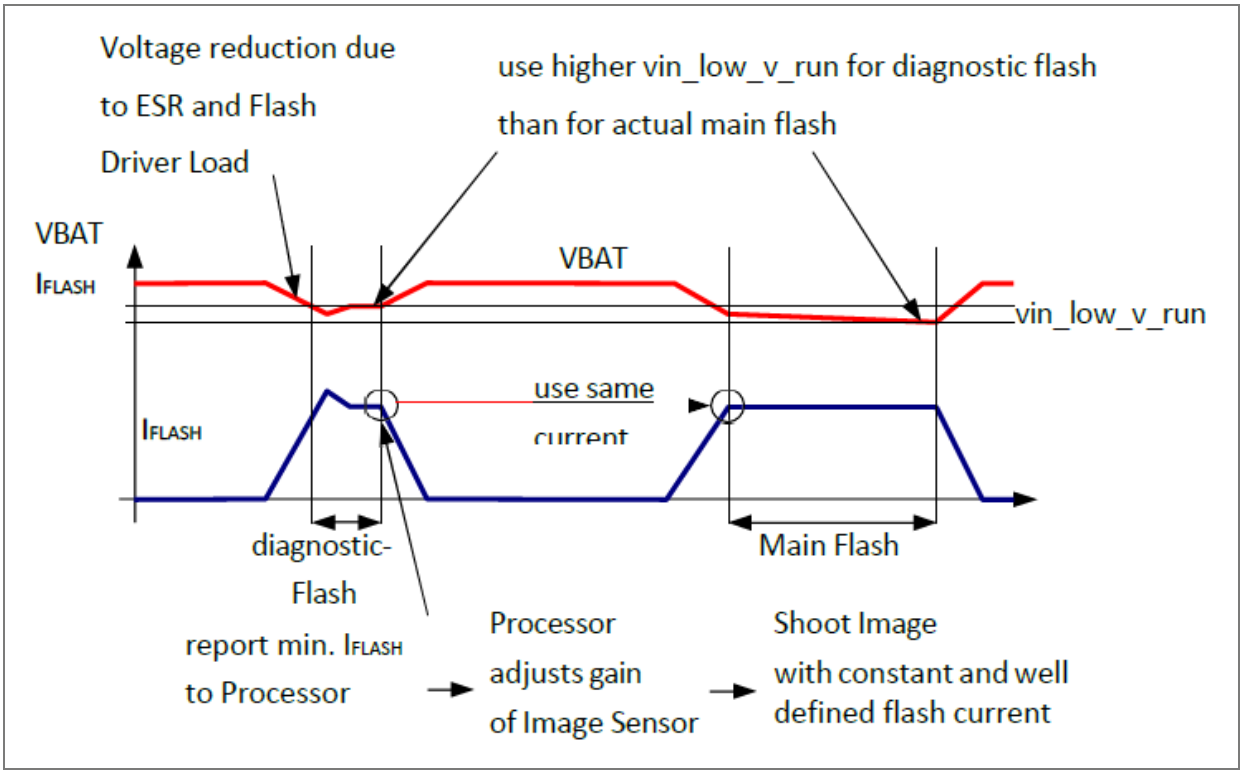
The diagnostic flash is initiated by the processor. After this diagnostic flash, the determined maximum flash current can be read back through the I²C interface from register led_current_min and used for the setting for the main flash. Therefore the current in the main-flash is constant and additionally the camera system can use this current for picture quality adjustments.

Figure 21: Low voltage current reduction waveform with diagnostic-flash and main-flash phase



If the diagnostic flash should be short (e.g. 10 ms) it is recommended to operate this diagnostic flash at slightly higher vin_low_v_run setting compared to the main flash.

Figure 22: Low voltage current reduction waveform with short diagnostic-flash and main-flash phase

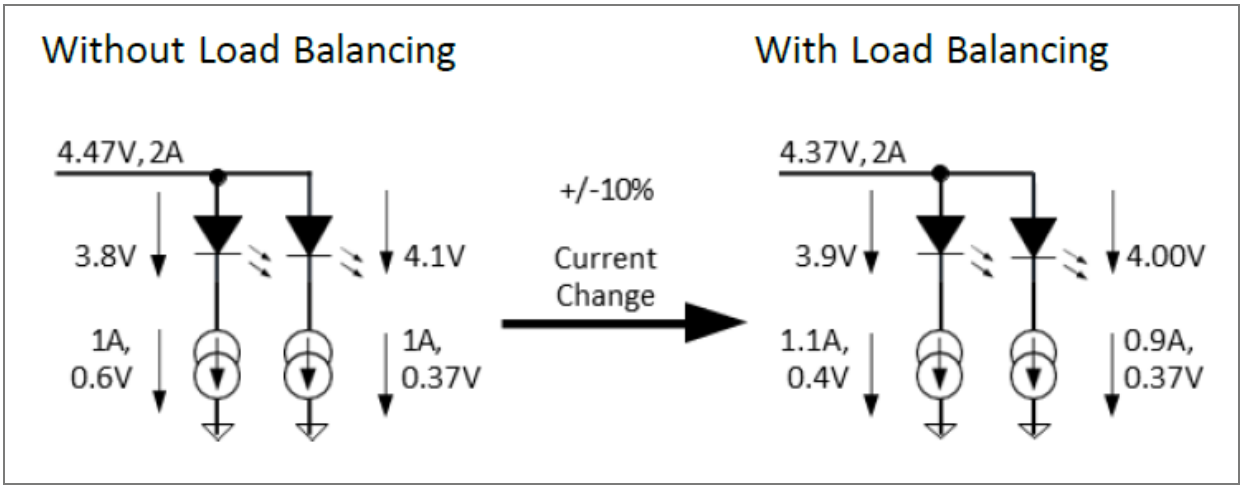


The different settings for vin_low_v_run allow a constant main flash current without dropping V_{IN} below vin_low_v_run.

7.5.8 Load balancing

To improve the efficiency of the AS1170 for LEDs with unmatched forward voltage and reduce the internal power dissipation of the AS1170, set the bit load_balance_on=1. This bit can change the currents through the LEDs by up to ±15% (up to 115%/85% of set current between LED_OUT1 to LED_OUT2) to match the forward voltage of the LED better.

Figure 23: Load balancing



7.5.9 Flash strobe timings

The flash timing are defined as follows:

1. Flash duration defined by register flash_timeout and flash is started immediately when this mode is selected by the I²C command: set strobe_on = 0, start the flash by setting out_on = 1
2. Flash duration defined by register flash_timeout and flash started with a rising edge on pin STROBE: set strobe_on = 1 and strobe_type = 0
3. Flash start and timing defined by the pin STROBE; the flash duration is limited by the timeout timer defined by flash_timeout: set strobe_on = 1 and strobe_type = 1

Figure 24: AS1170 flash duration defined by flash_timeout without using STROBE input

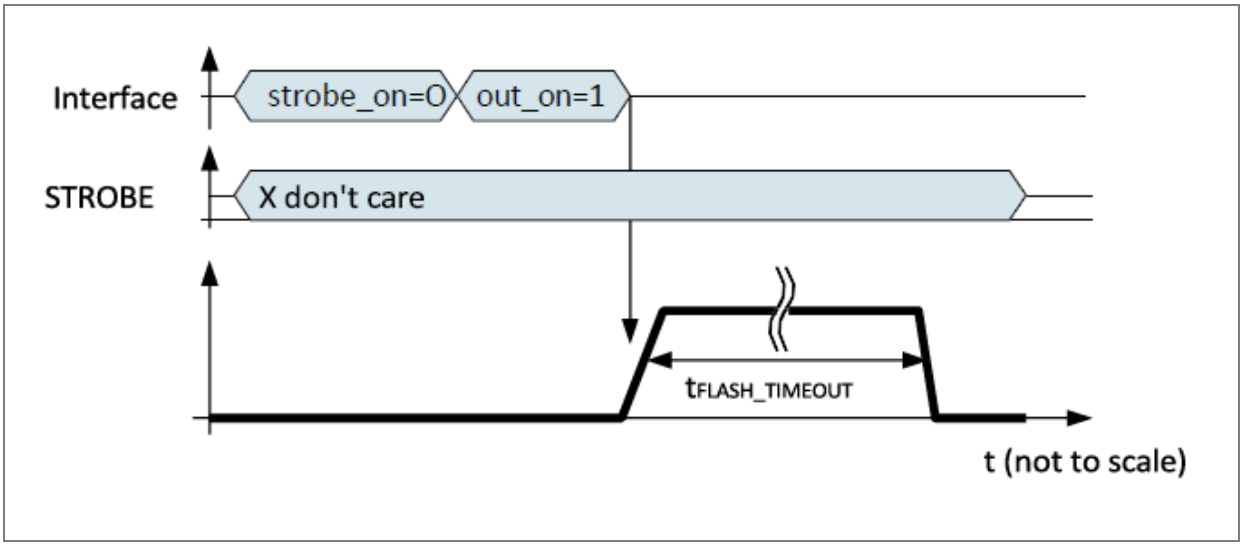


Figure 25: AS1170 flash duration defined by flash_timeout, starting with STROBE rising edge

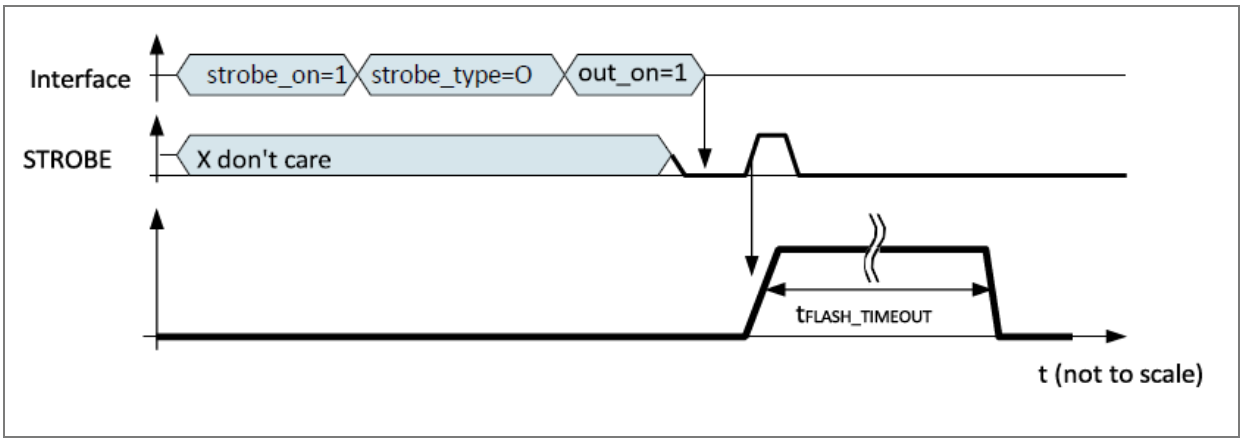


Figure 26: AS1170 flash duration & STROBE defined start, limited by flash_timeout; timer not expired

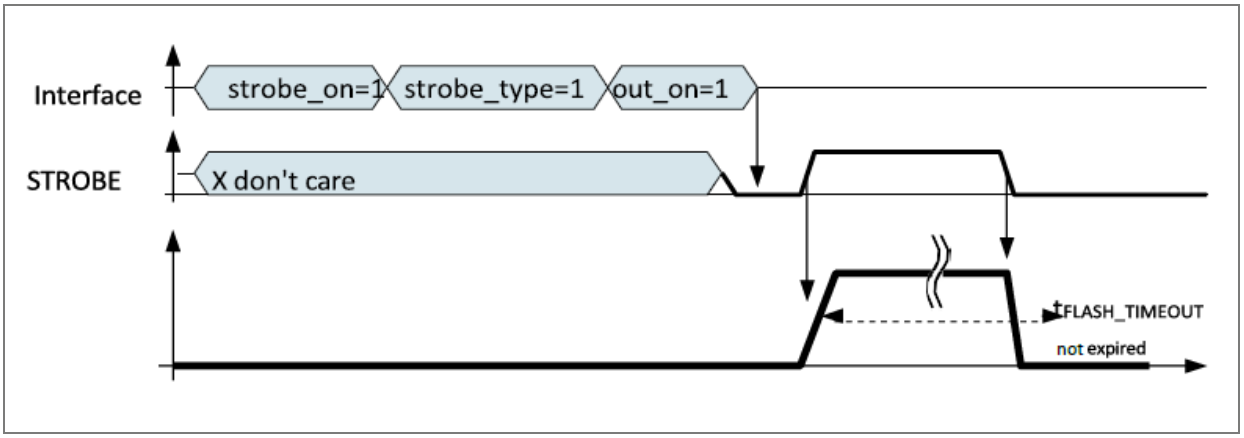
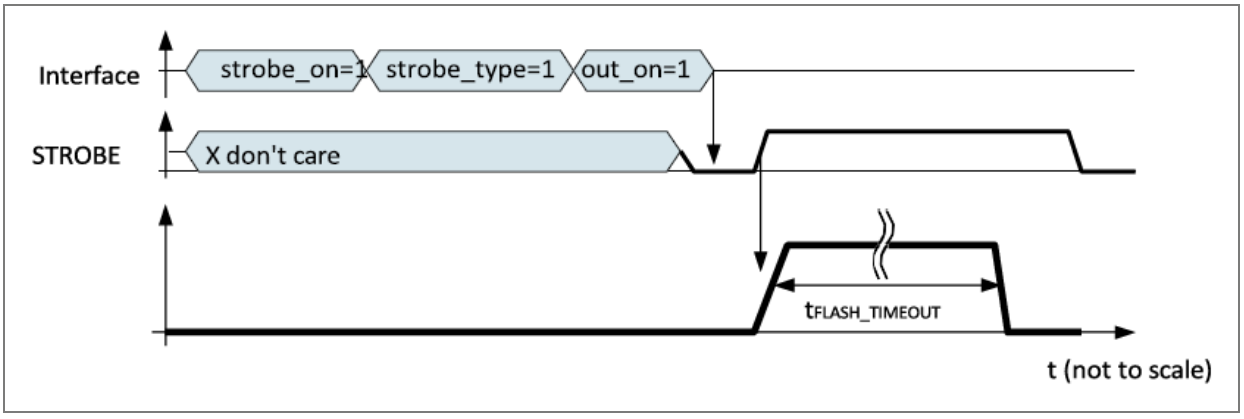


Figure 27: AS1170 flash duration and start defined by STROBE, flash_timeout; timer expired



7.5.10 I²C serial data bus

The AS1170 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The AS1170 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100 kHz maximum clock rate) and a fast mode (400 kHz maximum clock rate) are defined. The AS1170 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy

Both data and clock lines remain HIGH.

Start data transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

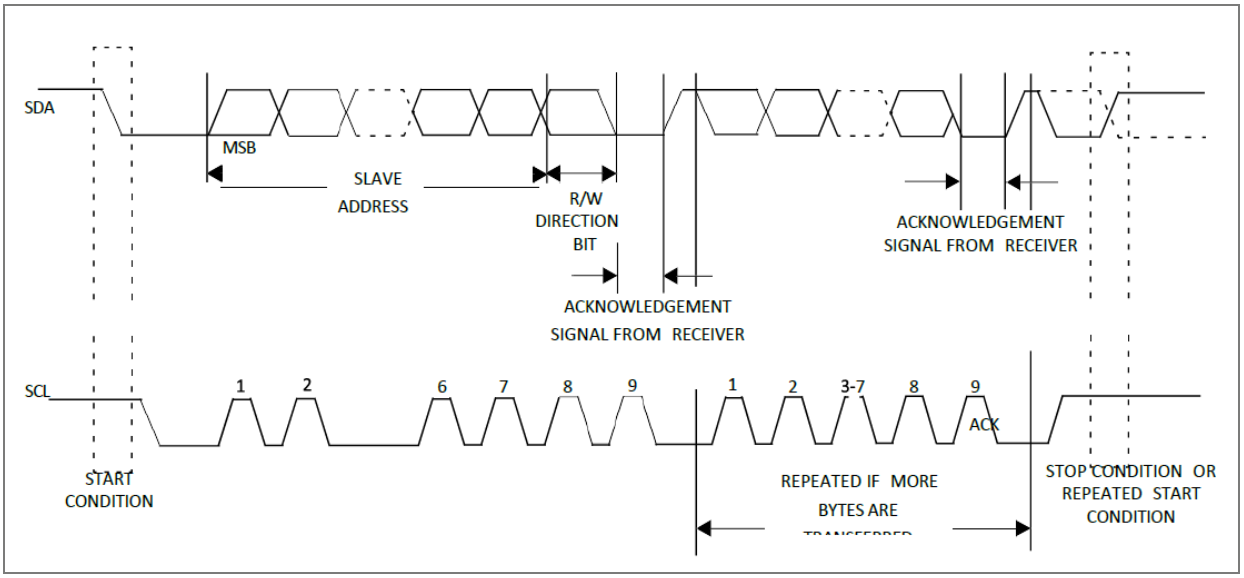
Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 28: Data transfer on I²C serial bus



Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver:**

   The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2. **Data transfer from a slave transmitter to a master receiver:**

   The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The AS1170 can operate in the following two modes:

1. **Slave receiver mode (write mode):**
   Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit. The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit AS1170 address, which is 0x30 (or 0x32 if I²C address select pin is high), followed by the direction bit (R/W), which, for a write, is 0[11]. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the AS1170 acknowledges the slave address + write bit, the master transmits a register address to the AS1170. This sets the register pointer on the AS1170. The master may then transmit zero or more bytes of data, with the AS1170 acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.

2. **Slave transmitter mode (read mode):**
   The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the AS1170 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit AS1170 address, which is 0x30 (or 0x32 if I²C address select pin is high), followed by the direction bit (R/W), which, for a read, is 1[12]. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The AS1170 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The AS1170 must receive a “not acknowledge” to end a read.

[11] The address for writing to the AS1170 is 60h = 01100000b ; or 64h if address select pin is high = 01100010b
[12] The address for reading from the AS1170 is 61h = 01100001b ; or 65h if address select pin is high = 01100011b

Figure 29: Data write - slave receiver mode

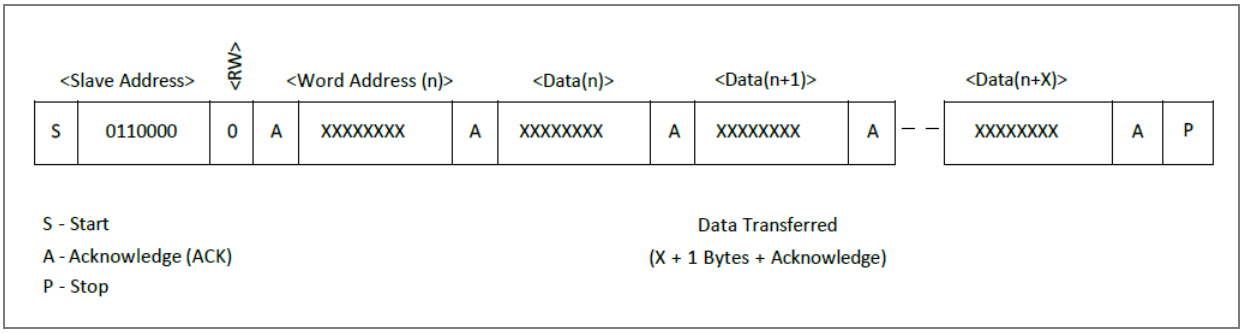


Figure 30: Data read (from current pointer location) - slave transmitter mode

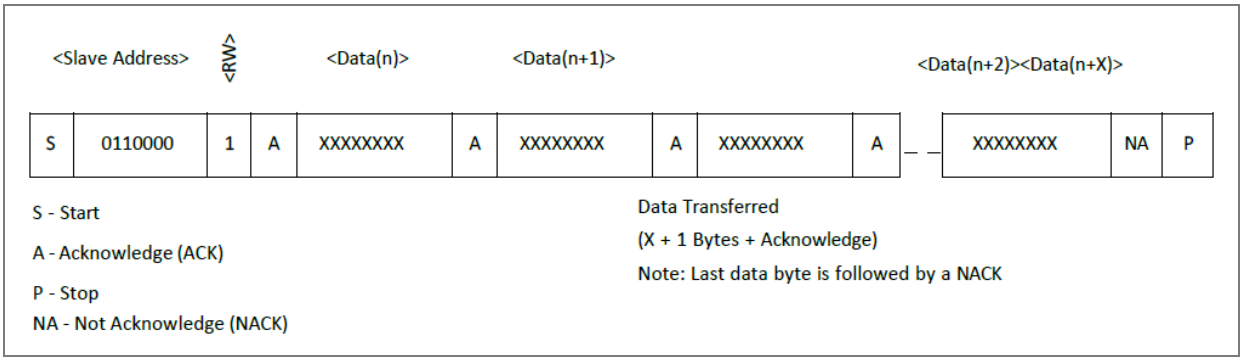
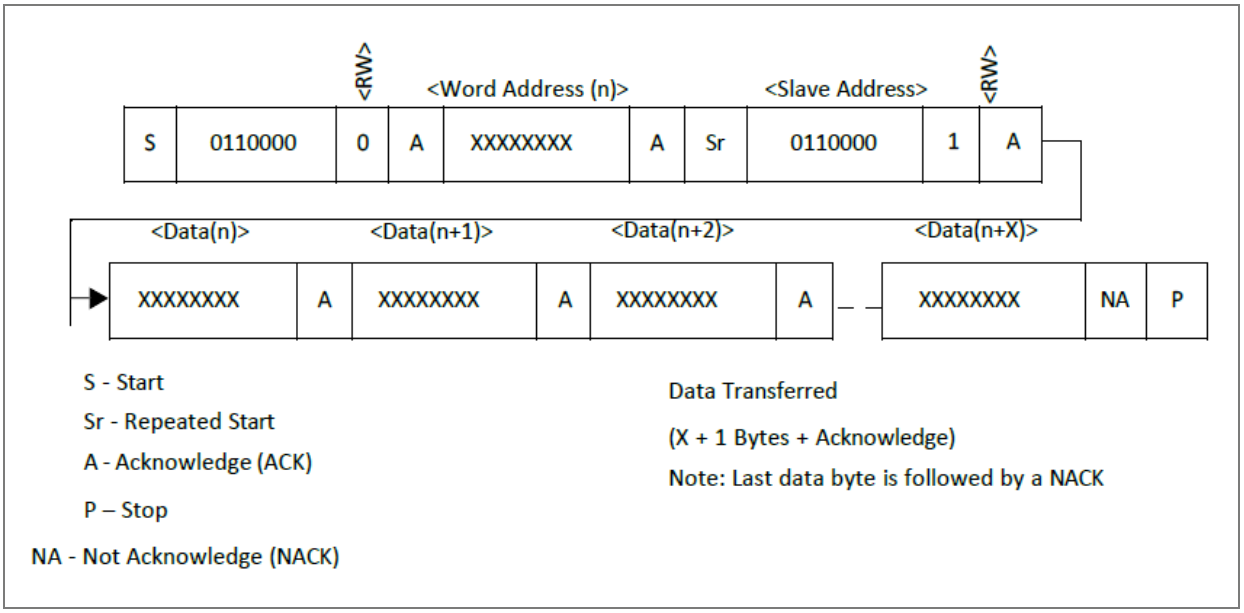


Figure 31: Data read (write pointer, then read) - slave receive and transmit



8 Register description

8.1 ChipID register

Table 7: ChipID register

Addr: 0		ChipID register		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
2:0	*version*	4h	R	AS1170 chip version number.
7:3	*fixed_id*	18h	R	This is a fixed identification (e.g. to verify the I²C communication).

(1) This register has a fixed ID.

8.2 Current set LED1 register

Table 8: Current set LED1 register

Addr: 1		Current set LED1 register		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*led_current1*	9Ch	R/W	**Caution**: Define the current on pin LED_OUT1 assist mode uses bits 6:0 of this current setting (max. half of full current setting) indicator or low current pwm mode uses only 5:0 of this current setting (max. 1/4 of full current setting).

Value	Description
0h	0 mA
1h	3.5 mA
2h	7.1 mA
...	...
3Fh	222.4 mA (maximum current for indicator or low current pwm mode, mode_setting=01)
...	...
7Fh	448.2 mA (maximum current for assist light mode, mode_setting=10)
...	...

Addr: 1		Current set LED1 register		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
				9Ch: 551 mA - default setting
				...: ...
				FEh: 896.5 mA (996.1 mA(2) if current_boost=1)
				FFh: 900 mA (1000 mA(2) if current_boost=1)

(1) This register defines design versions.
(2) Do not use current_boost=1 for currents <= 900 mA.

8.3 Current set LED2 register

Table 9: Current set LED2 register

Addr: 2		Current set LED2 register		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*led_current2*	9Ch	R/W	Define the current on pin LED_OUT2 in flash mode assist mode uses bits 6:0 of this current setting (max. half of full current setting) indicator or low current pwm mode uses only 5:0 of this current setting (max. 1/4 of full current setting). **Value** / **Description** 0h: 0 mA 1h: 3.5 mA 2h: 7.1 mA ...: ... 3Fh: 222.4 mA (maximum current for indicator or low current pwm mode, mode_setting=01) ...: ... 7Fh: 448.2 mA (maximum current for assist light mode, mode_setting=10) ...: ... 9Ch: 551 mA - default ...: ... FEh: 896.5 mA (996.1 mA(2) if current_boost=1) FFh: 900 mA (1000 mA(2) if current_boost=1)

(1) This register defines LED currents.

(2) Do not use current_boost=1 for currents <= 900 mA

8.4 Low voltage register

Table 10: Low voltage register

Addr: 4		Low voltage register		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
2:0	*vin_low_v_run*	4h	R/W	Voltage level on V_{IN} where current reduction triggers during operation (see Current Reduction by V_{IN} measurements in flash mode - only in flash mode; if V_{IN} drops below this voltage during current ramp up, the current ramp up is stopped; during operation the current is decreased until the voltage on V_{IN} rises above this threshold - fault_uvlo is set. **Value** / **Description** 0h: Function is disabled 1h: 3.0 V 2h: 3.07 V 3h: 3.14 V 4h: 3.22 V - default 5h: 3.3 V 6h: 3.38 V 7h: 3.47 V
5:3	*vin_low_v*	5h	R/W	Voltage level on V_{IN} where driver will change current before startup (only in flash mode) if before startup (out_on set from 0 to 1), the voltage on V_{IN} is below vin_low_v, the current is changed to 0 = shutdown (vin_low_v_shutdown=1) and fault_uvlo is set. **Value** / **Description** 0h: Function is disabled 1h: 3.0 V 2h: 3.07 V 3h: 3.14 V 4h: 3.22 V 5h: 3.3 V - default 6h: 3.38 V 7h: 3.47 V

Addr: 4		Low voltage register			
Bit	**Bit name**	**Default**	**Access**	**Bit description**	
6	*vin_low_v_shutdown*	0	R/W	Enables shutdown of current reduction under low voltage conditions.	
				Value	**Description**
				0	If before startup (out_on set from 0 to 1), the voltage on V_{IN} is below vin_low_v, the current is changed to fault_uvlo is set.
				1	If before startup (out_on set from 0 to 1), the voltage on V_{IN} is below vin_low_v, the operating mode stays in shutdown (zero LED current) and fault_uvlo is set.
7	*const_v_mode*	0	R/W	Enables constant output voltage mode.	
				Value	**Description**
				0	Normal operation defined by mode_setting.

(1) This register defines the operating mode with low battery voltage.

8.5 Flash timer register

Table 11: Flash timer register

Addr: 5		Flash timer register			
Bit	**Bit name**	**Default**	**Access**	**Bit description**	
7:0	*flash_timeout* (2)	23h	R/W	Define the duration of the flash timer and timeout timer.	
				Value	**Description**
				0h	1 ms
				1h	2 ms
				2h	3 ms
				...	...
				23h	36 ms - default
				...	...
				7F	128 ms
				80	136 ms (now 8 ms LSB steps from here on) (3).
				81	142 ms
				82	150 ms

Addr: 5		Flash timer register			
Bit	**Bit name**	**Default**	**Access**	**Bit description**	
				...	...
				FEh	1144 ms
				FFh	1152 ms

(1) This register identifies the flash timer and timeout settings.
(2) At maximum output current the flash duration should be limited to 120 ms (depending of VF of the LED, thermal design and ambient temperature) to avoid overheating of the AS1170.
(3) Internal calculation for codes above 7Fh: flash timeout [ms] = (flash_timeout-127) * 8 + 256 [ms]

8.6 Control register

Table 12: Control register

Addr: 6		Control register			
Bit	**Bit name**	**Default**	**Access**	**Bit description**	
1:0	*mode_setting*	00	R/W	Define the AS1170 operating mode.	
				Value	**Description**
				00	Shutdown.
				01	Indicator mode (or low current mode using PWM) LED current is defined by the 6LSB bits of led_current1 and led_current2 pwm modulated with 31.25 kHz defined by register inct_pwm (1/16...4/16).
				10	**Assist light mode** Led current is defined by the 7LSB(2) bits of led_current1 and led_current2.
				11	**Flash mode** Led current is defined by led_current1 and led_current2 (out_on and mode_setting are automatically cleared after a flash pulse).
2	*reserved*	X	R	Reserved - don't use, always write 0.	
3	*out_on*	0	R/W	Enables the output current sinks (pin LED_OUT1/2).	
				Value	**Description**
				0	Outputs disabled.
				1	Outputs enabled (out_on and mode_setting are automatically cleared after a flash pulse).
4	*auto_strobe*	1	R/W	Enables the auto trigger of flash mode with strobe pin.	
				Value	**Description**
				0	Single Flash / Strobe mode.
				1	In strobe mode, there is no need after flash timeout, the mode_setting and out_on bits are not cleared. A new pulse on STROBE pin will retrigger the flash again. There is no need to rewrite the CONTROL register with I²C command.

(1) This register identifies the operating mode and includes an all on/off bit.
(2) The MSB bit of this register not used to protect the LED; therefore the maximum assist light current = half the maximum flash current.

8.7 Strobe signaling register

Table 13: Strobe signaling register

Addr: 7		Strobe signaling register		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6	*strobe_type*	1	R/W	Defines if the STROBE input is edge or level sensitive; see also bit strobe_on. **Value** **Description** 0 STROBE input is edge sensitive. 1 STROBE input is level sensitive.
7	*strobe_on*	1	R/W	Enables the STROBE input. **Value** **Description** 0 STROBE input disabled. 1 STROBE input enabled in flash mode.

(1) This register defines the flash current reducing and mode for STROBE.

8.8 Fault register

Table 14: Fault register

Addr: 8		Fault register		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
0	*fault_uvlo*	0	R/sC(2)	An undervoltage event has happened - see Current Reduction by V_{IN} measurements in Flash Mode. **Value** **Description** 0 No 1 Yes
1	*reserved*	0	R	Reserved - don't use.
2	*reserved*	0	R	Reserved - don't use.
4	*fault_timeout*	0	R/sC(2)	See Flash Timeout. **Value** **Description** 0 No fault. 1 Flash timeout exceeded.
5	*fault_overtemp*	0	R/sC(2)	See Overtemperature Protection.

Addr: 8		Fault register		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
				Value **Description**
				0 No fault.
				1 Junction temperature limit has been exceeded.
6	*fault_led_short*	0	R/sC(2)	See Short Circuit Protection.
				Value **Description**
				0 No fault.
				1 A shorted LED is detected (pin LED_OUT1/2).
7	*fault_ovp*	0	R/sC(2)	See Overvoltage Protection.
				Value **Description**
				0 No fault.
				1 An overvoltage condition is detected (pin VOUT).

(1) This register identifies all the different fault conditions and provide information about the LED detection.
(2) R/sC = Read, self clear; after readout the register is automatically cleared.

8.9 PWM and indicator register

Table 15: PWM and indicator register

Addr: 9		PWM and indicator register		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
1:0	*inct_pwm*	00	R/W	Define the AS1170 PWM with 31.25 kHz operation for indicator or low current mode (mode_setting=01).
				Value **Description**
				00 1/16 duty cycle
				01 2/16 duty cycle
				10 3/16 duty cycle
				11 4/16 duty cycle
2	*freq_switch_on*	0	R/W	Exact frequency switching between 4 MHz/1 MHz for assist and flash modes for operation close to maximum pulse width.
				Value **Description**
				0 Pulseskip operation is allowed for all modes - results in better efficiency.

Addr: 9		PWM and indicator register		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
				1 In flash and assist light mode (indicator mode or low current mode using PWM always will use pulseskip) if led_current1>=40h and led_current2>=40h and current_boost=0, the DCDC is running at 4 MHz or 1 MHz (pulseskip is disabled) - results in improved noise performance.
3	*led_out1above2*	0	R	Measure the voltage difference between LED_OUT1 vs.LED_OUT2 during operation of the DCDC. **Value** **Description** 0 1 V(LED_OUT1) > V(LED_OUT2) + $V_{LED\_OUTCOMP\_HYST}$
4	*led_out2above1*	0	R	Measure the voltage difference between LED_OUT1 vs. LED_OUT2 during operation of the DCDC. **Value** **Description** 0 1 V(LED_OUT2) > V(LED_OUT1) + $V_{LED\_OUTCOMP\_HYST}$
5	*load_balance_on*	0	R/W	Balance the current sinks (up to +/-10% of set current) to improve application efficiency for unmatched LED forward voltages - see Load Balancing. **Value** **Description** 0 Disabled. 1 Enabled.

(1) This register defines the PWM mode (e.g. for indicator) and 4/1 MHz mode switching.

8.10 Minimum LED current register

Table 16: Minimum LED current register

Addr: Eh		Minimum LED current register		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*led_current_min* (2)(3)(4)	00h	R	Minimum current through the current sink (only including all current reductions as described in Current Reduction by V_{IN} measurements in Flash Mode.

(1) This register reports the minimum LED current from the last operation cycle.
(2) Only the current through LED_OUT1 is reported.
(3) As the internal change of this register is asynchronous to the readout, it is recommended to readout the register after the flash pulse. The register will store the minimum current through the LED after e.g. a previous flash. This current can be used for a subsequent flash pulse for a safe operating range.
(4) This register is only set if an actual current reduction happens (fault_uvlo=1) otherwise led_current_min=0.

8.11 Actual LED current register

Table 17: Actual LED current register

Addr: Fh		Actual LED current register		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*led_current_actual* (2)(3)	00h	R	Actual set current through the current sink (including all current reductions as described in Flash Current Reductions including LED current ramp up/down).

(1) This register reports the actual set LED current.
(2) Only the current through LED_OUT1 is reported.
(3) As the internal change of this register is asynchronous to the readout, it is recommended to readout the register twice and compare the results.

8.12 Password register

Table 18: Password register

Addr: 80h		Password register		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*password*	NA	W	Write A1h into this register to enable access to register 81h.

(1) Password protection for register current boost.

8.13 Current boost register

Table 19: Current boost register

Addr: 81h		Current boost register			
Bit	**Bit name**	**Default**	**Access**	**Bit description**	
0	*current_boost* (2)	0	R/W	Boost all LED currents by 11%.	
				Value	**Description**
				0	All LED current are as described in the tables.
				1	All LED current are increased by 11%.

(1) Increase output current by 11%.
(2) Write A1h into register password (0x80) to enable access to this register (password unlocking is only valid for a single I²C access) - required on any read or write access to this register.

9 Register map

Table 20: Register map (1)

Register definition	Addr	Default	<b7>	<b6>	<b5>	<b4>	<b3>	<b2>	<b1>	<b0>
ChipID	0	Bxh	fixed_id						version	
Current set LED1	1	9Ch	led_current1							
Current set LED2	2	9Ch	led_current2							
Low voltage	4	2Ch	const_v_mode	vin_low_v_shutdown	vin_low_v			vin_low_v_run		
Flash timer	5	23h	flash_timeout							
Control	6	00h				auto_strobe	out_on	reserved	mode_setting	
Strobe signalling	7	C0h	strobe_on	strobe_type						
Fault	8	00h	fault_ovp	fault_led_short	fault_overtemp	fault_timeout	fault_tx mask	reserved	reserved	fault_uvlo
PWM and Indicator	9	00h			load_balance_on	led_out2above1	led_out1above2	freq_switch_on	inct_pwm	load_balance_on
Minimum LED current	Eh	00h	led_current_min							
Actual LED current	Fh	00h	led_current_actual							
Password register	80h	00h	password							
Current boost	81h	00h								current_boost

(1) Always write ’0’ to undefined register bits (e.g. to bits 4..7 of register 6).

10 Application information

10.1 External components

10.1.1 Input capacitor C_{VIN}

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. Ceramic capacitors are required for input decoupling and should be located as close to the device as is practical.

Table 21: Recommended input capacitor

Part number	C	TC code	Rated voltage	Size	Manufacturer
GRM188R60J106ME47	10 µF >3 µF @ 4.5 V > 2 µF @ 5.25 V	X5R	6.3 V	0603	Murata
LMK107BBJ106MA	10 µF > 3 µF @ 4.5 V	X5R	6.3 V	0603	Taiyo Yuden

If a different input capacitor is chosen, ensure similar ESR value and at least 3 µF capacitance at the maximum input supply voltage. Larger capacitor values (C) may be used without limitations.

Add a smaller capacitor in parallel to the input pin V_{IN} (e.g. Murata GRM155R61C104, >50 nF @ 3 V, 0402 size).

10.1.2 Output capacitor C_{VOUT}

Low ESR capacitors should be used to minimize VOUT ripple. Multi-layer ceramic capacitors are recommended since they have extremely low ESR and are available in small footprints. The capacitor should be located as close to the device as is practical.

X5R dielectric material is recommended due to their ability to maintain capacitance over wide voltage and temperature range.

Table 22: Recommended output capacitor

Part number	C	TC code	Rated voltage	Size	Manufacturer
GRM219R61A116U	10 µF ±10% > 4.2 µF @ 5 V	X5R	10 V	0805	Murata
GRM188R60J106ME84	10 µF ±20% > 4.2 µF @ 4 V	X5R	6.3 V	0603 (1.6x0.8x0.85 mm max. 0.95 mm height)	

(1) Use only for V_{LED} < 3.75 V.

If a different output capacitor is chosen, ensure similar ESR values and at least 4.2 µF capacitance at 5 V output voltage.

10.1.3 Inductor L_{DCDC}

The fast switching frequency (4 MHz) of the AS1170 allows for the use of small SMDs for the external inductor. The saturation current $I_{SATURATION}$ should be chosen to be above the maximum value of I_{LIMIT}[13]. The inductor should have very low DC resistance (DCR) to reduce the I^2R power losses - high DCR values will reduce efficiency.

Table 23: Recommended inductor

Part number	L	DCR	$I_{SATURATION}$	Size	Manufacturer
C3-P1.5R	1.5 µH	58 mΩ	2.4 A @ 25°C, 2.0 A (1)	3x3x1.5 mm (height is max.)	Mitsumi
LQM32PN1R0MG0	1.0 µH > 0.6 µH @ 3.0 A	60 mΩ	3.0 A (2)	3.2x2.5x0.9 mm max 1.0 mm height	Murata
LQM2HPN1R0MGC	1.0 µH > 0.6 µH @ 2.0 A	100 mΩ	1.5 A (2.0 A) (3)	2.5x2.0x0.9 mm max 1.00 mm height	
CIG32W1R0MNE	1.0 µH > 0.7 µH @ 2.7 A > 0.6 µH @ 3.0 A	60 mΩ ±25%	3.0 A	3.2x2.5 mm max 1.0 mm height	Samsung Electro-Mechancs
NRH2412T1R0N	1.0 µH > 0.6 µH @ 2.5 A	77 mΩ	2.5 A (4)	2.4x2.4x1.2 mm (height is max.)	Taiyo Yuden
CKP3225N1R0M	1.0 µH > 0.6 µH @ 3.0 A	<60 mΩ	3.0 A	3.2x2.5x0.9 mm max 1.0 mm height	

[13] Can be adjusted in I²C mode with register coil_peak (see Page 24).

Part number	L	DCR	$I_{SATURATION}$	Size	Manufacturer
MAMK2520T1R0M	1.0 µH > 0.6µH @ 2.75 A	45 mΩ	3.0 A (5)	2.5x2.0x1.2 mm height is max	
MDMK2020T1R0M	1.0 µH > 0.6 µH @ 2.75 A	56 mΩ	2.55 A (6)	2.0x2.0x1.2 mm height is max	
MAKK2016T1R0M	1.0 µH > 0.6 µH @ 2.75 A	65 mΩ	2.0 A (7)	2.0x1.6x1.0 mm height is max	

(1) Do not exceed maximum $I_{SATURATION}$ - can be ensured by setting coil_peak (will limit LED current).
(2) Flash pattern: 200 ms / 3 A, 200 ms pause, 200 ms / 3 A, 2 s then repeat again (no limit on the number of total cycles) Alternative pattern with 1000 ms / 1.6 A, 200 ms pause, 200 ms / 3 A, 200 ms pause, 200 ms / 3 A, 2 s then repeat again. (no limit on the number of total cycles).
(3) Set current limit to 2 A (coil_peak=00b) - will limit maximum output current. Flash cycle limit: 150 ms on, 500 ms off; repeat maximum 50 times.
(4) Set current limit to 2.5 A (coil_peak=01b) - will limit maximum output current.
(5) Set current limit to 3.0 A (coil_peak=10b) - can limit maximum output current.
(6) Set current limit to 2.5 A (coil_peak=01b) - will limit maximum output current.
(7) Set current limit to 2 A (coil_peak=00b) - will limit maximum output current.

If a different inductor is chosen, ensure similar DCR values and at least 0.6 µH inductance at I_{LIMIT}.

10.2 PCB layout guideline

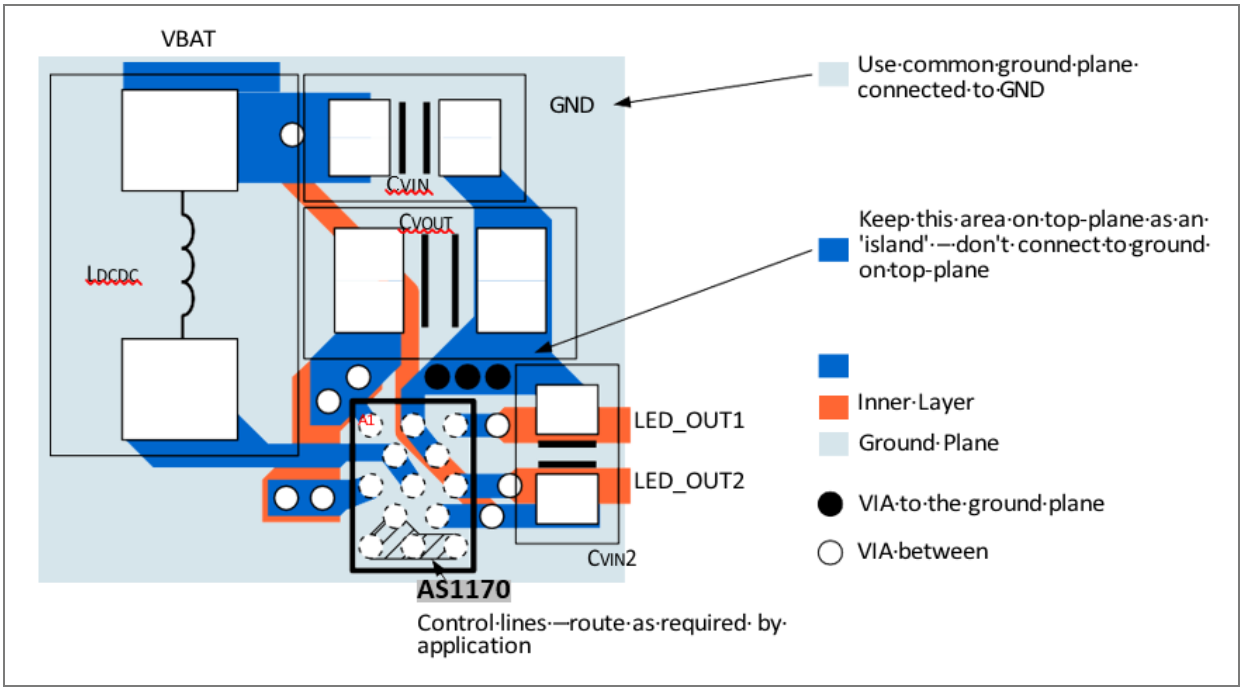
The high speed operation requires proper layout for optimum performance. Route the power traces first and try to minimize the area and wire length of the two high frequency/high current loops:

Loop1: C_{VIN}/C_{VIN2} - L_{DCDC} - pin SW1/2 - pin GND - C_{VIN}/C_{VIN2}

Loop2: C_{VIN}/C_{VIN2} - L_{DCDC} - pin SW1/2 - pin VOUT1/2 - C_{VOUT} - pin GND - C_{VIN}/C_{VIN2}

At the pin GND a single via (or more vias, which are closely combined) connects to the common ground plane. This via(s) will isolate the DCDC high frequency currents from the common ground (as most high frequency current will flow between Loop1 and Loop2 and will not pass the ground plane.

Figure 32: Layout recommendation



(1) If component placement rules allow, move all components close to the AS1170 to reduce the area and length of Loop1 and Loop2.

An additional 100 nF (e.g. Murata GRM155R61C104, > 50 nF @ 3 V, 0402 size) capacitor C_{VIN2} in parallel to C_{VIN} is recommended to filter high frequency noise for the power supply of AS1170. This capacitor should be as close as possible to the GND/V_{IN} pins of AS1170.

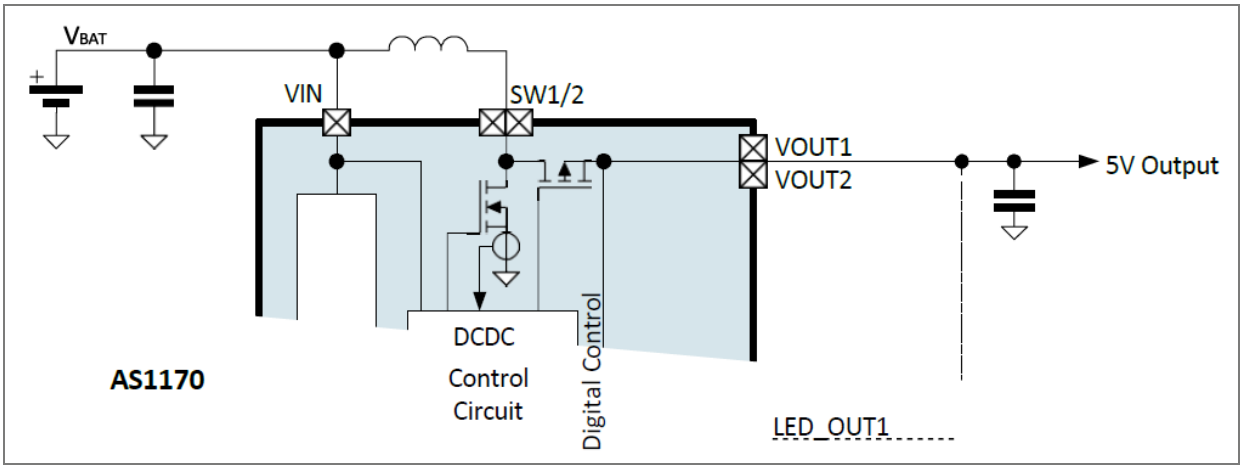
10.3 5 V operating mode

The AS1170 can be used to power a 5 V system (e.g. audio amplifier). The operating mode is selected by setting register bit const_v_mode=1. In this operating mode, the current sinks are disabled and cannot be switched on.

Information:

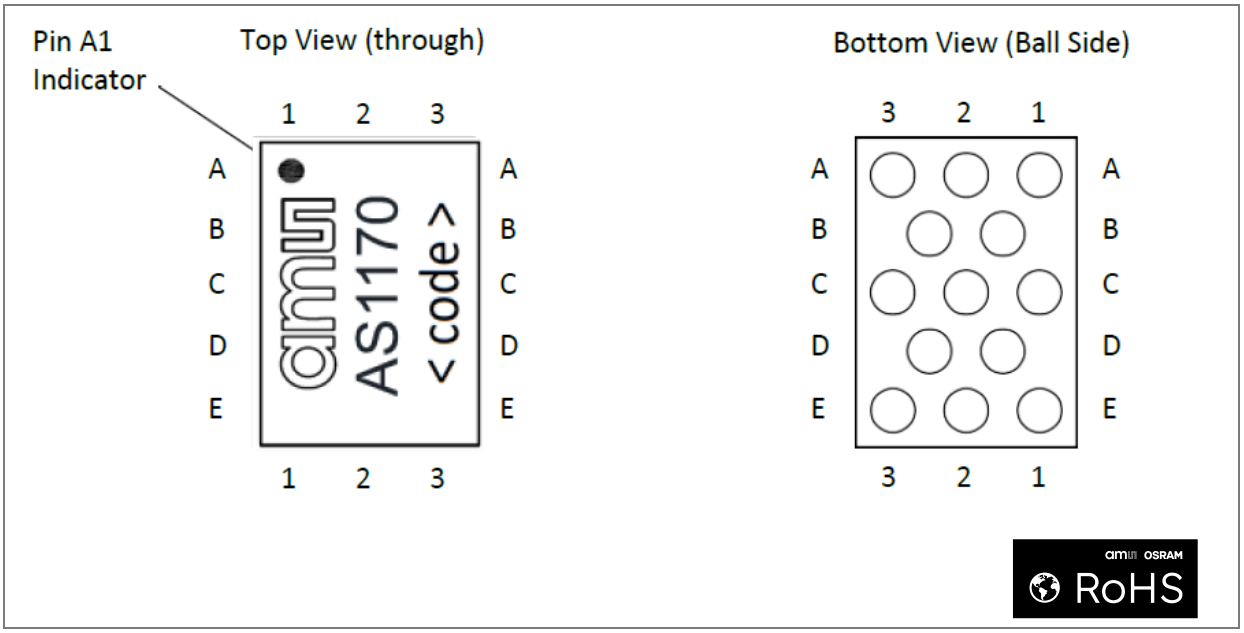
- There is always a diode between V_{IN} and VOUT1/2 due to the internal circuit. Therefore VOUT1/2 cannot be completely switched off.

Figure 33: 5V operating mode



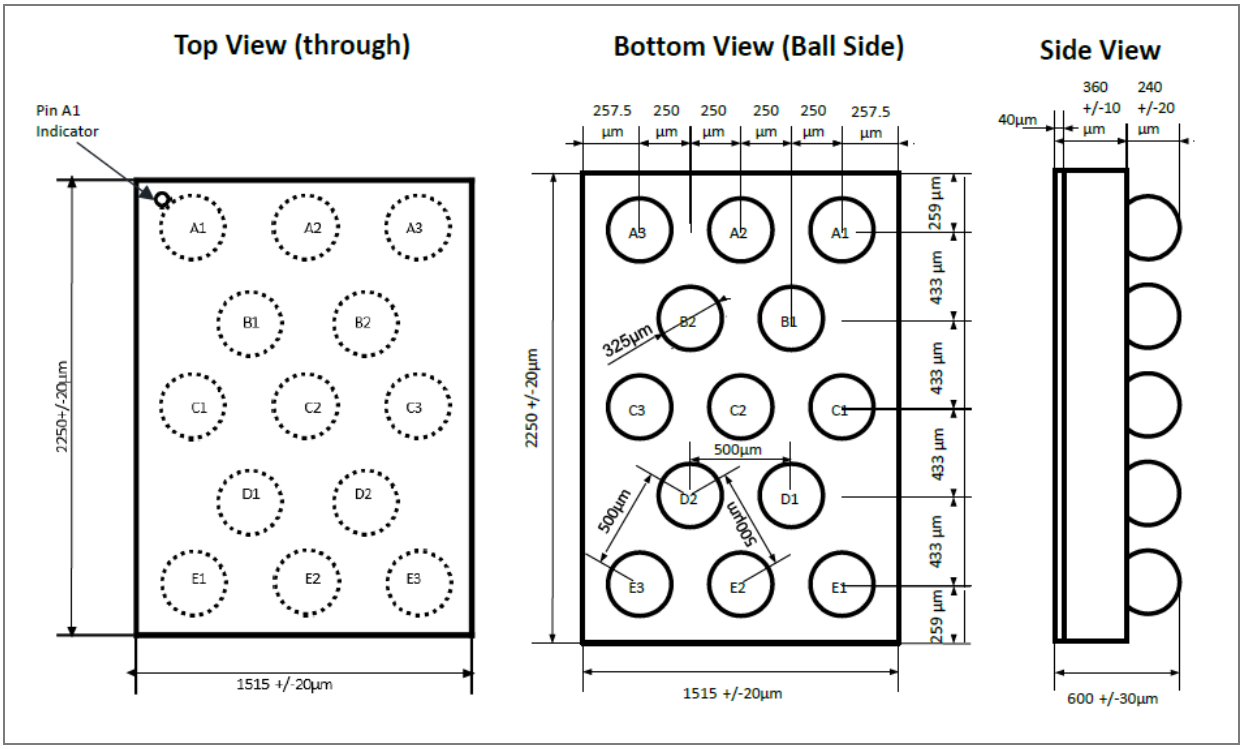
11 Package drawings and markings

Figure 34: WL-CSP13 marking



(1) Line 1: ams logo
Line 2: AS1170
Line 3: <Code> Encoded Datecode (4 characters)

Figure 35: WL-CSP13 package dimensions



(1) All dimensions are in µm.
(2) The co-planarity of the balls is 40 µm.

12 Revision information

Document status	Product status	Definition
Product Preview	Pre-development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Changes from previous version to current revision v1-00	Page
Initial production version	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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