1ED3140MU12F, 1ED3141MU12F, 1ED3142MU12F
Single-channel 3 kV (rms) isolated gate driver IC with separate outputs

Features

- Single-channel isolated gate driver
- For use with 600 V/650 V/1200 V/1700 V/2300 V IGBTs, Si and SiC MOSFETs
- Up to 6.5 A typical peak output current
- 45 ns propagation delay with 7 ns part-to-part matching (skew)
- 35 V absolute maximum output supply voltage
- High common-mode transient immunity CMTI > 300 kV/µs
- Separate source and sink outputs with active shutdown and short circuit clamping
- Galvanically isolated coreless transformer gate driver
- 3.3 V and 5 V input supply voltage
- Suitable for operation at high ambient temperature and in fast switching applications
- UL 1577 certification V_{ISO} = 3.0 kV (rms) for 1 min

Potential applications

- EV charging
- Energy storage systems
- Solar inverters
- Server and telecom switched mode power supplies (SMPS)
- UPS-systems
- AC and brushless DC motor drives
- Commercial air-conditioning (CAC)
- High voltage DC-DC converter and DC-AC inverter

Product validation

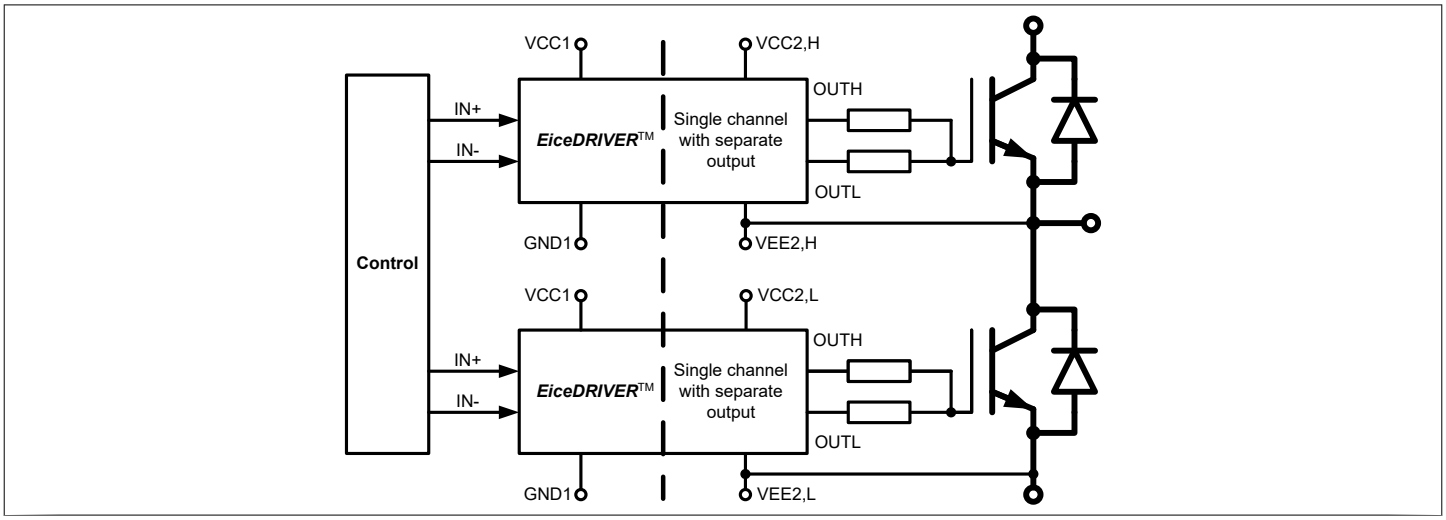
Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The 1ED314xMU12F gate driver ICs are galvanically isolated single channel gate driver ICs for IGBT, MOSFET and SiC MOSFET in DSO-8 150 mil package. They provide a typical output current of up to 6.5 A.

The input logic pins operate on a wide input voltage range from 3 V to 6.5 V using CMOS threshold levels to support 3.3 V microcontrollers.

Data transfer across the isolation barrier is realized by the coreless transformer technology. All variants have input and output undervoltage lockout (UVLO) and active shutdown.



Typical application diagram

Table 1 Ordering information

Product type	Typical UVLO (V_{UVLOL2}/V_{UVLOH2})	Typical output current source/sink	Certification	Package marking
1ED3140MU12F	8.5 V/9.3 V	6 A/6.5 A	UL 1577	3140MU12
1ED3141MU12F	11.0 V/12.0 V	6 A/6.5 A	UL 1577	3141MU12
1ED3142MU12F	12.5 V/13.6 V	6 A/6.5 A	UL 1577	3142MU12

Table 2 Related evaluation board

Board name	Gate driver	Power transistor	Short description
Eval-1ED3142MU12F-SiC	1ED3142MU12F	IMZA120R020M1H	Half-bridge evaluation board with 1ED3142MU12F gate drivers and shunt-based over-current protection paired with IMZA120R020M1H CoolSiC™ in TO247-4 package

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1 Block diagram reference

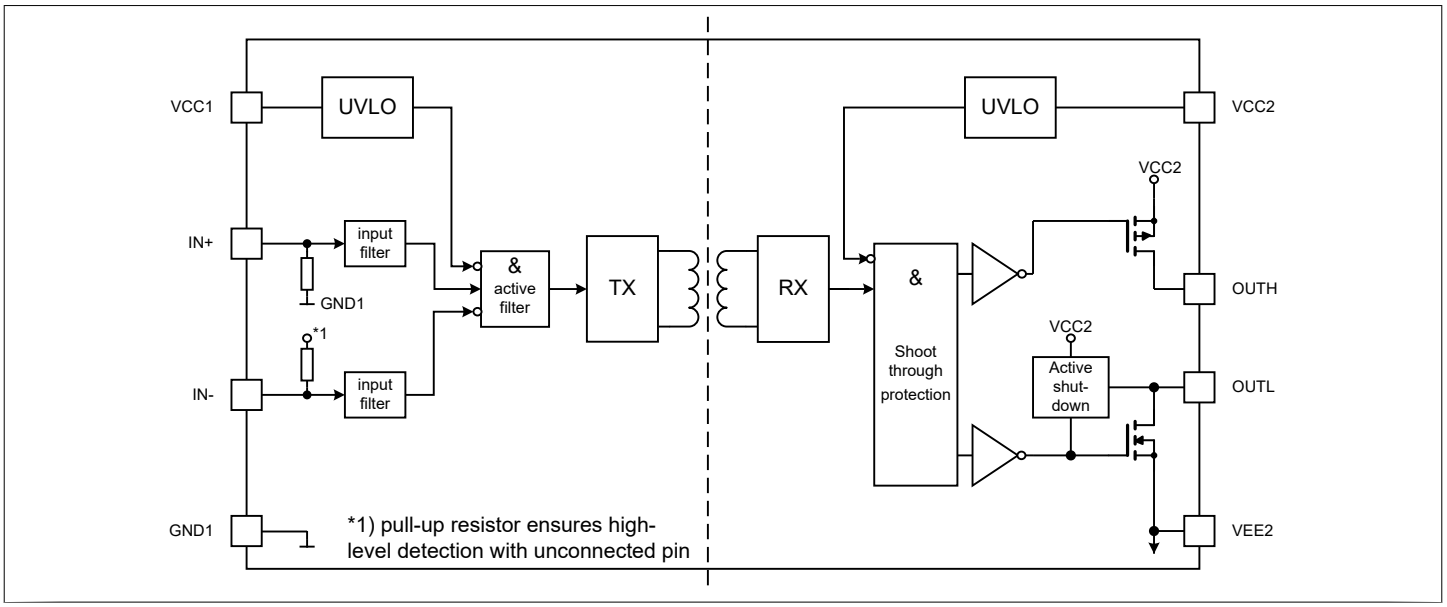


Figure 2 Block diagram

2 Pin configuration and description

Pin configuration DSO-8 150 mil

Table 3 Pin configuration

Pin No.	Name	Function
1	*VCC1*	Positive supply input side
2	*IN+*	Non-inverted driver input (active high)
3	*IN-*	Inverted driver input (active low)
4	*GND1*	Input side ground
5	*VCC2*	Positive power supply output side
6	*OUTH*	Driver sourcing output
7	*OUTL*	Driver sinking output
8	*VEE2*	Output side ground

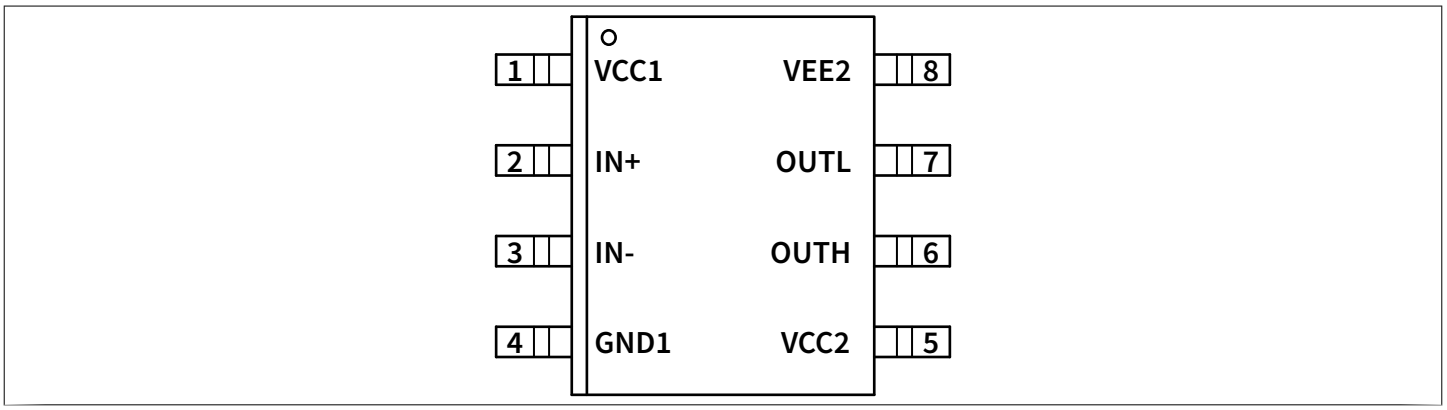


Figure 3 DSO-8 150 mil (top view)

Pin description

- *VCC1*: Input supply voltage. Connect to 3.3 V or 5 V and decouple with a capacitor to *GND1*. Use a low-ESR and ESL capacitor placed as close to the device as possible.
- *GND1*: Input ground. All the input side signals, *VCC1*, *IN+* and *IN-* are referenced to this ground.
- *IN+*: Non-inverted control signal for driver output. An internal filter provides robustness against noise at *IN+*. If left open, an internal weak pull-down resistor pulls this pin to a low state, as shown in Figure 2.
- *IN-*: Inverted control signal for driver output. An internal filter provides robustness against noise at *IN-*. If left open, an internal weak pull-up resistor pulls this pin to a high state, as shown in Figure 2.
- *VCC2*: Output positive power supply rail. Connect a decoupling capacitor from this pin to *VEE2*. Use a low ESR and ESL capacitor placed as close to the device as possible.
- *VEE2*: Output ground. All the output side signals, *VCC2*, *OUTH* and *OUTL* are referenced to this ground. In case of a bipolar supply (positive and negative voltage referred to IGBT emitter or MOSFET source), this pin should be connected to the negative supply voltage.
- *OUTH*: Driver sourcing output pin used to charge the gate of the external transistor (IGBT or MOSFET). During on-state this output is connected to *VCC2*. This output is controlled by *IN+* and *IN-* and will be turned off by an UVLO event.
- *OUTL*: Driver sinking output pin used to discharge the gate of the external transistor (IGBT or MOSFET). During off-state this output is connected to *VEE2*. This output is controlled by *IN+* and *IN-*. In case of an UVLO event *OUTL* will actively pulled low. For cases where the gate driver output is not supplied, the active shutdown circuit keeps the output voltage at a low level.

3 Electrical characteristics and parameters

3.1 Absolute maximum ratings

Table 4 Absolute maximum ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only. Operating the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Device reliability may be affected by exposure to absolute-maximum-rated conditions for extended periods of time.

Parameter	Symbol	Values		Unit	Note or condition
		Min.	Max.		
Power supply input side voltage	V_{VCC1}	-0.3	17	V	V_{VCC1} - V_{GND1}
Power supply output side voltage	V_{VCC2}	-0.3	35	V	V_{VCC2} - V_{VEE2}
Gate driver source output voltage	V_{OUTH}	V_{VCC2} - 35	V_{VCC2} + 0.3	V	
Gate driver sink output voltage	V_{OUTL}	V_{VEE2} - 0.3	V_{VEE2} + 35	V	
Logic input voltages (IN+, IN-)	V_{IN}	-0.3	6.5	V	
Input to output offset voltage	V_{OFFSET}		2300	V	1) V_{OFFSET} = |V_{VEE2} - V_{GND1}|
ESD robustness - human body model	|$V_{ESD,HBM}$|		4	kV	2)
ESD robustness - charged device model	*ESD,CDM*		TC1500		3)
Junction temperature	T_J	-40	150	°C	
Storage temperature	T_{Stg}	-55	150	°C	
Power dissipation (input side)	$P_{D,IN}$		100	mW	4) T_A = 85 °C
Power dissipation (output side)	$P_{D,OUT}$		500	mW	5) T_A = 85 °C
Thermal resistance junction to ambient	$R_{THJA,OUT}$		129	K/W	T_A = 85 °C, 2s2p - no vias, P_J = 500 mW
Characterization parameter junction to package top	Ψ_{Jtop}		6.1	K/W	T_A = 85 °C, 2s2p - no vias, P_J = 500 mW

1) for functional operation only
2) According to ANSI/ESDA/JEDEC-JS-001-2017 (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).
3) According to ANSI/ESDA/JEDEC-JS-002-2014 (TC = test condition in volt)
4) IC input-side power dissipation is derated linearly with 7.75 mW/°C above 137.1 °C
5) IC output-side power dissipation is derated linearly with 7.75 mW/°C above 85 °C

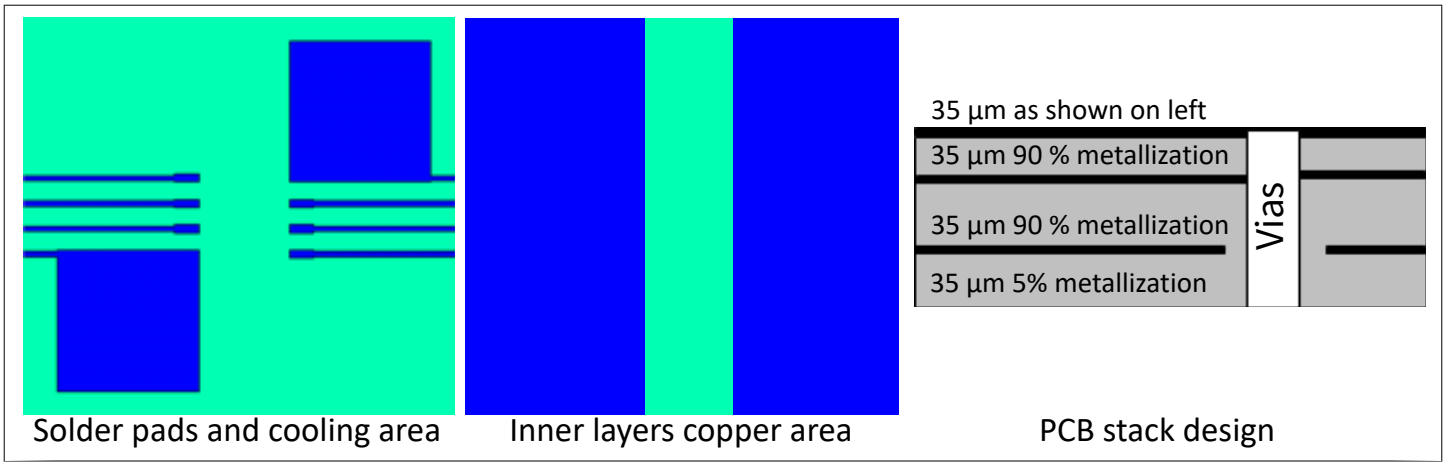


Figure 4 Reference layout for thermal data

This PCB layout represents the reference layout used for the thermal characterization of the 150 mil package.

3.2 Recommended operating conditions

Table 5 Recommended operating conditions

Parameter	Symbol	Values		Unit	Note or condition
		Min.	Max.		
Power supply input side voltage	V_{VCC1}	3.0	15	V	V_{VCC1} - V_{GND1}
Power supply output side voltage	V_{VCC2}	9.6	32	V	V_{VCC2} - V_{VEE2}, 1ED3140
Power supply output side voltage	V_{VCC2}	12.35	32	V	V_{VCC2} - V_{VEE2}, 1ED3141
Power supply output side voltage	V_{VCC2}	14	32	V	V_{VCC2} - V_{VEE2}, 1ED3142
Logic input voltages (IN+, IN-)	V_{IN}	-0.3	5.5	V	
Ambient temperature	T_A	-40	125	°C	
Junction temperature	T_J	-40	150	°C	

3.3 Electrical characteristics

The electrical characteristics include the spread of values over supply voltages and temperatures within the recommended operating conditions. Electrical characteristics are tested in production at T_A = 25°C. Typical values represent the median values measured at V_{VCC1} = 3.3 V, V_{VCC2} - V_{VEE2} = 15 V, and T_A = 25°C. Minimum and maximum values in characteristics are verified by characterization/design. This is valid for all electrical characteristics unless specified otherwise.

3.3.1 Power supply

Table 6 Power supply

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
UVLO threshold input side (on)	V_{UVLOH1}		2.86	3.0	V	V_{VCC1} - V_{GND1}
UVLO threshold input side (off)	V_{UVLOL1}	2.5	2.66		V	V_{VCC1} - V_{GND1}

(table continues...)

Table 6 (continued) Power supply

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
UVLO hysteresis input side	V_{HYS1}	0.1	0.2		V	V_{UVLOH1} - V_{UVLOL1}
Quiescent current input side	I_{Q1}			1.1	mA	IN+ = Low, IN- = Low
Quiescent current output side, ON state	$I_{Q2,ON}$			1.35	mA	IN+ = High, IN- = Low, V_{VCC2} - V_{VEE2} = 15 V
Quiescent current output side, OFF state	$I_{Q2,OFF}$			1.0	mA	IN+ = Low, IN- = High, V_{VCC2} - V_{VEE2} = 15 V
1ED3140						
UVLO threshold output side (on)	V_{UVLOH2}		9.3	9.6	V	V_{VCC2} - V_{VEE2}
UVLO threshold output side (off)	V_{UVLOL2}	8.25	8.55		V	V_{VCC2} - V_{VEE2}
UVLO hysteresis output side	V_{HYS2}		0.75		V	V_{UVLOH2} - V_{UVLOL2}
1ED3141						
UVLO threshold output side (on)	V_{UVLOH2}		12	12.35	V	V_{VCC2} - V_{VEE2}
UVLO threshold output side (off)	V_{UVLOL2}	10.7	11.05		V	V_{VCC2} - V_{VEE2}
UVLO hysteresis output side	V_{HYS2}		0.95		V	V_{UVLOH2} - V_{UVLOL2}
1ED3142						
UVLO threshold output side (on)	V_{UVLOH2}		13.6	14	V	V_{VCC2} - V_{VEE2}
UVLO threshold output side (off)	V_{UVLOL2}	12.15	12.55		V	V_{VCC2} - V_{VEE2}
UVLO hysteresis output side	V_{HYS2}		1.05		V	V_{UVLOH2} - V_{UVLOL2}

3.3.2 Logic input

Table 7 Logic input

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
IN+, IN- low input threshold voltage	$V_{IN,L}$	1.1			V	
IN+, IN- high input threshold voltage	$V_{IN,H}$			2.5	V	
IN+, IN- low/high hysteresis	$V_{IN,HYS}$	0.5	0.8		V	
IN+, IN- input current	I_{IN}			100	µA	V_{VCC1} = 5 V, V_{IN} <= V_{VCC1}
IN+ pull down resistor	$R_{IN,PD}$		75		kΩ	
IN- pull up resistor	$R_{IN,PU}$		75		kΩ	

3.3.3 Gate driver

Table 8 Gate driver

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High level output peak current	I_{OUTH}	3.5	6		A	1) V_{VCC2} - V_{VEE2} = 15 V, IN+ = High, IN- = Low, C_L = 100 nF
High level output on resistance	$R_{DSON,H}$	0.3	0.9	2.1	Ω	I_{OUTH} = 0.1 A
Low level output peak current	I_{OUTL}	3.5	6.5		A	1) V_{VCC2} - V_{VEE2} = 15 V, IN+ = Low, IN- = High, C_L = 100 nF
Low level output on resistance	$R_{DSON,L}$	0.2	0.5	1.1	Ω	I_{OUTL} = 0.1 A
Short circuit clamp voltage between OUTH and VCC2	V_{CLP_OUTH}			1.0	V	V_{OUTH} - V_{VCC2}, I_{OUTH} = -500 mA, t < 10 µs, IN+ = High, IN- = Low
Clamp voltage between VEE2 and OUTL	V_{CLP_OUTL}			1.0	V	V_{VEE2}-V_{OUTL}, I_{OUTL} = -500 mA, t < 10 µs, IN+ = Low, IN- = High

1) Parameter is not subject to production test - verified by design/characterization

3.3.4 Dynamic characteristics

Table 9 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input to output propagation delay ON	t_{PDON}	39	45	55	ns	V_{VCC2} - V_{VEE2} = 15 V, C_L = 100 pF, valid only for 1ED3140, 1ED3141
Input to output propagation delay ON	t_{PDON}	39	45	55	ns	V_{VCC2} - V_{VEE2} = 18 V, C_L = 100 pF, valid only for 1ED3142
Input to output propagation delay OFF	t_{PDOFF}	39	45	55	ns	V_{VCC2} - V_{VEE2} = 15 V, C_L = 100 pF, valid only for 1ED3140, 1ED3141
Input to output propagation delay OFF	t_{PDOFF}	39	45	55	ns	V_{VCC2} - V_{VEE2} = 18 V, C_L = 100 pF, valid only for 1ED3142
Input to output propagation delay distortion IN+	$\lvert t_{PDISTO,IN+}\rvert$		0	3	ns	1) $\lvert t_{PDOFF} - t_{PDON}\rvert$
Input to output propagation delay distortion IN-	$\lvert t_{PDISTO,IN-}\rvert$		0	5	ns	1) $\lvert t_{PDOFF} - t_{PDON}\rvert$
Input to output, part to part skew	t_{SKEW}			7	ns	1) 2) C_L = 100 pF, valid for same input pin and edge
Input to output, part to part skew plus	t_{SKEW+}		0	8	ns	1) C_L = 100 pF, valid for opposite output edge and any input combination
Input pulse suppression time (filter time)	t_{INFLT}	15			ns	shorter pulses will not propagate to the output
Minimum input pulse width	$t_{IN,min}$	23			ns	

(table continues...)

Table 9 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Rise time	t_{RISE}			20	ns	V_{VCC2} - V_{VEE2} = 15 V, C_L = 1 nF, valid only for 1ED3140, 1ED3141
Rise time	t_{RISE}			20	ns	V_{VCC2} - V_{VEE2} = 18 V, C_L = 1 nF, valid only for 1ED3142
Fall time	t_{FALL}			20	ns	V_{VCC2} - V_{VEE2} = 15 V, C_L = 1 nF, valid only for 1ED3140, 1ED3141
Fall time	t_{FALL}			20	ns	V_{VCC2} - V_{VEE2} = 18 V, C_L = 1 nF, valid only for 1ED3142
Input-side start-up time	$t_{START,VCC1}$		2.5	10	µs	3) IN+ = High, IN- = Low, V_{VCC2} > V_{UVLOH2}, C_L = 100pF
Input-side deactivation time	$t_{STOP,VCC1}$		2.5	10	µs	3) IN+ = High, IN- = Low, V_{VCC2} > V_{UVLOH2}, C_L = 100pF
Output-side start-up time	$t_{START,VCC2}$		5	10	µs	3) IN+ = High, IN- = Low, V_{VCC1} > V_{UVLOH1}, C_L = 100 pF
Output-side deactivation time	$t_{STOP,VCC2}$	0.5		1	µs	3) IN+ = High, IN- = Low, V_{VCC1} > V_{UVLOH1}, C_L = 100 pF
High-level common-mode transient immunity	$\|CM_H\|$	300			kV/µs	3) V_{CM} = 1500 V; *IN-* tied to GND1; *IN+* tied to *VCC1*
Low-level common-mode transient immunity	$\|CM_L\|$	300			kV/µs	3) V_{CM} = 1500 V; *IN-* tied to *VCC1*; *IN+* tied to *GND1*

1) value at same ambient temperature and operating conditions.
2) this parameter was previously called input to output, part to part propagation delay variation
3) Parameter is not subject to production test - verified by design/characterization

3.3.5 Active shut down

Table 10 Active shut down

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Active shut down voltage	V_{ACTSD}			1.8	V	V_{OUTL} - V_{VEE2}, I_{OUTL} = 500 mA, *VCC2* open, *OUTH* connected to R_G

4 Insulation characteristics

4.1 Safety limiting values

Table 11 Safety limiting values

This coupler is suitable for rated insulation only within the given safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum ambient safety temperature	T_S	–	–	150	°C	1)
Maximum continuous input power dissipation	P_{SI}	–	–	100	mW	2)
Maximum continuous output power dissipation	P_{SO}	–	–	970	mW	3)

1) According to IEC: The highest ambient temperature permitted in the event of a fault
2) Maximum output power dissipation at T_A= 25 °C; derating required from 137.1°C with 7.75 mW/°C, T_J = 150 °C
3) Maximum output power dissipation at T_A= 25 °C; derating required from 25°C with 7.75 mW/°C, T_J = 150 °C

4.2 Package specific insulation characteristics

Table 12 Package specific insulation characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Minimum external clearance	*CLR*	4			mm	
Minimum external creepage	*CPG*	4			mm	
Minimum comparative tracking index	*CTI*	600				
Isolation capacitance	C_{IO}			1	pF	1) V_{IO} = 1 V, f = 1 MHz

1) All pins on each side of the barrier tied together creating a two-pin device.

4.3 UL 1577 certification characteristics

Table 13 UL 1577 certification characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Insulation withstand voltage	V_{ISO}	3000	–	–	V (rms)	1 minute type test
Insulation test voltage	$V_{ISO,TEST}$	3600	–	–	V (rms)	1 s, production test

5 Typical characteristics

Unless otherwise noted,the measurements are done with V_{VCC1} = 3.3 V, 100 nF capacitor connected between *VCC1* and *GND1*, 4.7 µF capacitor between *VCC2* and *VEE2*.

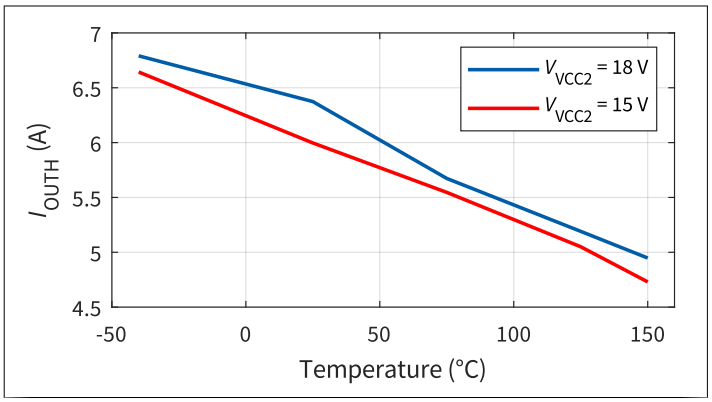


Figure 5 **High level output peak current vs. temperature**

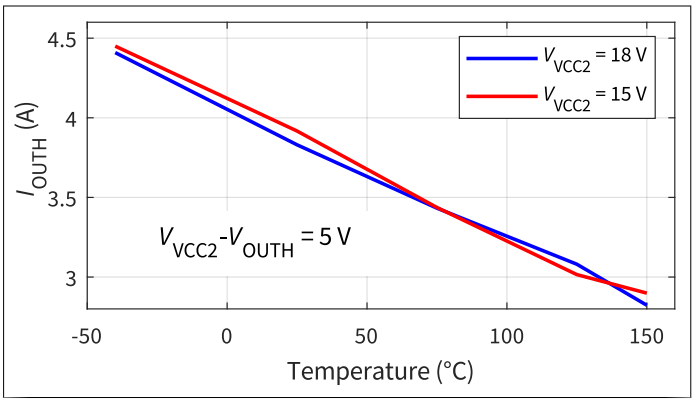


Figure 6 **High level output current with V_{VCC2} - V_{OUTH} = 5 V vs. temperature**

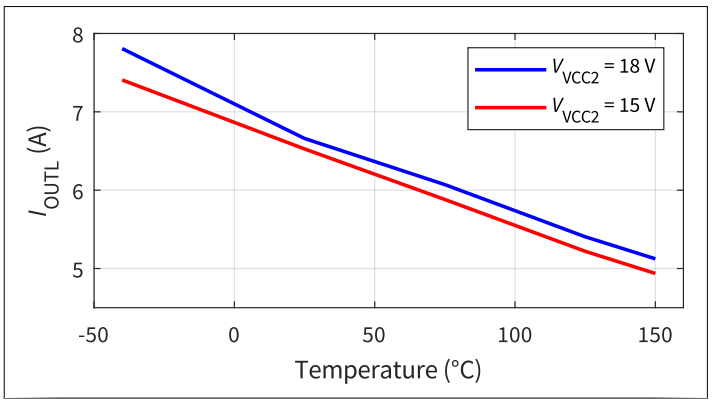


Figure 7 **Low level output peak current vs. temperature**

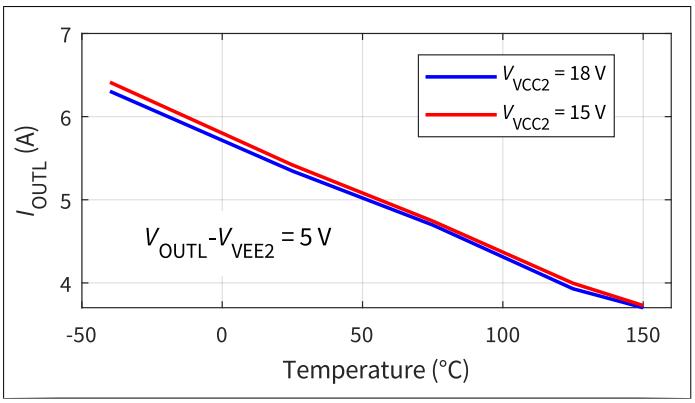


Figure 8 **Low level output current with V_{OUTL} - V_{VEE2} = 5 V vs. temperature**

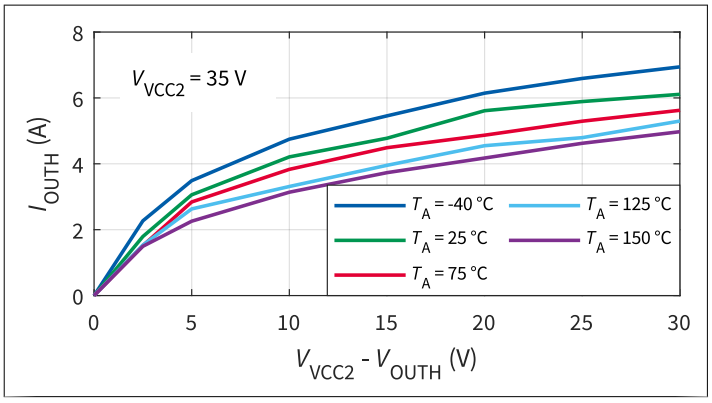


Figure 9 **High level output current vs. V_{VCC2}-V_{OUTH}**

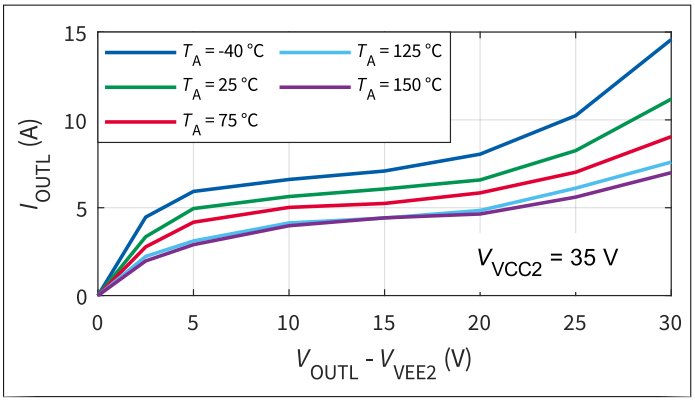


Figure 10 **Low level output current vs. V_{OUTL}-V_{VEE2}**

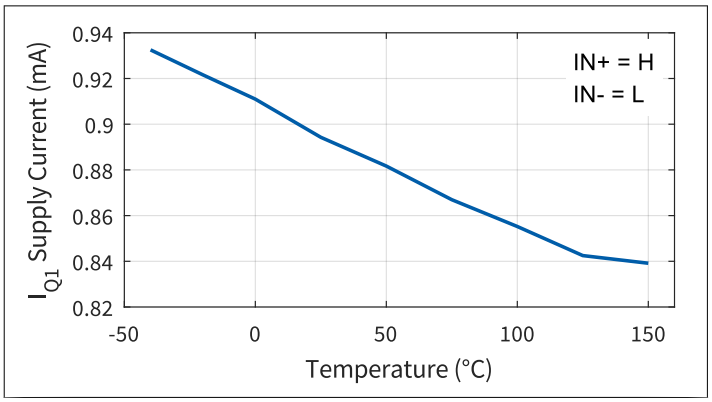


Figure 11 **I_{Q1} supply current vs. temperature**

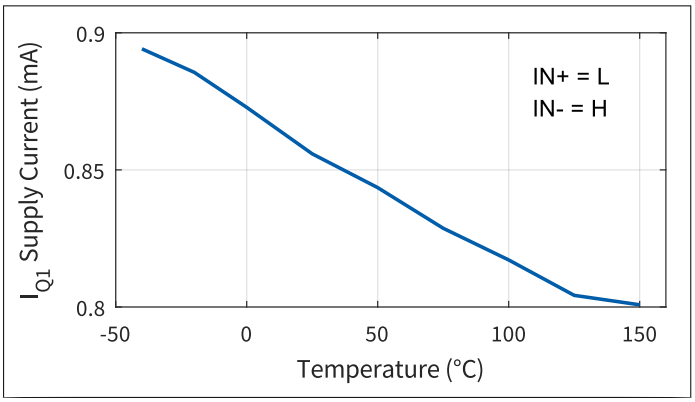


Figure 12 **I_{Q1} supply current vs. temperature**

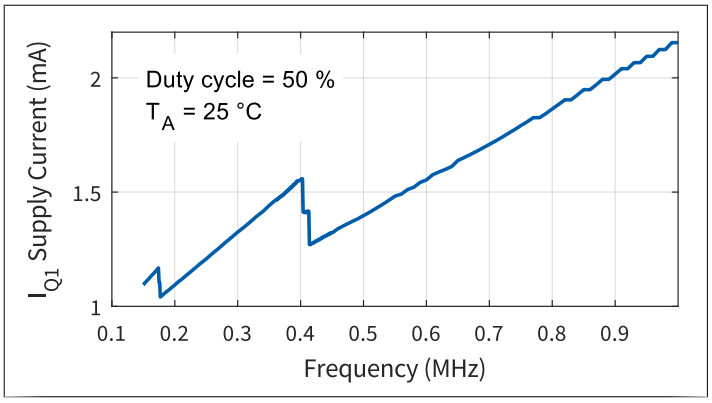


Figure 13 **I_{Q1} supply current vs. input frequency**

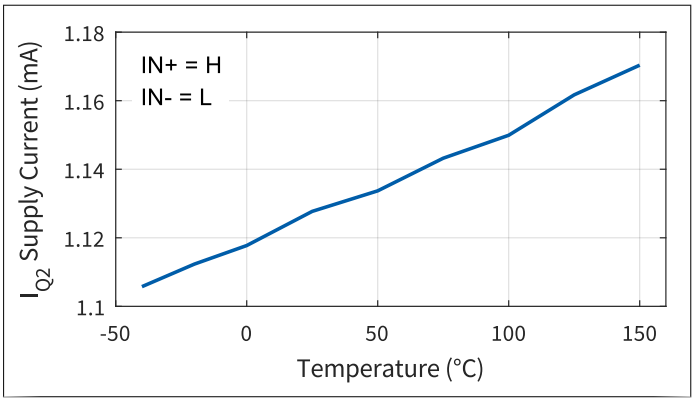


Figure 14 **I_{Q2} supply current vs. temperature**

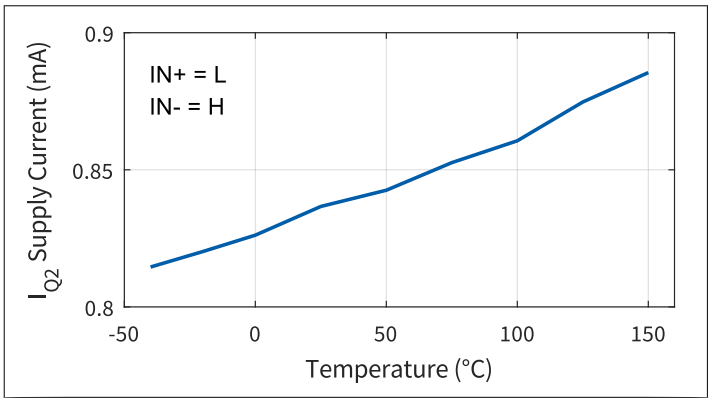


Figure 15 **I_{Q2} supply current vs. temperature**

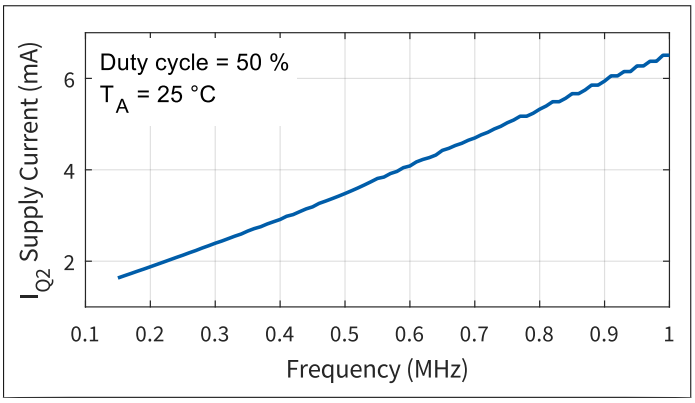


Figure 16 **I_{Q2} supply current vs. input frequency**

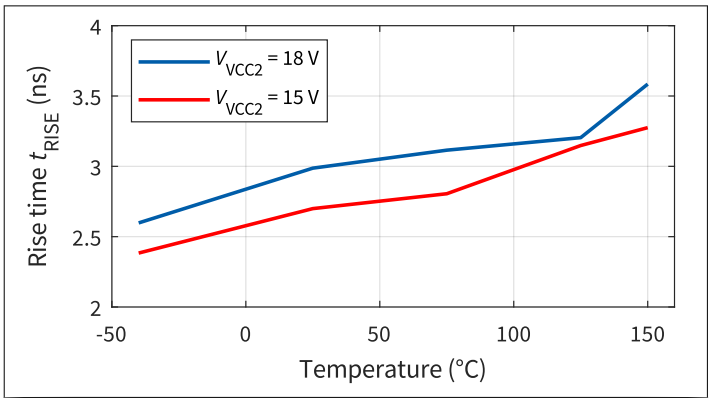


Figure 17 **Rise time t_{RISE} vs. temperature**

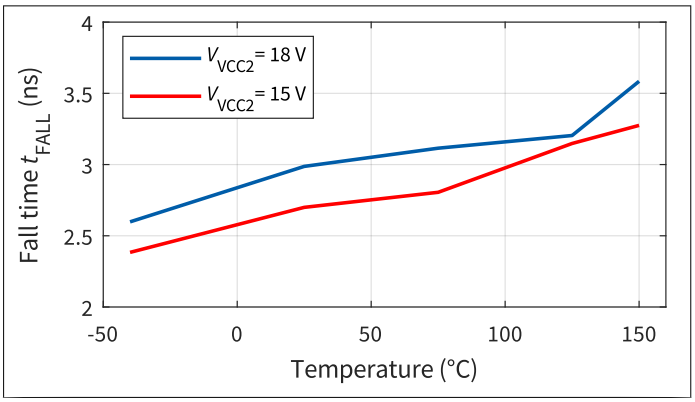


Figure 18 **Fall time t_{FALL} vs. temperature**

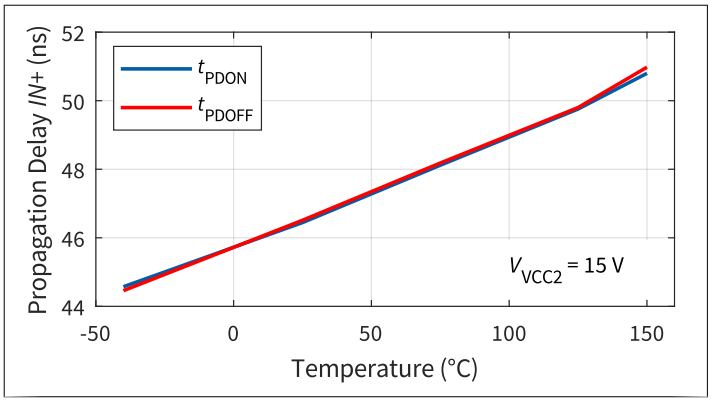


Figure 19 **Propagation delay for *IN+* vs. temperature (V_{VCC2} = 15 V)**

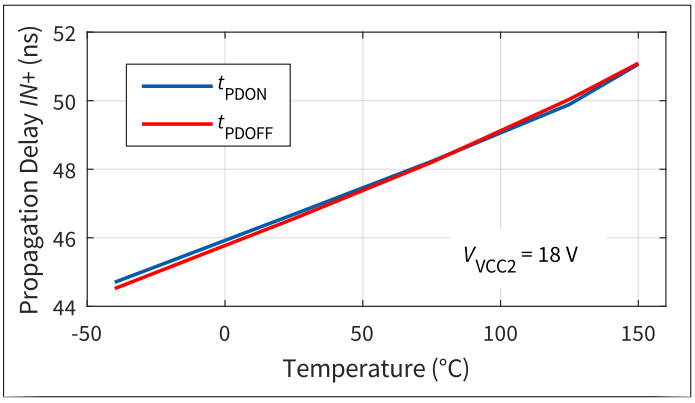


Figure 20 **Propagation delay for *IN+* vs. temperature (V_{VCC2} = 18 V)**

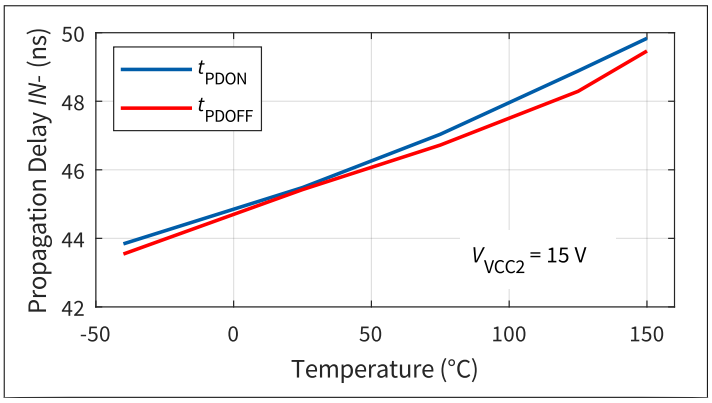


Figure 21 **Propagation delay for *IN-* vs. temperature (V_{VCC2} = 15 V)**

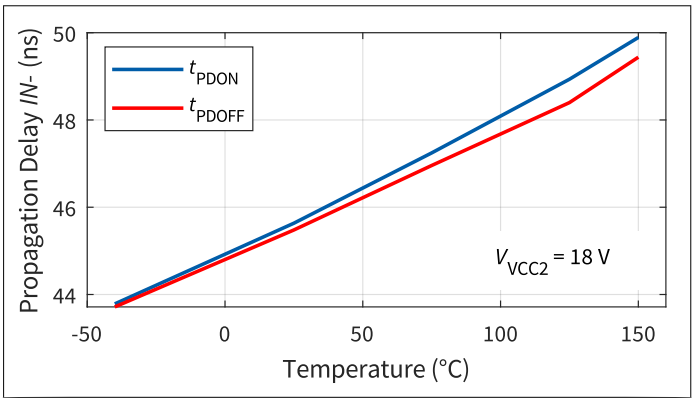


Figure 22 **Propagation delay for *IN-* vs. temperature (V_{VCC2} = 18 V)**

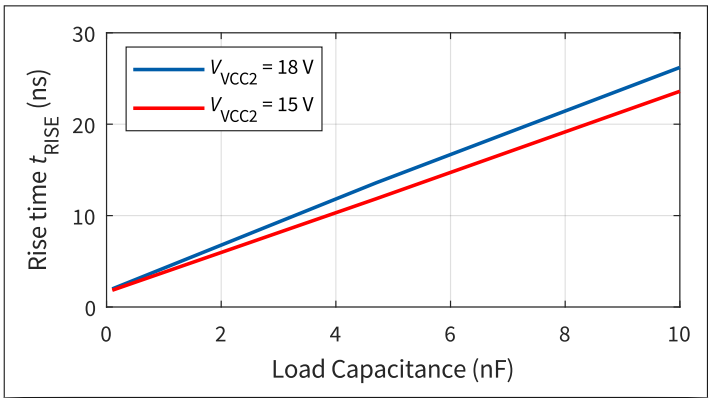


Figure 23 **Rise time t_{RISE} vs. load capacitance**

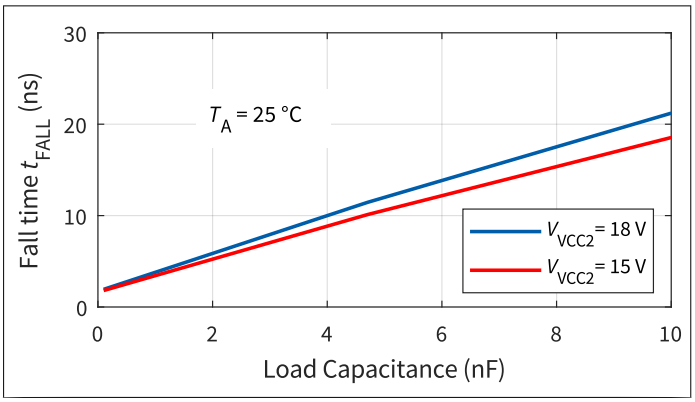


Figure 24 **Fall time t_{FALL} vs. load capacitance**

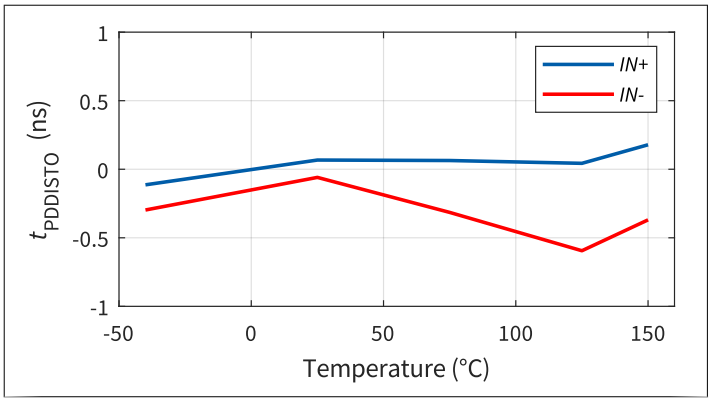


Figure 25 **Propagation delay distortion t_{PDISTO} vs. temperature**

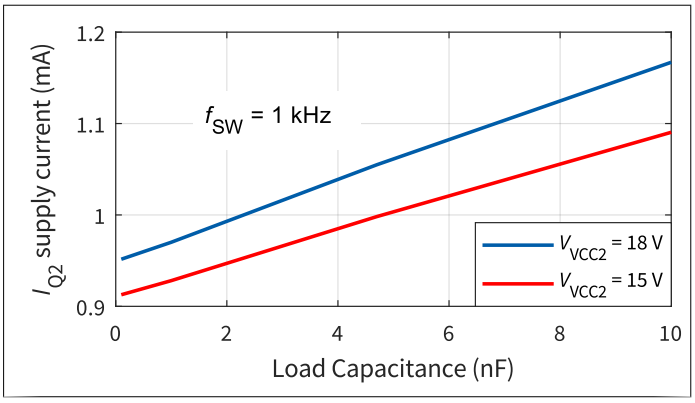


Figure 26 **I_{Q2} supply current vs. load capacitance**

6 Parameter measurement

6.1 Propagation delay, rise and fall time

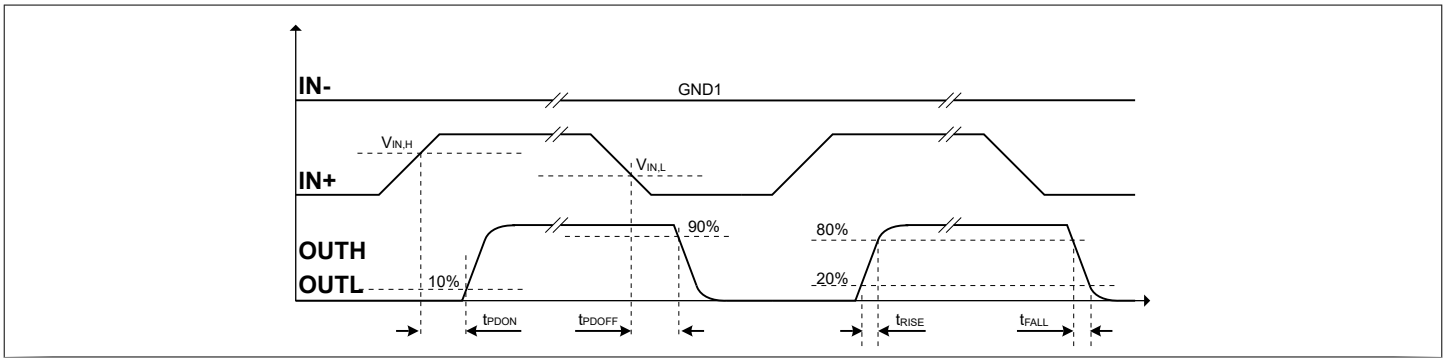


Figure 27 Propagation delay, rise time and fall time using the non-inverting input

Figure 27 and Figure 28 show the propagation delays t_{PDON} and t_{PDOFF} for the non-inverting input *IN+* and the inverting input *IN-* including the rise time, t_{RISE}, and fall time, t_{FALL}, diagrams.

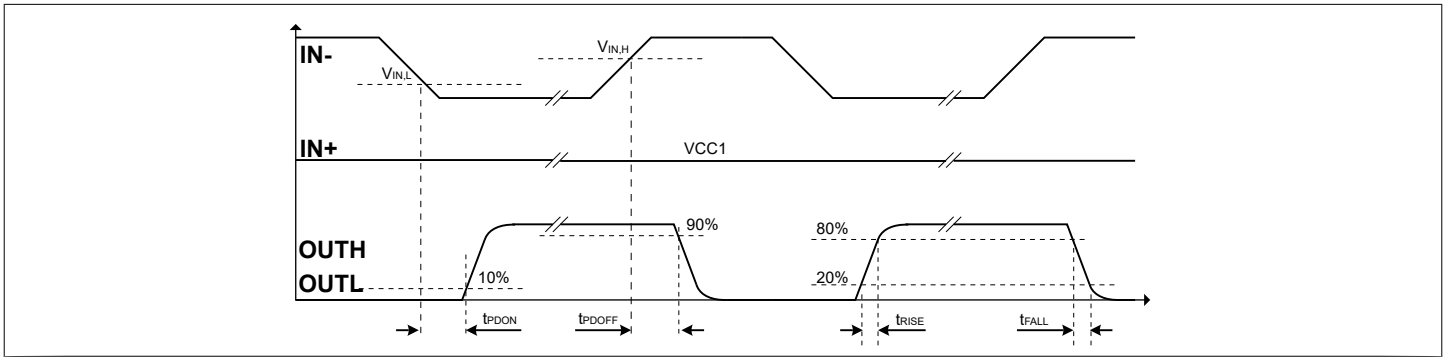


Figure 28 Propagation delay, rise time and fall time using the inverting input

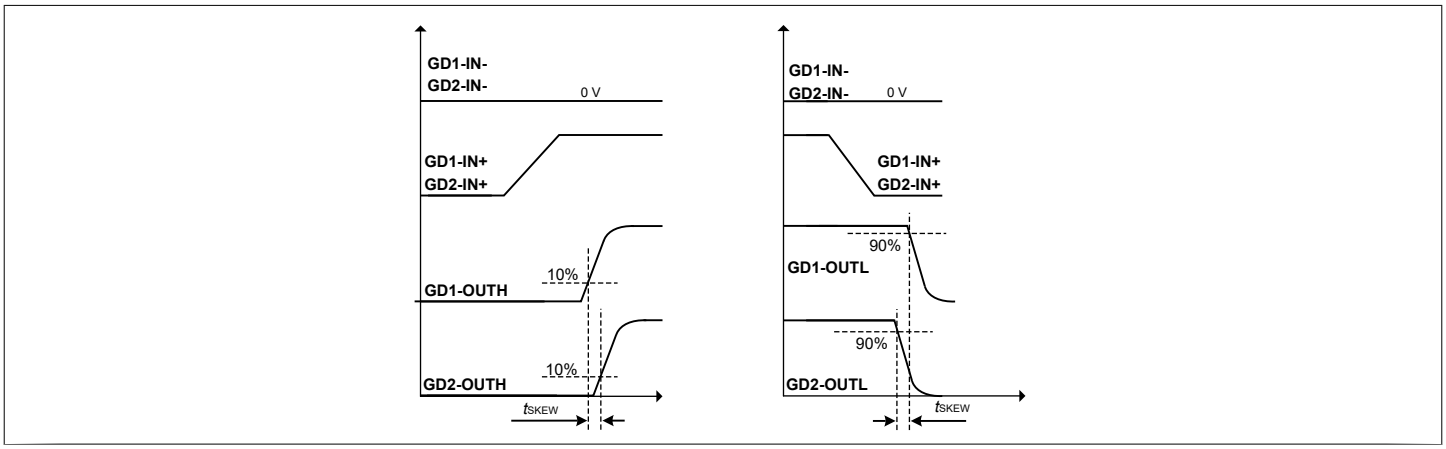


Figure 29 Input to output, part to part skew using non-inverting input

Figure 29 and Figure 30 show the input to output, part to part skew, t_{SKEW} measurement with the non-inverting and inverting inputs. This parameter highlights the part to part variation in propagation delay and is relevant when paralleling gate drivers. The parameter is always assuming the same conditions (temperature and supply voltages) between the parts.

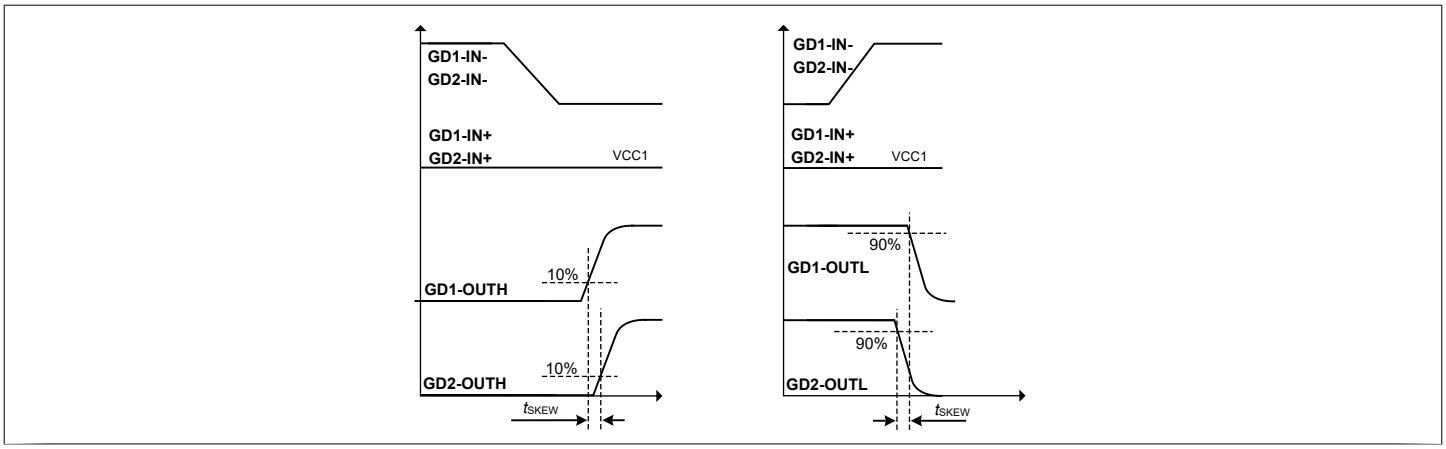


Figure 30 Input to output, part to part skew using the inverting input

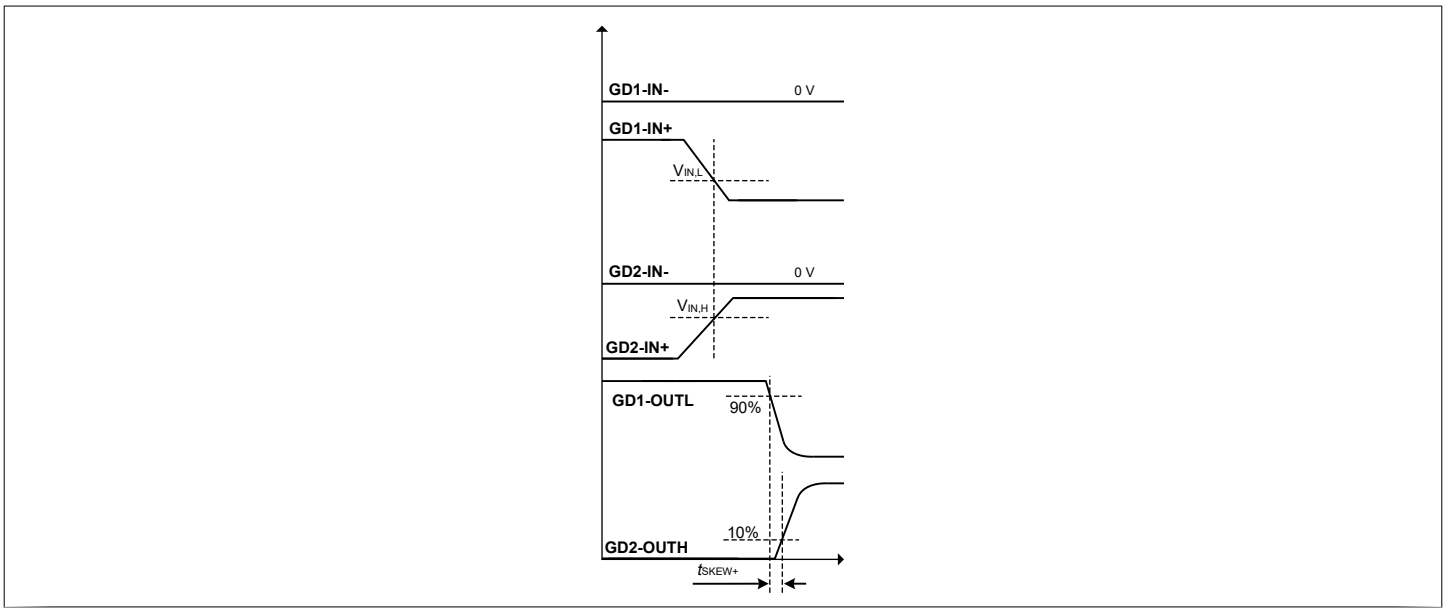


Figure 31 Skew plus using the non-inverting inputs

Figure 31, Figure 32, Figure 33 and Figure 34 show the skew plus (t_{SKEW+}) using the non-inverting or inverting inputs on the input side under all the possible combinations. The skew plus parameter is valid at the same temperature and supply voltages. The parameter describes the variation between the turn-on and turn-off propagation delays in a half-bridge, under the previous mentioned conditions and defines the minimum deadtime required from the gate driver perspective. This is relevant when driving the gate drivers complimentary, such as in a half-bridge.

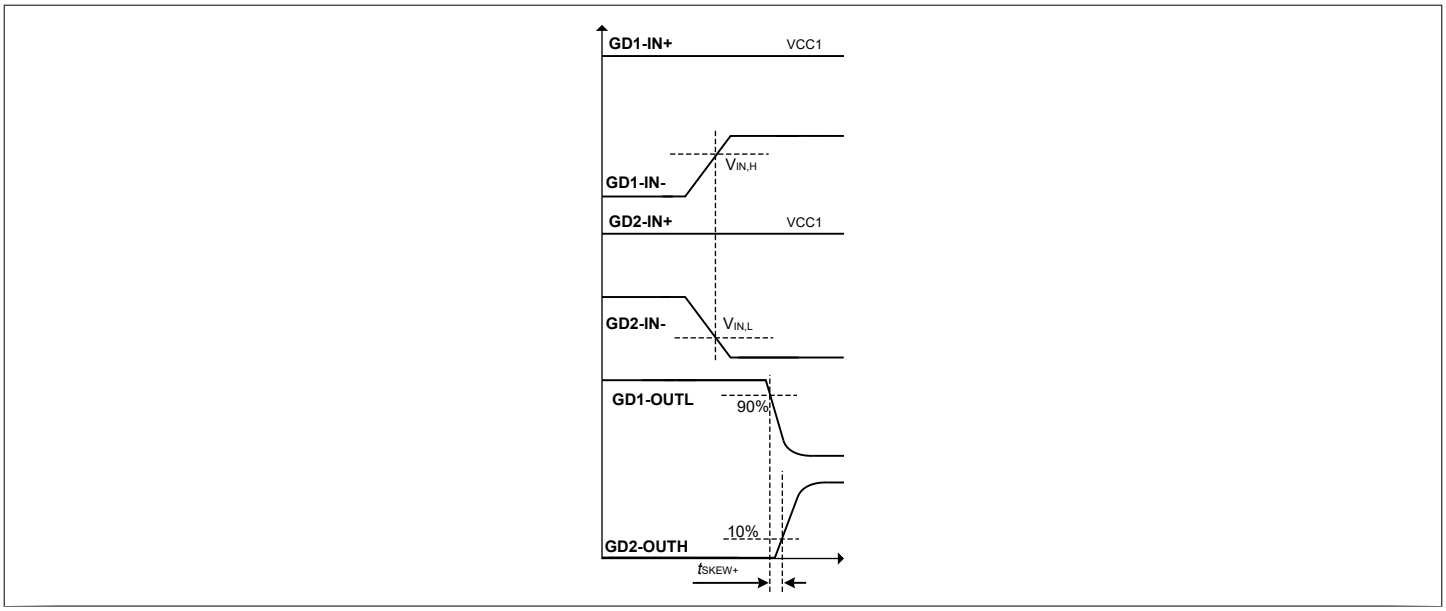


Figure 32 Skew plus using the inverting inputs

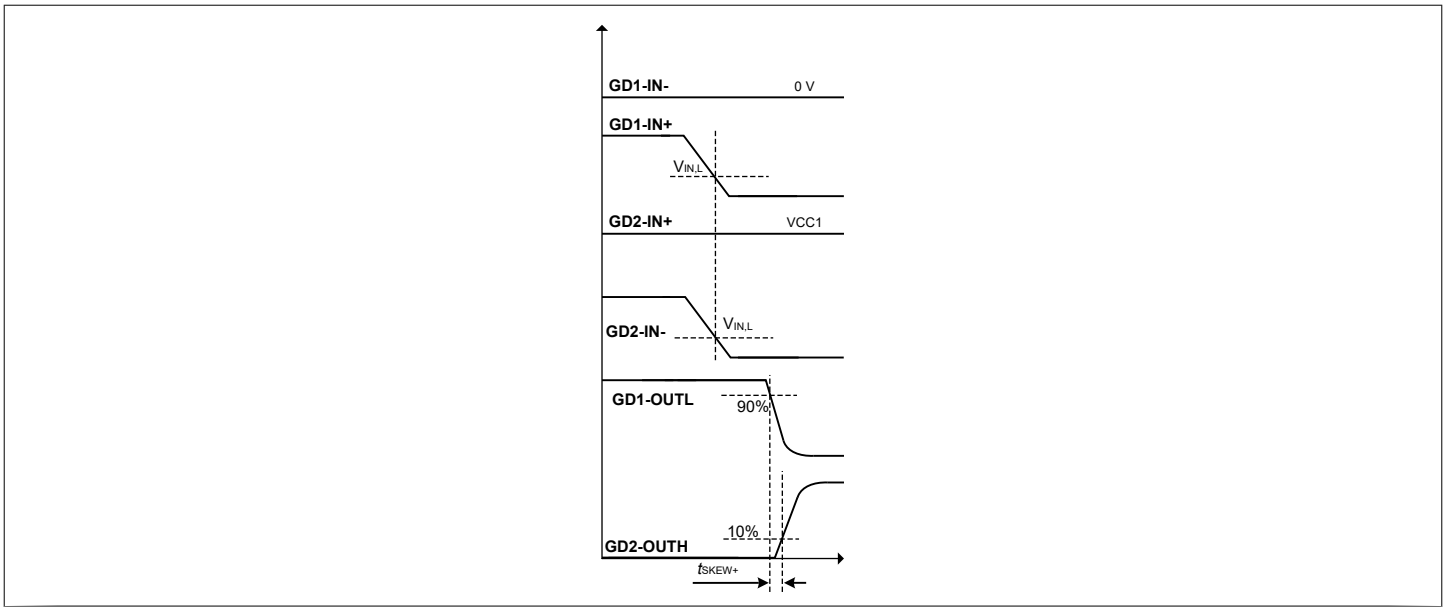


Figure 33 Skew plus using the inverting and non-inverting inputs with falling edges

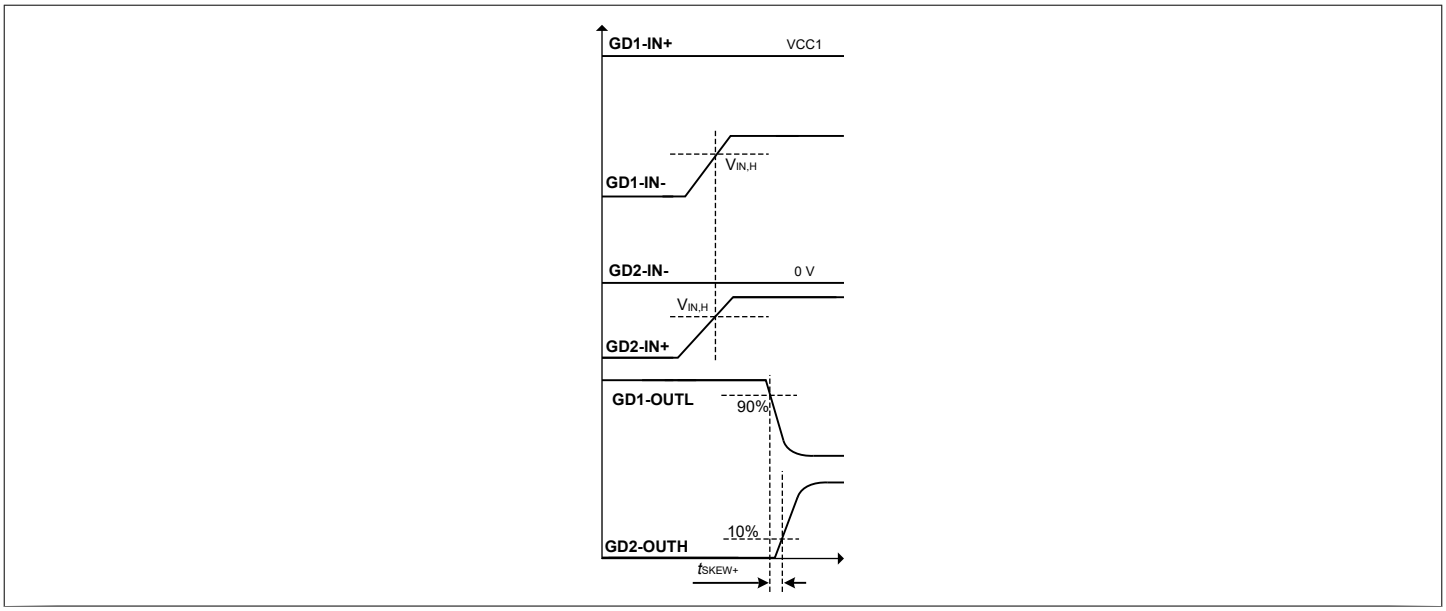


Figure 34 Skew plus using the inverting and non-inverting inputs with rising edges

6.2 Undervoltage lockout (UVLO)

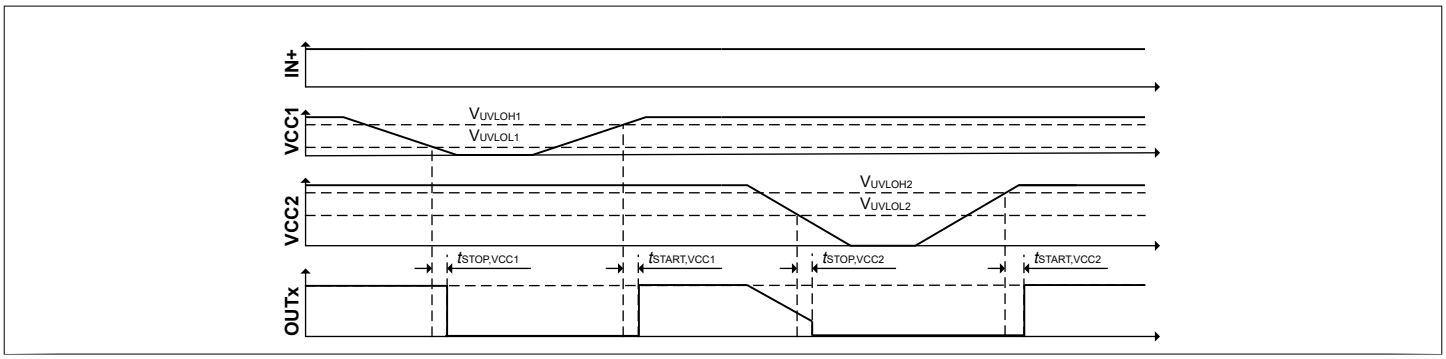


Figure 35 UVLO behavior

To ensure correct switching of IGBT, Si or SiC MOSFET, the device is equipped with an independent undervoltage lockout for both input and output side. Operation starts only after both supply voltage levels have increased beyond the respective V_{UVLOH} levels.

If the power supply voltage V_{VCC1} of the input chip drops below V_{UVLOL1} a turn-off signal is sent to the output chip before power-down. The IGBT, Si or SiC MOSFET is switched off and the signals at *IN+* and *IN-* are ignored until V_{VCC1} reaches the power-up voltage V_{UVLOH1} again.

If the power supply voltage V_{VCC2} of the output chip goes down below V_{UVLOL2} the IGBT, Si or SiC MOSFET is switched off and signals from the input chip are ignored until V_{VCC2} reaches the power-up voltage V_{UVLOH2} again.

Note: V_{VCC2} is always referred to VEE2 and does not differentiate between unipolar or bipolar supply.

6.3 CMTI measurement setup

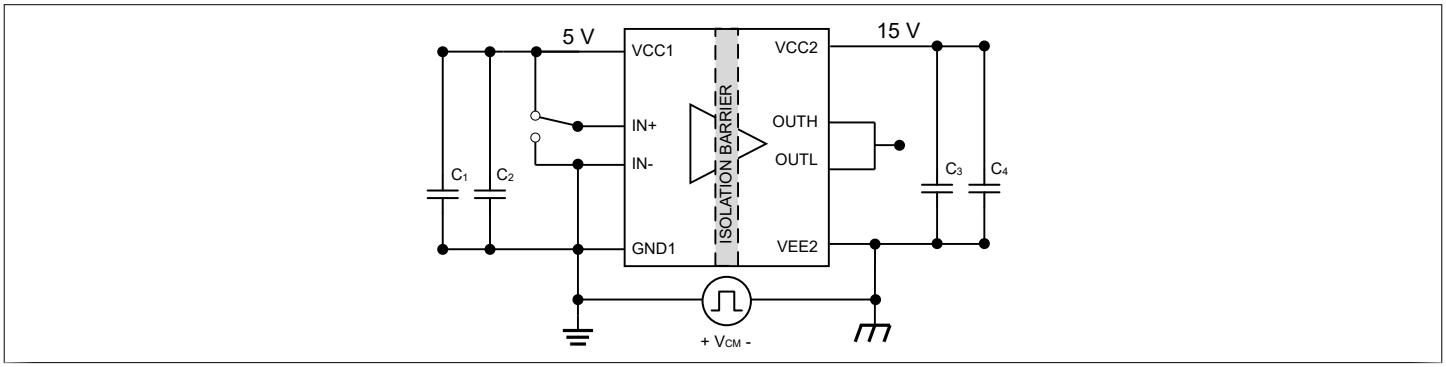


Figure 36 CMTI test circuit

Figure 36 shows CMTI test setup for the common mode transient immunity measurements.

7 Functional description

The EiceDRIVER™ 1ED314xMU12F (X3-Compact) gate driver ICs are compact, general purpose gate drivers for IGBTs and MOSFETs. They offer basic control and protection features enabling fast and easy design of highly reliable systems.

The integrated galvanic isolation, between the input control side and the driving output stage, grants additional safety. The gate driver IC's input voltage supply range supports the direct connection of various signal sources like microcontrollers and DSPs.

7.1 Input features

The input features of the gate driver IC include undervoltage lockout of input supply, pull-up and pull-down resistors of logic inputs, and signal filtering.

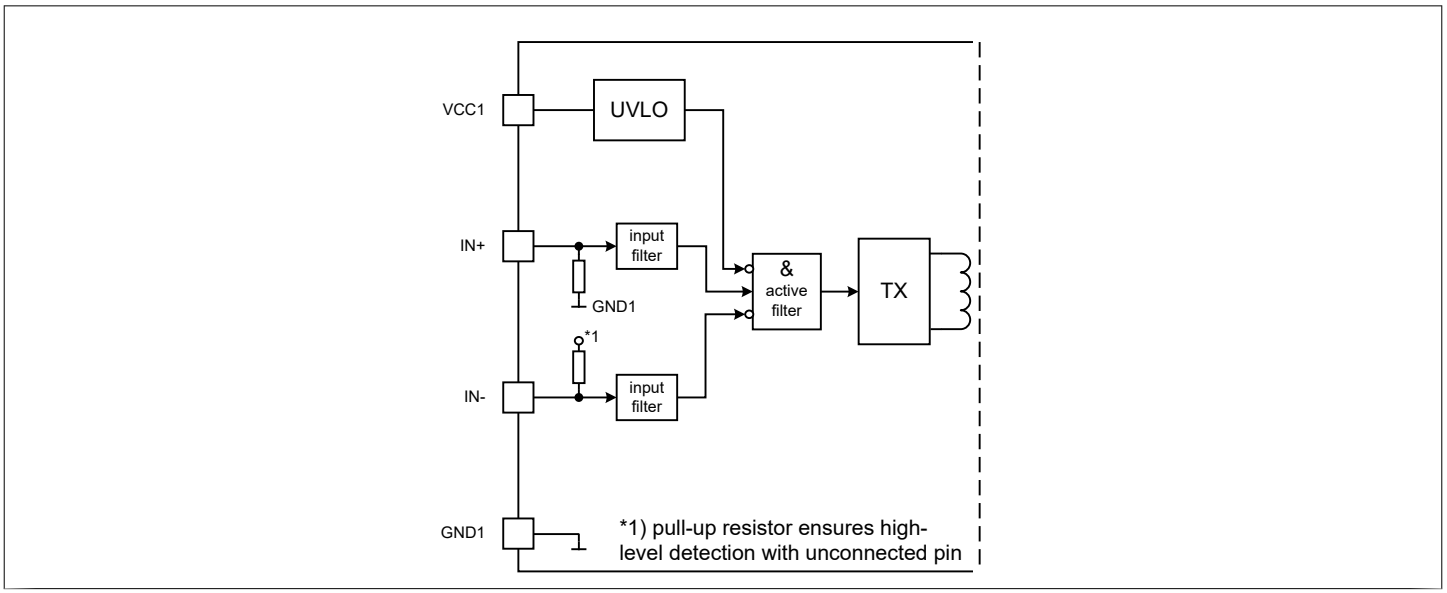


Figure 37 Block diagram of input section

The gate driver IC input section consists of the following functional blocks:

- input undervoltage lockout circuit
- signal filtering
- pull-up resistor for inverting input
- pull-down resistor for non-inverting input
- signal transmission to isolated output section

7.1.1 Input supply and undervoltage lockout (UVLO)

The input supply range has absolute maximum ratings of -0.3 V to 17 V. Static operation beyond the absolute maximum voltage (abs max) damages internal structures and is therefore considered a forbidden area.

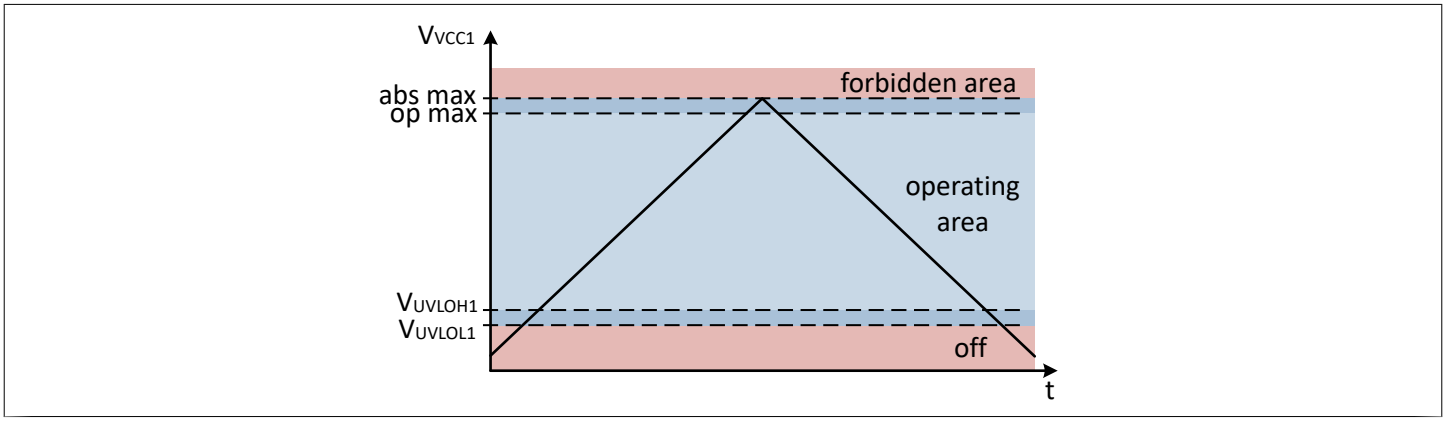


Figure 38 Input supply and UVLO threshold

At a crossing of the turn on undervoltage lockout threshold (V_{UVLOH1}) during a positive ramp at *VCC1* pin, the input section starts to operate. It evaluates the input signals *IN+* and *IN-* and transmits their current state to the output section. During V_{VCC1} ramp down and crossing of the turn-off undervoltage lockout threshold (V_{UVLOL1}), the input section will send a final off signal regardless of the *IN+* or *IN-* state. V_{UVLOL1} and V_{UVLOH1} form a hysteresis which offers stable operation even at low levels.

Any voltage overshoot above the absolute maximum voltage (abs max) rating can damage the driver circuits. In this area, the current consumption increases dramatically and therefore results in a violation of the maximum allowed input power loss. The operating area is defined between the turn-on undervoltage lockout threshold (V_{UVLOH1}) and the maximum recommended operating voltage.

7.1.2 Pull-up and pull-down resistors for the input pins

The input pull-up or pull-down resistors ensure an off state in case the corresponding input is not connected. These resistors have a typical value of 75 kΩ. Even with the maximum allowed voltage at *VCC1* pin, the input current due to these resistors stays below 1 mA.

The pull-up and pull-down resistors are designed to be connected to an external supply or ground potential for permanent activation of the individual driver input.

7.1.3 Input signal filtering (deglitch filter)

The input section of the driver IC filters both input signals to suppress short pulses triggered by external influences.

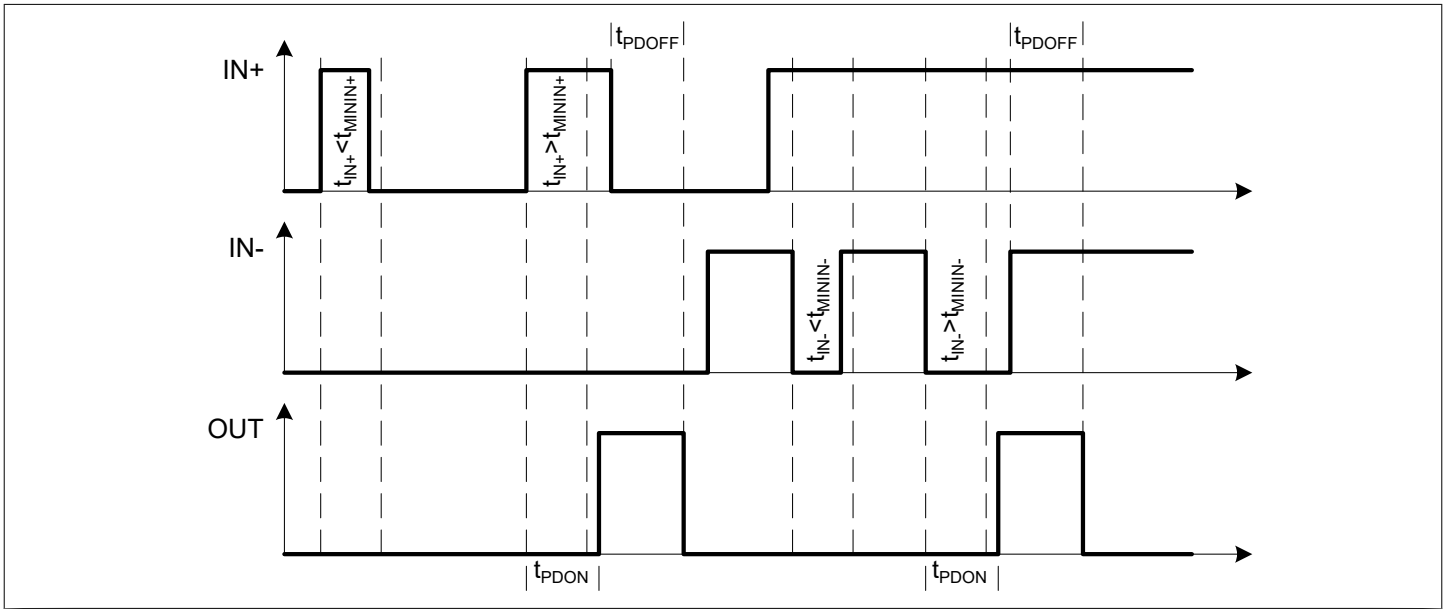


Figure 39 Input pulse suppression and turn-on/turn-off propagation delay

Every pulse at *IN+* or *IN-*, shorter than the input pulse suppression time t_{INFLT}, will be filtered and will not be transmitted to the output chip. Longer pulses will be sent to the output with the shown propagation delay t_{PDON} and t_{PDOFF}. This aids the design and an external RC filter for noise suppression will not be needed in most cases.

7.2 Output features

This section describes the gate driver output sections. The output features of the gate driver IC include undervoltage lockout for the output supply, shoot trough protection circuitry for the internal output stage and the active shutdown circuitry.

The current sourcing stage design of the gate driver ICs is designed with a PMOS-only MOSFET. The PMOS will deliver a strong current, not only at the beginning, but constantly all the way up to the *VCC2* rail, ensuring a fast turn-on of the IGBT, Si or SiC MOSFET.

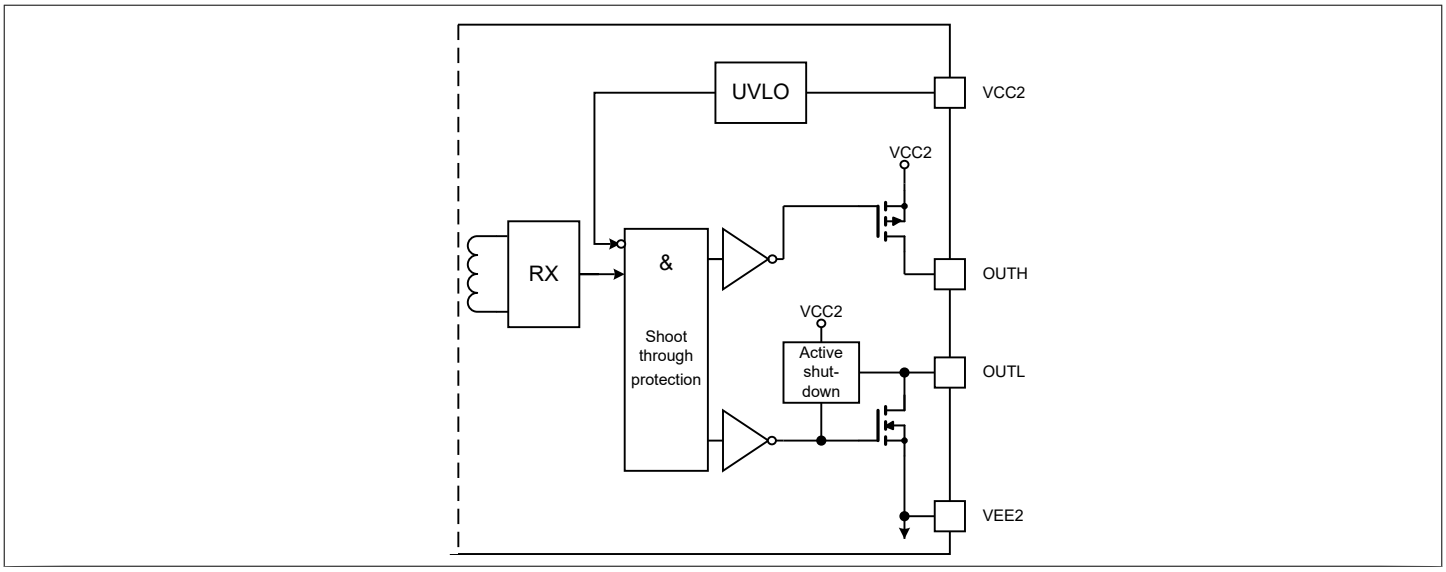


Figure 40 Block diagram of output section

The gate driver IC output section consists of the following functional blocks:

- output undervoltage lockout circuit
- isolated signal receiver from the input section
- sourcing and sinking output stage
- active shutdown circuitry

7.2.1 Output undervoltage lockout (UVLO)

The output supply range has a positive absolute maximum rating of 35 V for all variants. The gate driver ICs are therefore capable of providing a bipolar gate voltage to a connected power switch.

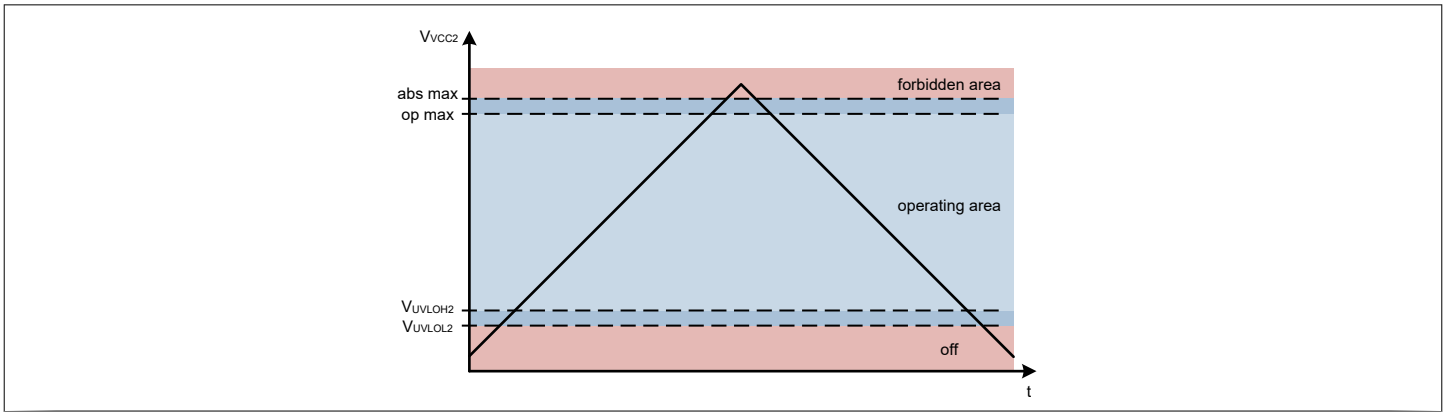


Figure 41 Output supply and UVLO threshold

At a crossing of the turn on undervoltage lockout threshold(V_{UVLOH2}) during a positive ramp at *VCC2* pin in relation to the *VEE2* pin, the output section starts operating. The messages received from the input side of the gate driver is received and evaluated. During V_{VCC2} ramp down and crossing of the turn-off undervoltage lockout threshold (V_{UVLOL2}), the output section will initiate a turn-off command regardless of the communication requests received from the input section. V_{UVLOL2} and V_{UVLOH2} form a hysteresis which offers stable operation even at low levels.

Any voltage overshoot above the absolute maximum voltage rating can damage the driver circuits. In this area, the current consumption increases dramatically and therefore results in a violation of the maximum allowed input power loss. The operating area is defined between the turn-on undervoltage lockout threshold (V_{UVLOH2}) and the maximum recommended operating voltage.

7.2.2 Active shutdown

The active shutdown function is a protection feature of the driver. It is designed to avoid a free-floating gate of a connected power switch to trigger a turn-on.

The active shut-down feature ensures a safe IGBT, Si or SiC MOSFET off-state in case the output chip is not connected to the power supply or an undervoltage lockout is in effect. The IGBT, Si or SiC MOSFET gate is clamped via the *OUT-* pin to *VEE2*.

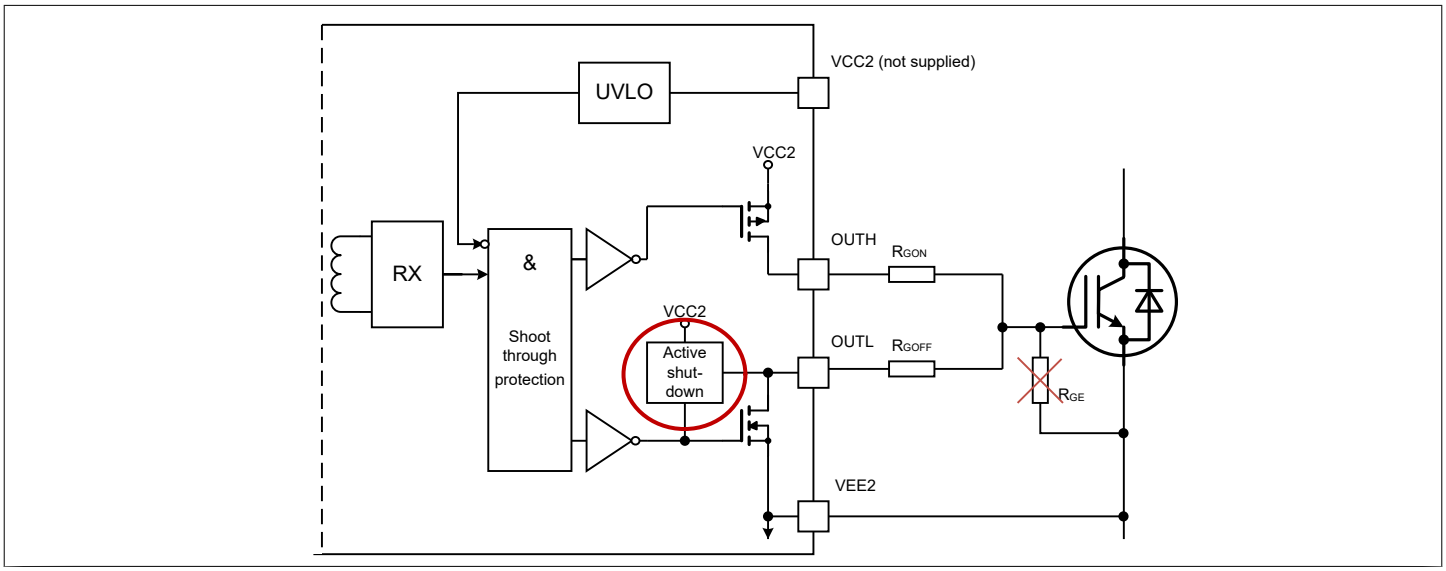


Figure 42 Block diagram showing active shutdown

In case of a missing or collapsing power supply at the *VCC2* pin, the output section of the driver operates in the active shutdown mode. In this case the driver uses the floating voltage of the connected gate to supply this internal circuit. This solution is by far stronger than using the external R_{GE}. At the same time, in case of fast dV/dt events on the switch that would generate miller current that could bias the gate, even when the gate driver is not powered on, the active shutdown circuit will use the voltage to self power and actively pull the gate low

7.2.3 Driver outputs and supply

The output driver section uses MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage during on-state and short circuit can be maintained as long as the driver's supply is stable. Due to the low internal voltage drop, switching behavior of the IGBT, Si or SiC MOSFET is predominantly governed by the gate resistor for as long as the current rating of the gate driver is not exceeded. Furthermore, it reduces the power to be dissipated by the driver as most of the energy is dissipated in the gate resistor.

With separated outputs for current sourcing and sinking in a gate driver IC, individual gate resistors can be used for turning a power switch on and off. By having separate sourcing *OUTH* and sourcing *OUTL* pins, the BOM can be optimized and save the bypass diode for each power switch used.

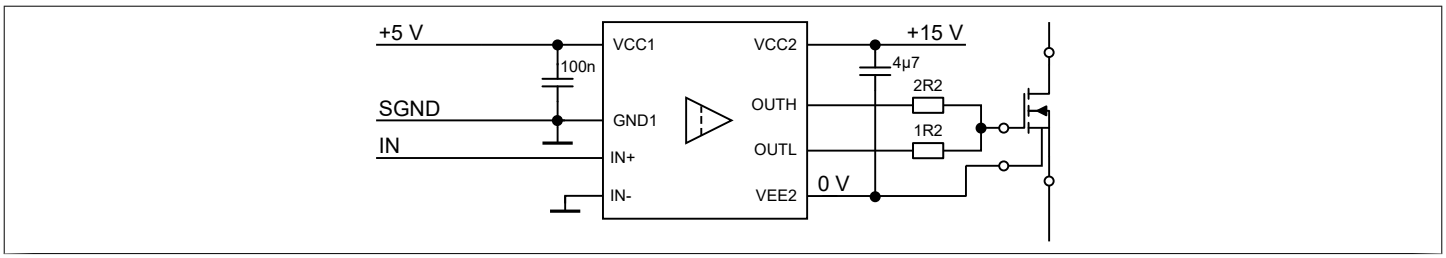


Figure 43 Circuit example for unipolar power supply driving SiC MOSFET

When driving the switch with unipolar power supplies, the *VEE2* pin should be connected directly to the source or emitter of the power transistor as shown in Figure 43.

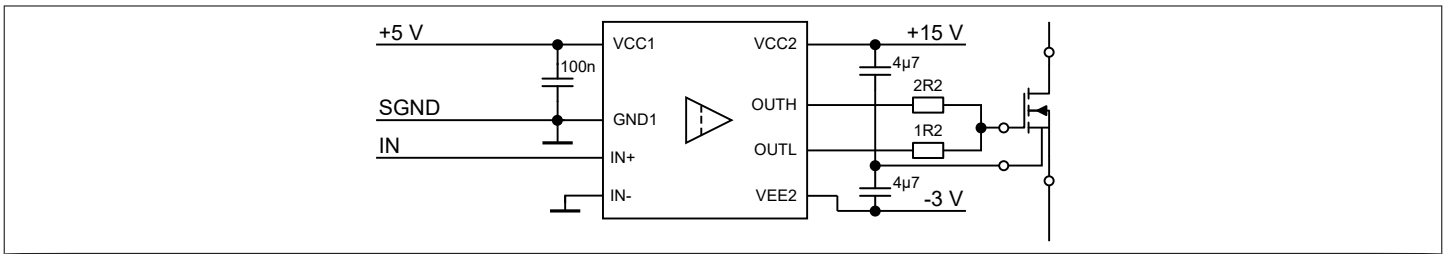


Figure 44 Circuit example for bipolar power supply driving SiC MOSFET

When driving the switch with bipolar power supplies, a virtual ground should be created between two capacitors connected to the *VCC2* and *VEE2* pins. This virtual ground should then be connected to the source or emitter of the power transistor as shown in Figure 44.

8 Application information

8.1 Application usage of *IN+* and *IN-*

The inverting, *IN-*, and non-inverting,*IN+*, input pins offer multiple possibilities to connect PWM input and logic signals for various control and protection uses.

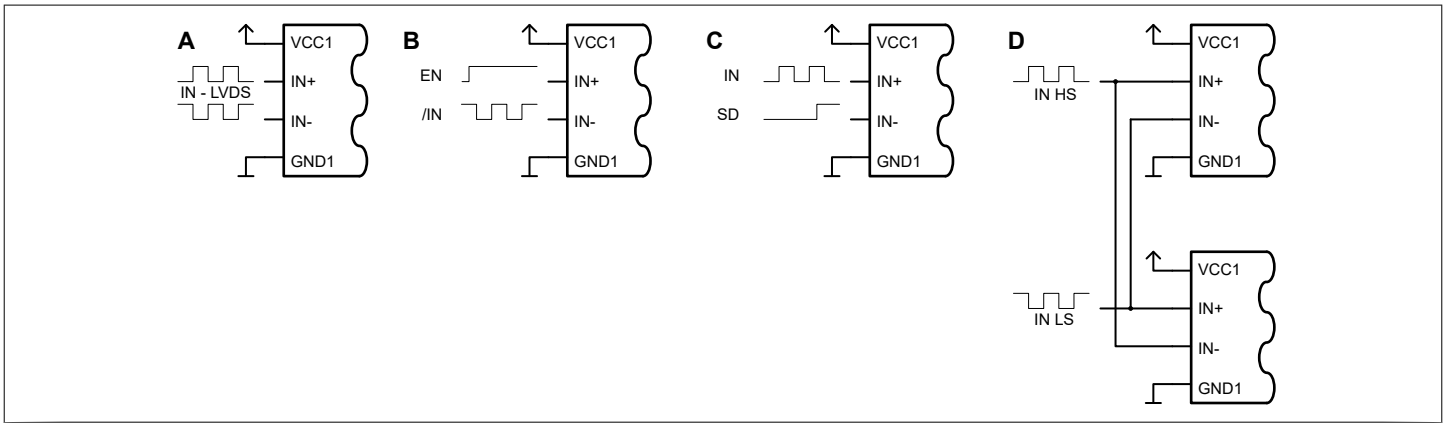


Figure 45 Input *IN+* and *IN-* usage

Apart from using both inputs with a differential signal (A) (*VCC1* and *GND1* levels), using only one input signal for actual switch control leaves the second input available for functions like Enable (B), Shutdown (C) or Interlock (D).

A) Differential signal

Applying a logic-level differential signal on both *IN+* and *IN-* with the positive level of *VCC1* pin and the negative level of *GND1* pin improves common-mode noise rejection.

B) Enable

Using the *IN+* pin as enable signal leaves the *IN-* to control the output PWM with an inverted logic input signal. The enable signal can then be shared between gate driver ICs of a complete inverter to start operation with a single control signal.

C) Shutdown

Using the *IN-* pin as shutdown signal leaves the *IN+* to control the output PWM with a non-inverted logic input signal. The shutdown signal can then be shared between gate driver ICs of a complete inverter to interrupt operation with a single control signal.

D) Interlock

Interlocking is often used in half-bridge configurations to avoid a shoot through current from the high-voltage DC bus supply. Connecting the following input signal pins of the top and bottom driver IC together inhibits a static turn-on for both channels at the same time

- top driver non-inverting input (*IN+*) with the bottom driver inverting input (*IN-*)
- bottom driver non-inverting input (*IN+*) with the top driver inverting input (*IN-*)

Dynamic turn-on and off characteristics of gate drivers and power switches can still lead to short-term shoot though. To avoid overlapping turn-on times at the power switches, a proper deadtime setting for the PWM generation at the microcontroller is recommended.

8.2 Gate resistor selection

The supply conditions are rarely the same as the supply conditions that are used in power transistor data sheets. Therefore, an adaptation of the power transistor datasheet values is required to obtain a starting point for the optimization of the final gate resistor. The method which is proposed here uses the same peak gate current value for both the actual application and the power transistor datasheet.

The peak gate current as per power transistor datasheet equals to:

$$I_{\mathrm{G,pk}} = \frac{\Delta V_{\mathrm{GE}}}{R_{\mathrm{G,\,datasheet}} + R_{\mathrm{G,int}}} = \frac{\Delta V_{\mathrm{GS}}}{R_{\mathrm{G,\,application}} + R_{\mathrm{G,int}}} \quad \text{with} \quad \Delta V_{\mathrm{GS}} = V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}} \tag{1}$$

Solving this equation for R_G leads to:

$$R_{\mathrm{G}} = \frac{\Delta V_{\mathrm{GS}}}{I_{\mathrm{G,pk}}} - R_{\mathrm{G,int}} \tag{2}$$

As the Miller voltage of IGBTs varies considerably as a function of the collector voltage and current, this method results in a starting point. Further evaluations, such as EMI measurements, are required for the final dimensioning of the gate resistors as they have to be adjusted to work with the circuitry inductance, margins and allowed dV/dt transients.

8.3 Power dissipation estimation

The gate driver input side losses are dominated by the quiescent losses, which are calculated by:

$$P_{\mathrm{Q1}} = V_{\mathrm{VCC1}} \cdot I_{\mathrm{VCC1}} \tag{3}$$

The gate driver output side losses consist of the quiescent current losses P_{Q2}at nominal switching frequency and no load, the sourcing losses P_{source} and the sinking losses P_{sink}:

$$P_{\mathrm{OUT}} = P_{\mathrm{Q2}} + P_{\mathrm{source}} + P_{\mathrm{sink}} \tag{4}$$

The turn-on, P_{source}, and turn-off, P_{sink}, losses can be estimated using the resistive voltage divider between inner gate driver resistance, $R_{DSON,H}$or $R_{DSON,L}$, and external gate resistor, $R_{G,ext}$, with the application related gate charge, Q_G, the total gate driving voltage, V_{VCC2} - V_{VEE2}, and switching frequency, f_{sw}:

$$P_{\mathrm{source}} = \frac{1}{2} Q_G \cdot f_{\mathrm{sw}} \cdot (V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}) \cdot \frac{R_{\mathrm{DSON,H}}}{R_{\mathrm{DSoON,\,H}} + R_{\mathrm{G},ext,\,\mathrm{ON}} + R_{\mathrm{G,int}}}$$
$$P_{\mathrm{sink}} = \frac{1}{2} Q_G \cdot f_{\mathrm{sw}} \cdot (V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}) \cdot \frac{R_{\mathrm{DSON,L}}}{R_{\mathrm{DSON,L}} + R_{\mathrm{G},ext,\,\mathrm{OFF}} + R_{\mathrm{G,int}}} \tag{5}$$

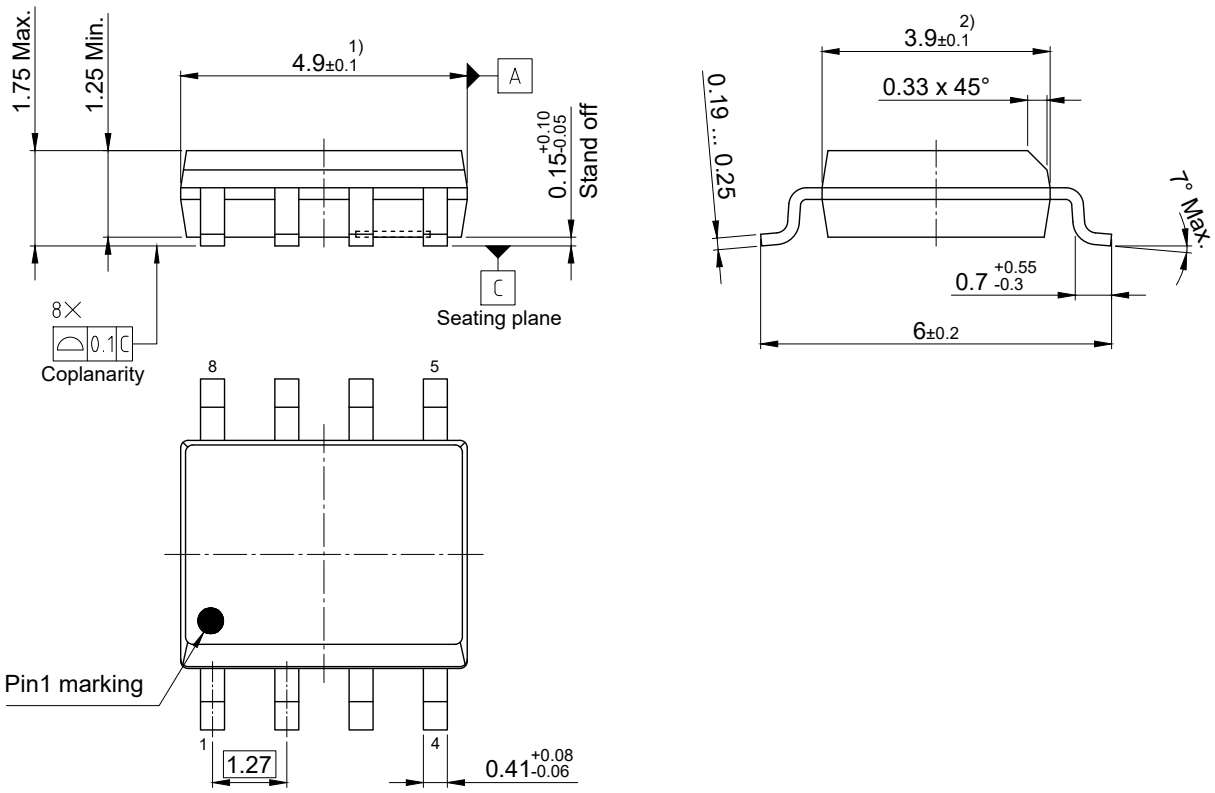
Additionally, external components that surround the gate driver can heat up the IC. The mere calculation of losses and the theoretical junction temperature alone are not sufficient for a proven gate driver circuit design. A verification by measurement is needed to avoid unexpected effects in the application. The identification of hot spots is possible, for example, by using an infrared camera.

9 Related products

Note: Please consider the gate driver IC power dissipation and insulation requirements for the selected power switch and operating condition.

Product group	Product name	Description
TRENCHSTOP™ IGBT Discrete	IKWH40N65WR6	650 V, 40 A IGBT with anti-parallel diode in TO-247-3-HCC
	IHW30N160R5	1600 V, 30 A IGBT Discrete with anti-parallel diode in TO-247
	IKW15N120CS7	1200 V IGBT7 S7, 15 A IGBT with anti-parallel diode in TO247
	IKQ75N120CS7	1200 V IGBT7 S7, 75 A IGBT with anti-parallel diode in TO247-3
CoolSiC™ SiC MOSFET Discrete	IMBF170R1K0M1	1700 V, 1000 mΩ SiC MOSFET in TO-263-7 with extended creepage
	IMZA120R040M1H	1200 V, 40 mΩ SiC MOSFET in TO247-4 package
	IMZA120R014M1H	1200 V, 14 mΩ SiC MOSFET in TO247-4 package
	IMBG120R030M1H	1200 V, 30 mΩ SiC MOSFET in TO-263-7 package
	IMYH200R012M1H	2000 V, 12 mΩ SiC MOSFET in TO-247-PLUS with high creepage and clearance
CoolSiC™ SiC MOSFET Module	FS33MR12W1M1H_B11	EasyPACK™ 1B 1200 V, 33 mΩ sixpack module
	FF17MR12W1M1H_B11	EasyDUAL™ 1B 1200 V, 17 mΩ half-bridge module
	FF4MR12W2M1H_B11	EasyDUAL™ 2B 1200 V, 4 mΩ half-bridge module
	F4-17MR12W1M1H_B11	EasyPACK™ 1B 1200 V, 17 mΩ fourpack module
TRENCHSTOP™ IGBT Modules	F4-100R17N3E4	EconoPACK™ 3 1700 V, 100 A fourpack IGBT module
	F4-200R17N3E4	EconoPACK™ 3 1700 V, 200 A fourpack IGBT module
	FP10R12W1T7_B11	EasyPIM™ 1B 1200 V, 10 A three phase input rectifier PIM IGBT module
	FS100R12W2T7_B11	EasyPACK™ 2B 1200 V, 100 A sixpack IGBT module
	FP150R12KT4_B11	EconoPIM™ 3 1200V three-phase PIM IGBT module
	FS200R12KT4R_B11	EconoPACK™ 3 1200 V, 200 A sixpack IGBT module

10 Package dimensions



1) Does not include plastic or metal protrusion of 0.15 mm max. per side
2) Does not include plastic protrusion of 0.25 mm max. per side.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]
Drawing according to ISO 8015, general tolerances ISO 2768-mK

Figure 46 DSO-8 150 mil (Plastic (green) dual small outline package, 150 mil)

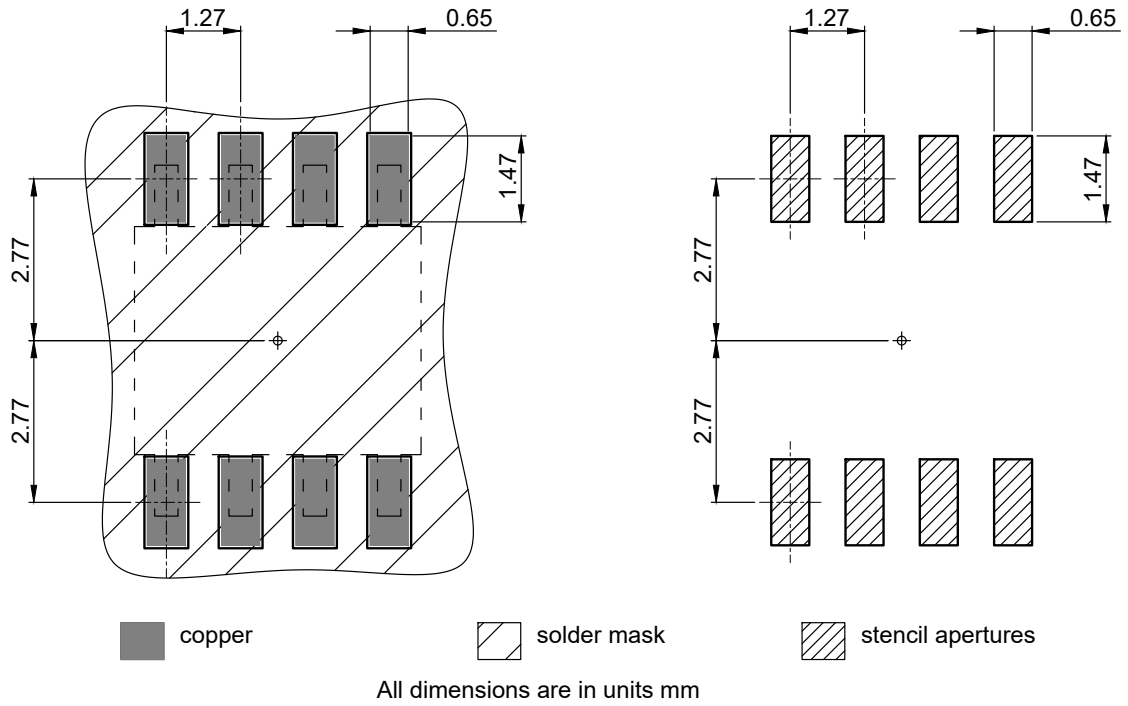


Figure 47 DSO-8 150 mil recommended footprint

Revision history

Document version	Date of release	Description of changes
v1.11	2023-07-26	• removed duplicate parameters from dynamic characteristics and active shut down
v1.10	2023-06-26	• increased CTI value to 600
v1.0	2023-01-15	• Initial release

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