NXT4556AUR

SIM card interface level translator

Rev. 1 — 5 December 2023 Product data sheet

1. General description

The NXT4556AUR device is built for interfacing a SIM card with a single low-voltage host side interface. The NXT4556AUR has three level translators to convert the data, RST and CLK signals between a SIM card and a host microcontroller. A high speed level translation capable of supporting class-B, class-C SIM cards. V_{CC_SIM} power-down initiates a shutdown sequence on SIM card pins in accordance with ISO-7816-3.

The NXT4556AUR is compliant with all ETSI, IMT-2000 and ISO-7816 SIM/Smart card interface requirements.

2. Features and benefits

- Support SIM cards and eSIM with supply voltages 1.62 V to 3.3 V
- Host micro-controller operating voltage range: 1.08 V to 1.98 V
- Automatic level translation of I/O, RST and CLK between SIM card and host side interface with capacitance isolation
- Incorporates shutdown feature for the SIM card signals according to ISO-7816-3
- High $V_{dis(UVLO\_AC)}$ switching level, arranging quick shut down when V_{CC_SIM} powers down
- Integrated pull-up resistors; no external resistor required
- Integrated EMI Filters suppresses higher harmonics of digital I/O's
- Low current shutdown mode < 1 μA
- Supports clock speed beyond 5 MHz clock
- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2 kV
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1 kV
  - IEC61000-4-2 level 4, contact and air discharge on all SIM card-side pins exceeds 8 kV and 15 kV
- Fast activation at power up
- Smooth IO signals at activation

3. Applications

- NXT4556AUR can be used with a range of SIM card attached devices including:
  - Mobile and personal phones
  - Wireless modems
  - SIM card terminals

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NXT4556AUR	-40 °C to +85 °C	WLCSP9	wafer level chip-scale package; 9 bumps; 0.92 × 0.92 × 0.42 mm body	SOT8057-1

5. Marking

Table 2. Marking

Type number	Marking code[1]
NXT4556AUR	z6

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram

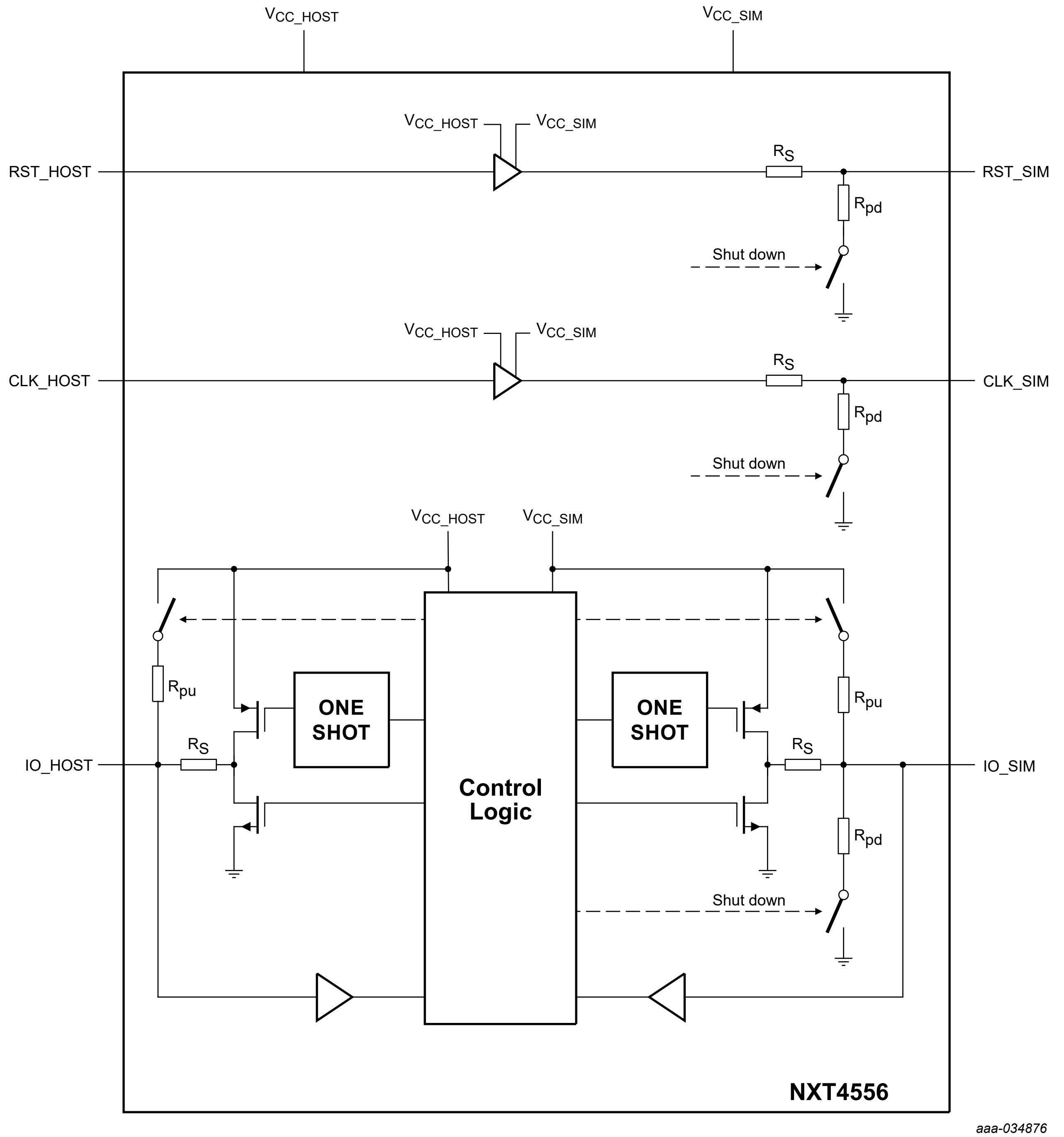


Fig. 1. Functional diagram

7. Pinning information

7.1. Pinning

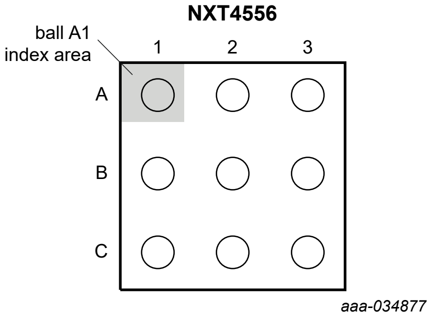


Fig. 2. Bump configuration for SOT8057-1 (WLCSP9)

NXT4556

	1	2	3
A	RST_HOST	V_{CC_HOST}	RST_SIM
B	CLK_HOST	GND	CLK_SIM
C	IO_HOST	V_{CC_SIM}	IO_SIM

aaa-034878

Transparent top view

Fig. 3. Bump mapping for SOT8057-1 (WLCSP9)

7.2. Pin description

Table 3. Pin description

Symbol	Bump	Type	Description
RST_HOST	A1	I	Reset input from host controller.
V_{CC_HOST}	A2	power	Supply voltage for the host controller side input/output pins (CLK_HOST, RST_HOST, IO_HOST). This pin should be bypassed with a 0.1 µF ceramic capacitor close to the pin.
RST_SIM	A3	O	Reset output pin for the SIM card.
CLK_HOST	B1	I	Clock input from host controller.
GND	B2	ground	Ground for the SIM card and host controller. Proper grounding and bypassing are required to meet ESD specifications.
CLK_SIM	B3	O	Clock output pin for the SIM card.
IO_HOST	C1	I/O	Host controller bidirectional data input/output. This pin can be driven from push-pull as well as open-drain drivers.
V_{CC_SIM}	C2	power	Supply voltage for the SIM CARD side input/output pins. This input voltage ranges from 1.62 V to 3.3 V. This pin should be bypassed with a 0.1 µF ceramic capacitor close to the pin.
IO_SIM	C3	I/O	SIM card bidirectional data input/output. The SIM card output must be on an open-drain driver.

8. Functional description

8.1. Function table

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level, X = don't care.

V_{CC_HOST}	V_{CC_SIM}	Operation	IO_HOST	RST_SIM	CLK_SIM	IO_SIM
1.08 V to 1.98 V	1.62 V to 3.3 V	OPERATIONAL	R_{pu} = 20 kΩ; L/H	L/H	L/H	R_{pu} = 20 kΩ; L/H
1.08 V to 1.98 V	0 V	SHUT DOWN	R_{pu} = 20 kΩ	R_{pd} = 400 Ω	R_{pd} = 400 Ω	R_{pd} = 400 Ω
0 V	1.62 V to 3.3 V	SHUT DOWN	undefined	R_{pd} = 400 Ω	R_{pd} = 400 Ω	R_{pd} = 400 Ω

When both V_{CC_HOST} and V_{CC_SIM} are biased in the recommended range the product is operational and parameters are specified. Pull up resistors (R_{pu}) are enabled on IO_HOST and IO_SIM but additionally high drive output (L/H) can appear, overruling the R_{pu} = 20 kΩ. Operation of the channels in operational mode is explained in Section 8.2.

When V_{CC_SIM} drops below 86% of V_{CC}, the shutdown sequence is initiated. This shutdown sequence is described in Section 8.3. For this partial power down mode the parameters R_{pd} and I_{CC_HOST} are defined for V_{CC_SIM} = 0 V.

When V_{CC_HOST} drops out, the product also turns to shut down mode. For this partial power down mode the parameters R_{pd} and I_{CC_SIM} are defined for V_{CC_HOST} = 0 V.

8.2. Operational mode

The functional diagram of the NXT4556AUR is shown in Fig. 1.

The upper part of Fig. 1 shows the RST and CLK channels which are uni-directional level shifters from the host to the SIM card side.

The bottom part shows the architecture of the bidirectional I/O channel. Both on IO_HOST and IO_SIM a resistor R_{pu} pulls up the I/O node. On both sides an output stage is present that consists of a PMOST and an NMOST device. Each output stage drives the output through a series resistor R_S. Input stages sense the I/O nodes and pass LOW/HIGH information to the control logic that controls the translator outputs and several pull-up and pull-down resistors.

The NXT4556AUR I/O channel does not require a dedicated input signal to control the direction of data flow from IO_HOST to IO_SIM or from IO_SIM to IO_HOST. Change in driving direction is possible when both sides are at HIGH state. The control logic recognizes the I/O node with the first falling edge and grants control over the opposite I/O node. When for example the IO_HOST is turned LOW, the control circuit will turn on the NMOST on the IO_SIM side, pulling LOW IO_SIM. The IO_SIM pin is then an output only, until IO_HOST is turned HIGH and the translator has turned IO_SIM HIGH again.

The PMOST devices are used to actively turn high the outputs. Each PMOST is driven by a one-shot circuit that generates a pulse. For example: Assuming HOST to SIM communication, when the IO_HOST is turned HIGH, it will activate the one shot circuit on the IO_SIM side. A pulse starts, arranging a fast LOW to HIGH transition on IO_SIM. When the pulse has finished, the PMOST is released. At that stage, the system returns to a standard open drain state whereby the pull resistors keep the I/O nodes HIGH.

At the same time, at a LOW to HIGH transition, the one shot on the input side is activated as well. In an open drain application, this creates a typical input LOW to HIGH waveform. Fig. 4 shows an example of a LOW to HIGH transition in an open drain application.

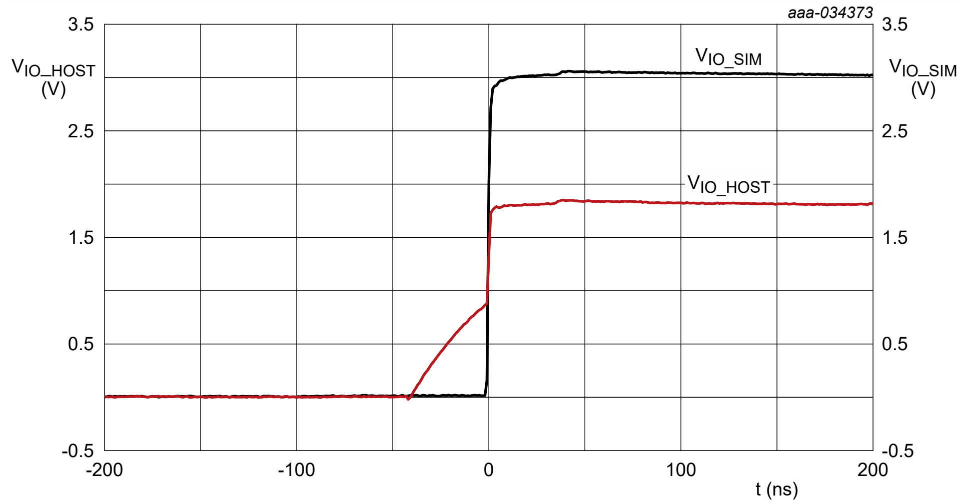


Fig. 4. LOW to HIGH transition for IO_HOST to IO_SIM communication

Looking at the input signal, the first part of the LOW to HIGH transition is an exponential curve caused by the I/O node capacitance being charged via the pull-up resistor. The second part starts when the input signal crosses the input switching level. The rising edge is accelerated dramatically by the PMOST that is turned on by the one shot on the input side.

In case of a communication error or some other unforeseen incident that may drive both connected sides of the drivers at the same time, the internal logic automatically prevents stuck-at situation. This ensures that both I/Os will return to HIGH level once released from being driven LOW.

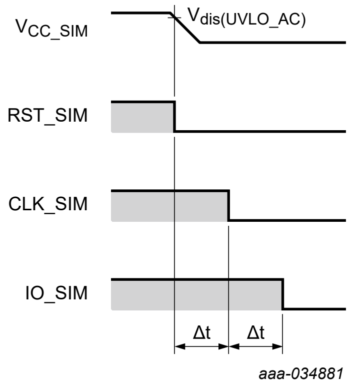
In shut down mode, the control circuit disables all output stages. Additionally, in shut down mode, the pull-up resistor on IO_SIM side is disabled, and all pull-down resistors R_{pd} on SIM side are enabled, pulling LOW the pins on the SIM side. The shut down sequence is explained in more detail in Section 8.3.

8.3. Shutdown sequence

The ISO 7816-3 specification specifies the shutdown sequence for the SIM card signals to ensure that the card is properly disabled for power savings. Also, during hot swap, the orderly shutdown of these signals helps to avoid any improper write and corruption of data.

When V_{CC_SIM} drops below $V_{dis(UVLO\_AC)}$, the shutdown sequence is initiated. Fig. 5 illustrates the shutdown sequence initiated by V_{CC_SIM} being powered down.

The shut down sequence starts by pulling down the RST_SIM output. Once RST_SIM is turned LOW, CLK_SIM and IO_SIM are pulled LOW sequentially, one-by-one. Internal pull-down resistors on the SIM pins are used to pull the SIM channels LOW. The internal pull-down resistors, R_{pd}, that pull down the three pins on the SIM side are shown in Fig. 1. The shutdown sequence is completed in a few microseconds. The interval time (Δt), is typically 4 μs.



Δt = 4 μs (typical)

The shaded areas indicate that the signals are HIGH or LOW.

Fig. 5. Shutdown sequence for RST_SIM, CLK_SIM and IO_SIM of NXT4556 SIM card translator

8.4. UVLO

When V_{CC_SIM} drops below $V_{dis(UVLO\_AC)}$, the translator goes to shut down mode. This is illustrated in Fig. 5. The switching level $V_{dis(UVLO\_AC)}$ has a high value of approximately 86 % × V_{CC_SIM}. The circuitry uses an AC detection mechanism that operates accurately with a falling slope that is typical in the SIM card application. Next to this AC detection, a standard UVLO detection is in place that has no condition with respect to the slope of the rising or falling V_{CC_SIM}. For the standard UVLO, the parameters $V_{en(UVLO)}$ and $V_{dis(UVLO)}$ are involved which have lower values than $V_{dis(UVLO\_AC)}$. When V_{CC_SIM} is powered up, the translator is enabled when V_{CC_SIM} crosses $V_{en(UVLO)}$.

8.5. EMI filter

All output driver stages of I/O, RST and CLK channels are equipped with EMI filters to reduce interference towards sensitive mobile communication.

8.6. ESD protection

The device has robust ESD protections on all SIM card pins. The architecture prevents any stress for the host: the voltage translator discharges any stress to supply ground.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	SIM card side; IEC 61000-4-2; level 4; contact discharge	-	±8	kV
		SIM card side; IEC 61000-4-2; level 4; air discharge	-	±15	kV
		all other pins; IEC 61000-4-2; level 4	-	±2	kV
		all other pins; HBM [1]	-	±2	kV
		all other pins; CDM [2]	-	±1	kV
V_{CC_HOST}	supply voltage		GND - 0.5	4.6	V
V_{CC_SIM}	SIM card supply voltage		GND - 0.5	4.6	V
V_I	input voltage	CLK_HOST; input signal voltage, HOST side	GND - 0.5	4.6	V
		RST_HOST; input signal voltage, HOST side	GND - 0.5	4.6	V
		IO_HOST; input signal voltage, HOST side	GND - 0.5	4.6	V
		CLK_SIM; input signal voltage, SIM side	GND - 0.5	4.6	V
		RST_SIM; input signal voltage, SIM side	GND - 0.5	4.6	V
		IO_SIM; input signal voltage, SIM side	GND - 0.5	4.6	V
I_O	output current	IO_HOST, IO_SIM, RST_SIM, CLK_SIM	-50	50	mA
T_{stg}	storage temperature		-55	+125	°C

[1] Human Body Model (HBM) according to JESD22-A-A114.
[2] Charged-Device Model (CDM) according to JESD22-C101.

10. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC_HOST}	supply voltage	[1]	1.08	-	1.98 V	V
V_{CC_SIM}	card side supply voltage	[1]	1.62	-	3.3	V
V_I	input voltage	HOST side	-0.3	-	$V_{CC\_HOST} + 0.3$	V
		SIM side	-0.3	-	$V_{CC\_SIM} + 0.3$	V
T_{amb}	ambient temperature		-40	+25	+85	°C

[1] $V_{CC\_SIM} \geq V_{CC\_HOST}$

11. Electrical characteristics

Table 7. Electrical characteristics

1.08 V ≤ V_{CC_HOST} ≤ 1.98 V; 1.62 V ≤ V_{CC_SIM} ≤ 3.3 V; GND = 0 V; unless otherwise specified.

Symbol	Parameter	Conditions		T_{amb} = -40 °C to +85 °C			Unit
				Min	Typ[1]	Max	
I_{CC_HOST}	supply current	operating mode: RST_HOST: static f_{clk} = 1 MHz; IO_HOST = IO_SIM = HIGH	[2]	-	1.5	3	μA
		operating mode: RST_HOST, CLK_HOST: static IO_HOST = IO_SIM = HIGH	[2]	-	0.01	1	μA
		shutdown mode: RST_HOST, CLK_HOST: static IO_HOST = HIGH V_{CC_SIM} = 0 V	[3]	-	-	1	μA
I_{CC_SIM}	card side supply current	operating mode; RST_HOST: static f_{clk} = 1 MHz IO_HOST = IO_SIM = HIGH C_{CLK_SIM} = 50 pF V_{CC_SIM} = 3.6 V	[2]	-	150	300	μA
		operating mode: RST_HOST, CLK_HOST: static IO_HOST = IO_SIM = HIGH	[2]	-	2	8	μA
		shutdown mode: RST_HOST = CLK_HOST = LOW IO_HOST = LOW; V_{CC_HOST} = 0 V	[3]	-	1.5	4.5	μA
$V_{en(UVLO)}$	undervoltage lockout enable voltage	V_{CC_SIM} rising; V_{CC_HOST} = 1.8 V		0.85	1.2	1.6	V
$V_{dis(UVLO)}$	undervoltage lockout disable voltage	V_{CC_SIM} falling; V_{CC_HOST} = 1.8 V		0.65	1.0	1.3	V
$V_{dis(UVLO\_AC)}$	undervoltage lockout disable voltage	V_{CC_SIM} falling;					
		-dV/dt = 0.9 V/ms to 9 V/ms; V_{CC_SIM} = 1.8 V		-	1.55	-	V
		-dV/dt = 1.5 V/ms to 15 V/ms; V_{CC_SIM} = 3.0 V		-	2.58	-	V
		-dV/dt = 0.9 V/ms to 9 V/ms; V_{CC_SIM} = 1.71 V to 1.89 V		-	0.86 × V_{CC_SIM}	-	V
		-dV/dt = 1.5 V/ms to 15 V/ms; V_{CC_SIM} = 2.85 V to 3.15 V		-	0.86 × V_{CC_SIM}	-	V

[1] Typical values measured at 25 °C.
[2] Internal pull-up resistance active on IO_HOST and IO_SIM
[3] Internal pull-up resistance active on IO_HOST

Table 8. Static characteristics

$1.08\ V \leq V_{CC\_HOST} \leq 1.98\ V$; $1.62\ V \leq V_{CC\_SIM} \leq 3.3\ V$; GND = 0 V; unless otherwise specified.

Symbol	Parameter	Conditions		T_{amb} = -40 °C to +85 °C			Unit
				Min	Typ[1]	Max	
Level shifter							
V_{IH}	HIGH-level input voltage	RST_HOST, CLK_HOST	[2]	0.7 × V_{CC_HOST}	-	V_{CC_HOST} + 0.3	V
		IO_HOST	[2]	0.7 × V_{CC_HOST}	-	V_{CC_HOST} + 0.3	V
		IO_SIM	[2]	0.7 × V_{CC_SIM}	-	V_{CC_SIM} + 0.3	V
V_{IL}	LOW-level input voltage	RST_HOST, CLK_HOST	[2]	-0.3	-	0.3 × V_{CC_HOST}	V
		IO_HOST	[2]	-0.3	-	0.3 × V_{CC_HOST}	V
		IO_SIM	[2]	-0.3	-	0.3 × V_{CC_SIM}	V
R_{pu}	pull-up resistance	IO_SIM connected to V_{CC_SIM}		12	20	26	kΩ
		IO_HOST connected to V_{CC_HOST}		12	19	26	kΩ
V_{OH}	HIGH-level output voltage	RST_SIM, CLK_SIM; I_{OH} = -1 mA		0.85 × V_{CC_SIM}	-	V_{CC_SIM} + 0.3	V
		IO_SIM; I_{OH} = -10 μA		0.8 × V_{CC_SIM}	-	V_{CC_SIM} + 0.3	V
		IO_HOST; I_{OH} = -8 μA		0.8 × V_{CC_HOST}	-	V_{CC_HOST} + 0.3	V
V_{OL}	LOW-level output voltage	RST_SIM, CLK_SIM; I_{OL} = 1 mA		-	50	200	mV
		IO_SIM; I_{OL} = 1 mA		-	50	200	mV
		IO_HOST; I_{OL} = 1 mA		-	50	200	mV
R_{pd}	pull-down resistance	CLK_SIM, RST_SIM, IO_SIM; shutdown mode					
		V_{CC_HOST} = 0 V; V_{CC_SIM} = 1.62 V to 3.3 V		-	400	-	Ω
		V_{CC_HOST} = 1.08 V to 1.98 V V_{CC_SIM} = 0 V		-	400	-	Ω
EMI filter							
R_S	series resistance	IO_SIM		-	44	-	Ω
		RST_SIM		-	44	-	Ω
		CLK_SIM		-	44	-	Ω
C_{io}	input/output capacitance	IO_SIM		-	8	-	pF
		RST_SIM		-	6	-	pF
		CLK_SIM		-	6	-	pF

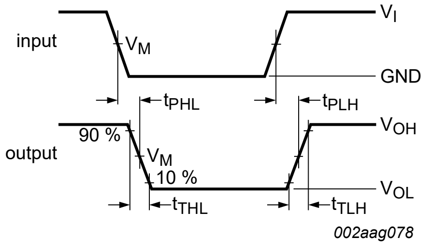
[1] Typical values measured at 25 °C.
[2] V_{IL}, V_{IH} depend on the individual supply voltage per interface.

Table 9. Dynamic characteristics
Push-pull: test circuit see Fig. 7; C_L = 50 pF.
For waveform see Fig. 6.

Symbol	Parameter	Conditions		T_{amb} = -40 °C to +85 °C;					Unit
			V_{CC_SIM} = 1.8 V ± 0.18 V			V_{CC_SIM} = 3.0 V ± 0.3 V			
			Min	Typ[1]	Max	Min	Typ[1]	Max	
V_{CC_HOST} = 1.2 V ± 0.12 V									
t_{pd}	propagation delay	I/O channel; push-pull	[2]	-	12	25	-	12	25	ns
		CLK and RST channels; push-pull	-	12	20	-	12	20	ns
t_t	transition time	IO_HOST; push-pull [3]	-	-	10	-	-	10	ns
		IO_SIM; RST_SIM; CLK_SIM; push-pull	-	-	10	-	-	10	ns
t_{sk}	skew time	between channels IO_SIM and CLK_SIM; push-pull	-	2	-	-	2	-	ns
f_{clock}	clock frequency	CLK channel; push-pull [4]	-	-	25	-	-	25	MHz
f_{data}	data rate	I/O channel; push-pull [4]	-	-	5	-	-	5	Mbps
		I/O channel; open-drain; C_{IO_HOST} = 10 pF; C_{IO_SIM} = 30 pF [4]	-	-	100	-	-	100	kbps
V_{CC_HOST} = 1.8 V ± 0.18 V									
t_{pd}	propagation delay	I/O channel; push-pull [2]	-	8	15	-	8	15	ns
		CLK and RST channels; push-pull	-	7	12	-	7	12	ns
t_t	transition time	IO_HOST; push-pull [3]	-	-	10	-	-	10	ns
		IO_SIM; RST_SIM; CLK_SIM; push-pull	-	-	10	-	-	10	ns
t_{sk}	skew time	between channels IO_SIM and CLK_SIM; push-pull	-	2	-	-	2	-	ns
f_{clock}	clock frequency	CLK channel; push-pull [4]	-	-	25	-	-	25	MHz
f_{data}	data rate	I/O channel; push-pull [4]	-	-	5	-	-	5	Mbps
		I/O channel; open-drain; C_{IO_HOST} = 10 pF; C_{IO_SIM} = 30 pF [4]	-	-	100	-	-	100	kbps

[1] Typical values measured at 25 °C.
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
[3] t_t is the same as t_{THL} and t_{TLH}.
[4] Criteria: duty cycle between 40% and 60%; Voltage swing between 10% V_{CCI} and 90% V_{CCI}.

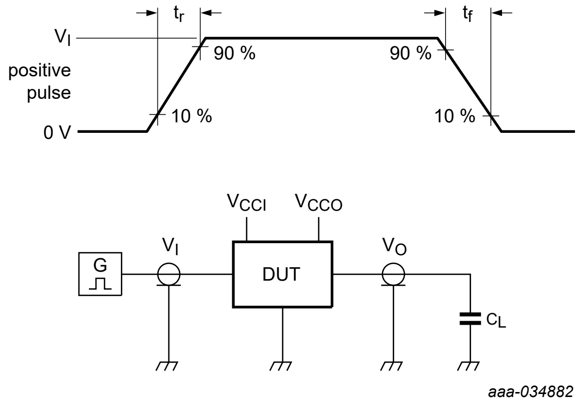
11.1. Waveforms and test circuits



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. Data input to data output propagation delay times



Test data is given in Table 10.

All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz; Z_O = 50 Ω; t_r, t_f ≤ 2.5 ns;

C_L = Load capacitance including jig and probe capacitance;

V_{CCI} is the supply voltage associated with the input;

V_{CCO} is the supply voltage associated with the output.

Fig. 7. Test circuit for measuring switching times for push-pull drive

Table 10. Test data for push-pull drive

Supply voltage		Direction	Input		Output	Load
V_{CC_HOST}	V_{CC_SIM}		V_I	V_M	V_M	C_L
1.08 V to 1.98 V	1.62 V to 3.3 V	host side to SIM card side	V_{CC_HOST}	0.5 × V_{CC_HOST}	0.5 × V_{CC_SIM}	50 pF
1.08 V to 1.98 V	1.62 V to 3.3 V	SIM card side to host side	V_{CC_SIM}	0.5 × V_{CC_SIM}	0.5 × V_{CC_HOST}	50 pF

12. Application information

The application circuit for the NXT4556AUR, which shows the typical interface with a SIM card, is shown in Fig. 8. Supply decoupling capacitors are recommended and should be placed close to the translator product.

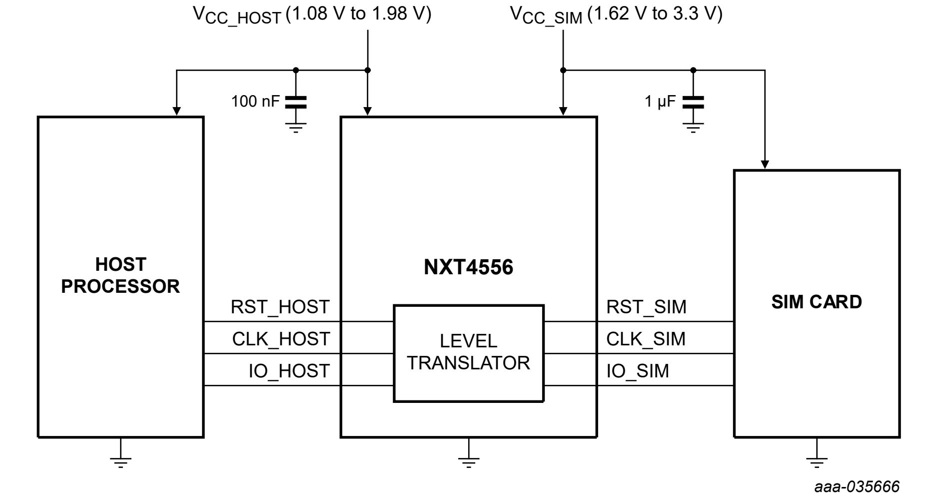


Fig. 8. NXT4556AUR application circuit interfacing with typical SIM card

13. Design and assembly recommendations

13.1. PCB design guidelines

For optimum performance, use a Non-Solder Mask PCB Design (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. For this case, refer to Table 11 for the recommended PCB design parameters.

Table 11. Recommended PCB design parameters

Parameter	Value or specification
PCB Cu pad shape	circular
PCB Cu pad diameter	170 µm
PCB solder resist diameter	220 µm
WLCSP pad diameter (UBM)	170 µm

13.2. PCB assembly guidelines for Pb-free soldering

Table 12. Assembly recommendations

Parameter	Value or specification
PCB stencil shape	circular
PCB stencil aperture diameter	180 µm
PCB stencil thickness	60 µm
Solder paste material	SAC alloy
Solder reflow profile	See Fig. 9; refer to Surface mount relfow soldering for additional information

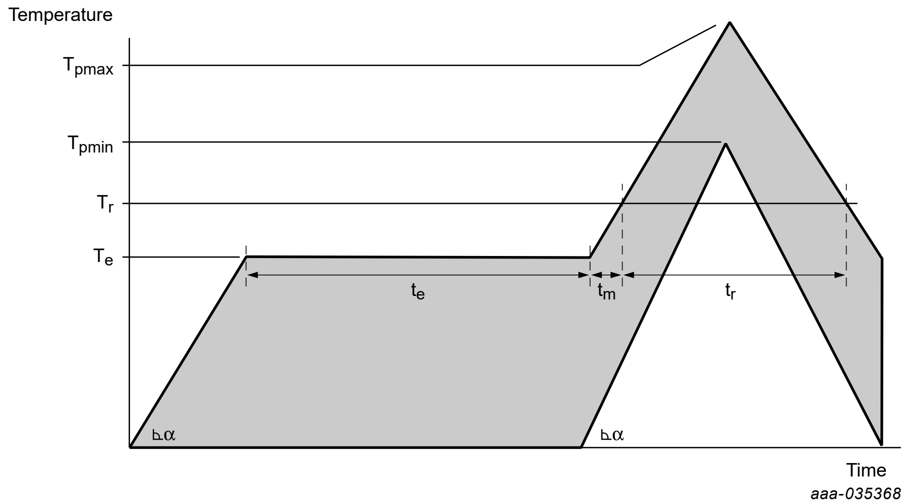


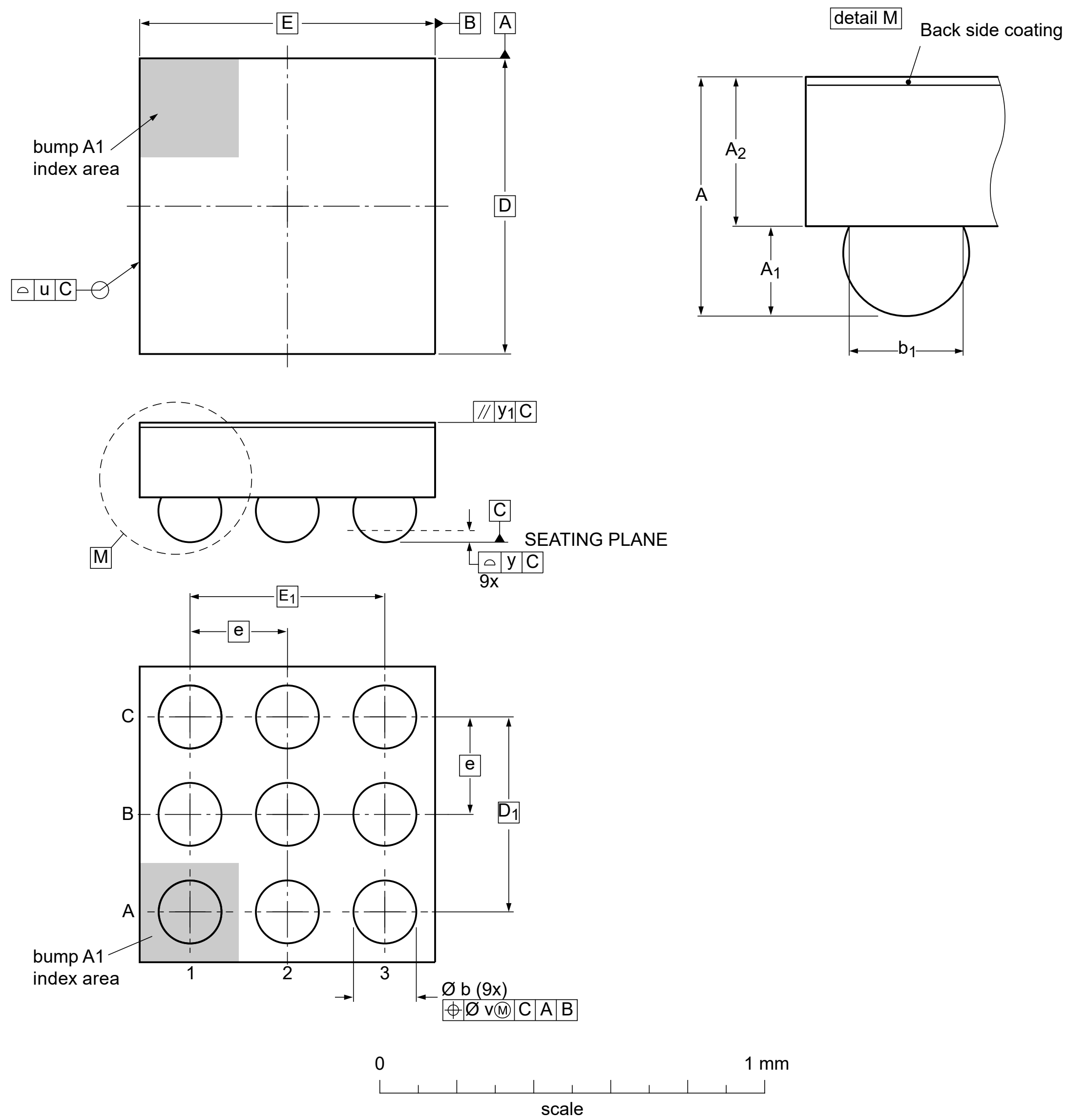
Fig. 9. Reflow profile requirements for SAC reflow soldering

Table 13. Explanation of the reflow temperature profile

Parameter	Value(s)	Remark
α	<10 °C/s	Please check solder paste and component (e.g. ceramic capacitors) and board limitations
T_e	160 °C to 180 °C	Below the liquidus temperature of the solder alloy
T_r	217 °C	Liquidus temperature (solder alloy dependent)
t_e	As short as possible, < 60 s preferred	Depends on the solder paste used - contact your solder paste supplier – solder balling and hot slump behavior might be affected. Hot slump might be avoided by predrying 45 min 45 °C.
t_r	< 70 s	Time above liquidus of the solder, with time the number of voids in the solder increases, weakening the solder joints
t_m	2-30 s	As short as possible, taking heating rate into account
$T_{p(min)}$	235 °C	Temperature measured in the solder at the coldest spot, depends on the solder alloy type
$T_{p(max)}$	260 °C	Depends on the board and the board finish (OSP is most critical) and the most temperature-sensitive component used on the board. $T_{p(max)}$ - $T_{p(min)}$ should be as small as possible.
Reflow atmosphere	-	General purpose reflow is under air atmosphere, nitrogen reflow is allowed

14. Package outline

WLCSP9: wafer level chip-scale package; 9 bumps; 0.92 × 0.92 × 0.42 mm body **SOT8057-1**



Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	A_2	b	b_1	D	D_1	E	E_1	e	u	v	y	y_1
mm	max	0.415		0.275	0.205	0.17 REF	0.92 BSC	0.60 BSC	0.92 BSC	0.60 BSC	0.30 BSC	0.03	0.015	0.05	0.06
	nom			0.250	0.185										
	min		0.11	0.225	0.165										

sot8057-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8057-1						~~23-02-01~~ 23-06-01

Fig. 10. Package outline SOT8057-1 (WLCSP9)

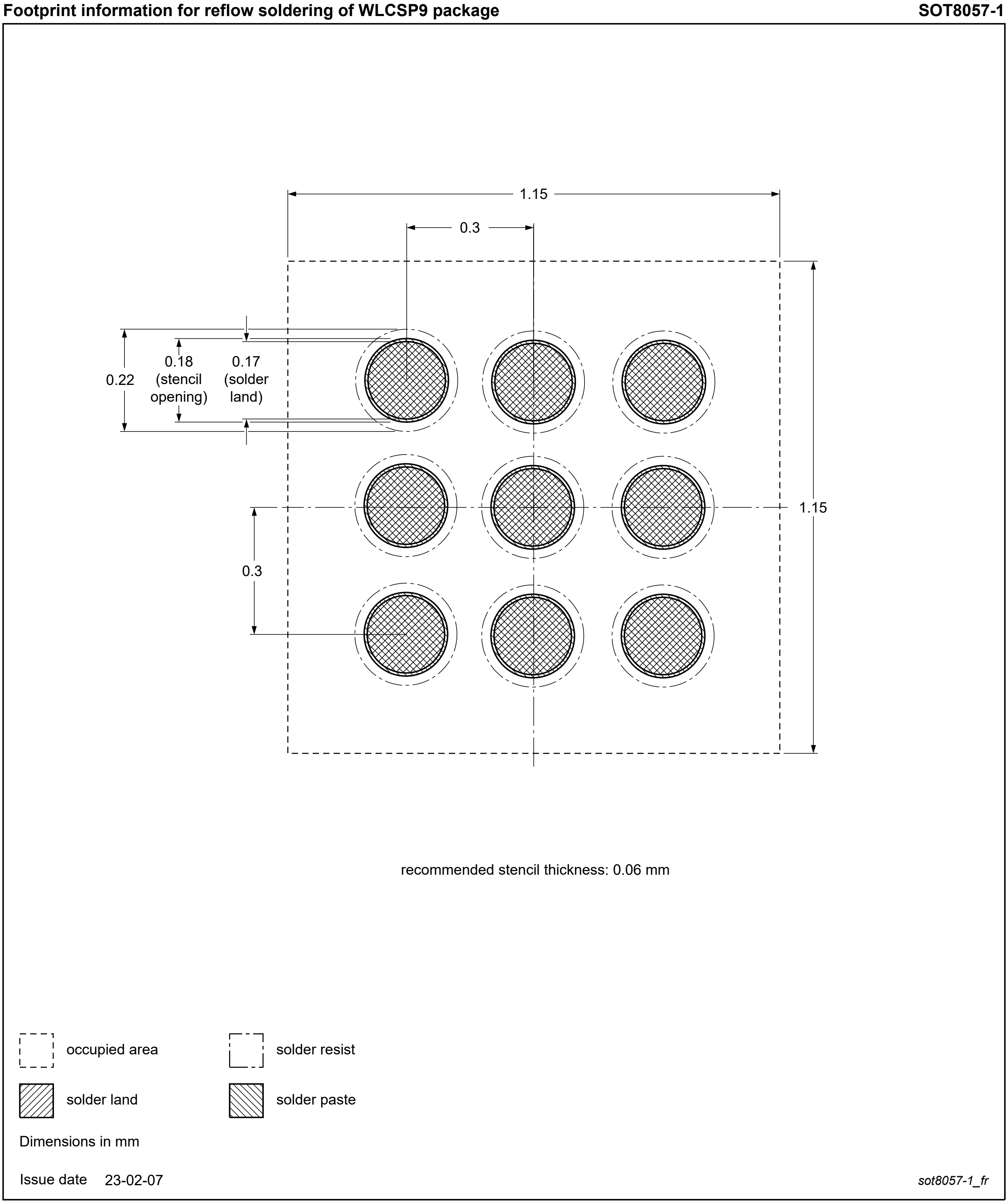


Fig. 11. Reflow soldering footprint SOT8057-1 (WLCSP9)

15. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged-Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
SIM	Subscriber Identification Module

16. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXT4556AUR v.1	20231205	Product data sheet	-	-

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 5 December 2023