



# XDP<sup>™</sup> XDP700-002 evaluation PCBA user guide

## About this document

#### Scope and purpose

This document describes how to set up the XDP<sup>™</sup> XDP700-002 Evaluation Board and configure the internal registers to evaluate the performance of the XDP700-002 hot-swap controller for negative rail.

#### **Intended audience**

This document is intended for test engineers who want to evaluate the performance of the XDP700-002 hot-swap controller.



**Important notice** 

## **Important notice**

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## Safety precautions

# Safety precautions

*Note:* Please note the following warnings regarding the hazards associated with development systems.

Table 1	Safety precautions
	Warning: The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death.
_	<b>Caution:</b> The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.
	<b>Caution:</b> The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing, or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.
	<b>Caution:</b> The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.



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Introduction

# 1 Introduction

Infineon's XDP<sup>™</sup> XDP7x0-002 family of devices (XDP700-002, XDP710-002) are highly integrated wide-input voltage system monitoring and inrush current protection devices. These are digitally configurable and use a power management bus (PMBus) communication interface to access their register map to configure their features.

The USB007A series dongle is a PC-USB COM port-to-PMBus bridge dongle that allows access to XDP700-002 registers from the software configurator.

This document describes how to set up the evaluation board and configure the internal registers to evaluate the performance of XDP700-002 in limiting the inrush current during startup by using regulation on the programmed FET safe operating area (SOA). This document also highlights the fault detection control.



#### Hardware and software requirements

# 2 Hardware and software requirements

The following hardware and software are required for the setup:

- XDP700-002 Evaluation Board
   Order code: EVAL\_XDP700
- XDP<sup>™</sup> Designer USB dongle USB007 or higher
   Order code: USB007A1
- XDP<sup>™</sup> Designer GUI
  - Download from Infineon Development Center

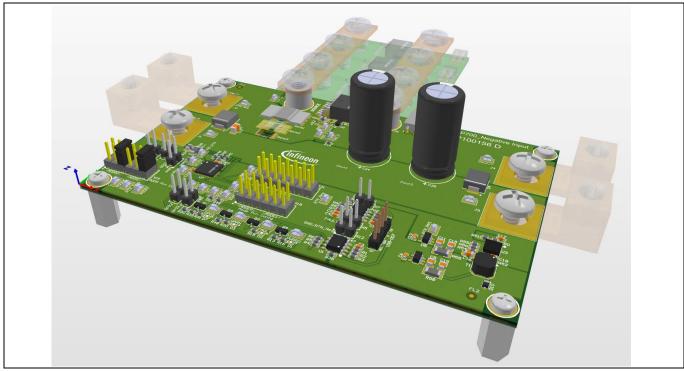


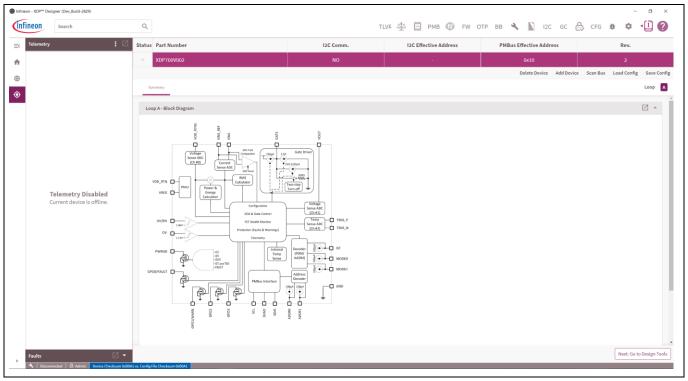
Figure 1 XDP700-002 Evaluation Board

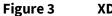


Figure 2 USB007A1 dongle



#### Hardware and software requirements





**XDP<sup>™</sup> Designer** 



## 3 XDP700-002 evaluation platform

The following sections describe the XDP700-002 Evaluation Board highlighting the electrical specifications, block diagram, schematics, layout, bill of materials (BOM), and different configuration settings that could be used on this evaluation board.

## **3.1 Electrical specifications**

- Input and output voltage range: -12 V DC to -80 V DC
- Input current range: Up to 40 A
- Note:

The input current range depends on the number of paralleled MOSFET adapter boards. The MOSFET adapter boards can be removed and added to the evaluation board based on the required current level. The board can handle up to 75 A of current with three MOSFET adapter boards without the need of forced air cooling.

## 3.2 Block diagram

The XDP700-002 evaluation platform consists of the following:

- **XDP700-002 Evaluation Board**: Negative input hot-swap controller and eFuse circuitry designed to run a single-channel controller including its corresponding FET. Additionally, communication, control, and protection circuitry are included.
- **USB007A1 dongle**: Acts as the interface between the PC and XDP700-002. XDP<sup>™</sup> Designer uses PMBus communication to send commands to XDP700-002. The USB007A1 dongle translates these commands from USB to PMBus, enabling XDP700-002.
- **XDP<sup>™</sup> Designer**: Configuration and general control software tool for XDP700-002 PMBus communication.

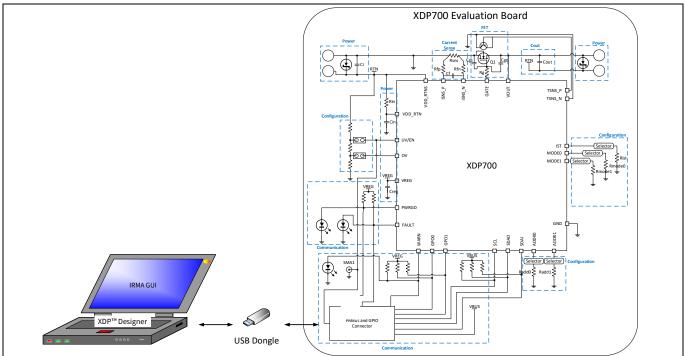


Figure 4 XDP700-002 evaluation platform





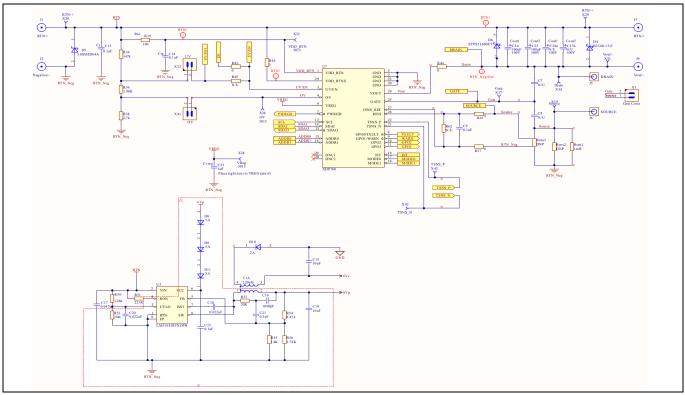


Figure 5

Main IC and bias

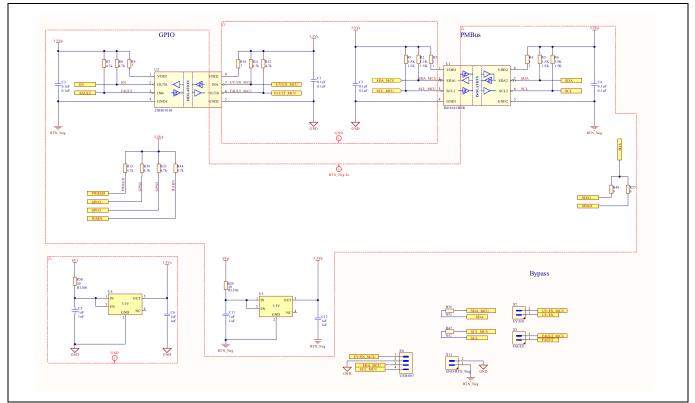
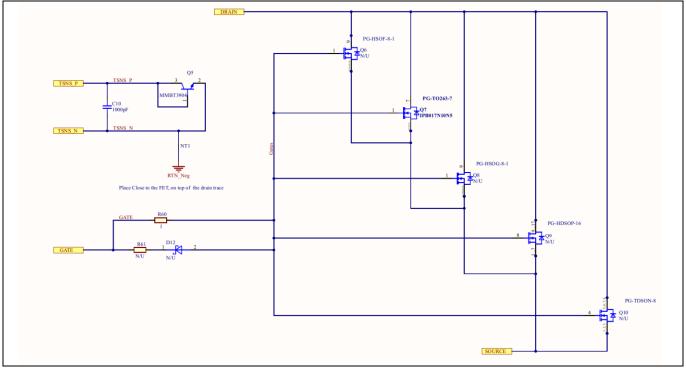
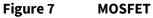
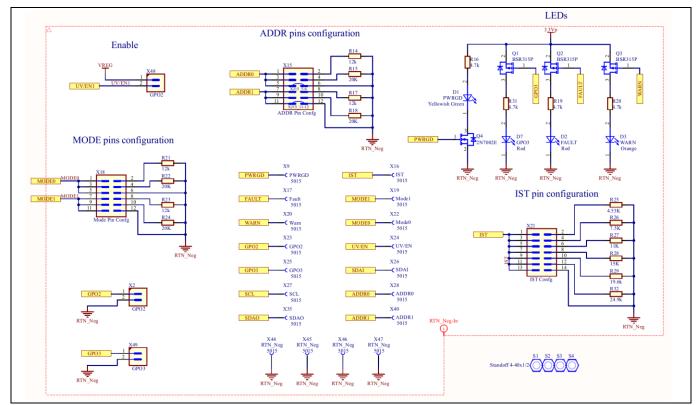


Figure 6 Communication and isolation



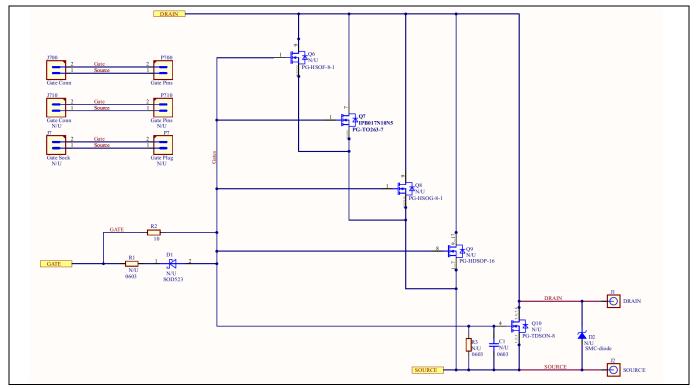














## 3.4 XDP700-002 Evaluation Board layout

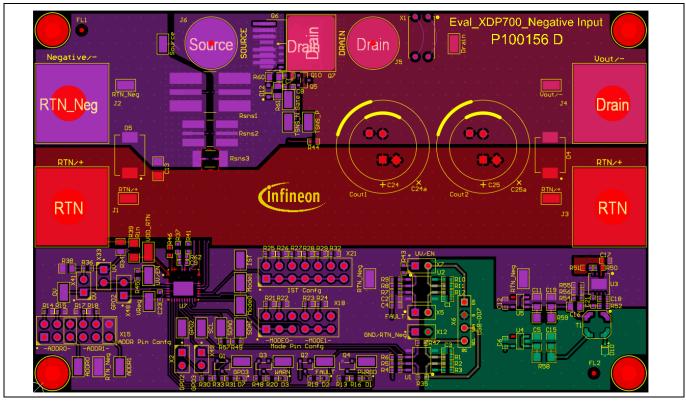


Figure 10 Top layer layout of main PCB



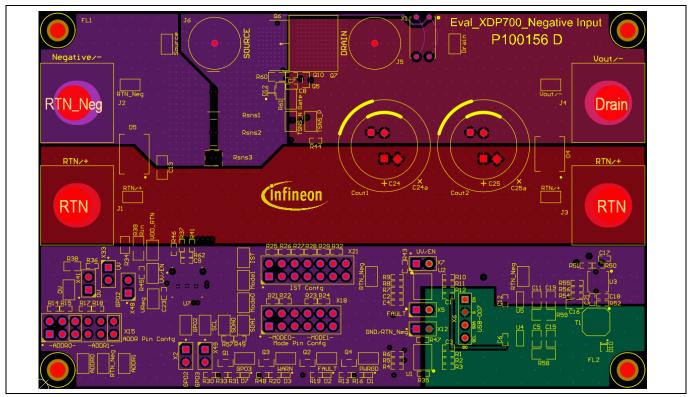


Figure 11 Mid 1 layer layout of main PCB

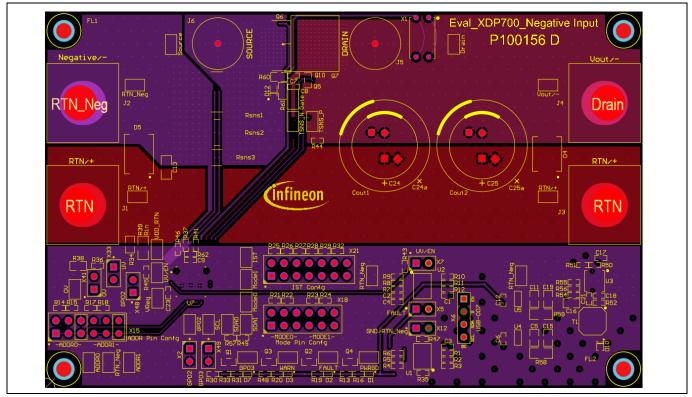


Figure 12 Mid 2 layer layout of main PCB



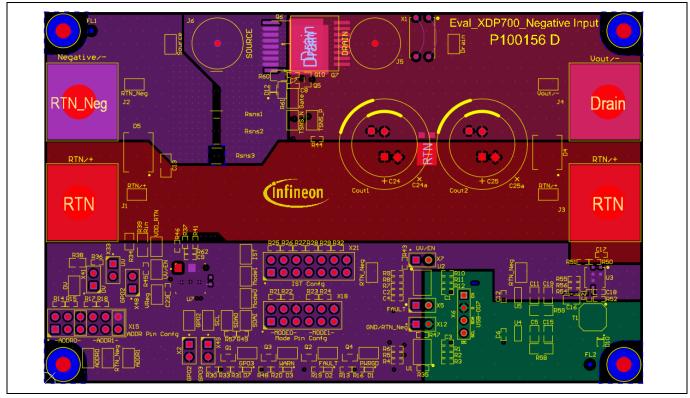


Figure 13 Bottom layer layout of main PCB



Figure 14 Top, Mid 1, Mid 2, and bottom layer layouts of MOSFET PCB



## 3.5 XDP700-002 Evaluation Board bill of materials

Table 2Bill of materials (BOM) for the main PCBA

ltem	Qty	Reference designator	Value	Footprint	Manufacturer	Part number	
1	1	BRD1	PC Board (FAB)	-	-	P100156 D	
2	7	C1, C2, C3, C4, C9, C21, C22	0.1 uF	C0603	AVX	06031C104K4 Z2A	
3	2	C5, C11	1 uF	C0805	TDK	C2012X7R1H 05K125AB	
4	3	C6, C12, C23	1 uF	C0603	ТДК	C1608X7R1E1 05K080AB	
5	1	C10	1000 pF	C0603	ТДК	C1608C0G2A: 02J080AA	
6	2	C13, C14	0.1 uF	C1206	ТДК	C3216C0G2A: 04J160AE	
7	2	C15, C19	10 uF	C0805	Samsung	CL21B106KO QNNNE	
8	1	C16	1000 pF	C0805	TDK	C2012C0G2A: 02J060AA	
9	1	C17	0.047 uF	C0603	TDK	C1608X7R1H4 73K080AA	
10	2	C18, C20	0.022 uF	C0603	TDK	C1608X7R1H2 23K080AA	
11	2	C24, C25	100 uF	Cap12p5x25m m	Panasonic	EEU-EE2C101	
12	1	D1	Yellowish Green	LED-SMD- SMLP13BC8T	ROHM Semiconductors	SML- P11MTT86R	
13	2	D2, D7	Red	LED-SMD- SMLP13BC8T	ROHM Semiconductors	SML- P11UTT86R	
14	1	D3	Orange	LED-SMD- SMLP13BC8T	ROHM Semiconductors	SML- P11DTT86R	
15	1	D4	B3100-13-F	DIOM7959X250 N	Diodes Incorporated	B3100-13-F	
16	1	D5	5.0SMDJ64A	DIOM7959X262 N	Bourns	5.0SMDJ64A	
17	1	D6	STPS5L60SFY	V10PL45-M3	STMicroelectron ics	STPS5L60SFY	
18	3	D8, D9,D11	.5A	SOD523	NXP	BAS516,135	
19	1	D10	.2A	SOD323	On	BAS20HT1G	
20	4	J1, J2, J3, J4	PEM NUT 8-32	Screw and nut for JACK1	Penn Eng	P-KF2-832-ET	
21	2	J5,J6	7466105R	CON-MOSFET	Würth Elektronik	7466105R	



ltem	Qty	<b>Reference designator</b>	Value	Footprint	Manufacturer	Part number	
22	3 Q1, Q2, Q3 E		BSR315P	SOT23	Infineon Technologies	BSR315P	
23	1	Q4	2N7002E	sot23	On	2N7002ET1G	
24	1	Q5	MMBT3904	Sot23	Nexperia	MMBT3904,2 15	
25	1	Q7	IPB017N10N5	PG-TO263-7	Infineon Technologies	IPB017N10N5 ATMA1	
26	4	R1, R2, R5, R6	1.5K	R0603	Panasonic	ERJ- 3EKF1501V	
27	4	R3, R4, R9, R10	1	R0603	Panasonic	ERJ- 3GEYJ1ROV	
28	12	R7, R8, R11, R12, R13, R16, R19, R20, R30, R31, R33, R48	4.7k	R0603	Yageo	RC0603FR- 074K7L	
29	4	R14, R17, R21, R23	12k	R0603	Vishay	CRCW060312 KOFKEAC	
30	6	R15, R18, R22, R24, R52, R53	20К	R0603	Panasonic	ERJ- 3EKF2002V	
31	1	R25	4.53K	R0603	Panasonic	ERJ- 3EKF4531V	
32	1	R26	7.5K	R0603	Panasonic	ERJ- 3EKF7501V	
33	1	R27	11K	R0603	Panasonic	ERJ- 3EKF1102V	
34	1	R28	15K	R0603	Panasonic	ERJ- 3EKF1502V	
35	1	R29	19.6k	R0603	Vishay	CRCW060319 K6FKEA	
36	1	R32	24.9k	R0603	Vishay	CRCW060324 K9FKEA	
37	1	R34	147k	R0805	Vishay	CRCW080514 7KFKEA	
38	1	R36	1.96K	R0603	Panasonic	ERJ- 3EKF1961V	
39	7	R37, R41, R43, R44, R46, R49, R57	0	R0603	Panasonic	ERJ- 3GEY0R00V	
40	1	R38	2.7k	R0805	Vishay	CRCW08052K 70FKEA	
41	1	R39	100	R1206	Panasonic	ERJ- 8ENF1000V	
42	1	R50	124k	R0603	Vishay	CRCW060312 4KFKEA	
43	1	R51	221K	R0603	Panasonic	ERJ- 3EKF2213V	



ltem	Qty	<b>Reference designator</b>	Value	Footprint	Manufacturer	Part number		
44	1	R54	8.87k	R0603	Vishay	CRCW06038K 87FKEA		
45	1	R55	14k	R0603	Panasonic	ERJ- 3EFK1402V		
46	1	R56	2.74K	R0603	Panasonic	ERJ- 3EKF2741V		
47	2	R58, R59	20	R1206	Panasonic	ERJ- 8GEYJ200V		
48	1	R60	1	R0805	Panasonic	ERJ- 6RQF1R0V		
49	1	Rsns1	1mR	5930	Bourns	CSS2H- 5930K-1L00F		
50	1	Rsns2	1mR	3920	Bourns	Not Used		
51	1	Rsns3	0.5uR	2512	Bourns	Not Used		
52	1 T1		220uH	LPD5030V	Coilcraft	LPD5030V- 224MRC		
53	1	U1	ISO1641B	SO8	ТІ	ISO1641BDR		
54	1	U2	2DIB1410F	SO8	Infineon	2DIB1410FXU MA1		
55	1	U3	LM5018SD/NO PB	WSON-8	Texas Instruments	LM5018SD/N OPB		
56	2	U4, U5	3.3 V	SOT23-5	STMicroelectron ics	LDK320AM33 R		
57	1	U7	XDP700-002	IFX-PG-VQFN- 29-1	Infineon Technologies	XDP700-002		
58	1	X1	CON4-H	CON2_HZ_BCS- 102-X-S-HE	Samtec	BCS-102-F-S- HE		
59	8	X2, X5, X7, X12, X33, X41, X48, X49	CON2	CON-M-THT- M20-9770246_2	Harwin	M20-9770246		
60	1	Х6	CON4	CONN4PIN100	Würth Elektronik	61300411121		
61	29 X9, X16, X17, X19, X20, X22, X23, X24, X25, X26, X27, X28, X29, X30, X31, X32, X34, X35, X36, X37, X38, X39, X40, X42, X43, X44, X45, X46, X47		TP SMD	CON-SMD-TP- 5015	Keystone Electronics	5015		
62	2	X15, X18	CON12	CON-M-THT- TSW-106-07-L-D	Samtec	TSW-106-07- L-D		
63	1	X21	CON14	CON-M-THT- HTSW-107-07-L- D	Samtec	HTSW-107- 07-L-D		



ltem	Qty Reference designator		Value	Footprint	Manufacturer	Part number	
64	4	S1a, S2a, S3a, S4a	Screw PHMS 4-40 x 1/4	-	Keystone	9900	
65	4	S1, S2, S3, S4	Standoff 4- 40x1/2	mtg_hole_125	Keystone	2203	
66	2	C7, C8	N/U	C0603	ТДК	Not used	
67	2	C24a, C25a	N/U	CAP18X46mm	Nichicon	Not used	
68	1	D12	N/U	DO-219AC	Vishay	Not used	
69	1	Q6	N/U	PG-HSOF-8-1	Infineon Technologies	Not used	
70	1	Q8	N/U	PG-HSOG-8-1	Infineon Technologies	Not used	
71	1	Q9	N/U	PG-HDSOP-16	Infineon Technologies	Not used	
72	1	Q10	N/U	PG-TDSON-8_1	Infineon Technologies	Not used	
73	4	R35, R45, R47, R62	N/U	R0603	Yageo	Not used	
74	1	R61	N/U	R0805	Panasonic	Not used	

#### Table 3 BOM for MOSFET PCBA

Item	Qty	Reference designator	eference designator Value Footprint			
1	1	BRD1	PC Board (FAB)	-	Manufacturer	Part number P100173 A
2	2	J1, J2	SO-SMD-M5- FEMALE	CON-MOSFET	Würth Elektronik	7466105R
3	1	J700	CON4-H	CON2_HZ_BCS- 102-X-S-HE	Samtec	BCS-102-F-S- HE
4	1	P700	CON2	CON2_RA_TSW- 102-08-F-S-RA	Samtec	TSW-102-08- F-S-RA
5	1	Q7	IPB017N10N5	PG-TO263-7	Infineon Technologies	IPB017N10N 5ATMA1
6	1	R2	10	R0603	Panasonic	ERJ- 3EKF10R0V
7	1	C1	N/U	C0603	ТDК	Not used
8	1	D1	N/U	SOD523	On	Not used
9	1	D2	N/U	SMC-diode	Littelfuse	Not used
10	1	J7	N/U	CON2_SMD_AVX- 20-9159	KYOCERA AVX	Not used
11	1	J710	N/U	CON2_HZ_BCS- 102-X-S-HE	Samtec	Not used
12	1	Р7	N/U	CON2_SMD_AVX- 10-9159	KYOCERA AVX	Not used



Item	Qty	Reference designator	Value	Footprint	Manufacturer	Part number
13	1	P710	N/U	CON2_RA_TSW- 102-08-F-S-RA	Samtec	Not used
14	1	Q6	N/U	PG-HSOF-8-1	Infineon Technologies	Not used
15	1	Q8	N/U	PG-HSOG-8-1	Infineon Technologies	Not used
16	1	Q9	N/U	PG-HDSOP-16	Infineon Technologies	Not used
17	1	Q10	N/U PG-TDSON-8_2		Infineon Technologies	Not used
18	1	R1	N/U	R0603	Panasonic	Not used
19	1	R3	N/U	R0603	Panasonic	Not used

# 3.6 XDP700-002 Evaluation Board default settings

See the jumpers on the board as shown in Table 4.

l able 4	Jumper settings							
Reference designator	Default configuration Usage							
X48	Open	Shorted 1 to 2: Connects UV/EN to VREG						
		<b>Open</b> : UV/EN can be driven by dongle						
X15	Between Pin 5 and 6 and in between Pins 11 and 12	ADDRx pins configuration to 0x10. Move the jumper to change the PMBus address.						
X18 Open MODEx pins configuration. Leave them open for fully dig (FDM)								
X21	Open	IST pin configuration						
X33	Open	Shorted: Connects UV/EN to voltage divider						
		<b>Open</b> : UV/EN can be driven by Vreg or dongle						
X6	Open	Shorted: Bypass isolation between UV/EN and UV/EN_MCU						
X5	Open	Shorted: Bypass isolation between FAULT and FAULT_MCU						
X12	Open	<b>Shorted</b> : Connects RTN_Neg and GND together and bypass isolation						
X2	Open	<b>Shorted</b> : Connects GPO2 to GND (used to test CGDN application)						
X49	Open	<b>Shorted</b> : Connects GPO3 to GND (used to test PMBUS Disable application)						
X41	Open	<b>Shorted</b> : Connects OV to voltage divider <b>Open</b> : This header can be left open for DCM						

## Table 4 Jumper settings



Table 5	<b>Resistors and capacitors</b>	
Reference designator	Default configuration	Notes
R44	Check depending on FET	-
C7, C8	DNF	$C_{gd}$ and $C_{gs}$ of FET
R37, R41	Check depending on sense resistor	Can be populated: 10 $\Omega$
C9	Max 100 nF	R <sub>sns</sub> filter
R62	DNF	Used to modify the gain of R <sub>sns</sub> for accurate telemetry
C10	1 nF	Temperature sensor filter
R43	0 Ω	Populate: If EN is driven by dongle
		<b>DNF</b> : If EN is driven by header X48
R45	DNF	Populate: If EN is driven by header X48
		<b>DNF</b> : If EN is driven by dongle
Rin	100 Ω	Or lower depending on test slew rate requirements

## 3.7 Current sensing resistor (R<sub>sns</sub>)

The following three footprints are provided to support different resistor sizes, with the default onboard resistor of  $1 \text{ m}\Omega$ . These footprints are optimized for resistor packages:

- R<sub>sns1</sub>: 5930, 5931
- R<sub>sns2</sub>: 3920, 3921, 2818
- R<sub>sns3</sub>: 2512

## 3.8 FET board

The XDP700-002 Evaluation Board comes with an option to parallel up to three FET boards to increase the current-carrying capability for testing heavy loads. This allows the board to drive multiple parallel N-channel MOSEFTs. Necessary heatsinking is provided via a copper bus bar; forced cooling is required if operating at currents greater than 50 A.

## 3.9 Different FET footprint options on the FET board

The FET footprint supports D<sup>2</sup>PAK, TOLL, and TDSON packages in the following positions:

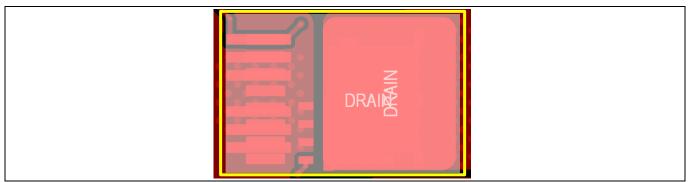


Figure 15 D2PAK7 position (top side)



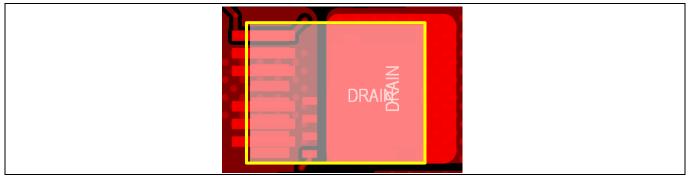
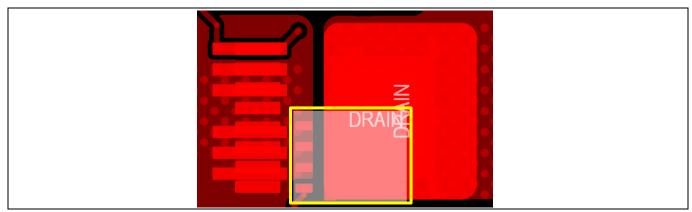
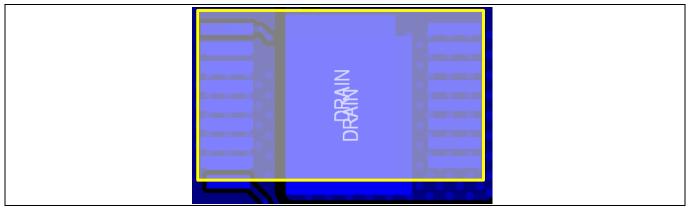
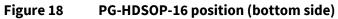


Figure 16 TOLL position (top side)

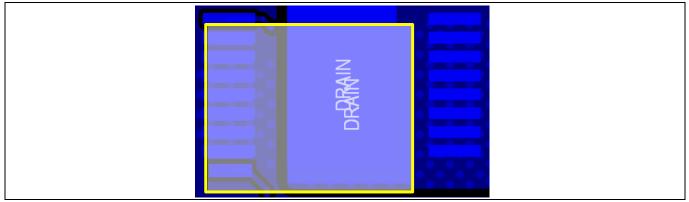


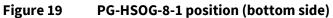
#### Figure 17 PG-TDSON-8-1 position (top side)



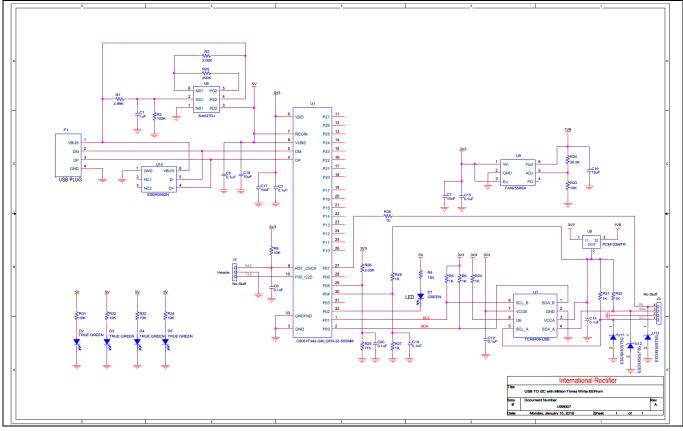








# 3.10 USB007A dongle schematics







## 4 Programming, setup, and turn-on instructions

Set up the system as follows:

- 1. Connect the USB007 dongle to the XDP700-002 Evaluation Board connector X6 as shown in Figure 21.
- 2. Connect the USB007 dongle to the PC USB port.
- 3. Ensure that the jumpers are connected properly.
- 4. Connect 48 V from RTN/+ (J1 connector) to Negative/- (J2) on the left of the board.

XDP700-002 powers up as soon as RTN/+ is equal to or greater than 9 V. At this point, communication and programming is possible, but the FET will be OFF. To turn ON the FET, a minimum of 14 V is required. After turn on, at least the following registers must be programmed to turn ON the device.

- FET select
- R<sub>sns</sub>

The UV/EN signal (signal used to enable or disable the hot-swap controller) can be controlled in one of the following ways:

- Controlled by a dongle; it will hold the signal down until it is toggled manually inside the GUI as shown in Figure 40.
- Controlled by the UV/EN1 signal, which is controlled by the X48 header. It must be held LOW until the necessary registers are written.

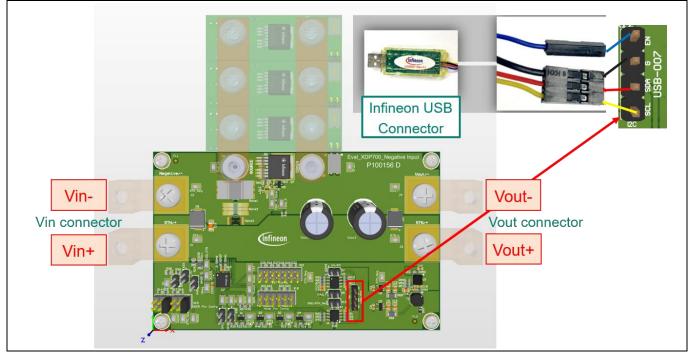


Figure 21

XDP700-002 Evaluation Board and dongle setup

#### **XDP<sup>™</sup> Designer communication setup** 4.1

Install XDP<sup>™</sup> Designer from the Infineon Development Center.

#### Dongle connection in XDP<sup>™</sup> Designer 4.1.1

- 1. Open XDP<sup>™</sup> Designer.
- 2. Wait for a few moments and check the bottom status bar for the dongle connection. When the dongle is detected, the highlighted area shown in Figure 22 turns green and displays USB007.
- 3. Ensure that the enable signal is LOW (EN L); if not, click on it to toggle to EN L from EN H.

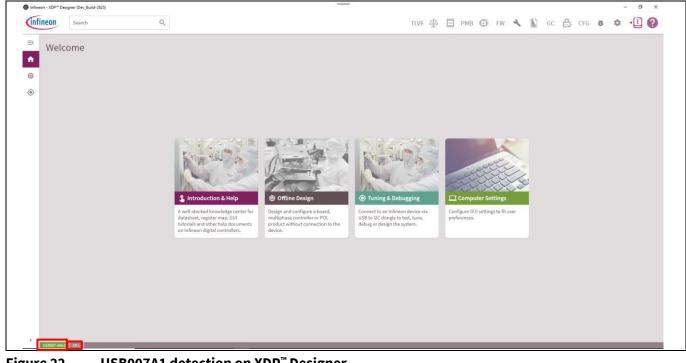


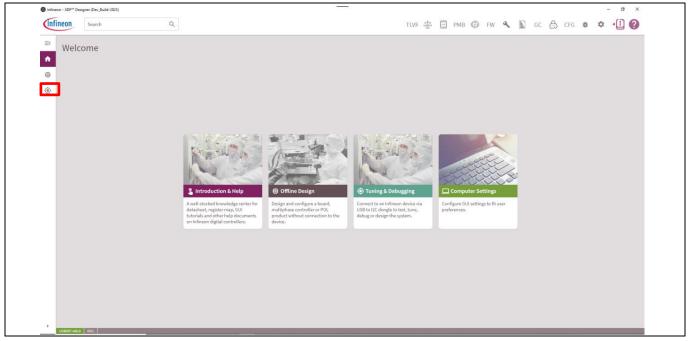
Figure 22 USB007A1 detection on XDP<sup>™</sup> Designer

ineon



## 4.1.2 Detecting XDP700-002

1. Click the button highlighted in Figure 23 and then wait for a few seconds to detect the device. If the device is not detected on its own, click on **Scan For Devices**, as shown in Figure 24.



#### Figure 23 XDP700-002 detection

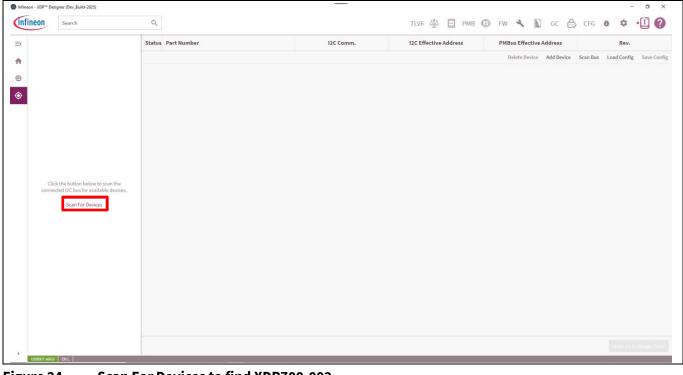
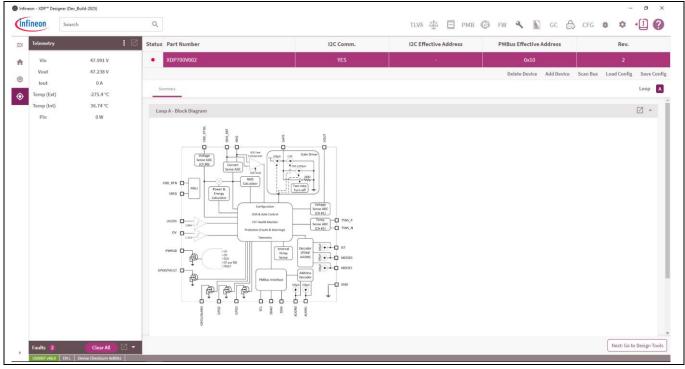
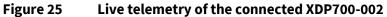


Figure 24Scan For Devices to find XDP700-002

XDP700V002 is detected, with **Telemetry** displayed on the left as shown in Figure 25.







2. Click the **PMB** button to view PMBus registers and their stored values. See Figure 26.

nfineon Sear	:					ТЦУБ ФДА 🔁 РИМВ 🕼 FW 🔦 🖺 GC 合 СЕБ 🗰 🌣 📲
Active Controller	:	Search	All Fault Mi	FR Status	Telem Vout	Live Read (On)
() XDP700V00	02: 0×10	Code	Command		oop A Value	
🔴 Loop A	: Vout = 47.26V   Iout = 0A	0x01	OPERATION	0x80	value	
Televenter	: 2	1		UXBU		
Telemetry	47.991 V	0x03	CLEAR_FAULTS	24		
Vin Vout	47.991 V 47.26 V	0x19	CAPABILITY	0xD0		
lout	0 A	0x42	VOUT_OV_WARN_LIMIT	0x0FFF	88.0077 V	
Temp (Ext)	-275.4 °C	0x43	VOUT_UV_WARN_LIMIT	0x0000	0 V	
Temp (Int)	36.74 °C	0x44	VOUT_UV_FAULT_LIMIT	0x0000	0 V	
Pin	0 W	0x4A	IOUT_OC_WARN_LIMIT	0x0FFF	53.5683 A	
		0x4F	OT_FAULT_LIMIT	0x0FFF	512.0962 °C	
		0x51	OT_WARN_LIMIT	0x0FFF	512.0962 °C	
		0x55	VIN_OV_FAULT_LIMIT	0x0FFF	88.0077 V	
		0x57	VIN_OV_WARN_LIMIT	0x0FFF	88.0077 V	
		0x58	VIN_UV_WARN_LIMIT	0x0000	0 V	
		0x59	VIN_UV_FAULT_LIMIT	0x0000	οv	
		0x6B	PIN_OP_WARN_LIMIT	0xFFFF	4716.0035 W	
		0x78	STATUS_BYTE	0x40	-	
		0x79	STATUS_WORD	0x0840		
		0x7A	STATUS_VOUT	0x00		
	Clear All	0x7B	STATUS_IOUT	0x00		

Figure 26 XDP<sup>™</sup> Designer displaying PMBus registers of connected XDP700-002



## 4.1.3 Reading and writing registers

- 1. To edit a register individually, click on the corresponding PMBus register.
- 2. Make the necessary changes, and then click **Write**. See Figure 27.

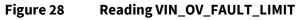
infi	neon Searc	h	Q				TLVF 🕸 🗔 PMB 🕼 FW 🔦 🖺 GC 🚓 CFG 🗰 🌣 📲 🔇
=<	Active Controller	:	Search	All Fault MF	R Status T	elem Vout	VIN_OV_FAULT_LIMIT Live Read (On) 🛑 🗙
ft	() XDP700V002	2: 0x10	Code	Command	Hex	Value	Selected Loop
٢	Loop A :	Vout = 47.28V   Iout = 0A	0x01	OPERATION	0x80		Loop A
0	Telemetry	: 2	0x03	CLEAR_FAULTS			Command Value (Decimal)
	Vin	48.012 V	0x19	CAPABILITY	0xD0		69.9978508489
	Vout	47.281 V 0 A	0x42	VOUT_OV_WARN_LIMIT	0x0F73	84.9989 V	
	Temp (Ext)	-275.4 °C	0x43	VOUT_UV_WARN_LIMIT	0x0000	0 V	
	Temp (Int)	37.17 °C	0x44	VOUT_UV_FAULT_LIMIT	0x06E8	37.997 V	
	Pin	0 W	0x4A	IOUT_OC_WARN_LIMIT	0x0FFF	35.3566 A	
			0x4F	OT_FAULT_LIMIT	0x0FFF	512.0962 °C	
			0x51	OT_WARN_LIMIT	0x0FFF	512.0962 °C	
			0x55	VIN_OV_FAULT_LIMIT	0x0CB9	69.9979 V	Read
			0x57	VIN_OV_WARN_LIMIT	0x0FFF	88.0077 V	
			0x58	VIN_UV_WARN_LIMIT	0x0000	0 V	Description The VIN_OV_FAULT_LIMIT command sets the value of the input voltage measured at the VDD_RTNS pin that causes an input overvoltage fault.
			0x59	VIN_UV_FAULT_LIMIT	0x0000	0 V	OV fault can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM RNG settings.
			0x6B	PIN_OP_WARN_LIMIT	0xFFFF	3112.7102 W	
			0x78	STATUS_BYTE	0x40		
			0x79	STATUS_WORD	0x0840		
			0x7A	STATUS_VOUT	0x00		
	Faults (2)	Clear All 🛛 🗸 🔹	0×7B	STATUS_IOUT	0x00		
•		Clear All	0.70	ATITUA 010117			

Figure 27 Editing VIN\_OV\_FAULT\_LIMIT

Most of the registers are updated automatically.

#### 3. To read the latest register values, click **Read**. See Figure 28.

	neon Searc		٩				TLVF 🤹 🖬 🎮 🕼 🕫 FW 🔧 📓 GC 🐣 CFG 🛎 🌣 🗗 🚺
×	Active Controller	:	Search	All Fault MFF	R Status	Telem Vout	VIN_OV_FAULT_LIMIT Live Read (On)
r	xDP700V002		Code	Command	Hex	Value	Selected Loop
	🛑 Loop A : 1	Vout = 47.28V   Iout = 0A	0x01	OPERATION	0x80		Loop A
>.	Telemetry	: 2	0x03	CLEAR_FAULTS			Command Value (Decimal)
	Vin	48.012 V	0x19	CAPABILITY	0xD0	-	69.9978508489 — + v
	Vout	47.281 V 0 A	0x42	VOUT_OV_WARN_LIMIT	0x0F73	84.9989 V	
	lout Temp (Ext)	mp (Ext) -275.4 °C	0x43	VOUT_UV_WARN_LIMIT	0x0000	o v	
	Temp (Int) 37.17 °C	0x44	VOUT_UV_FAULT_LIMIT	0x06E8	37.997 V		
	Pin	Pîn OW	0x4A	IOUT_OC_WARN_LIMIT	0x0FFF	35.3566 A	
			0x4F	OT_FAULT_LIMIT	0x0FFF	512.0962 °C	
			0x51	OT_WARN_LIMIT	0x0FFF	512.0962 °C	
			0x55	VIN_OV_FAULT_LIMIT	0x0CB9	69.9979 V	Read Write
			0x57	VIN_OV_WARN_LIMIT	0x0FFF	88.0077 V	
			0x58	VIN_UV_WARN_LIMIT	0x0000	0 V	Description The VIN_OV_FAULT_LIMIT command sets the value of the input voltage measured at the VDD_RTNS pin that causes an input overvoltage fault.
			0x59	VIN_UV_FAULT_LIMIT	0x0000	0 V	OV fault can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM RNG settings.
			0x6B	PIN_OP_WARN_LIMIT	0xFFFF	3112.7102 W	
			0x78	STATUS_BYTE	0x40		
			0x79	STATUS_WORD	0x0840		
			0x7A	STATUS_VOUT	0x00		
4	Faults <b>2</b>	Clear All 🛛 🔽 🔻	0x7B	STATUS_IOUT	0x00		



User manual



## 4.1.4 Programming the FET

Note:

This section is applicable only if fully digital mode (FDM) is used. If using analog-assisted digital mode (AADM), the FET will be pre-programmed. These modes are discussed in detail in Section 4.2. You can skip this step in that case.

If FDM is used, the FET must be programmed in the FET\_SELECT bits of the MODE register (0xD1) according to the one populated on the board. The board has the **IPB017N10N5** FET populated.

- 1. Select the IPB017N10N5 FET.
- 2. Modify the FET\_SELECT bit to 0xB, and then click **Write**. See Figure 29.

fineon - XDP <sup>**</sup> Designer (De		Q					TLVR		РМВ 🕼	FW	٩	G	c 🐣	CFG	<b>ë</b> 1	¢ •(	ī) (
Active Controller		Search	All Fault MF	R Status 1	felem Vout	MODE								L	ive Read (	Dn) 📧	
	02: 0x10	Code	Command	Hex	Value	Selected Loop											
Loop A	: Vout = 47.26V   Iout = 0A	0x97	READ_PIN	0x0000	0 W	Loop A											
Telemetry	: 2	0×98	PMBUS_REVISION	0x33		Command Value											
Vin	48.012 V	0x99	MFR_ID	0x004649	4	FET_SELECT 0xB	$-\pm$										
Vout	47.26 V	0x9A	MFR_MODEL	0x0000000		MODE 0x1	-+										
lout Temp (Ext)	0 A -275.4 ℃	0x9B	MFR_REVISION	0x0001	-												
Temp (Lnt)	36.74 °C	0xD0	PMBUS_CFG	0x10													
Pin	Pin 0 W		MODE	0x4B													
		0xD3	REG_CFG	0x0803													
		0xD4	V_SNS_CFG	0x0028													
		0xD5	I_SNS_CFG	0xB418	-										Read		Write
		0xD6	I_SNS_OFFSET_COMP	0x0000	2										near		-
		0xD7	TSNS_LVL_CTRL	0x07BF	-	Description FET_SELECT [5:0] bits se	ect FET's SOA curve to	be used from a	list of pre-p	rogramme	d ones, MC	DE [6] bit :	elects the	UV. OV ani	d OUV fault	sources i	n Fully
		0xD8	WATCHDOG_TMR	0x67	3	Digital mode. Either ana compared digitally with	og comparators at the	UV/EN, OV and	FB pins are	used to trig	ger the UV,	OV and OI	IV faults; o	r ADC com	versions re		
		0xD9	V_TMR	0x0FFF	-	MODE 0x0	Description Analog Comparators	Mode (ACM)									
		0xDA	PIN_POLARITY	0x01	-	0x1	Digital Comparators										
		0xDB	GPO_CFG	0x0000		FET_SELECT 0x00 (00 0000 bin)	Description BSC027N10NS5ATM	IA1 - DC Line		FET_SEL			scription C027N10N		- 10ms line		
		0xDC	IOUT_UC_WARN_LIMIT	0x0000		0x01 (00 0001 bin) 0x02 (00 0010 bin)	BSC035N10NS5ATM BSC040N10NS5ATM	IA1 - DC Line		0x21 (10 0x22 (10	0001 bin)	BS	C035N10N	IS5ATMA1	- 10ms line - 10ms line	ń.	
1	- 2007 - 2008 - 1 March 1 - 2	0xDD	ONCHIP_TSD_FAULT_LIMIT	0x03	3	0x03 (00 0011 bin) 0x04 (00 0100 bin)	IPTG011N08NM5 - E	OC Line		0x23 (10 0x24 (10	0011 bin)	IP'	G011N08	NM5 - 10m	sline		
Faults 2	Clear All 🛛 🔽 🔻					0.01 (00 0100 bill)	IDDOLTNIONCI CATA			0.01 (10					10 P		

Figure 29 FET selection in FDM



# 4.1.5 Programming R<sub>sns</sub>

The sense resistor value must be programmed in the  $R_{sns}$  bits of the REG\_CFG register according to the one populated on the board. The board has  $R_{sns}$  of **1 m** $\Omega$  populated.

- 1. Select the 1 m  $\Omega$  resistor.
- 2. Modify the R<sub>sns</sub> bit to 0xD, and then click **Write**. See Figure 30.

	ineon Searc	v_Build-2825)	Q						tlvr 🎝 🖻	РМВ 🕼	FW 🔧 📗	GC 🖨	CFG 👪	* ·[] (
×	Active Controller	:	Search	All Fault MF	R Status 1	elem Vout	REG_CFG							(On) 🛑 🗎 🔪
ł	() XDP700V00	02: 0x10	Code	Command	Hex	Value	Selected Loop							
•	Loop A :	: Vout = 47.28V   Iout = 0A	0x97	READ_PIN	0x0000	0 W	Loop A							
>	Telemetry	: 2	0x98	PMBUS_REVISION	0x33		Command Value							
_	Vin	47.969 V	0x99	MFR_ID	0x004649		RSNS		-+					
	Vout	47.281 V	0x9A	MFR_MODEL	0×0000000		RMS_EN							
	lout Temp (Ext)	0 A -275.4 °C	0x9B	MFR_REVISION	0x0001		BOOSTMODE_EN							
	Temp (Int)	37.17 °C	0xD0	PMBUS_CFG	0×10		BOOSTMODE_TMR BOOSTMODE_DC		-+					
	Pin	0 W	0xD1	MODE	0x4B		0000111001_00	over (						
			0xD3	REG_CFG	0x080D									
			0xD4	V_SNS_CFG	0x0028									
			0xD4 0xD5	V_SNS_CFG	0x0028 0xB458	•								
						•							Read	Write
			0xD5 0xD6	I_SNS_CFG I_SNS_OFFSET_COMP	0xB458 0x0000	•	RSNS	Description	RSNS	Description	RSNS	Description	RSNS	Description
			0xD5	I_SNS_CFG	0x8458	• • •	0x00 (00 0000 bin)	0.2 mΩ	0x10 (01 0000 bin)	1.25 mΩ	RSNS 0x20 (10 0000 bin)	2.8 mΩ	RSNS 0x30 (11 0000 bin)	Description 4.5 mΩ
			0xD5 0xD6 0xD7	L_SNS_CFG L_SNS_OFFSET_COMP TSNS_LVL_CTRL	0xB458 0x0000 0x07BF	•					RSNS		RSNS	Description
			0xD5 0xD6	I_SNS_CFG I_SNS_OFFSET_COMP	0xB458 0x0000	• • •	0x00 (00 0000 bin) 0x01 (00 0001 bin)	0.2 mΩ 0.25 mΩ	0x10 (01 0000 bin) 0x11 (01 0001 bin)	1.25 mΩ 1.3 mΩ	RSNS 0x20 (10 0000 bin) 0x21 (10 0001 bin)	2.8 mΩ 3 mΩ	RSNS 0x30 (11 0000 bin) 0x31 (11 0001 bin)	Description           4.5 mΩ           4.6 mΩ
			0xD5 0xD6 0xD7	L_SNS_CFG L_SNS_OFFSET_COMP TSNS_LVL_CTRL	0xB458 0x0000 0x07BF	· · ·	0x00 (00 0000 bin) 0x01 (00 0001 bin) 0x02 (00 0010 bin) 0x03 (00 0011 bin) 0x04 (00 0100 bin)	0.2 mΩ 0.25 mΩ 0.3 mΩ 0.33 mΩ 0.4 mΩ	0x10 (01 0000 bin) 0x11 (01 0001 bin) 0x12 (01 0010 bin) 0x13 (01 0011 bin) 0x14 (01 0100 bin)	1.25 mΩ 1.3 mΩ 1.4 mΩ 1.5 mΩ 1.6 mΩ	RSNS           0x20 (10 0000 bin)           0x21 (10 0001 bin)           0x22 (10 0010 bin)           0x23 (10 0011 bin)           0x24 (10 0100 bin)	2.8 mΩ 3 mΩ 3.1 mΩ 3.2 mΩ 3.3 mΩ	RSNS           0x30 (11 0000 bin)           0x31 (11 0001 bin)           0x32 (11 0010 bin)           0x33 (11 0011 bin)           0x34 (11 0100 bin)	Description           4.5 mΩ           4.6 mΩ           4.7 mΩ           4.8 mΩ           4.9 mΩ
			0xD5 0xD6 0xD7 0xD8	I_SNS_CFG I_SNS_OFFSET_COMP TSNS_LVL_CTRL WATCHDOG_TMR	0xB458 0x0000 0x07BF 0x67	• • • •	0x00 (00 0000 bin) 0x01 (00 0001 bin) 0x02 (00 0010 bin) 0x03 (00 0011 bin) 0x04 (00 0100 bin) 0x05 (00 0101 bin)	0.2 mΩ 0.25 mΩ 0.3 mΩ 0.33 mΩ 0.4 mΩ 0.47 mΩ	0x10 (01 0000 bin) 0x11 (01 0001 bin) 0x12 (01 0010 bin) 0x13 (01 0011 bin) 0x14 (01 0100 bin) 0x15 (01 0101 bin)	1.25 mΩ 1.3 mΩ 1.4 mΩ 1.5 mΩ 1.6 mΩ 1.7 mΩ	RSNS           0x20 (10 0000 bin)           0x21 (10 0001 bin)           0x22 (10 0010 bin)           0x23 (10 0011 bin)           0x24 (10 0100 bin)           0x25 (10 0101 bin)	2.8 mΩ 3 mΩ 3.1 mΩ 3.2 mΩ 3.3 mΩ 3.4 mΩ	RSNS           0x30 (11 0000 bin)           0x31 (11 0001 bin)           0x32 (11 0010 bin)           0x33 (11 0011 bin)           0x33 (11 0011 bin)           0x35 (11 0101 bin)	Description           4.5 mΩ           4.6 mΩ           4.7 mΩ           4.8 mΩ           4.9 mΩ           5 mΩ
			0xD5 0xD6 0xD7 0xD8	I_SNS_CFG I_SNS_OFFSET_COMP TSNS_LVL_CTRL WATCHDOG_TMR	0xB458 0x0000 0x07BF 0x67	• • • • •	0x00 (00 0000 bin) 0x01 (00 0001 bin) 0x02 (00 0010 bin) 0x03 (00 0011 bin) 0x04 (00 0100 bin) 0x05 (00 0101 bin) 0x06 (00 0110 bin)	0.2 mΩ 0.25 mΩ 0.3 mΩ 0.33 mΩ 0.4 mΩ 0.47 mΩ 0.5 mΩ	0x10 (01 0000 bin) 0x11 (01 0001 bin) 0x12 (01 0010 bin) 0x13 (01 0011 bin) 0x14 (01 0100 bin) 0x15 (01 0101 bin) 0x16 (01 0110 bin)	1.25 mΩ 1.3 mΩ 1.4 mΩ 1.5 mΩ 1.6 mΩ 1.7 mΩ 1.8 mΩ	RSNS           0x20 (10 0000 bin)           0x21 (10 0001 bin)           0x22 (10 0010 bin)           0x23 (10 0011 bin)           0x24 (10 0100 bin)           0x25 (10 0101 bin)           0x26 (10 0110 bin)	2.8 mΩ 3 mΩ 3.1 mΩ 3.2 mΩ 3.3 mΩ 3.4 mΩ 3.5 mΩ	RSNS           0x30 (11 0000 bin)           0x31 (11 0001 bin)           0x32 (11 0010 bin)           0x33 (11 0011 bin)           0x34 (11 0100 bin)           0x35 (11 0111 bin)           0x36 (11 0111 bin)	Description           4.5 mΩ           4.6 mΩ           4.7 mΩ           4.8 mΩ           4.9 mΩ           5 mΩ
			0xD5 0xD6 0xD7 0xD8 0xD9 0xDA	L_SNS_CFG L_SNS_OFFSET_COMP TSNS_LVR_CTRL WATCHDOG_TMR V_TMR PIN_POLARITY	0x8458 0x0000 0x078F 0x67 0x0FFF 0x01	• • • • •	0x00 (00 0000 bin) 0x01 (00 0001 bin) 0x02 (00 0010 bin) 0x03 (00 0011 bin) 0x04 (00 0100 bin) 0x05 (00 0110 bin) 0x06 (00 0110 bin) 0x07 (00 0111 bin)	0.2 mΩ 0.25 mΩ 0.3 mΩ 0.33 mΩ 0.4 mΩ 0.47 mΩ 0.5 mΩ 0.6 mΩ	0x10 (01 0000 bin) 0x11 (01 0001 bin) 0x12 (01 0010 bin) 0x13 (01 0011 bin) 0x14 (01 0100 bin) 0x15 (01 0101 bin) 0x16 (01 0110 bin) 0x17 (01 0111 bin)	1.25 mΩ           1.3 mΩ           1.4 mΩ           1.5 mΩ           1.6 mΩ           1.7 mΩ           1.8 mΩ           1.9 mΩ	RSNS           0x20 (10 0000 bin)           0x21 (10 0001 bin)           0x22 (10 0010 bin)           0x23 (10 0011 bin)           0x24 (10 0100 bin)           0x25 (10 0101 bin)           0x26 (10 0110 bin)           0x27 (10 0111 bin)	2.8 mΩ 3 mΩ 3.1 mΩ 3.2 mΩ 3.3 mΩ 3.4 mΩ 3.5 mΩ 3.6 mΩ	RSNS           0x30 (11 0000 bin)           0x31 (11 0011 bin)           0x32 (11 0010 bin)           0x33 (11 0011 bin)           0x34 (11 0100 bin)           0x35 (11 0110 bin)           0x36 (11 0110 bin)           0x37 (11 0111 bin)	Description           4.5 mΩ           4.6 mΩ           4.7 mΩ           4.8 mΩ           4.9 mΩ           5 mΩ           5.5 mΩ           6 mΩ
			0xD5 0xD6 0xD7 0xD8 0xD9	L_SNS_CFG L_SNS_OFFSET_COMP TSNS_LVL_CTRL WATCHDOG_TMR V_TMR	0x8458 0x0000 0x07BF 0x67 0x0FFF	• • • • • •	0x00 (00 0000 bin) 0x01 (00 0001 bin) 0x02 (00 0010 bin) 0x03 (00 0011 bin) 0x05 (00 0111 bin) 0x05 (00 0101 bin) 0x06 (00 0110 bin) 0x07 (00 0111 bin) 0x08 (00 1000 bin)	0.2 mΩ 0.25 mΩ 0.3 mΩ 0.33 mΩ 0.4 mΩ 0.47 mΩ 0.5 mΩ 0.6 mΩ 0.67 mΩ	0x10 (01 0000 bin) 0x11 (01 0001 bin) 0x12 (01 0010 bin) 0x13 (01 0011 bin) 0x14 (01 0100 bin) 0x15 (01 0101 bin) 0x16 (01 010 bin) 0x17 (01 0111 bin) 0x18 (01 1000 bin)	1.25 mΩ           1.3 mΩ           1.4 mΩ           1.5 mΩ           1.6 mΩ           1.7 mΩ           1.8 mΩ           1.9 mΩ           2 mΩ	RSNS           0x20 (10 0000 bin)           0x21 (10 0001 bin)           0x22 (10 0010 bin)           0x23 (10 0011 bin)           0x24 (10 0100 bin)           0x25 (10 011 bin)           0x26 (10 0110 bin)           0x26 (10 111 bin)           0x27 (10 111 bin)           0x28 (10 1000 bin)	2.8 mΩ 3 mΩ 3.1 mΩ 3.2 mΩ 3.3 mΩ 3.4 mΩ 3.5 mΩ 3.6 mΩ 3.7 mΩ	RSNS           0x30 (11 0000 bin)           0x31 (11 0011 bin)           0x33 (11 0011 bin)           0x34 (11 0100 bin)           0x35 (11 0110 bin)           0x36 (11 0110 bin)           0x36 (11 0110 bin)           0x37 (11 0111 bin)           0x38 (11 1011 bin)	Description           4.5 mΩ           4.6 mΩ           4.7 mΩ           4.8 mΩ           4.9 mΩ           5 mΩ           6 mΩ           6.5 mΩ
			0xD5 0xD6 0xD7 0xD8 0xD9 0xD4 0xDA	L_SNS_CFG L_SNS_OFFSET_COMP TSNS_LVL_CTRL WATCHDOG_TMR V_TMR PIN_POLARITY GP0_CFG	0x8458 0x0000 0x078F 0x67 0x0FFF 0x01 0x01	• • • • • •	0x00 (00 0000 bin)           0x01 (00 0001 bin)           0x02 (00 0010 bin)           0x03 (00 0011 bin)           0x04 (00 0100 bin)           0x05 (00 0101 bin)           0x06 (00 0110 bin)           0x06 (00 0110 bin)           0x06 (00 0111 bin)           0x06 (00 0111 bin)           0x08 (00 0100 bin)           0x08 (00 0100 bin)           0x09 (00 1000 bin)	0.2 mΩ 0.25 mΩ 0.3 mΩ 0.33 mΩ 0.4 mΩ 0.47 mΩ 0.5 mΩ 0.6 mΩ 0.67 mΩ 0.7 mΩ	0x10 (01 0000 bin) 0x11 (01 0001 bin) 0x12 (01 0010 bin) 0x13 (01 0011 bin) 0x14 (01 0100 bin) 0x15 (01 0101 bin) 0x17 (01 0111 bin) 0x17 (01 0111 bin) 0x19 (01 1000 bin)	1.25 mΩ           1.3 mΩ           1.4 mΩ           1.5 mΩ           1.6 mΩ           1.7 mΩ           1.8 mΩ           1.9 mΩ           2 mΩ           2.1 mΩ	RSNS           0x20 (10 0000 bin)           0x21 (10 0001 bin)           0x22 (10 0010 bin)           0x23 (10 0010 bin)           0x24 (10 1010 bin)           0x25 (10 0110 bin)           0x26 (10 0110 bin)           0x27 (10 0111 bin)           0x27 (10 0111 bin)           0x28 (10 0100 bin)           0x29 (10 1001 bin)	2.8 mΩ 3 mΩ 3.1 mΩ 3.2 mΩ 3.3 mΩ 3.4 mΩ 3.5 mΩ 3.6 mΩ 3.7 mΩ 3.8 mΩ	RSNS           0x30 (11 0000 bin)           0x32 (11 0001 bin)           0x32 (11 0010 bin)           0x33 (11 0010 bin)           0x34 (11 0100 bin)           0x36 (11 0110 bin)           0x36 (11 0110 bin)           0x37 (11 0111 bin)           0x38 (11 1000 bin)           0x36 (11 0100 bin)           0x36 (11 0100 bin)           0x38 (11 1000 bin)	Description           4.5 mΩ           4.6 mΩ           4.7 mΩ           4.8 mΩ           5 mΩ           5.5 mΩ           6 mΩ           6.5 mΩ           7 mΩ
			0xD5 0xD6 0xD7 0xD8 0xD9 0xDA	L_SNS_CFG L_SNS_OFFSET_COMP TSNS_LVR_CTRL WATCHDOG_TMR V_TMR PIN_POLARITY	0x8458 0x0000 0x078F 0x67 0x0FFF 0x01	· · · · · ·	0x00 (00 0000 bin) 0x01 (00 0001 bin) 0x02 (00 0010 bin) 0x03 (00 0011 bin) 0x04 (00 0110 bin) 0x05 (00 0101 bin) 0x07 (00 0111 bin) 0x07 (00 0111 bin) 0x08 (00 1000 bin) 0x08 (00 1000 bin)	0.2 mΩ 0.25 mΩ 0.3 mΩ 0.33 mΩ 0.4 mΩ 0.47 mΩ 0.5 mΩ 0.6 mΩ 0.67 mΩ	0x10 (01 0000 bin) 0x11 (01 0001 bin) 0x12 (01 0010 bin) 0x13 (01 0011 bin) 0x14 (01 0100 bin) 0x15 (01 0101 bin) 0x15 (01 010 bin) 0x17 (01 0111 bin) 0x19 (01 1000 bin) 0x14 (01 1000 bin)	1.25 mΩ           1.3 mΩ           1.4 mΩ           1.5 mΩ           1.6 mΩ           1.7 mΩ           1.8 mΩ           1.9 mΩ           2 mΩ	RSNS           0x20 (10 0000 bin)           0x21 (10 0001 bin)           0x22 (10 0011 bin)           0x23 (10 0011 bin)           0x25 (10 0101 bin)           0x26 (10 010 bin)           0x27 (10 0111 bin)           0x28 (10 1001 bin)           0x28 (10 100 bin)           0x28 (10 100 bin)           0x28 (10 1001 bin)           0x28 (10 1001 bin)           0x24 (10 1001 bin)	2.8 mΩ 3 mΩ 3.1 mΩ 3.2 mΩ 3.3 mΩ 3.4 mΩ 3.5 mΩ 3.6 mΩ 3.7 mΩ	RSNS           0x30 (11 0000 bin)           0x31 (11 0001 bin)           0x32 (11 0011 bin)           0x33 (11 0011 bin)           0x34 (11 0100 bin)           0x35 (11 0101 bin)           0x36 (11 0100 bin)           0x37 (11 011 bin)           0x38 (11 1000 bin)           0x37 (11 011 bin)           0x39 (11 1000 bin)           0x39 (11 1000 bin)           0x34 (11 1000 bin)	Description           4.5 mΩ           4.6 mΩ           4.7 mΩ           4.8 mΩ           4.9 mΩ           5 mΩ           5.5 mΩ           6.5 mΩ           7 mΩ           7 mΩ           7.5 mΩ
			0xD5 0xD6 0xD7 0xD8 0xD9 0xD4 0xDA	L_SNS_CFG L_SNS_OFFSET_COMP TSNS_LVL_CTRL WATCHDOG_TMR V_TMR PIN_POLARITY GP0_CFG	0x8458 0x0000 0x078F 0x67 0x0FFF 0x01 0x01	• • • • • • • • •	0x00 (00 0000 bin)           0x01 (00 0001 bin)           0x02 (00 0010 bin)           0x03 (00 0011 bin)           0x04 (00 0100 bin)           0x05 (00 0101 bin)           0x06 (00 0110 bin)           0x06 (00 0110 bin)           0x06 (00 0111 bin)           0x06 (00 0111 bin)           0x08 (00 0100 bin)           0x08 (00 0100 bin)           0x09 (00 1000 bin)	0.2 mΩ           0.25 mΩ           0.3 mΩ           0.4 mΩ           0.47 mΩ           0.5 mΩ           0.6 mΩ           0.67 mΩ           0.77 mΩ	0x10 (01 0000 bin) 0x11 (01 0001 bin) 0x12 (01 0010 bin) 0x13 (01 0011 bin) 0x14 (01 0100 bin) 0x15 (01 0101 bin) 0x17 (01 0111 bin) 0x17 (01 0111 bin) 0x19 (01 1000 bin)	1.25 mΩ           1.3 mΩ           1.4 mΩ           1.5 mΩ           1.6 mΩ           1.7 mΩ           1.8 mΩ           1.9 mΩ           2.1 mΩ           2.2 mΩ	RSNS           0x20 (10 0000 bin)           0x21 (10 0001 bin)           0x22 (10 0010 bin)           0x23 (10 0010 bin)           0x24 (10 1010 bin)           0x25 (10 0110 bin)           0x26 (10 0110 bin)           0x27 (10 0111 bin)           0x27 (10 0111 bin)           0x28 (10 0100 bin)           0x29 (10 1001 bin)	2.8 mΩ 3 mΩ 3.1 mΩ 3.2 mΩ 3.4 mΩ 3.4 mΩ 3.5 mΩ 3.6 mΩ 3.7 mΩ 3.8 mΩ 3.9 mΩ	RSNS           0x30 (11 0000 bin)           0x32 (11 0001 bin)           0x32 (11 0010 bin)           0x33 (11 0010 bin)           0x34 (11 0100 bin)           0x36 (11 0110 bin)           0x36 (11 0110 bin)           0x37 (11 0111 bin)           0x38 (11 1000 bin)           0x36 (11 0100 bin)           0x36 (11 0100 bin)           0x38 (11 1000 bin)	Description           4.5 mΩ           4.6 mΩ           4.7 mΩ           4.8 mΩ           5 mΩ           5.5 mΩ           6 mΩ           6.5 mΩ           7 mΩ

Figure 30 R<sub>sns</sub> selection



## 4.1.6 Selecting the watchdog timer

Set the watchdog timer higher than the turn-on time to ensure that the watchdog timer does not expire before the turn-on. At the same time, ensure that the watchdog timer is not set much longer than the turn-on time to prevent damage to the FET in the event of a short-circuit during turn-on. The watchdog timer is modified to 200 ms, as shown in Figure 31.

ineon	Search	Q				۵ <u>ا</u>	🛆 РМВ 🕼 FW 🔧	🖺 ec 🚓 🏟 📲
Active Contro	ller :	Search	All Fault MFR S	tatus Telem Vout	WATCHDOG_TMR			Live Read (On)
XDP70	00V002: 0x10	Code	Command	Loop A	Selected Loop			
O Lo	op A : Vout = 0.04V   Iout = 0A	0xD7	TSNS_LVL_CTRL	0x07BF	Loop A			
Telemetry	: 🛛	0xD8	WATCHDOG_TMR	0x66	Command Value			
Vin	48.098 V	0xD9	V_TMR	0x0FB6	0x66			
Vout	0.043 V	0xDA	PIN_POLARITY	0×01	WATCHDOG 0x6	-+		
lout Temp (Ext)	0 A 31.33 °C	0xDB	GPO_CFG	0x0000	EN_DG 0x6			
Temp (Int)	35 °C	0xDC	IOUT_UC_WARN_LIMIT	0x0000				
Pin	0 W	0xDD	ONCHIP_TSD_FAULT_LIMIT	0x03				
		0xDE	ENABLE_FAULTS	0x7EFF				
		0xDF	MASK_FAULTS	0x7EFF				
		0xE0	STATUS_FAULTS	0×0000				Read
		0xE1	ENABLE_WARNS	0x0FDC	2:0 WATCHDOG the FET		now rong to be can accempe to po	wer up the output without runy enhance
		0xE2	MASK_WARNS	0x0FDC	WATCHDOG	Description	EN_DG	Description
		0xE3	STATUS_WARNS	0x0000	0x0 (0000 bin) 0x1 (0001 bin)	5ms 10ms	0x0 (0000 bin) 0x1 (0001 bin)	0ms 4ms
		0xE4	PWRGD_DG_TMR	0xF5	0x2 (0010 bin) 0x3 (0011 bin)	20ms 50ms	0x2 (0010 bin) 0x3 (0011 bin)	8ms 16ms
		0xE5	SOA_TMR	0x0002	0x4 (0100 bin) 0x5 (0101 bin)	75ms 100ms	0x4 (0100 bin) 0x5 (0101 bin)	32ms 64ms
		0xE6	TURN_OFF_CTRL	0×0002	0x6 (0110 bin) 0x7 (0111 bin)	200ms 500ms	0x6 (0110 bin) 0x7 (0111 bin)	128ms 256ms
		0xE7	RETRY	0x3E3F	0x8 (1000 bin) 0x9 (1001 bin)	750ms 1000ms	0x8 (1000 bin) 0x9 (1001 bin)	300ms 400ms
Faults	Clear All	0xE8	TELEMETRY_EN	0x7FFF	0xA (1010 bin) 0xB (1011 bin) 0xC (1100 bin)	2000ms 3000ms 5000ms	0xA (1010 bin) 0xB (1011 bin) 0xC (1100 bin)	512ms Reserved Reserved

Figure 31 Watchdog timer selection

# 4.1.7 Programming the current sense range (CS\_RNG) and start-up current limit (IST)

*Note:* If using AADM, skip this step because the resistor on the IST pin selects the start-up current limit and current sense range.

In FDM, program the desired current sense range and start-up current limit in the I\_SNS\_CFG register (0xD5), as shown in Figure 32.

Note: Do not set the current sense range as 100 mV with  $1 \text{ m}\Omega$  sense resistor. The SOA regulation loop does not work when (current sense range (mV)/ R (mohm)) > 83.33 A.



fineon sea	v_Build-2825) rch	Q						TLVF 4	РМВ	Ø.	w 🔍	GC	₿ (	FG i	Ŭ 1	¢ •(	I (
Active Controller	:	Search	All Fault MF	R Status Te	elem Vout	I_SNS_CFG								Live	Read (	0n) 📢	
<b>()</b> XDP700V0	02: 0x10	Code	Command	Hex	Value '	Selected Loop											
🔴 Loop A	: Vout = 47.3V   Iout = 0A	0x97	READ_PIN	0x0000	0 W	Loop A											
Telemetry	: 2	0x98	PMBUS_REVISION	0x33		Command Value											
Vin	48.012 V	0x99	MFR_ID	0x004649		START_ILIM	0x5	-+									
Vout	47.303 V 0 A	0x9A	MFR_MODEL	0x0000000	8	SOC_FAULT_LIMIT	0x3	-+									
Temp (Ext)	-275.4 °C	0x9B	MFR_REVISION	0x0001		CS_RNG_TRIM	0xB4	-+									
Temp (Int) Pin	36.74 °C 0 W	0xD0	PMBUS_CFG	0x10													
***		0xD1	MODE	0x4B	0												
		0xD3	REG_CFG	0x080D	8												
		0xD4	V_SNS_CFG	0x0028	-												
		0xD5	I_SNS_CFG	0xB45D	- 1									Re	ead		Write
		0xD6	I_SNS_OFFSET_COMP	0x0000		0x0 (000 bin) 0x1 (001 bin)				7	00% of OC 5% of OC						_
		0xD7	TSNS_LVL_CTRL	0x07BF	-	0x2 (010 bin) 0x3 (011 bin)				2	0% of OC 5% of OC						_
		0xD8	WATCHDOG_TMR	0x67		0x4 (100 bin) 0x5 (101 bin)				1	5% of OC 2.5% of OC						
		0xD9	V_TMR	0x0FFF		0x6 (110 bin) 0x7 (111 bin)					% of OC % of OC						_
		0xDA 0xDB	PIN_POLARITY GPO_CFG	0x01	-	SOC_FAULT_LIMIT			CS_RNG 12.5mV	2'b0x		25n	_RNG 2'bi	1x			_
		0xDC	IOUT_UC_WARN_LIMIT	0x0000		0x1 (001 bin) 0x2 (010 bin)			18.75mV 25mV	0		50 n					_
			ONCHIP_TSD_FAULT_LIMIT	0x03		0x3 (011 bin) 0x4 (100 bin)			37.5mV 50mV			75n 100	)mV				_
Faults 2	Clear All 🛛 💌		and a sea and a seal	0.000		0x5 (101 bin)			75mV			150	DmV				

Figure 32 Current sense range and start-up current limit setting

## 4.1.8 **Programming VIN\_UV\_FAULT\_LIMIT**

If using AADM or ACM, skip this step because the input undervoltage (UV) fault limit is set by external resistors on the UV pin.

If using DCM, program the desired UV fault limit in the VIN\_UV\_FAULT\_LIMIT register (0x59). If the UV fault is not used, the register can be programmed to 0 V, or the fault can be disabled.

inf	ineon Searc	:h	Q				TLVR 🕸 📃 PMB 🕼 FW 🔧 🖹 GC 🚓 CFG 🐞 🌣 📲 👔
≡¢	Active Controller	:	Search	All Fault MF	R Status 1	Felem Vout	VIN_UV_FAULT_LIMIT Live Read (0n) 🗰 🗙
ħ	() XDP700V002	2: 0x10	Code	Command	Hex	Value	selected Loop
۲	🔴 Loop A :	Vout = 47.28V   lout = 0A	0x01	OPERATION	0×80		Loop A
Ø	Telemetry	: 🛛	0x03	CLEAR_FAULTS			Command Value (Decimal)
	Vin	48.012 V	0x19	CAPABILITY	0xD0		37.9969911885 — 🕂 V
	Vout	47.281 V	0x42	VOUT_OV_WARN_LIMIT	0x0F73	84.9989 V	
	lout Temp (Ext)	0 A -275.4 °C	0x43	VOUT_UV_WARN_LIMIT	0×0000	٥v	
	Temp (Int)	37.17 °C	0x44	VOUT_UV_FAULT_LIMIT	0x06E8	37.997 V	
	Pin 0W 0x4A IOUT_OC_WARN_LIMIT 0x0FFF 35.3566.A						
			0x4F	OT_FAULT_LIMIT	0x0FFF	512.0962 °C	
			0x51	OT_WARN_LIMIT	0x0FFF	512.0962 °C	
			0x55	VIN_OV_FAULT_LIMIT	0x0CB9	69.9979 V	Read Write
			0x57	VIN_OV_WARN_LIMIT	0x0FFF	88.0077 V	Lean Mille
			0x58	VIN_UV_WARN_LIMIT	0x0000	0 V	Description This command sets the value of the input voltage measured at the VDD_RTNS pin that causes an input undervoltage fault.
			0x59	VIN_UV_FAULT_LIMIT	0x06E8	37.997 V	UV fault can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM RNG settings.
			0x6B	PIN_OP_WARN_LIMIT	0xFFFF	3112.7102 W	
			0x78	STATUS_BYTE	0x40		
			0x79	STATUS_WORD	0x0840		
			0x7A	STATUS_VOUT	0x00		
		Clear All	0x7B	STATUS_IOUT	0x00		

Figure 33 Program VIN\_UV\_FAULT\_LIMIT



## 4.1.9 **Programming VIN\_OV\_FAULT\_LIMIT**

Note:

If using AADM or ACM, skip this step because the input overvoltage (OV) fault limit is set by external resistors on the OV pin.

If using DCM, program the desired OV fault limit in the VIN\_OV\_FAULT\_LIMIT register (0x55). If the OV fault is not used, the register can be programmed to 88 V, or the fault can be disabled.

Infineon - XDP™ Desi	igner (Dev_Build+2825)					- 0 >>
infineon	Search	Q				TLVF 🕸 📃 PMB 🕼 FW 🔦 🖺 GC 🚓 CFG 🛎 🌣 💶 🔮
Active Cont	roller :	Search	All Fault MFR	Status T	ielem Vout	VIN_OV_FAULT_LIMIT Live Read (On) 🛑 🗙
n 🕴 🚺	700V002: 0x10	Code	Command	Hex	on A Yalue	selected Loop
ji 🦾 🔶 I	Loop A : Vout = 47.28V   Iout = 0A	0x01	OPERATION	0x80		Loop A
Telemetry	: 🛛	0x03	CLEAR_FAULTS	-		Command Value (Decimal)
Vin	48.012 V	0x19	CAPABILITY	0xD0		69.9978508489 — 🕂 v
Vout	47.281 V	0x42	VOUT_OV_WARN_LIMIT	0x0F73	84.9989 V	
lout Temp (Ext)	0 A -275.4 °C	0x43	VOUT_UV_WARN_LIMIT	0x0000	0 V	
Temp (Int)	37.17 °C	0x44	VOUT_UV_FAULT_LIMIT	0x06E8	37.997 V	
Pin	0 W	0x4A	IOUT_OC_WARN_LIMIT	0x0FFF	35.3566 A	
		0x4F	OT_FAULT_LIMIT	0x0FFF	512.0962 °C	
		0x51	OT_WARN_LIMIT	0x0FFF	512.0962 °C	
		0x55	VIN_OV_FAULT_LIMIT	0x0CB9	69.9979 V	
		0x57	VIN_OV_WARN_LIMIT	0x0FFF	88.0077 V	Read Write
		0x58	VIN_UV_WARN_LIMIT	0x0000	0V	Description
		0x59	VIN_UV_FAULT_LIMIT	0x0000	0V	The VIN_OV_FAULT_LIMIT command sets the value of the input voltage measured at the VDD_RTNS pin that causes an input overvoltage fault. OV fault can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM RNG settings.
		0x6B	PIN_OP_WARN_LIMIT	0x5555	3112.7102 W	
		0x78	STATUS_BYTE	0x40		
		0x79	STATUS_WORD	0x0840		
		0x7A	STATUS_VOUT	0x00		
Faults [ 2]	Clear All 🔽 👻	0x7B	STATUS_IOUT	0x00	· ·	
USB007 v66.0	EN L Device Checksum 0x95FD	0.70	ATITUA UIBLIT	0.00	_	

Figure 34 Program VIN\_OV\_FAULT\_LIMIT



## 4.1.10 **Programming VOUT\_UV\_FAULT\_LIMIT**

To program the desired UV fault limit, set the VOUT\_UV\_FAULT\_LIMIT register (0x44). If the UV fault is not used, the fault can be disabled.

Note:

If enabled, VOUT\_UV\_FAULT should not be set to 0 V because hot swap will turn off after turning on, detecting it as a VOUT\_UV fault.

<b>fineon</b> Sear	ch	Q				TLVF 🕂 📃 PMB 🕼 FW 🔧 🖹 GC 🚓 CFG 🗰 🌣 📲
Active Controller	:	Search	All Fault MFF	l Status	Telem Vout	VOUT_UV_FAULT_LIMIT Live Read (On)
<b>XDP700V00</b>	12: 0x10	Code	Command	Hex	on A Yalue	Selected Loop
Loop A	: Vout = 48.14V   Iout = 0A	0x01	OPERATION	0x80		Loop A
Telemetry	: 2	0x03	CLEAR_FAULTS		1.1	Command Value (Decimal)
Vin	48.098 V	0x19	CAPABILITY	0xD0		35.9962806791
Vout	48.141 V	0x42	VOUT_OV_WARN_LIMIT	0x0BD0	64.9903 V	
lout Temp (Ext)	0 A -123.1 °C	0x43	VOUT_UV_WARN_LIMIT	0x06E8	37.997 V	
Temp (Int)	37.61 °C	0x44	VOUT_UV_FAULT_LIMIT	0x068B	35.9983 V	
Pin	0 W	0x4A	IOUT_OC_WARN_LIMIT	0x090C	19.9965 A	
		0x4F	OT_FAULT_LIMIT	0x07A0	99.9808 °C	
		0x51	OT_WARN_LIMIT	0x076C	89.9808 °C	
		0x55	VIN_OV_FAULT_LIMIT	0x0B45	62.003 V	
		0x57	VIN_OV_WARN_LIMIT	0x0AE8	60.0043 V	Read Write
		0x58	VIN_UV_WARN_LIMIT	0x0717	39.0071 V	Description The YOUT_UV_FAULT_LIMIT command sets the value of the output voltage measured at the YOUT pin that causes an output undervoltage fault.
		0x59	VIN_UV_FAULT_LIMIT	0x06E8	37.997 V	OUV fault can be programmed from 0 to 22, 0 to 44 or 0 to 88V (absolute value) depending on VTLM RNG settings.
		0x6B	PIN_OP_WARN_LIMIT	0x62B1	1200.0095 W	
		0x78	STATUS_BYTE	0x40		
		0x79	STATUS_WORD	0x0840		
		0x7A	STATUS_VOUT	0x20		
c # 0		0x7B	STATUS_IOUT	0x00		
Faults 2	Clear All		ATTUA HIALT	0.40		

Figure 35 Program VOUT\_UV\_FAULT\_LIMIT

## 4.2 Programming XDP700-002 in different modes

XDP700-002 can be operated in two different modes: FDM and AADM. FDM has two selections: DCM and ACM. AADM or FDM can be selected based on the resistor connected on the Mode 0 and Mode 1 pins on the evaluation board. Based on the mode selected, you need to configure different PMBus registers.

## 4.2.1 Fully Digital Mode (FDM)

FDM lets you select the FET, start-up current limit, and current sense range via PMBus registers. In digital comparator mode (DCM), the fault sensing on input and output voltages is done via digital comparators and is based on the telemetry of the device. This approach reduces the analog circuitry required while in analog comparator mode (ACM). This method uses external voltage dividers on the UV and OV pins. The voltage on the divider is compared with the internal threshold to detect faults. Voltage warnings are set internally via PMBus. You need to program the following registers through PMBus in FDM for both DCM and ACM:

- FET\_SELECT: See Section 4.1.4
- R<sub>sns</sub>: See Section 4.1.5
- Watchdog (optional): See Section 4.1.6
- Current sense range (CS\_RNG) and start-up current limit (IST): See Section 4.1.7

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- Enable telemetry
- Enable warnings (if needed)
- Setting warnings (if needed)

## 4.2.1.1 Digital Comparator Mode (DCM)

If the device is programmed using DCM, select DCM in the register 0xD1 and modify bit '7' to '1'. You need to modify the following register to detect the necessary faults if the corresponding fault bits are enabled in the PMBus register (0xDE).

- VOUT\_UV\_FAULT\_LIMIT (0x44): See Section 4.1.10
- VIN\_OV\_FAULT\_LIMIT (0x55): See Section 4.1.9
- VIN\_UV\_FAULT\_LIMIT (0x59): See Section 4.1.8

To turn ON the FET, toggle the enable signal to **HIGH** (EN H) on the GUI, as shown in Figure 36.

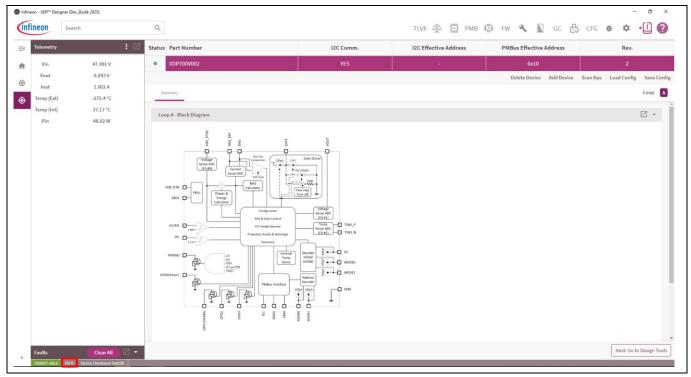


Figure 36 Enabling FET by toggling enable signal high

## 4.2.1.2 Analog Comparator Mode (ACM)

If the device is programmed using ACM, select the ACM in the 0xD1 register, and modify bit '7' to '0'. In this mode, all the voltage faults are sensed using external resistors. Therefore, you need to place the following jumpers on the evaluation board to detect faults if the corresponding fault bits are enabled in the PMBus register (0xDE):

- VIN\_OV\_FAULT\_LIMIT (OV pin): Jumper is required on connector X41; the input OV fault limit can be set by modifying R34, R36, and R38.
- VIN\_UV\_FAULT\_LIMIT (UV pin): Jumper is required on connector X33. If UV\_FAULT is disabled, ensure that the UV pin gets the necessary enable signal voltage to turn ON the FET.



## 4.2.2 Analog Assisted Digital Mode (AADM)

AADM lets you select the FET, start-up current (IST) limit, and current sense range (CS\_RNG) via external resistors connected on pins Mode 0, Mode 1, and IST. For the evaluation board, the settings are done as shown in Table 6.

#### Table 6AADM selection resistors

Connector	Jumper position (resistor)	Function
X18 (mode pins)	Between 3 and 4 (Mode 0: Open)	Selects the FET
	Between 9 and 10 (Mode 1: 20 kΩ (2.0 V))	IPB017N10N5ATMA1
X21 (IST pins)	Between 5 and 6 recommended (IST: 11 kΩ (1.1 V))	25 mV current sense range is selected and IST as 12.5 percent of overcurrent (OC) level is selected.

Place the following jumpers on the evaluation board to detect faults if the corresponding fault bits are enabled in the PMBus register (0xDE):

- VIN\_OV\_FAULT\_LIMIT (OV pin): Jumper is required on connector X41; the input OV fault limit can be set by modifying R34, R36 and R38.
- VIN\_UV\_FAULT\_LIMIT (UV pin): Jumper is required on connector X33. If UV\_FAULT is disabled, ensure that the UV pin gets the necessary enable signal voltage to turn on the FET.

Modify the necessary PMBus registers for proper operation:

- R<sub>sns</sub>: See Section 4.1.5
- Watchdog: See Section 4.1.6
- Enable telemetry
- Enable warnings (if needed)
- Setting warnings (if needed)



#### Loading the configuration file

# 5 Loading the configuration file

You can load the configuration file into the device, which eliminates the need to manually modify the required registers. The configuration file can be loaded into the device as follows:

- 1. Click Load Config, as shown in Figure 37.
- 2. Click **Browse** and select the *.txt* file, as shown in Figure 38.
- 3. Click **Load** to load the configuration onto the device, as shown in Figure 39.

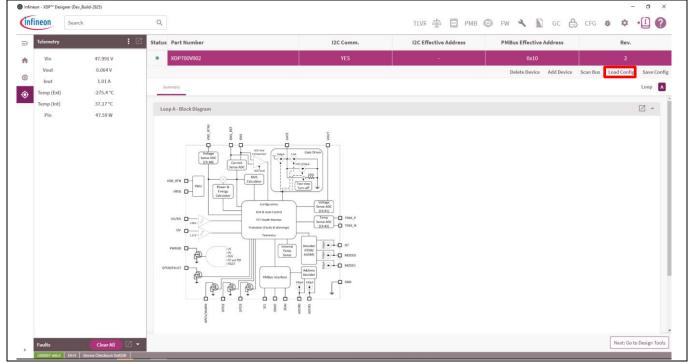


Figure 37 Select Load Config option

Load Config File	×
Select a Configuration File	
	Browse
	Close

Figure 38 Browse to select the necessary configuration file



#### Loading the configuration file

Load Config	File				×
Select a Co	onfiguration File	e			
XDP700V00	2_EvalBoard-0x0	000291F.txt		Bro	wse
Type: Checksum: Created By: Select Targ		File Versior GUI Versior Created Da	: Dev_Build		:47
Conf	ig File Device	<b>→</b>	Connected D	evice	
XDP7	00V002:0x10		(DP700V002:	0x10	~
			Clo	se	Load

Figure 39 Load to load the selected configuration file

An example configuration file in .txt format is available in the XDP700-002 Evaluation Board page [2] as *XDP700V002\_EvalBoard-0x0000291F.txt*. This configuration file is compatible with the evaluation board in the default configuration.

## 6 Hands-on

Ensure the following:

- Proper input voltage (48 V) is available on the input of the evaluation board.
- The example configuration is loaded onto the device.
- The device is not yet enabled.

## 6.1 Turn ON FET test

The FET is turned ON by toggling the enable signal to HIGH (EN H) as shown in Figure 40.

*Note:* Ensure that the load is not ON when enabling the FET because it could cause the watchdog timer fault; in such a case, the FET will not turn ON.

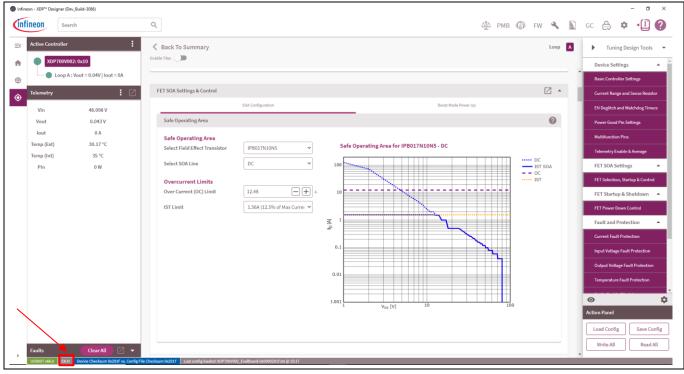


Figure 40 Enabling FET by toggling enable signal to high

Figure 41 shows the turn-on waveforms. Note that the start-up current follows the programmed SOA of the FET as shown in Figure 41 closely, and ensures that the FET SOA is not violated during turn-on operation, thereby providing a safe and fast turn-on. Additionally, the maximum startup current observed is 1.626 A at an IST setting of 12.5%. Figure 42 highlights the regulation current at various VDS levels based on the SOA of IPB017N10N5.

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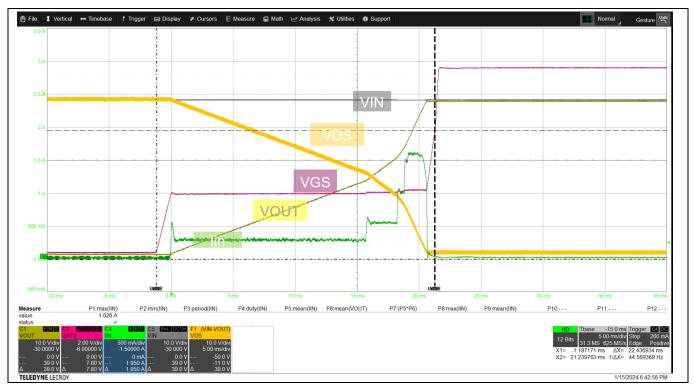


Figure 41 Startup current waveform at 48 V input



Figure 42

Startup current regulation at various VDS levels



## 6.2 Boost mode test

For FETs with weaker SOA, with current capability of less than 0.25 A at higher voltages, it is recommended to turn ON the FET in boost mode. In the following example, boost mode is enabled, and the parameters are set as follows:

- Type of boost mode: Automatic boost mode
- SOA line: 1 ms
- Duty cycle: 20%

If the SOA is below 0.5 A, boost mode is activated; the controller sends gate pulses allowing the drain current for only 1 ms with its limit restricted to 8x the programmed SOA level. When the regulation current reaches 0.5 A, boost mode turns off, and the FET is regulated with regular SOA. Figure 43 shows the startup behavior with automatic boost mode and at  $V_{DS} = 25$  V where  $I_{SOA} = 0.5$  A, the controller resumes with regular current regulation.

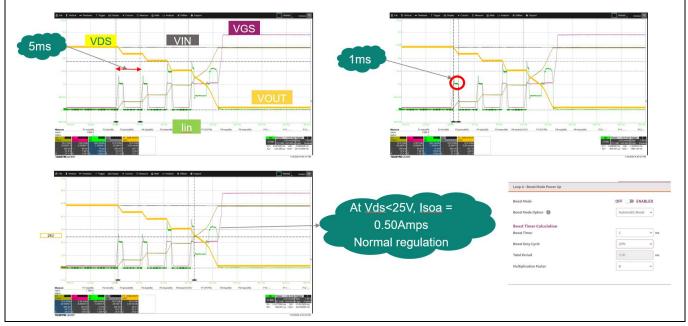


Figure 43 Automatic boost mode operation

Attention: Set the duty cycle according to  $C_{gs}$  to provide sufficient time for the gate to discharge to avoid double pulses and violation of SOA on 1 ms line.



## 6.3 Turn-ON in output short test

The output of the evaluation board is shorted together, and the watchdog timer is reduced down to 200 ms from 500 ms. Hot swap is enabled by toggling the enable signal to **HIGH** (EN H). Figure 44 shows that the current has been regulated down to the minimum level of 0.25 A; after the watchdog timer expires, the gate is turned OFF and a watchdog timer fault is issued.



Figure 44 Turn on in output short



#### Programming SOA, OTP, and MTP

# 7 **Programming SOA, OTP, and MTP**

Do the following to program the required settings in internal commands or OTP at power-up. See the XDP700-002 datasheet [1] for details.

- 1. Apply a voltage at the VDD\_RTN and VDD\_RTNS pins:
  - At least 9 V to program commands (evaluation board bias is activated at 9 V)
  - At least 20 V to program OTP or MTP
- 2. Keep the UV/EN pin at chip GND potential.
- 3. Wait for the device to enter STANDBY state. Communication via PMBus is possible now.
- 4. Program the commands, OTP, or MTP.
- *Note:* To ensure successful programming, keep the internal temperature of the device below 125°C at all times.

## 7.1 **Program OTP or MTP sections**

- 1. Program the commands in volatile memory as required.
- 2. Click the button highlighted in red as shown in Figure 45.

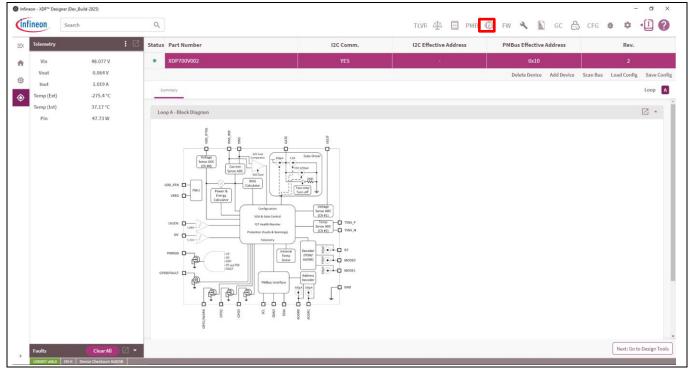
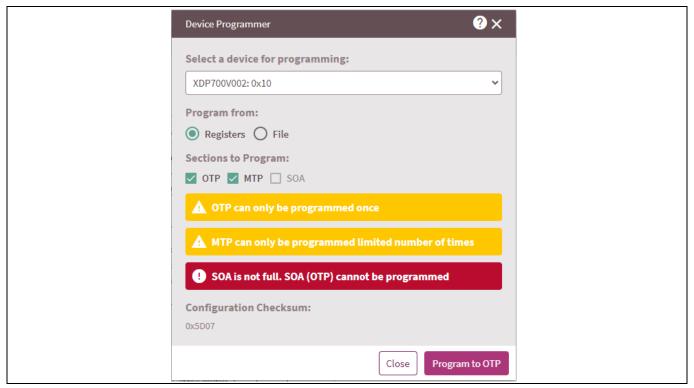


Figure 45 Programming tab

3. Set the program from **Registers**, select the memory section that needs to be programmed, and click **Program to OTP**, as shown in Figure 46.



#### Programming SOA, OTP, and MTP



#### Figure 46 OTP and MTP programming

The command configuration will be automatically copied to the selected memory section.



#### References

## References

- [1] Infineon Technologies AG: XDP700-002 hot-swap controller datasheet; Available online
- [2] Infineon Technologies AG: XDP700-002 Evaluation Board webpage; Available online



## **Revision history**

# **Revision history**

Document revision	Date	Description of changes
V 1.0	2024-04-12	Initial release

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