Alveo V80 Data Center Accelerator Cards Data Sheet:

DS1013 (v1.0) May 8, 2024 **Product Specification**

Summary

The AMD Alveo™ V80 high-performance data center accelerator card is designed for deployment in any server on-prem or in the cloud and targets accelerating memory-bound, compute-intensive, high bandwidth workloads in:

- Genomic sequencing
- High-performance computing (HPC)
- Packet processing
- Big data analytics and search
- Financial computing
- Storage services

Featuring the powerful AMD Versal™ XCV80 HBM series adaptive SoC, the Alveo V80 card packs high bandwidth memory (HBM2e) and 800 Gb/s of high-speed networking into a full-height ¾ length form factor dual-slot card, and is designed for deployment in a server on-prem or in the cloud.

The V80 accelerator is optimized for maximizing I/O capabilities through the AMD Versal architecture. It features 32 GB of DDR4 DIMM memory tailored for use with compute fabric and DSP engines, supplemented by an additional 4 GB of discrete memory specifically crafted for Arm® cores on the Versal silicon. Additionally, the card offers Mini Cool Edge I/O (MCIO) expansion connectors targeting diverse applications (direct connection to NVMe storage) at PCI Express® Gen5 speeds. The V80 card supports PCIe Gen4 x16 or dual Gen5 x8, contains 32 GB of high-bandwidth memory (HBM2e) at 819 GB/s of bandwidth, and Ethernet networking capability with four QSFP56 connectors capable of 4 x 200 Gb/s. All this HBM2e bandwidth, power-optimized fabric performance, and capability are unlocked and available via the AMD Vivado™ Design Suite with a flow that is streamlined for hardware designers.

The following figure shows the Alveo V80 data center accelerator card.

Figure 1: **Alveo V80 Card**

Product Details

The following table provides high-level product details.

Table 1: **Alveo V80 Card Product Details**

Specification	V80
Product SKU	A-V80-P64G-ES3-G (with 32 GB DIMM) A-V80-P64G-PQ-G (with 32 GB DIMM) A-V80-P32G-PQ-G
Thermal design power (TDP)[1]	190W
Thermal cooling solution	Passive
Weight	958g
Form factor	Full-height, ¾ length, double-slot
PCIe physical	x16 PCIe
PCIe functionality support	PCIe Gen5 x8x8 or Gen4 x16
Network I/F	4x QSFP56 supporting 56G PAM4
Memory	• 32 GB HBM2e @ 819 GB/s • 4 GB @ 3200 MT/s, 64b + 8b ECC • DDR4 288-pin DIMM socket
AUX power connectors	Two 8-pin PCIe AUX connectors
Expansion port	• 2 x MCIO x4 • 1 x MCIO x8
Card management[2]	Inband (over PCIe), out-of-band (over SMBus), management controller in adaptive SoC RPU
Power management[2]	Power management with power management bus (PMBus) for voltage, current, and temperature monitoring including telemetry for major regulators
Manufacturing interface	ADK2[3]

Table 1: **Alveo V80 Card Product Details** *(cont'd)*

Specification	V80
Configuration option	• 2 Gb OSPI • JTAG over microUSB

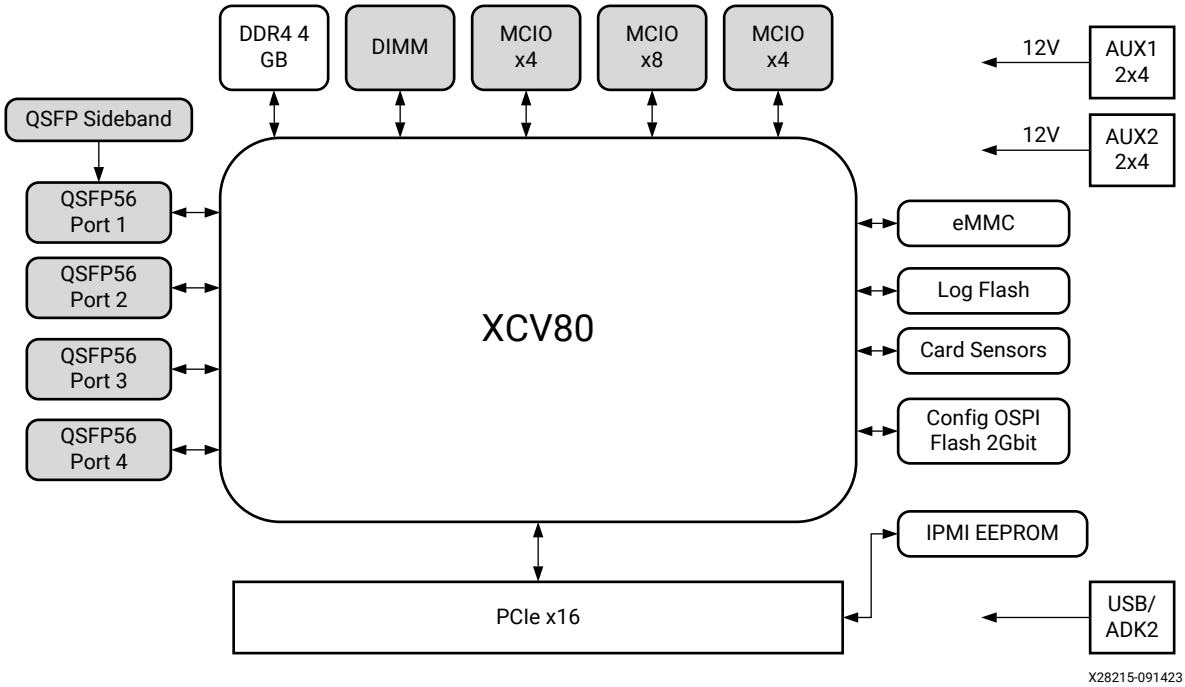
Notes:
1. TDP is the maximum power consumption, in watts, the card can operate. Actual power consumption is dependent on the work load.
2. Card and power management features are delivered via the Alveo Versal Example Design.
3. The Alveo debug kit (ADK2) connector is for manufacturing support only.

Card Specifications

Block Diagram

The high-level block diagram for the Alveo V80 card is given in the following figure.

Figure 2: **Alveo V80 High-Level Block Diagram**



Card Interfaces

The following images show the various card interfaces:

- MCIO expansion ports
- PCIe AUX power connectors
- ADK2 (for manufacturing only)
- Micro USB
- QSFP56 Ports and associated LEDs

Figure 3: **Card Interfaces**

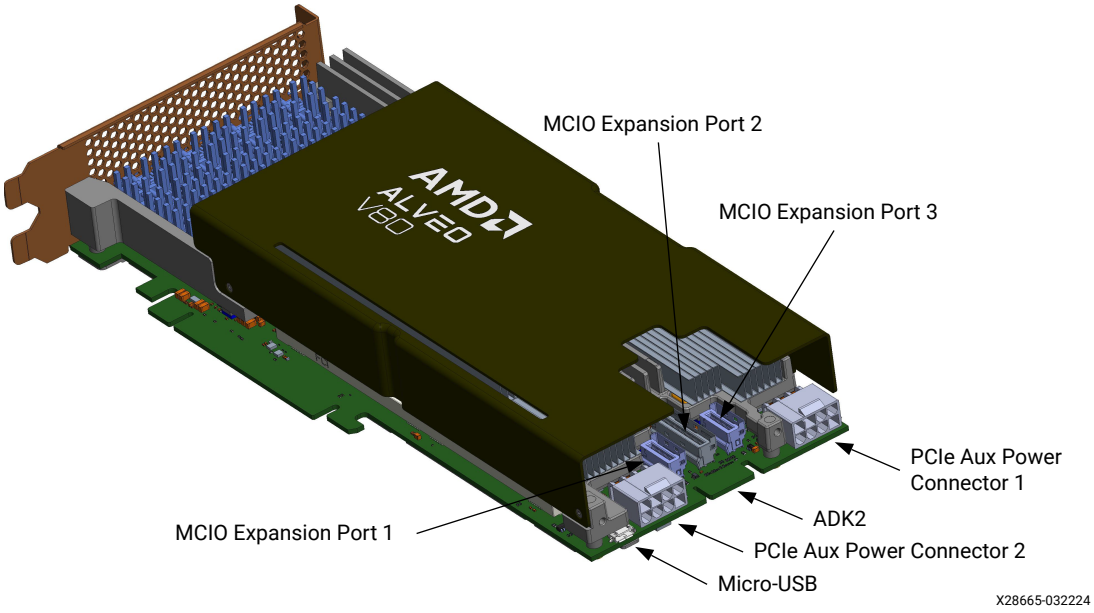
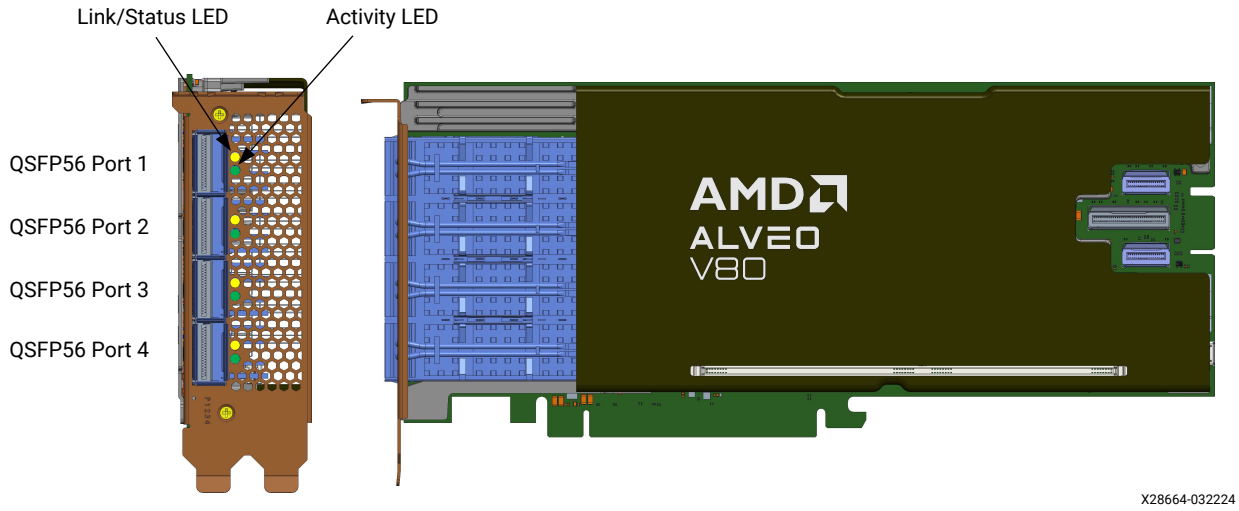


Figure 4: **QSFP56 Network Ports and LEDs**



Adaptive SoC Resources

The Alveo V80 card uses the Versal XCV80 HBM device. The key specifications for this device are given in the following table.

Table 2: **Versal XCV80 Adaptive SoC Details**

Specification	V80
HBM DRAM (GB)	32
Total Block RAM (Mb)	132
UltraRAM (Mb)	541
Total PL Memory (Mb)	752
DSP Engines	10,848

Table 2: **Versal XCV80 Adaptive SoC Details** *(cont'd)*

Specification	V80
System logic cells (K)	5,631
LUTs	2.6M
GTYP transceivers (32.75 Gb/s)[1]	32
GTM Transceivers (56G)[2]	16
CCIX and PCIe with DMA (CPM)	1
PCIe	16
400G High-speed Crypto Engines	3
100G Multirate Ethernet MAC	6
600G Ethernet MAC	3
600G Interlaken	1
Application processing unit	Dual-core Arm Cortex®-A72, 48 KB/32 KB L1 Cache with parity and ECC; 1 MB L2 Cache with ECC
Real-time processing unit	Dual-core Arm Cortex-R5F, 32 KB/32 KB L1 Cache, and 256 KB TCM with ECC

Notes:

1. While the adaptive SoC has 68 GTYP transceivers, only 32 are used by the card.
2. While the adaptive SoC has 30 GTM transceivers, only 16 are used by the card.

Adaptive SoC I/O Bank Mapping

The following table provides the adaptive SoC bank I/O allocation, associated function, and bank type. Allocation of bank type is dependent on the required function.

Table 3: **Adaptive SoC Bank Allocation**

Adaptive SoC Bank	Bank Type	Function(s)
105 – 102	GTYP	PCIe x16 to Edge Connector: • PCIe lane 3–0 on bank 105 • PCIe lane 7–4 on bank 104 • PCIe lane 11–8 on bank 103 • PCIe lane 15–12 on bank 102
111	GTM	QSFP56 4
112	GTM	QSFP56 3
210	GTM	QSFP56 2
209	GTM	QSFP56 1
213 – 214	GTYP	MCIO_2 (x8): • TX/RX 1–4 assigned to bank 213 • TX/RX 5–8 assigned to bank 214
200	GTYP	MCIO_1 (x4)
218	GTYP	MCIO_3 (x4)
700 – 702	XPIO	DDR4 discrete memory
703 – 705	XPIO	DDR4 DIMM
500, 503	PMC	Config, OSPI, and eMMC

Table 3: **Adaptive SoC Bank Allocation** *(cont'd)*

Adaptive SoC Bank	Bank Type	Function(s)
501 – 502	PMC/LPD	I2C QSFP sideband signals - Adaptive SoC LPD I2C1 in bank 502 is used as a management bus for QSFP56 ports and expansion connectors: • MCIO sideband signals • Logging flash I2C Main - Adaptive SoC LPD I2C0 in bank 502 is used as a management bus for VRMs, input power monitor, clock generator, and MFG EEPROM: • LEDs • PWRBRK#

I2C Memory Map

The following table provides the I2C base address memory map for accessible devices. There are two I2C interfaces, I2C_QSFP and I2C_MAIN, and an SMBUS. The I2C interfaces are accessible from the adaptive SoC (shown below). The table groups these registers accordingly. For specific I2C register details, see the manufacturer's respective device datasheet.

Table 4: **I2C Base Address Memory Map**

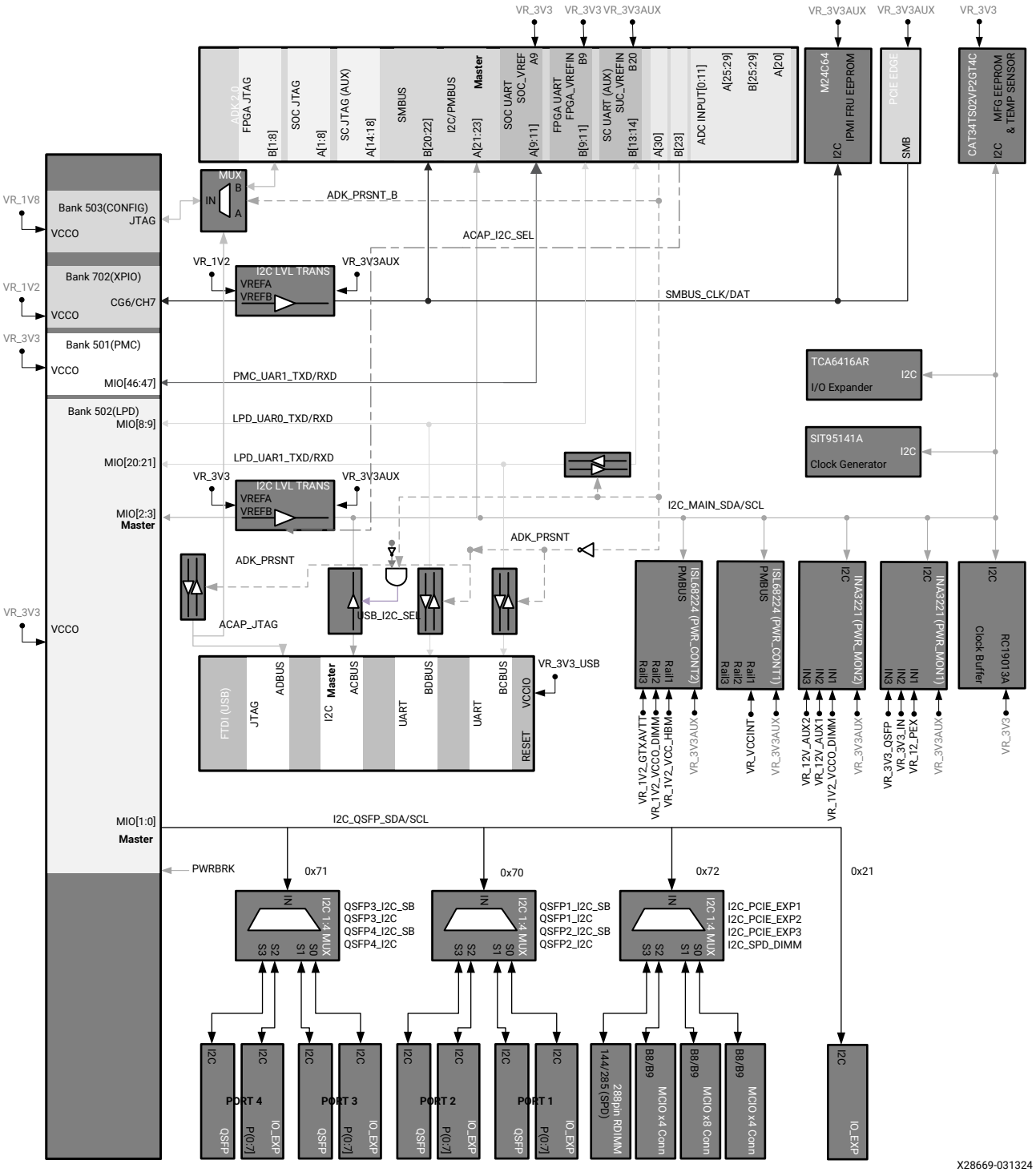
Register Name	8-bit (HEX) Address	7-bit (HEX) Address	Description	Manufacturer/Device	Comment
Accessible from SMBUS Interface					
FRU_EEPROM	0xA0	0X50	64 Kb EEPROM	ST M24C64	FRU EEPROM (See Alveo Data Center Accelerator Cards FRU Data Specification)
Accessible from I2C_MAIN Adaptive SoC Interface					
Clock generator	0x12	0x09	Clock generator component	SiTime SiT95141	Clock generator status and control registers
TempSensor_IO_Bracket	0X34	0x1A	Temperature Sensor	Onsemi CAT34TS02VP2GT4C	I/O bracket temperature sensor
IO_Expander	0X40	0X20	I2C I/O Expander	TI TCA6416AR	GPIO Expander
PWR_MON1	0X80	0X40	Current/voltage monitor	TI INA3221	Read voltage and current for: • 12V_PEX • 3V3_PEX • 3V3_QSFP
PWR_MON2	0X82	0X41	Current/voltage monitor	TI INA3221	Read voltage and current for: • 1V2_DIMM • 12V_AUX1 • 12V_AUX2
MFG EEPROM	0XA4	0x52	MFG EEPROM	Onsemi CAT34TS02VP2GT4C	
PCIe_ClkBuf	0XD8	0x6C	PCIe Clock Buffer	Renesas RC19013A	Access clock buffer status.

Table 4: **I2C Base Address Memory Map** *(cont'd)*

Register Name	8-bit (HEX) Address	7-bit (HEX) Address	Description	Manufacturer/Device	Comment
PWR_CONT1	0XC0	0X60	6-Phase PWM Controller 1	Renesas ISL68224IRAZ	Read voltage and current and other status for core voltage VCCINT.
PWR_CONT2	0XC2	0X61	6-Phase PWM Controller 2	Renesas ISL68224IRAZ	Read voltage and current and other status for HBM, CPM5, and GTXAVTT.
QSFP56 - Accessible from the Adaptive SoC I2C_QSFP Interface					
QSFP56_EN_PG	0X42	0X21	I2C I/O Expander	TI TCA6408APWR	QSFP56 1–4 Enable and Power Good. Access directly off the I2C_QSFP interface.
QSFP56 1/2 Mux	0XE0	0X70	Four-channel I2C Mux	NXP PCA9545ABS	Mux between QSFP56 1/2
QSFP56 3/4 Mux	0XE2	0X71	Four-channel I2C Mux	NXP PCA9545ABS	Mux between QSFP56 3/4
QSFP56_IO_EXP	0x40	0x20	I2C I/O Expander	TI TCA6408APWR	QSFP56 1–4 Sideband signal access. Access indirectly via QSFP56 Mux.
QSFP56_REG_ACCESS	0XA0/0XA4	0X50/0X52	Pass-through to QSFP56 module	N/A	QSFP56 1–4 access to QSFP56 I2C registers. Access indirectly via QSFP56 Mux. Address is QSFP56 module dependent. See module data sheet.
DIMM and PCIe I2C Expansion	0XE4	0X72	Four-channel I2C Mux	NXP PCA9545ABS	I2C interface for • MCIO expansion ports • SPD DIMM (EEPROM 0x50 7-bit; Temp Sensor 0x18 7-bit)

The following figure shows the devices accessible via the I2C interfaces, as well as those accessible through SMBUS, UART, and JTAG.

Figure 5: **I2C and JTAG Accessible Devices**



LED Indicators

Figure 4 shows the QSFP56 port location and number along with the activity and link/status LEDs associated with each port that are visible through the I/O bracket.

The following table lists the two LEDs present for each QSFP port along with the recommended operation and source control logic. Actual logic implementation is left to the user.

Table 5: **QSFP LEDs**

LED	Colors	Recommended Operation	Control
Link/Status[1]	Yellow/Green	Green when physical link is present and operating at the highest supported link rate. Yellow when operating at lower rates. Off in the absence of physical link.	QSFP sideband
Activity	Green	LED illuminated or blinking green to show link activity. Off when there is no activity.	Adaptive SoC

Notes:
1. For status LED pinout, refer to the XDC file.

Network Interfaces

The V80 has four QSFP56 network ports, as shown in Figure 4. Table 3 provides the QSFP56 port to adaptive SoC GT Quad mapping.

Port Labels

The QSFP56 network ports on the card are labeled Port 1 through Port 4, with their locations shown in Figure 4.

Note: Block diagrams, register maps, and the XDC file reference the QSFP56 ports as QSFP56-1 through QSFP56-4. These references map to the card QSFP56 labeling Port 1 through Port 4 as outlined in the following table.

Table 6: **QSFP56 Card Port Label to XDC/Block Diagram Net Port Label**

QSFP56 Port Label	Net/Block Diagram Port Label
QSFP56 Port 1	QSFP56_1
QSFP56 Port 2	QSFP56_2
QSFP56 Port 3	QSFP56_3
QSFP56 Port 4	QSFP56_4

Network MAC Address

Each card has 16 contiguous MAC addresses.

Determine Allocated MAC Addresses

Use the following steps to determine the allocated MAC addresses.

1. Determine the Base MAC Address
2. Use Formula to Compute Allocated MAC Addresses

Determine the Base MAC Address

To determine the base MAC address, use the management controller to display the board information or look at a sticker on the physical card.

Use Alveo Management Interface to Display Board Info

The Alveo management interface (AMI) tool can be used to display board information using the `ami_tool mfg_info` command. Board MAC0 is the base MAC address. See Alveo Versal Example Design for support details.

Identify Base MAC Address From Sticker

On the PCIe interface of the card, a sticker displays two MAC addresses:

- **MAC1:** Denotes the base MAC
- **MAC16:** Represents the last allocated MAC

Use Formula to Compute Allocated MAC Addresses

With the base MAC address, use the following formula to compute the allocated MAC addresses:

$$\mathrm{MAC}(i) = \mathrm{MAC\ base\ address} + i$$

Where i is an integer from 0 to 15.

Port LEDs

See LED Indicators.

Isolation Logic

To ensure the I2C bus is not taken down in the case of a malfunctioning QSFP56 module, each sideband I/O expander consists of an electrical isolation boundary and short circuit protection logic.

GTM Lane Mapping

QSFP56 GTM interface lane mapping and high-speed connections are detailed in Table 3 and the V80 XDC file.

QSFP56 I2C Access

As shown in the following figure, the card uses a combination of I2C multiplexers (PCA9545A) and I/O expanders (TCA6408A) to access and control power and sideband signals for all four QSFP56 modules. The sideband signals include:

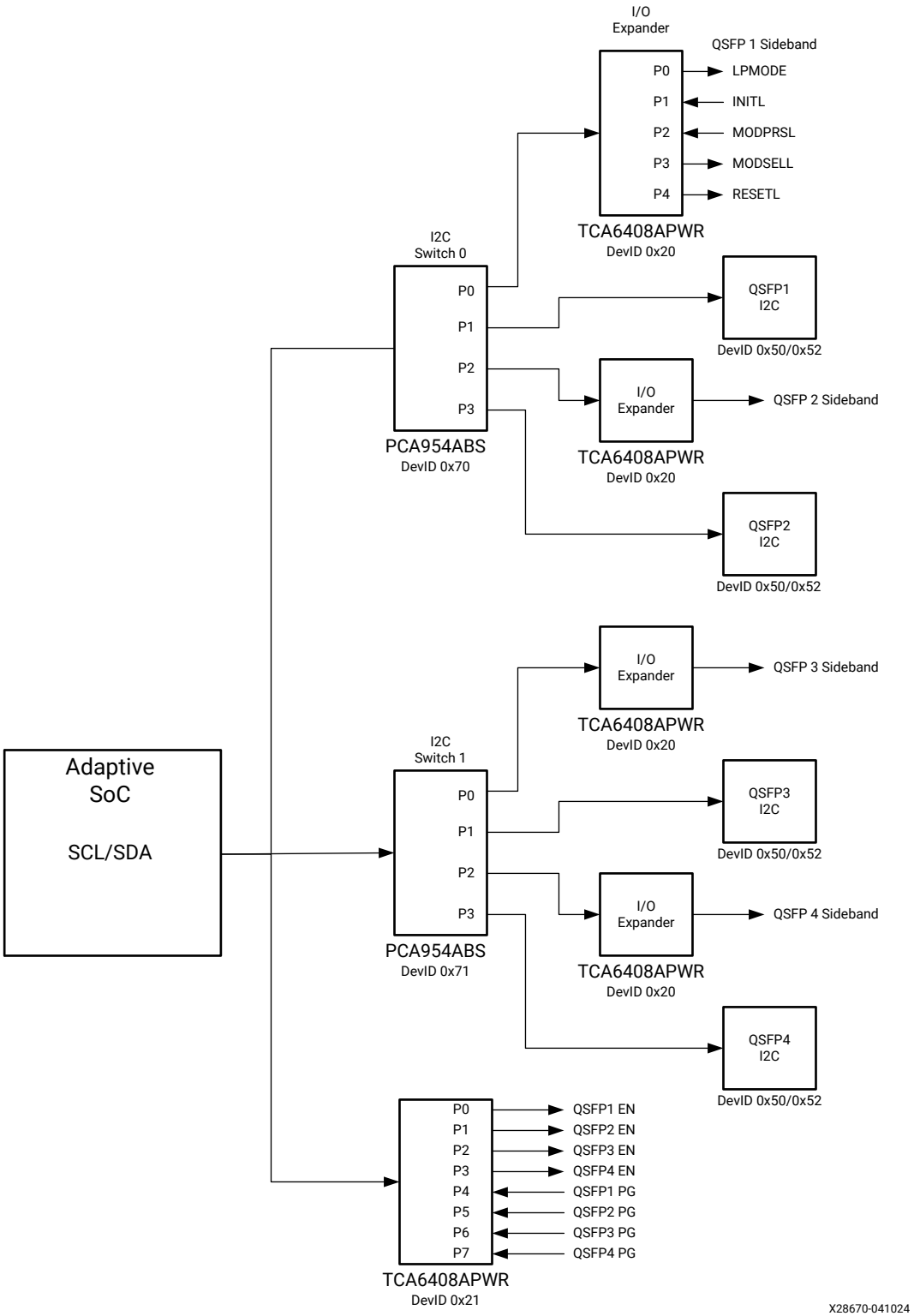
- LPMODE
- INTR
- MODPRSL
- MODSELL
- RESETL

The power signals include:

- QSFP_EN (power enable)
- QSFP_PG (power good)

The other QSFP56 I/O expanders have identical sideband signals but are not explicitly shown. To access/control particular QSFP56 signals requires enabling a particular combination of I2C multiplexers and I/O expanders.

Figure 6: **QSFP56 I2C Logic**



Powering On/Off the QSFP56 Domains

Enabling or disabling the individual QSFP56 power domains is achieved by configuring a TCA6408APWR I/O expander that drives the power enable signals.

- Ports 0 to 3 must be configured as outputs. They control the power enables for each domain.
- Ports 4 to 7 must be configured as inputs. They return the power good status of each domain.

Note: While the card can operate without either AUX power connected, power to the QSFP cages, DDR, and DIMMs requires at least AUX power connector 1 to be connected.

The following table provides the TCA6408APWR I/O expander bit settings and function.

Table 7: **QSFP56 Power Good/Enable Bit Allocation**

Bit	Function	Direction	Signal
0	QSFP56 1 Power Enable	Output	QSFP EN
1	QSFP56 2 Power Enable	Output	QSFP EN
2	QSFP56 3 Power Enable	Output	QSFP EN
3	QSFP56 4 Power Enable	Output	QSFP EN
4	QSFP56 1 Power Good	Input	QSFP PG
5	QSFP56 2 Power Good	Input	QSFP PG
6	QSFP56 3 Power Good	Input	QSFP PG
7	QSFP56 4 Power Good	Input	QSFP PG

The following table provides the three steps necessary to configure the I/O expander, enable the outputs, and read back the power good values for verification.

Table 8: **QSFP56 Power Good/Enable Bit Allocation**

Function	I2C	Sequence
Set power enable pins	0x21, 0x01, 0x0F	Programs output value register.
Enable output mode for even numbered pin	0x21, 0x03, 0xF0	Programs output config register (0 = output, 1 = input)
Read power good status	0x21, 0x00, 0xFF (expected read data)	Reads input value register

Configuring/Reading QSFP Sideband Signals

Once enabled, the QSFP sideband signals are configured by configuring two PCA9545A I2C multiplexer devices to route the I2C to the TCA6408A I/O Expander controlling the target QSFP sideband signals. This is done by a series of I2C transfers.

1. Configure both PCA9545A (IDs 0x70 and 0x71) to route the I2C path.
2. Configure the output pin value and output enable for the targeted TCA6408A.

WARNING! *Each TCA6408A has an identical I2C address, so the I2C multiplexers must be configured to route to only one such device to prevent bus contention.*

Each TCA6408A is enabled by means of pull-up resistors. This can be manually overwritten by driving the respective QSFP56_IO_RESET_B signal from the adaptive SoC. See QSFP56 Peripheral Resets for details.

Before accessing one of the QSFP56 module's I2C port or sideband expander, it is necessary to first program both I2C multiplexers to configure the appropriate routing.

***Note*:** Because of duplicate target device IDs, the multiplexers must have only one target path enabled at a time. This can be managed by performing two I2C sequences when changing targets using the following reference table.

Table 9: **I2C Multiplexer Settings to Access QSFP56 Low-Speed Sideband Signal**

Target Port	Target Device	Selected Mux Port	First I2C Sequence (Program I2C Mux 0)	Second I2C Sequence (Program I2C Mux 1)
QSFP56 1	TCA6408APWR I/O Expander	Mux 0x70, Port 0	0x70, 0x01	0x71, 0x00
QSFP56 1	External QSFP Module	Mux 0x70, Port 1	0x70, 0x02	0x71, 0x00
QSFP56 2	TCA6408APWR I/O Expander	Mux 0x70, Port 2	0x70, 0x04	0x71, 0x00
QSFP56 2	External QSFP Module	Mux 0x70, Port 3	0x70, 0x08	0x71, 0x00
QSFP56 3	TCA6408APWR I/O Expander	Mux 0x71, Port 0	0x70, 0x00	0x71, 0x01
QSFP56 3	External QSFP Module	Mux 0x71, Port 1	0x70, 0x00	0x71, 0x02
QSFP56 4	TCA6408APWR I/O Expander	Mux 0x71, Port 2	0x70, 0x00	0x71, 0x04
QSFP56 4	External QSFP Module	Mux 0x71, Port 3	0x70, 0x00	0x71, 0x08

Each QSFP56 low-speed sideband signal is connected to a TCA6408A I/O expander whose pinouts are detailed in the following table. Access to these signals involves configuring the PCA9545A I2C multiplexers to route to the targeted I/O expander, then configuring or reading the I/O expander.

Table 10: **QSFP56 Sideband Signal Definition**

Pin	Signal Name	Input/Output	Output Value
0	MODSELL	Output	0
1	RESETL	Output	1
2	LPMODE	Output	0
3	MODPRSL	Input	0
4	INTR_B	Input	0
5	N/C	Input	0
6	N/C	Input	0
7	N/C	Input	0

By default, the I/O expanders are configured for input only, so the LPMODE, MODSELL, and RESETL signals are not driven until initialized. The following table illustrates how QSFP56_1 can be initialized. Similar steps must be taken to initialize the other expanders.

Table 11: **Example Configuring QSFP56_1 I/O Expander**

Function	Sequence	Description
Disable PCA9545A (0x70)	0x70, 0x00	Gates I2C communication to QSFP56_1 and QSFP56_2 expanders
Disable PCA9545A (0x71)	0x71, 0x00	Gates I2C communication to QSFP56_3 and QSFP56_4 expanders
Disable PCA9545A (0x72)	0x72, 0x00	Gates I2C comms to PCIe and DIMMs

Table 11: **Example Configuring QSFP56_1 I/O Expander** *(cont'd)*

Function	Sequence	Description
Enable Port 2 of PCA9545A (0x70)	0x70, 0x04	Enables I2C routing to QSFP56 sideband expander
Program QSFP56_1 TCA6008A (0x20)	0x20, 0x01, 0x02	Sets RESETL, clears LPMODE, MODSEL (pins 0,1,2)
Program QSFP56_1 TCA6008A (0x20)	0x20, 0x03, 0xF8	Configures output enables for pins 0,1,2

QSFP56 Peripheral Resets

Each I2C I/O expander and multiplexer component has an active-Low reset connected to the adaptive SoC. All components have an external pull-up resistor and therefore are enabled following a power reset. However, they can also be manually controlled by the adaptive SoC using the following pins.

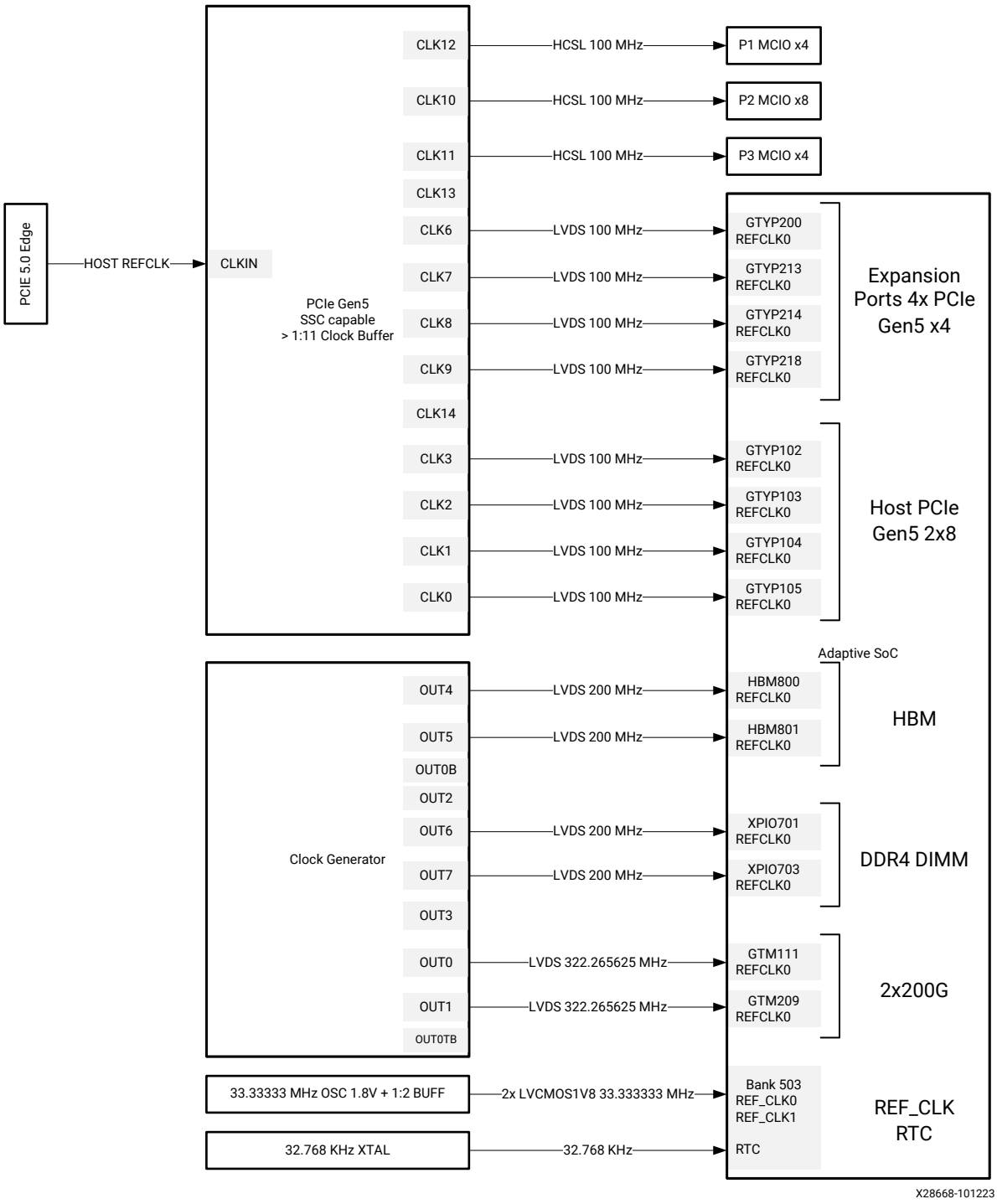
Table 12: **I2C Peripheral Resets**

Signal	Peripheral	Adaptive SoC Pin	External Pullup
I2C_QSFP_RST_B	Mux 0 and 1, power enable, MCIO expansion port	BJ5	3.3V
QSFP56_1_IOEXP_RST	QSFP56 1 I/O expander	BJ4	3.3V
QSFP56_2_IOEXP_RST	QSFP56 2 I/O expander	BH4	3.3V
QSFP56_3_IOEXP_RST	QSFP56 3 I/O expander	BE6	3.3V
QSFP56_4_IOEXP_RST	QSFP56 4 I/O expander	BF6	3.3V

Clocking

The following high-level clock tree diagram shows the advanced clocking logic.

Figure 7: **Clock Tree**



It includes a PCIe Gen5 clock buffer (Renesas RC19013A) to distribute the 100 MHz PCIe Gen5 clock, originating from the PCIe edge connector. The following table lists various output clocks from the buffer.

Table 13: **PCIe Clock Buffer Output Frequencies**

Clock Output Reference	Frequency	Destination Adaptive SoC Bank	Block Reference Clock	XDC Net Name
OUT0	LVDS 100 MHz	GTYP105	Host PCIe Gen5 2x8	PCIE_105_REFCLK0_N PCIE_105_REFCLK0_P
OUT1	LVDS 100 MHz	GTYP104		PCIE_104_REFCLK0_N PCIE_104_REFCLK0_P
OUT2	LVDS 100 MHz	GTYP103		PCIE_103_REFCLK0_N PCIE_103_REFCLK0_P
OUT3	LVDS 100 MHz	GTYP102		PCIE_102_REFCLK0_N PCIE_102_REFCLK0_P
OUT4	NOT CONNECTED			
OUT5	NOT CONNECTED			
OUT6	LVDS 100 MHz	GTYP200	Expansion Ports 4x PCIe Gen5 x4	MCIO_200_REFCLK0_N MCIO_200_REFCLK0_P
OUT7	LVDS 100 MHz	GTYP213		MCIO_213_REFCLK0_N MCIO_213_REFCLK0_P
OUT8	LVDS 100 MHz	GTYP214		MCIO_214_REFCLK0_N MCIO_214_REFCLK0_P
OUT9	LVDS 100 MHz	GTYP218		MCIO_218_REFCLK0_N MCIO_218_REFCLK0_P
OUT10	HCSL 100 MHz	MCIO J12 (MCIO Port 2)		MCIO_C_P2_REFCLK_C_N MCIO_C_P2_REFCLK_C_P
OUT11	HCSL 100 MHz	MCIO J11 (MCIO Port 3)		MCIO_C_P3_REFCLK_C_N MCIO_C_P3_REFCLK_C_P
OUT12	HCSL 100 MHz	MCIO J10 (MCIO Port 1)		MCIO_C_P1_REFCLK_C_N MCIO_C_P1_REFCLK_C_P
OUT13	NOT CONNECTED			
OUT14	NOT CONNECTED			

In addition, it also includes a clock generator (SiTime SiT95141) which provides reference clocks for the various blocks detailed in the following table.

Table 14: **Clock Generator Output Frequencies**

SiTime SiT95141	Frequency	Destination Adaptive SoC Bank	Block Reference Clock	XDC Net Name
OUT4	LVDS 200 MHz	800	HBM	HBM_800_REFCLK_N HBM_800_REFCLK_P
OUT5	LVDS 200 MHz	801	HBM	HBM_801_REFCLK_N HBM_801_REFCLK_P
OUT6	LVDS 200 MHz	701	DDR4 memory controller	sys_clk0_0_clk_n sys_clk0_0_clk_p
OUT7	LVDS 200 MHz	703	DDR4 DIMM	sys_clk0_1_clk_n sys_clk0_1_clk_p
OUT0	322.265 MHz	GTM111	QSFP56	QSFP_GTM111_REFCLK_N QSFP_GTM111_REFCLK_P
OUT1	322.265 MHz	GTM209	QSFP56	QSFP_GTM209_REFCLK_N QSFP_GTM209_REFCLK_P

Finally, there are two on-board LVCMOS18 33.333333 MHz reference clocks sourced by the Onsemi NB3V1102CMTTBG clock buffer. The clock is sourced by a 33.33333 MHz oscillator. Details are given in the following table.

Table 15: **System Reference Clocks**

Onsemi NB3V1102CMTTBG Clock Output Reference	Frequency	Destination Adaptive SoC Bank	Block Reference Clock	XDC Net Name
Q0	LVCMOS18 33.333333 MHz	503	Reference Clock	REF_CLK0
Q1	LVCMOS18 33.333333 MHz	503	Reference Clock	REF_CLK1

Card Power System

There are five power rails with the names and source given in the following table. Each QSFP56 uses isolated power, delivered by a dedicated regulator to provide power enable and over-current control per port.

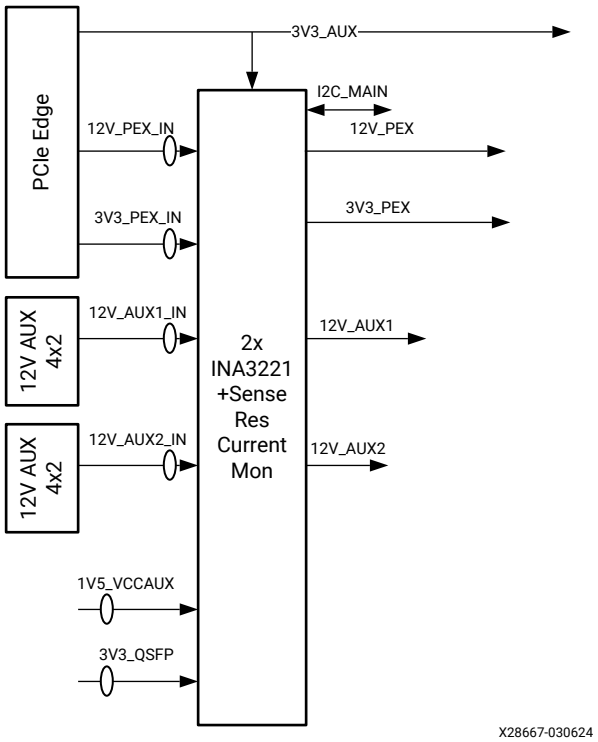
***Note*:** While the card can operate without either AUX power connected, power to the QSFP cages, DDR, and DIMMs requires at least AUX power connector 1 to be connected.

Table 16: **Power Rails**

Power Rail Name	Source
12V_PEX	PCIe Edge Connector
3V3_PEX	PCIe Edge Connector
3V3_AUX	PCIe Edge Connector
12V_AUX1	PCIe AUX Power Connector 1
12V_AUX2	PCIe AUX Power Connector 2

The following figure shows the top-level power tree.

Figure 8: **Power Tree**



PCIe Connector

The Alveo V80 card has a PCIe Gen5 x8x8 (or Gen4 x16) interface compliant with PCIe CPM 5.0 that is configured as a PCIe Endpoint that supports bifurcation.

Power Brake (PCIe)

This section details the Power Brake (also known as Emergency Power Reduction or eBrake) feature. The Alveo V80 card is designed to support the Power Brake feature through the PCIe connector. The PWRBRK# is connected to PMC bank 501 MIO 37. Implementation of the logic to act upon the PWRBRK# signal is left to the user.

DDR4 Specifications

There are five discrete DDR4 memory parts for a total of 4 GB DDR4. This bank is implemented with 5 x16 DDR4 discrete devices to support 64b + 8b ECC. The following table details the DDR4 memory component used. The discrete DDR4 memory is always powered on and must be initialized upon power-on.

Table 17: **DDR4 Component Specification**

Parameter	Description
Manufacturer	Micron
Part number	MT40A512M16TB
Total number of parts on card	Five
Details	4 GB, 3200 MT/s, 64b + 8b ECC

DDR4 DIMM Specification

A single 288-pin DIMM socket is present on the V80 card. Certain card SKUs have the socket populated with a 32 GB DDR4 DIMM module (see Table 1). The following table details the populated 32 GB DIMM module. Power to the DIMM is enabled on the V80 when the card is powered on and must be initialized upon power-on. Power to the DIMM can be disabled via the I2C if the DIMM interface is not utilized.

Table 18: **DIMM Specification**

Parameter	Description
Manufacturer	Micron
Part number	MTA18ASF4G72PZ-3G2F1
Total number of parts on card	One
Details	32 GB, 3200 MT/s, 64b + 8b ECC

OSPI Configuration Memory

The card is populated with 2 Gb Octal Serial Peripheral Interface (OSPI) flash memory, which provides space to store up to four maximum-sized adaptive SoC bitstreams. The following table details the OSPI component.

Table 19: **OSPI Device Details**

Parameter	Description
Manufacturer	Micron
Part number	MT35XU02GCBA1G12
Details	• Speed: 100 MHz • Density: 2 Gb (256M x 8)

Two adaptive SoC configuration modes are supported:

- Adaptive SoC configurable over JTAG (micro USB)
- Octal SPI configuration flash memory

The card has a fixed pin strap to OSPI boot mode (0x8). JTAG can still be accessed over micro USB.

Manufacturing EEPROM

A manufacturing EEPROM is connected to the adaptive SoC via the I2C main interface. See Table 4 for the address. The following table provides the manufacturing EEPROM register map. Data locations 0–127 are in a write protected area of the device and are set at time of manufacturing. Data locations 128–255 are in a re-writable area and can be accessed/modified by the user. The AMI tool can be used to view EEPROM information using the `ami_tool mfg_info` and `ami_tool eeprom_rd/eeprom_wr` commands.

Table 20: **Manufacturing EEPROM Register Map**

Location (Hex)	Location (Dec)	No. of Bytes	Field Name	Stored Format
0	0	4	EEPROM Version	ASCII

Table 20: **Manufacturing EEPROM Register Map** *(cont'd)*

Location (Hex)	Location (Dec)	No. of Bytes	Field Name	Stored Format
4	4	2	Data Checksum	Literal/Binary
6	6	36	Alveo Product Name	ASCII
2A	42	24	Alveo Part Number	ASCII
42	66	16	Manufacturing Alveo Part Number	ASCII
52	82	5	Manufacturing Alveo Part Revision	ASCII
57	87	14	Product Serial Number	ASCII
65	101	4	Manufacturing Date	Literal/Binary
69	105	1	Number of MAC IDs	Literal/Binary
6A	106	6	MAC ID 1	Literal/Binary
70	112	16	UUID	Literal/Binary
80	128	128		

The following sections provide the description of the various fields. Unless stated, all values must be programmed starting with the MSB at the lowest address (that is, Big Endian method). All the trailing unused bytes in each field must be set to 0xFF at the time of EEPROM programming. For example, the maximum length of Alveo Product Name is 36 bytes. A 24-byte long Alveo Product Name leaves the last 12 bytes set to the default value of 0xFF.

EEPROM Version

Format: (ASCII) `NN.N`

Up to 4 characters (including '.') when N is numeric, to identify the EEPROM version, for example, `4.0`.

Data Checksum

Format: 2-byte numeric value

Inverted value of the sum of data in locations 6 to 128.

Note: The product name and serial number can be tracked by scanning the 2D barcode printed on the Alveo accelerator card with the AMD Device Lookup app downloadable on Android and iOS.

Number of MAC IDs

Format: 1-byte number defining the quantity of MAC IDs

MAC ID 1

Format: 6-byte Hexadecimal notation, for example, `AB3241CDAB9F` with colons omitted

The number of MAC IDs required is product dependent but fixed and contiguous (as defined in ARDs). The MAC ID 1 field is the mandatory field. Management controller firmware reads the MAC ID 1 field and calculates all the other required MAC IDs using the Number of MAC IDs field and passes on required information via in-band or out-band, as needed.

UUID

Format: 128-bit UUID conforming to UUID V1

Hyphens/dashes in UUID are not encoded into this field.

MCIO Expansion Ports

The V80 card has two MCIO x4 and one MCIO x8 expansion connectors which provide additional access to the card. They are to be used with SFF-TA-1016 expansion cables. Connectors meet OCP M-XIO base specification, v.0.8 pinout with the following exceptions:

- FLEXIO signals are not supported
- USB2 signals are not supported

FRU EEPROM

An intelligent platform management interface (IPMI) FRU EEPROM is attached to the PCIe edge connector SMBus and allows card discovery capabilities when the server hosting the card is in standby mode (only 3.3V auxiliary power is available to the card). IPMI FRU EEPROM follows the Alveo Data Center Accelerator Cards FRU Data Specification. This 64 kb EEPROM is located at address 0x50 and is powered from the 3.3V auxiliary domain. It can be accessed directly by the baseboard management controller (BMC) to make card discovery in standby mode when the adaptive SoC is not powered. Write protect is controlled by a sticky bit from the adaptive SoC.

Adaptive SoC Configuration

Adaptive SoC configuration is supervised by an on-chip platform management controller (PMC). Upon card power-on or reset, the MODE pins (shown in the following table) dictate the primary boot memory device. The card has fixed pin strap to OSPI boot mode (0x8). JTAG mode (0x0) can always be selected by accessing the MODE register through JTAG chain. See the Xilinx Design Constraints (XDC) file for more details.

Table 21: **Mode Pins**

Mode Pin	Default Value	Adaptive SoC Pin
0	0	BG2
1	0	BH2
2	0	BJ2
3	1	BK2

Adaptive SoC eMMC Memory

The following table details the eMMC memory component used.

Table 22: **Adaptive SoC eMMC Specification**

Parameter	Description
Manufacturer	Micron
Part number	MTFC64GBCAQTC
Total number of parts on card	One
Details	64 GB

Adaptive SoC Logging Memory

An additional 32 Mb flash provides data logging storage accessible via SPI x1 flash over SPI0 interface.

PCIe AUX Power

The Alveo V80 accelerator card has two 8-pin PCIe AUX power connectors, AUX1 and AUX2, that each provide 150W additional power. While the card can operate without either AUX power connected, power to the QSFP cages, DDR, and DIMMs requires at least AUX power connector 1 to be connected. The location of the PCIe AUX power connectors is shown in Figure 4.

***Note*:** The PCIe AUX 8-pin connector is not compatible with an ATX12V/EPS12V power cable source. Ensure that the appropriate PCIe auxiliary power source is available, and not an ATX12V/EPS12V power source. For more details, see Answer Record 72298.

The following table shows the maximum power available with and without AUX 2x4 power cables connected. At a minimum, the 75W PCIe slot power is always used.

Table 23: **Power Availability**

AUX Power Configuration	Maximum Power Available AUX 2x4
No AUX power cable connected[1]	75W
Two AUX power cables connected	300W[2]

Notes:

1. QSFP cages, DDR, and DIMMs are not powered.
2. Maximum card power is limited by the TDP given in Table 1.

Card Thermal and Electrical Protections

Built-in shutdown logic protects the card from damage by removing power to the device when either electrical or thermal limits reach or exceed their respective shutdown thresholds. The voltage regulator module (VRM) monitors the VCCINT current and temperature. When any of the thresholds are exceeded, card power is removed. A cold reboot of the server hosting the card is subsequently necessary to reload the device configuration and re-enumerate the card in the server. The following table lists the card shutdown thermal and electrical thresholds of the VRM. The temperature thresholds apply equally with and without AUX power connected.

Table 24: **Thermal and Electrical Protection Thresholds**

Sensor Description	Card Shutdown Threshold
VCCINT Current	• 60A (no PCIe AUX power) • 180A (one 2x4 PCIe AUX power) • 360A (two 2x4 PCIe AUX power)
VCCINT Temperature	125°C

There is no external system controller on the V80 card that is monitoring voltage and temperature thresholds like previous Alveo cards. While the VRM protects the card from physical damage, precautions must be taken to avoid these limits to prevent a system failure. This includes installing the V80 card in a server that provides sufficient managed airflow as well as preventative in-system monitoring of temperature and voltage via the design on the Versal device or via communication with the host (PCIe in-band or BMC Out of Band).

The Alveo Versal Example Design shows an example of RPU firmware that collects telemetry on the card and can be used as a starting point for a thermal and electrical monitoring solution. It is the user's responsibility, however, to ensure adequate protection measures such as clock throttling are implemented for their application to avoid the system failure resulting from hitting the shutdown thresholds. Refer to the Alveo Versal Example Design documentation for more information on the example implementation.

Mechanical

The Alveo V80 card dimensions, shown in the following table, are compliant with PCIe CEM 5.0 full-height ¾ length card specifications.

Table 25: **Card Dimensions**

Parameter	Dimension
Height	4.376 inch (111.15 mm)
Primary side width	1.37 inch (34.80 mm)
Secondary side width	0.105 inch (2.67 mm)
Length	10.00 inch (254 mm)

Thermal

Operating and Storage Temperature Conditions

The following table provides the operating and storage temperatures, and humidity conditions.

Table 26: **Operating and Storage Temperatures and Humidity Conditions**

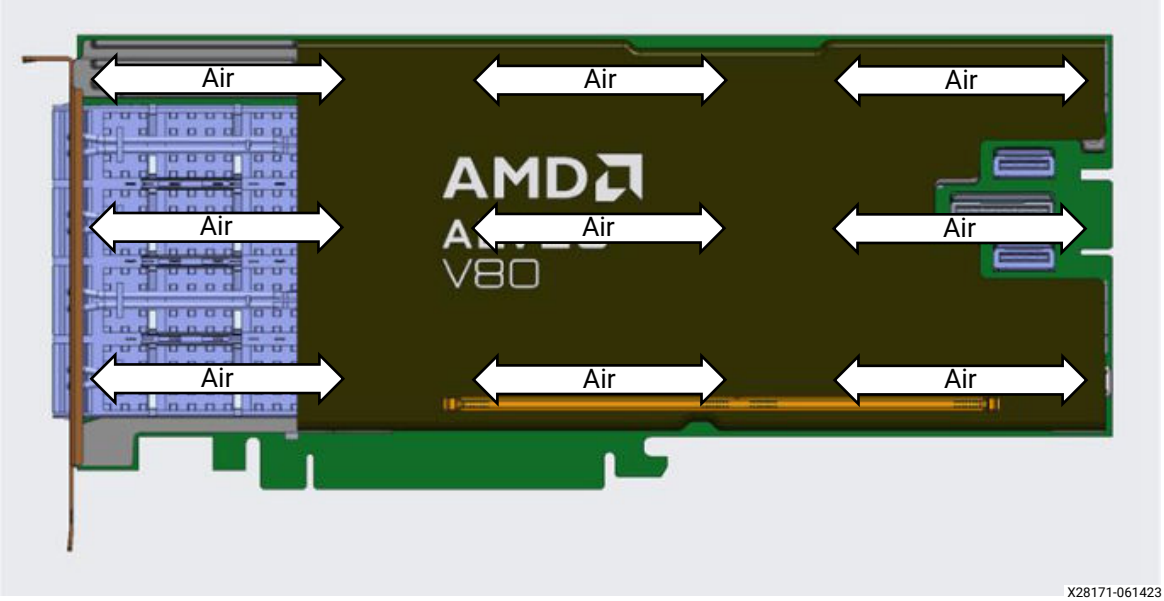
Specification	Condition
Operating temperature	0°C to 45°C
Storage temperature	–40°C to 75°C
Operating humidity, non-condensing	8% to 90%, and a dew point of –12°C
Storage humidity, non-condensing	5% to 95%

Airflow Direction Support

The Alveo V80 card is designed for passive cooling and require an external mechanism to ensure proper airflow for cooling. The card supports bidirectional airflow which includes normal (forward) airflow direction from retainer bracket to I/O bracket and reverse airflow, as illustrated in the following figure.

CAUTION! *Passive cards should not be powered without a forced airflow mechanism in place. Ensure that the minimum airflow requirements are sufficiently met.*

Figure 9: **Supported Airflow Directions for V80 Card**



Operating Conditions

The following tables provide the required airflow rate and airflow speed to the V80 card under various operating conditions. The thermal design power (TDP) of the V80 card might fluctuate depending on factors such as inlet temperature, CFM/LFM airflow conditions, and the card's placement within the server. The LFM/CFM values for the V80 card, as indicated in the following tables, are significantly lower when the QSFP power is at 3.2W.

Table 27: **Inlet Temperature vs Airflow (Out of I/O Bracket) Requirement of PCIe Card Slot (98.4 mm x 40.66 mm) for Normal Flow at Sea Level for 190W TDP with QSFP Power at 4.5W**

Inlet Temperature to the Card (°C)	CFM	LFM	Static Pressure
25	17.8	413	0.24
30	20.8	482	0.30
35	24.6	573	0.38
40	29.9	695	0.52

Table 28: **Inlet Temperature vs Airflow (Out of I/O Bracket) Requirement of PCIe Card Slot (98.4 mm x 40.66 mm) for Normal Flow at 1800m above Sea Level for 190W TDP with QSFP Power at 4.5W**

Inlet Temperature to the Card (°C)	CFM	LFM	Static Pressure
25	19.8	460	0.28
30	23.2	538	0.35
35	27.5	640	0.46

Table 29: **Inlet Temperature vs Airflow (Into I/O Bracket) Requirement of PCIe Card Slot (103.32 mm x 33.49 mm) for Normal Flow at Sea Level for 190W TDP with QSFP Power at 4.5W**

Inlet Temperature to the Card (°C)	CFM	LFM	Static Pressure
25	8.6	230	0.09
30	9.9	267	0.12
35	11.7	313	0.15
40	13.9	373	0.20
45	16.9	453	0.28

Table 30: **Inlet Temperature vs Airflow (Into I/O Bracket) Requirement of PCIe Card Slot (103.32 mm x 33.49 mm) for Normal Flow at 1800m above Sea Level for 190W TDP with QSFP Power at 4.5W**

Inlet Temperature to the Card (°C)	CFM	LFM	Static Pressure
25	9.5	256	0.11
30	11.1	297	0.14
35	13.0	350	0.18
40	15.6	418	0.24
45	18.9	509	0.34

Regulatory and Compliance Information

FCC Class A Products

See this table for a list of the products referred to in this document: Table 1.

***Note*:** These devices are for use with UL Listed Servers or I.T.E.

Regulatory compliance statements are valid for the production version of this product; not for engineering sample (ES) products.

Safety

The following safety standards apply to all products listed in this document.

IEC 62368-1A:2018 (Third edition)

EN 62368-1A:2019 (Third Edition)

UL 62368-1 Ed. 3-2019

CSA C22.2 No. 62368-1A:2019 (Third Edition)

EU LVD Directive 2014/35/EU

EMC Compliance

Class A Products

The following standards apply:

- FCC Part 15 – Radiated & Conducted Emissions (USA)
- CAN ICES-3(A)/NMB-3(A) – Radiated & Conducted Emissions (Canada)
- CISPR 32 – Radiated & Conducted Emissions (International)
- EN55032: 2015 – Radiated & Conducted Emissions (European Union)
- EN55035:2017 – Immunity (European Union)
- EMC Directive 2014/30/EU
- VCCI (Class A)– Radiated & Conducted Emissions (Japan)
- CNS13438 – Radiated & Conducted Emissions (Taiwan)
- CNS 15663 - RoHS (Taiwan)
- AS/NZS CISPR 32 – Radiated and Conducted Emissions (Australia/New Zealand)
- Article 58-2 of Radio Waves Act, Clause 3 (Korea)

Regulatory Compliance Markings

When required, these products are provided with the following product certification markings:

- UL Listed Accessories Mark for the USA and Canada
- CE mark
- UKCA mark
- FCC markings
- VCCI marking
- Australian RCM mark
- Korea MSIP mark

- Taiwan BSMI mark
- German GS mark

FCC Class A User Information

The Class A products listed above comply with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

CAUTION! *This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at their own expense.*

ATTENTION! *Cet équipement a été testé et jugé conforme à la Class A digital device, conformément à la règle 15 du standard FCC. Ces limites sont conçues pour fournir des protections contre des interférences nuisibles lorsque l'équipement est utilisé dans un environnement commercial. Cet équipement génère, utilise et peut émettre des énergies de radio-fréquence et, s'il n'est pas installé et utilisé conformément aux instructions, peut nuire aux communications radio. L'exploitation de cet équipement dans une zone résidentielle est susceptible de causer des interférences nuisibles, auquel cas l'utilisateur peut être tenu de prendre des mesures adéquates à ses propres frais.*

VORSICHT! *Dieses Gerät wurde getestet und entspricht den Grenzwerten für digitale Geräte der Klasse A gemäß Teil 15 der FCC-Bestimmungen. Diese Grenzwerte bieten einen angemessenen Schutz gegen schädliche Interferenzen, wenn das Gerät in einer gewerblichen Umgebung betrieben wird. Dieses Gerät erzeugt und verwendet Hochfrequenzenergie und kann diese abstrahlen. Wenn es nicht gemäß den Anweisungen installiert und verwendet wird, kann dies Funkstörungen verursachen. Der Betrieb dieses Geräts in einem Wohngebiet kann schädliche Interferenzen verursachen. In diesem Fall muss der Benutzer die Interferenz auf eigene Kosten beheben.*

CAUTION! *If the device is changed or modified without permission from AMD, the user may void their authority to operate the equipment.*

ATTENTION! *Si l'appareil est modifié sans l'autorisation d'AMD, l'utilisateur peut annuler son abilité à utiliser l'équipement.*

VORSICHT! *Wenn das Gerät ohne Erlaubnis von AMD geändert wird, kann der Benutzer seine Berechtigung zum Betrieb des Geräts verlieren.*

Canadian Compliance (Industry Canada)

CAN ICES-3(A)/NMB-3(A)

RoHS Compliance

- RoHS Directive 2011/65/EU

- RoHS 3 Directive 2015/863
- SJ/T 11363-2006, 11364-2006, and GB/T 26572-2011 (China RoHS)

VCCI Class A Statement

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この場合には使用者が適切な対策を構ずるよう要求されることがあります。 VCCI-A

KCC Notice Class A (Republic of Korea Only)

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CLASS A device (commercial broadcasting and communication equipment	This device has been appoved by EMC registration. Distributors or users pay attention to this point. This device is usually aimed to be used in other area except at home

BSMI Class A Notice (Taiwan)

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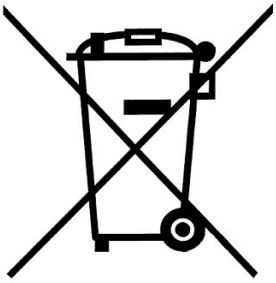
此為甲類資訊技術設備，於居住環境中使用時，可能會造成射頻擾動，在此種情況下，使用者會被要求採取某些適對當的對策。

EU WEEE Logo



[redacted]

Manufacturer Declaration European Community

Manufacturer Declaration

Xilinx declares that the equipment described in this document is in conformance with the requirements of the European Council Directives listed below:

- Low Voltage Directive 2014/35/EU
- EMC Directive 2014/30/EU
- RoHS 3 Directive 2011/65/EU, 2015/863
- China RoHS Declaration: Standards SJ/T 11363-2006, 11364-2006, and GB/T 26572-2011
- REACH Regulation 1907/2006
- POP Regulation 2019/1021

These products follow the provisions of the European Directive 2014/53/EU.

Dette produkt er i overensstemmelse med det europæiske direktiv 2014/53/EU.

Dit product is in navolging van de bepalingen van Europees Directief 2014/53/EU.

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Ce produit est conforme aux exigences de la Directive Européenne 2014/53/EU.

Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie 2014/53/EU.

Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer 2014/53/EU.

Questo prodotto è conforme alla Direttiva Europea 2014/53/EU.

Dette produktet er i henhold til bestemmelsene i det europeiske direktivet 2014/53/EU.

Este produto cumpre com as normas da Diretiva Européia 2014/53/EU.

Este producto cumple con las normas del Directivo Europeo 2014/53/EU.

Denna produkt har tillverkats i enlighet med EG-direktiv 2014/53/EU.

EN 55032 (CISPR 32 Class A) RF Emissions Control

EN 55035:2017 (CISPR 35) Electromagnetic compatibility of multimedia equipment – Immunity requirements

EN 62368-1A:2019 (Third Edition)

EN 50581:2012 - Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances.

CAUTION! *In a domestic environment, Class A products could cause radio interference, in which case the user may be required to take adequate measures.*

ATTENTION! *Dans un environnement domestique, les produits de Classe A peuvent causer des interférences radio, auquel cas l'utilisateur peut être tenu de prendre des mesures adéquates.*

VORSICHT! *In einer häuslichen Umgebung können Produkte der Klasse A Funkstörungen verursachen. In diesem Fall muss der Benutzer möglicherweise geeignete Maßnahmen ergreifen.*

Responsible Party

Xilinx, Inc.
2100 Logic Drive, San Jose, CA 95124
United States of America
Phone: (408) 559-7778

References

These documents provide supplemental material useful with this guide:

1. *Alveo Card Debug Kit User Guide* (UG1538)
2. *Alveo V80 Data Center Accelerator Card Installation Guide* (UG1617)
3. Answer Record 72298
4. Intelligent Platform Management Interface (IPMI) FRU Specification
5. *Alveo Card Out-of-Band Management Specification for Server BMC* (XD038)
6. Alveo Cards GitHub Documentation
7. Answer Record 71752

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
05/08/2024 Version 1.0	
Initial release.	N/A

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