GANB4R8-040CBA

40 V, 4.8 mOhm bi-directional Gallium Nitride (GaN) FET in a 2.1 mm x 2.1 mm Wafer Level Chip-Scale Package (WLCSP)

10 April 2024 Product data sheet

1. General description

The GANB4R8-040CBA is a 40 V, 4.8 mΩ bi-directional Gallium Nitride (GaN) High Electron-Mobility-Transistor (HEMT) in a Wafer Level Chip-Scale (WLCSP) package. It is a normally-off e-mode device offering superior performance.

2. Features and benefits

- Enhancement mode - normally-off power switch
- Bi-directional device
- Ultra high switching speed capability
- Ultra-low on-state resistance
- RoHS, Pb-free, REACH-compliant
- High efficiency and high power density
- Wafer Level Chip-Scale Package (WLCSP) 2.1 mm x 2.1 mm

3. Applications

- High-side load switch
- OVP protection in smart phone USB port
- Power switch circuits
- Stand-by power system

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	drain-drain voltage	-40 °C ≤ T_j ≤ 125 °C	[1]	-	-	40	V
I_D	drain current	V_{GD} = 5 V; T_{mb} = 25 °C	[2] [3]	-	-	20	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Fig. 1		-	-	13	W
T_j	junction temperature			-40	-	125	°C
Static characteristics							
R_{DDon}	drain-drain on-state resistance	V_{GD2} = 5 V; I_{D1} = 10 A; T_j = 25 °C; see Fig. 9 and Fig. 10	[1]	-	4	4.8	mΩ
		V_{GD2} = 5 V; I_{D1} = 10 A; T_j = 125 °C; see Fig. 9 and Fig. 11	[1]	-	7	-	mΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 20 V; V_{GS} = 5 V; T_j = 25 °C; see Fig. 12 and Fig. 13	[2]	-	15.8	-	nC

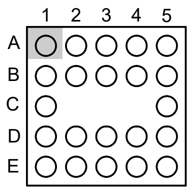
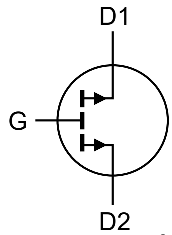
[1] Parameters are understood to apply for either polarity of bias. For example, V_{DD} is the same whether D1 is the source and D2 is the drain or vice versa..

[2] D1 and D2 are symetrical with respect to the gate, G. Either can take the function of source or drain. For datasheet parameters, the source is defined as the terminal, D1 or D2, which has lower potential in the test circuit. The drain is the terminal with the higher potential.

[3] Limited by solder ball.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
A1-A5, D1-D5	D1	drain1	 Transparent top view **WLCSP22_SOT8086**	 aaa-037587
B1-B5, E1-E5	D2	drain2		
C5	G	gate		
C1	NC	not connected		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GANB4R8-040CBA	WLCSP22_SOT8086	WLCSP22, 2.1 mm x 2.1 mm	WLCSP22_SOT8086

7. Marking

Table 4. Marking codes

Type number	Marking code
GANB4R8-040CBA	4R8ACBA

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).T_j = 25 °C unless otherwise stated.

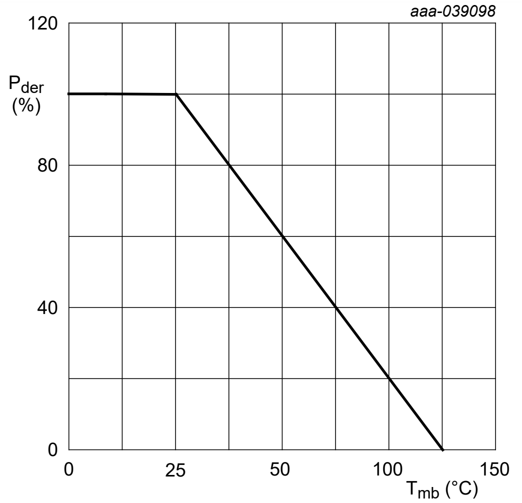
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	drain-drain voltage	-40 °C ≤ T_j ≤ 125 °C	[1]	-	40	V
V_{DG}	drain-gate voltage		[1]	-	40	V
V_{GD}	gate-drain voltage		[1]	-	6	V
I_D	drain current	V_{GD} = 5 V; T_{mb} = 25 °C	[2] [3]	-	20	A
I_{DM}	peak drain current	pulsed; t_p ≤ 300 µs; T_{mb} = 25 °; see Fig. 2	[2] [3]	-	100	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Fig. 1		-	13	W
T_{stg}	storage temperature			-40	150	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-40	125	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C

[1] Parameters are understood to apply for either polarity of bias. For example, VDD is the same whether D1 is the source and D2 is the drain or vice versa.

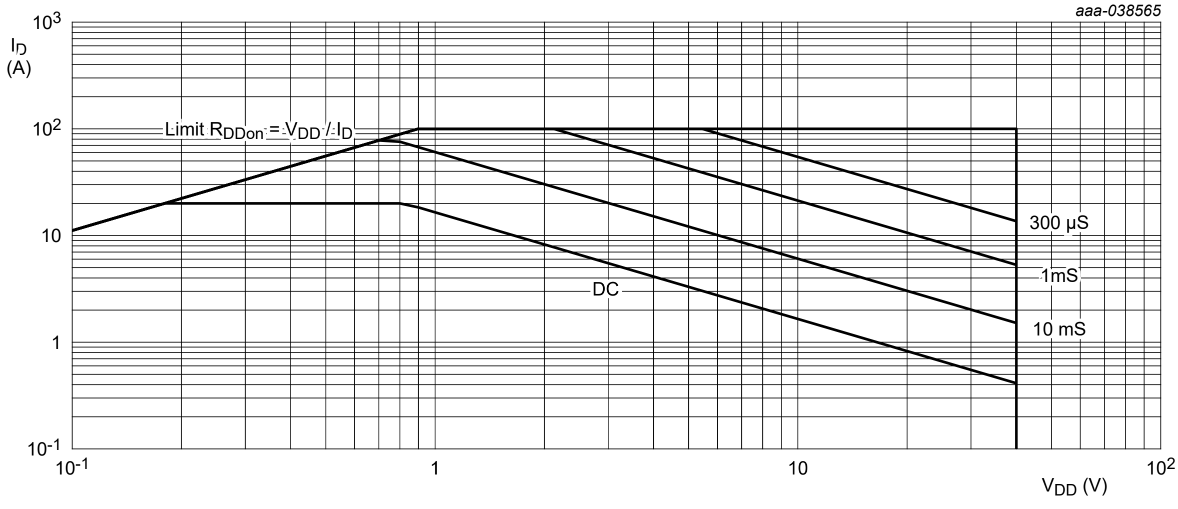
[2] D1 and D2 are symetrical with respect to the gate, G. Either can take the function of source or drain. For datasheet parameters, the source is defined as the terminal, D1 or D2, which has lower potential in the test circuit. The drain is the terminal with the higher potential.

[3] Limited by solder ball.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-drain voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-c)}$	thermal resistance from junction to case		[1]	-	-	12.6	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Fig. 3		-	-	7.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[2]	-	-	59.3	K/W

[1] Thermal junction to top side of package.
[2] $R_{th(j-a)}$ is determined with the device mounted on one square inch of copper pad single layer 2 oz copper on FR4 board.

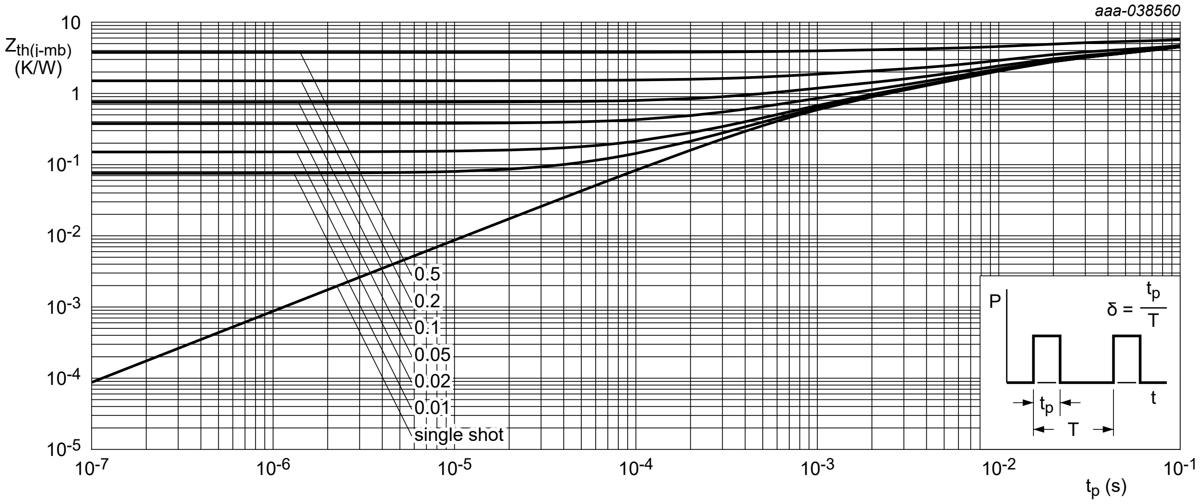


Fig. 3. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

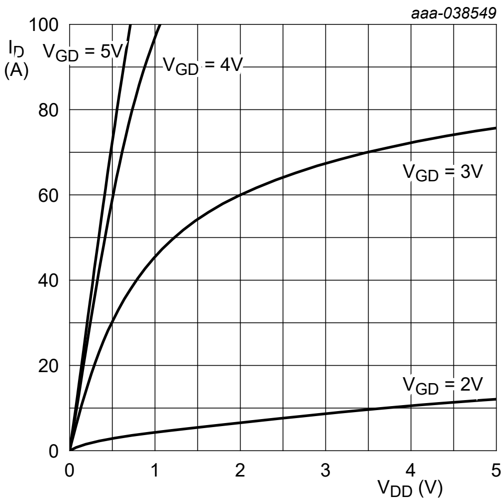
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
BV_{DDS}	drain-drain breakdown voltage	I_{D1D2} = 500 µA; V_{D2} = V_G = 0V; T_j = 25 °C	[1]	40	-	-	V
$V_{GD(th)}$	gate-drain threshold voltage	I_D = 1 mA; V_{D1} = 0 V; V_{D2} = V_G; T_j = 25 °C; see Fig. 8	[1]	0.8	1.35	2.4	V
		I_D = 1 mA; V_{D1} = 0 V; V_{D2} = V_G; T_j = 125 °C; see Fig. 8	[1]	-	1.1	-	V
I_{DDS}	drain-drain leakage current	V_{DD} = 40 V; V_{GD} = 0 V; T_j = 25 °C	[1]	-	1	20	µA
I_{GDS}	gate-drain leakage current	V_{GD} = 5 V; V_{DD} = 0 V; T_j = 85 °C	[1]	-	0.5	3	µA
		V_{GD} = -5 V; V_{DD} = 0 V; T_j = 85 °C		-30	-	-	µA
		V_{GD} = 6 V; V_{DD} = 0 V; T_j = 85 °C		-	5	30	µA
		V_{GD} = -6 V; V_{DD} = 0 V; T_j = 85 °C		-40	-	-	µA
R_{DDon}	drain-drain on-state resistance	V_{GD2} = 5 V; I_{D1} = 10 A; T_j = 25 °C; see Fig. 9 and Fig. 10	[1]	-	4	4.8	mΩ
		V_{GD2} = 5 V; I_{D1} = 10 A; T_j = 125 °C; see Fig. 9 and Fig. 11		-	7	-	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C	[1]	-	4	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DS} = 20 V; V_{GS} = 5 V; I_D = 10 A; T_j = 25 °C; see Fig. 12 and Fig. 13	[2]	-	15.8	-	nC
Q_{GS}	gate-source charge			-	1.9	-	nC
Q_{GD}	gate-drain charge			-	8.6	-	nC
C_{iss}	input capacitance	V_{DS} = 20 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Fig. 14	[2]	-	887	-	pF
C_{oss}	output capacitance			-	381	-	pF
C_{rss}	reverse transfer capacitance			-	226	-	pF
Q_{oss}	output charge	V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25 °C; see Fig. 7	[2][3]	-	12.2	-	nC

[1] Parameters are understood to apply for either polarity of bias. For example, V_{DD} is the same whether D1 is the source and D2 is the drain or vice versa.

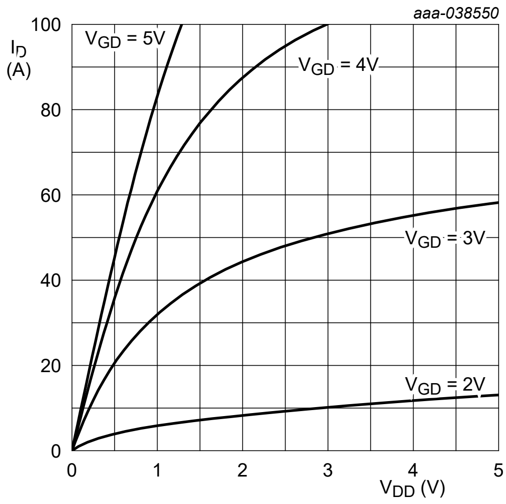
[2] D1 and D2 are symetrical with respect to the gate, G. Either can take the function of source or drain. For datasheet parameters, the source is defined as the terminal, D1 or D2, which has lower potential in the test circuit. The drain is the terminal with the higher potential.

[3] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since Q_r = Q_{oss} + Q_D, and Q_D = 0. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)



T_j = 25 °C

Fig. 4. Output characteristics; drain current as a function of drain-drain voltage; typical values



T_j = 125 °C

Fig. 5. Output characteristics; drain current as a function of drain-drain voltage; typical values

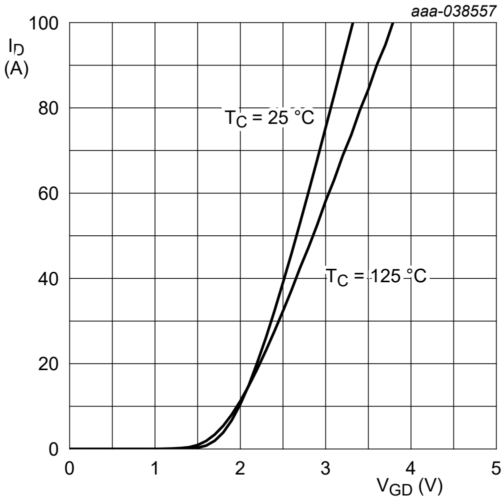
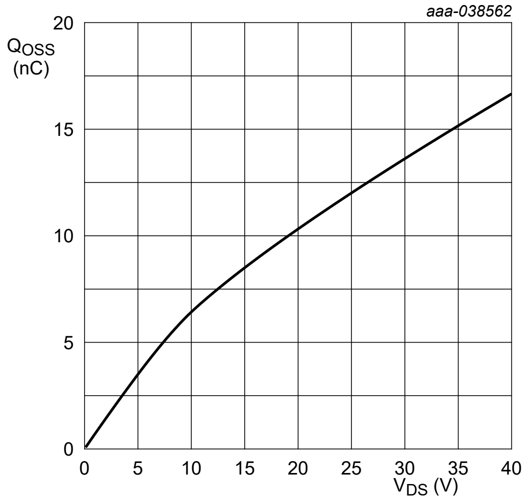
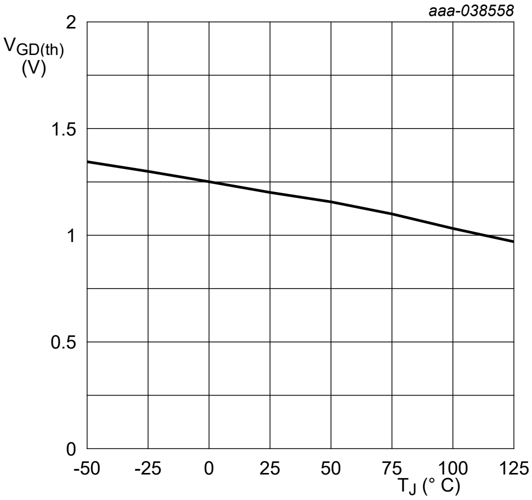


Fig. 6. Transfer characteristics; drain current as a function of gate-drain voltage; typical values



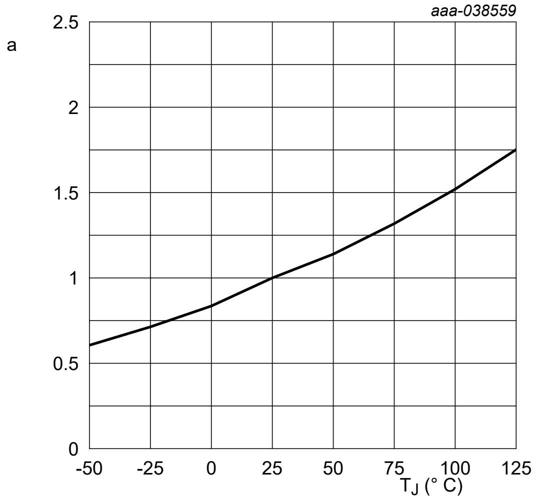
f = 1 MHz

Fig. 7. Output charge as a function of drain-source voltage; typical values



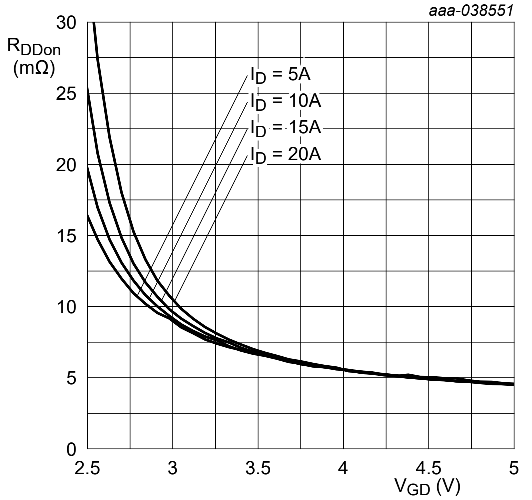
I_D = 1 mA ; V_{DD} = V_{GD}

Fig. 8. Gate-drain threshold voltage as a function of junction temperature



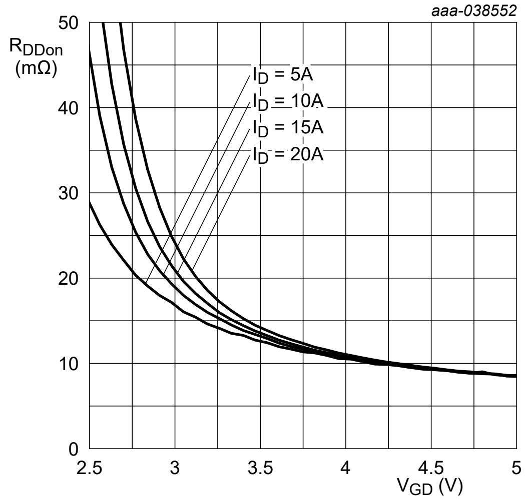
$$a = \frac{R_{DDon}}{R_{DDon}\,(25°C)}$$

Fig. 9. Normalized drain-drain on-state resistance factor as a function of junction temperature; typical values



T_j = 25 °C

Fig. 10. Drain-drain on-state resistance as a function of gate-drain voltage; typical values



T_j = 125 °C

Fig. 11. Drain-drain on-state resistance as a function of gate-drain voltage; typical values

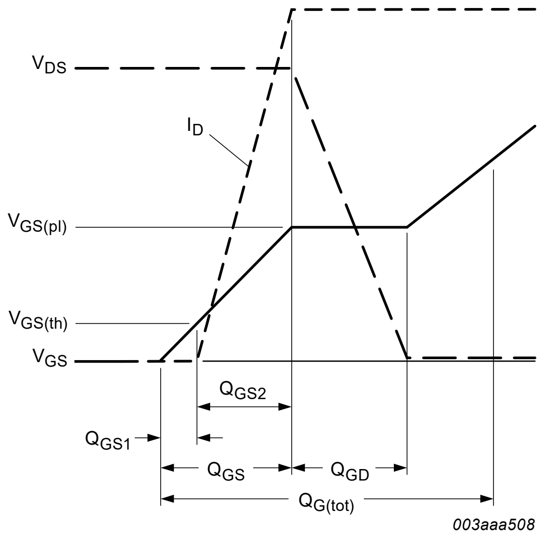
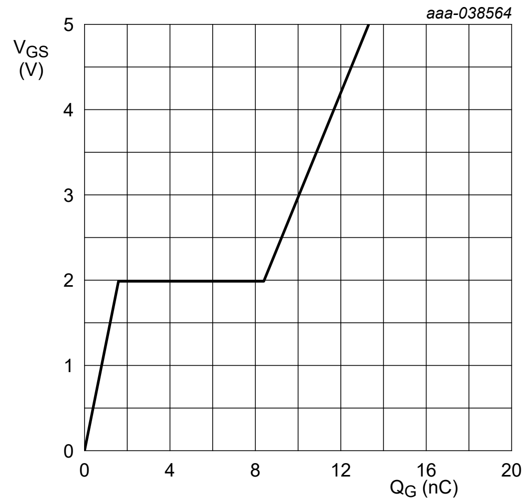
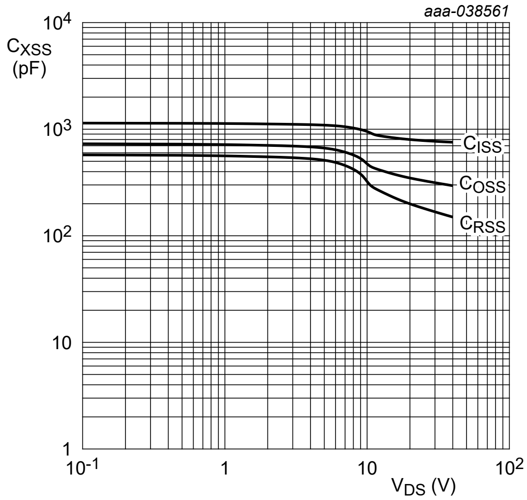


Fig. 12. Gate charge waveform definitions



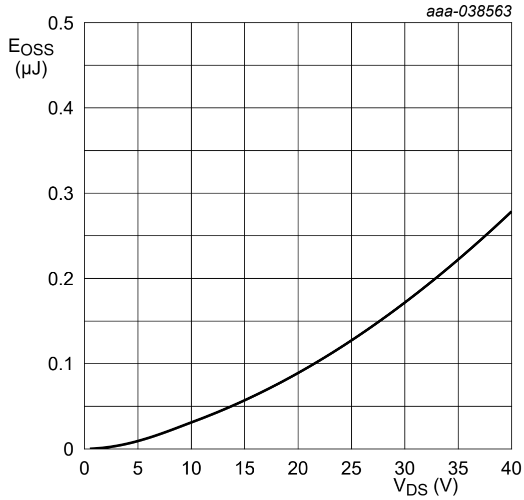
$T_j = 25$ °C; $I_D = 10$ A

Fig. 13. Gate-source voltage as a function of gate charge; typical values



$V_{GD} = 0$ V; f = 1 MHz

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



f = 1 MHz

Fig. 15. C_{OSS} stored energy as a function of drain-source voltage; typical values

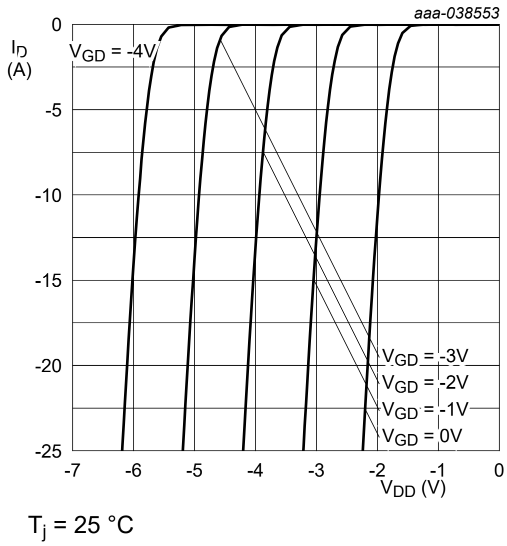


Fig. 16. Reverse drain current as a function of drain-drain voltage; typical values

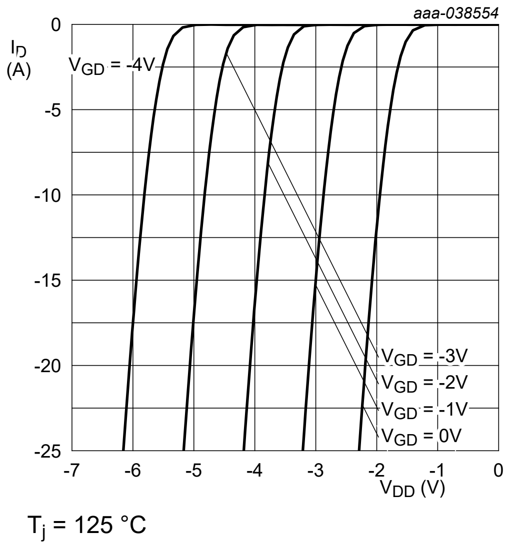


Fig. 17. Reverse drain current as a function of drain-drain voltage; typical values

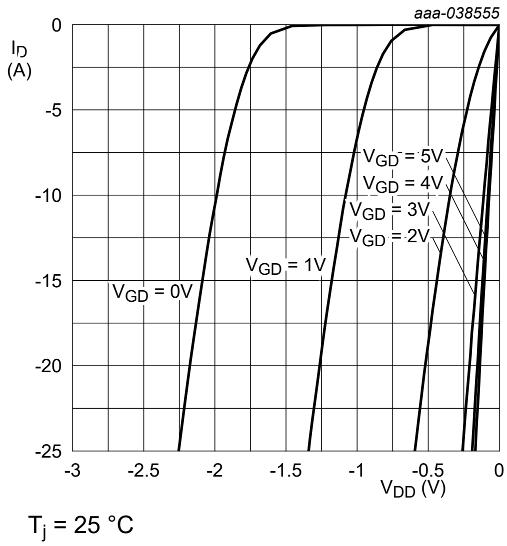


Fig. 18. Reverse drain current as a function of drain-drain voltage; typical values

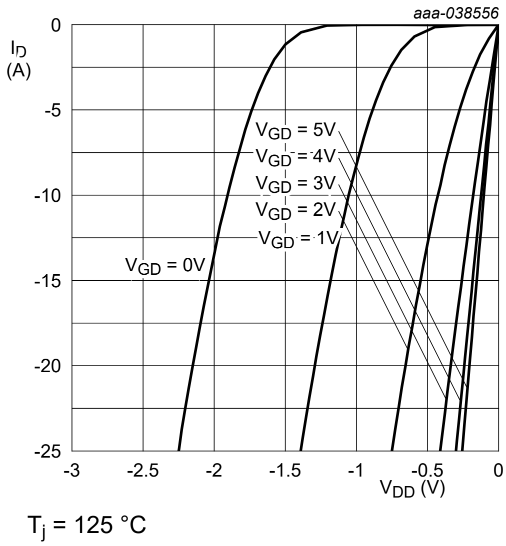
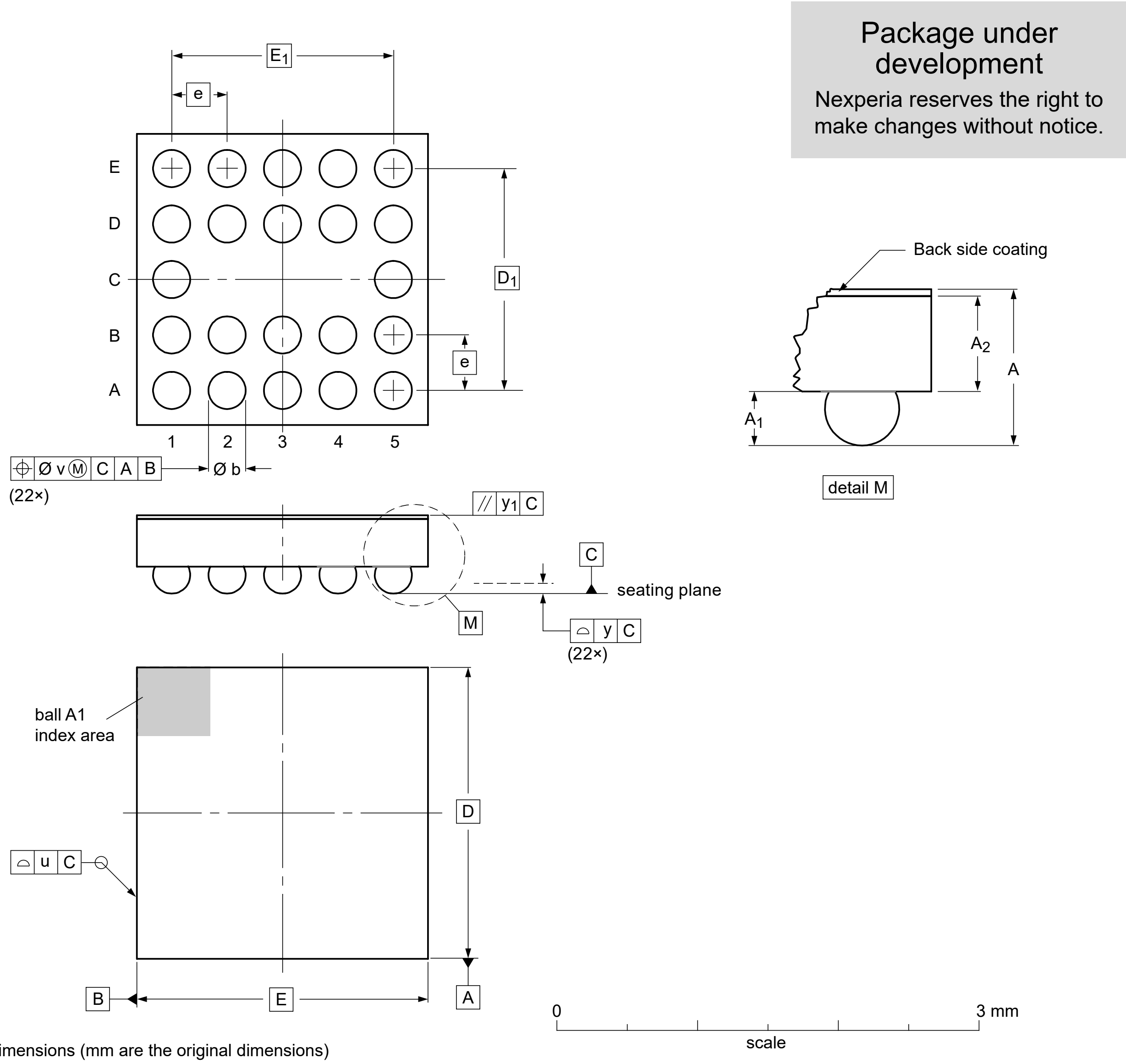


Fig. 19. Reverse drain current as a function of drain-drain voltage; typical values

11. Package outline

Package description line 1
Package description line 2

WLCSP22_SOT8086



Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	A_2	b	D	D_1	E	E_1	e	u	v	y	y_1
mm	max	0.611	0.225	0.358	0.295	2.1 BSC	1.6 BSC	2.1 BSC	1.6 BSC	0.4 BSC	0.025	0.05	0.05	0.1
	nom	0.564	0.195	0.344	0.268									
	min	0.517	0.165	0.330	0.241									

wlcsp22_sot8086_po

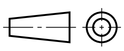
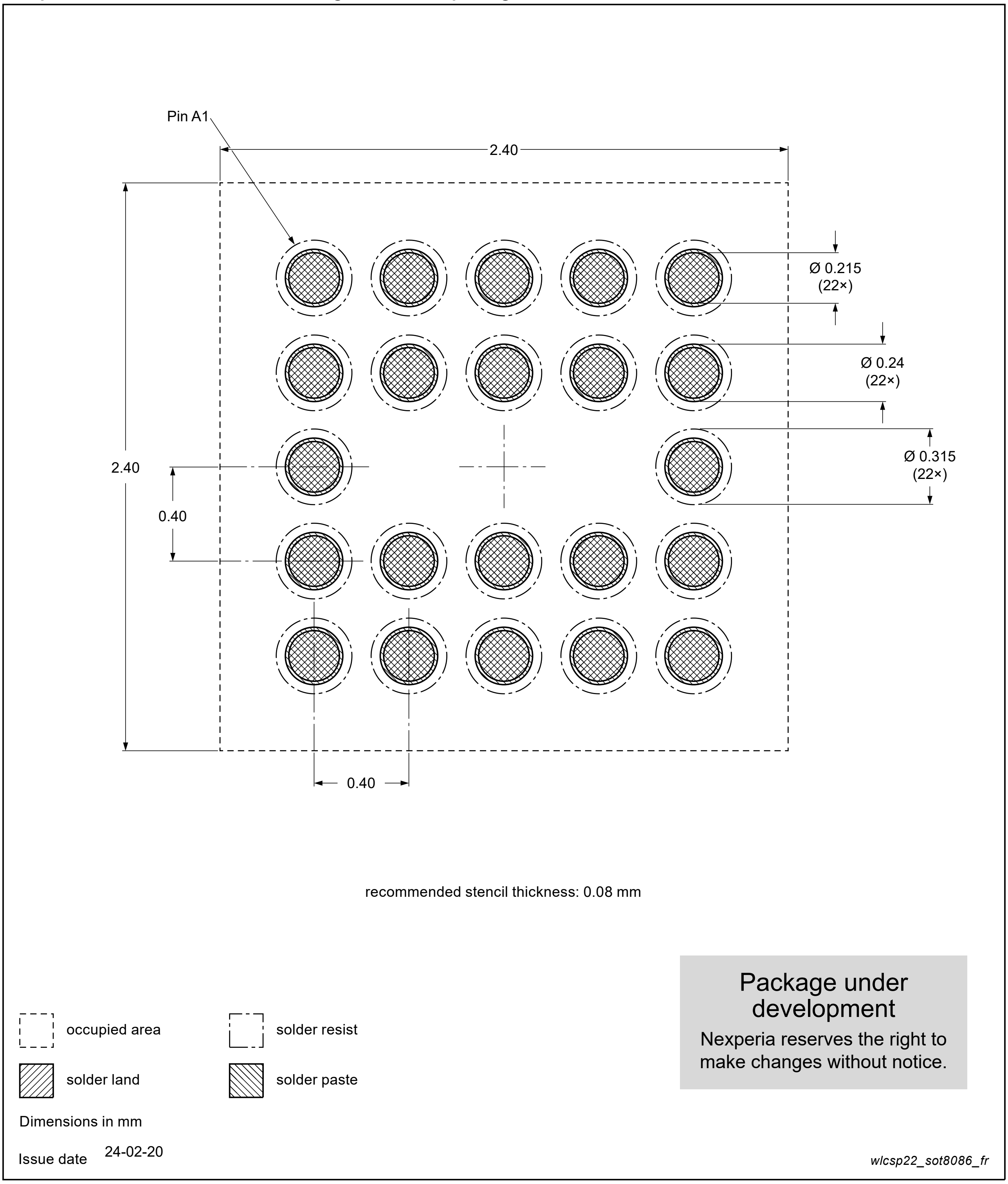
Outline version	References: IEC	References: JEDEC	References: JEITA		European projection	Issue date
WLCSP22_SOT8086		MO-211				24-02-19

Fig. 20. Package outline WLCSP22_SOT8086

12. Soldering

Footprint information for reflow soldering of WLCSP22 package **SOT8086-1**



13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 10 April 2024