For Air-Conditioner Fan Motor

3-Phase Brushless Fan Motor Controller

BD62012BFS

General Description

This controller synthesizes the optimal driving signal from hall sensor signals, and outputs the synthesized signal to control the external power transistor. The replacement is also easy because of its pin compatibility with BD62018BFS. This controller provides optimum motor drive for a wide variety of applications, and enables motor unit standardization.

Key Specifications

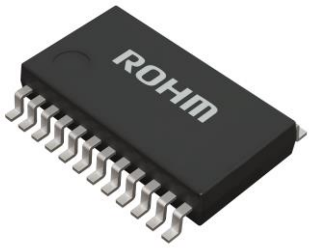
- Duty Control Voltage Range: 2.1V to 5.4V
- Phase Control Range: 0° to +30°
- Maximum Junction Temperature: +150°C

Features

- 150° Commutation Logic
- PWM Control (Upper arm switching)
- Phase control supported from 0° to +30° at 1° intervals
- Rotational Direction Switch
- FG signal output with pulse number switch (4 or 12)
- VREG Output (5V/30mA)
- Protection Circuits Provided: OCP, TSD, UVLO, MLP and the external fault input

Package

Package	W(Typ) x D(Typ) x H(Max)
SSOP-A24	10.0mm x 7.8mm x 2.1mm



SSOP-A24

Applications

- Air Conditioners; Air Purifiers; Water Pumps; Dishwashers; Washing Machines

Typical Application Circuit

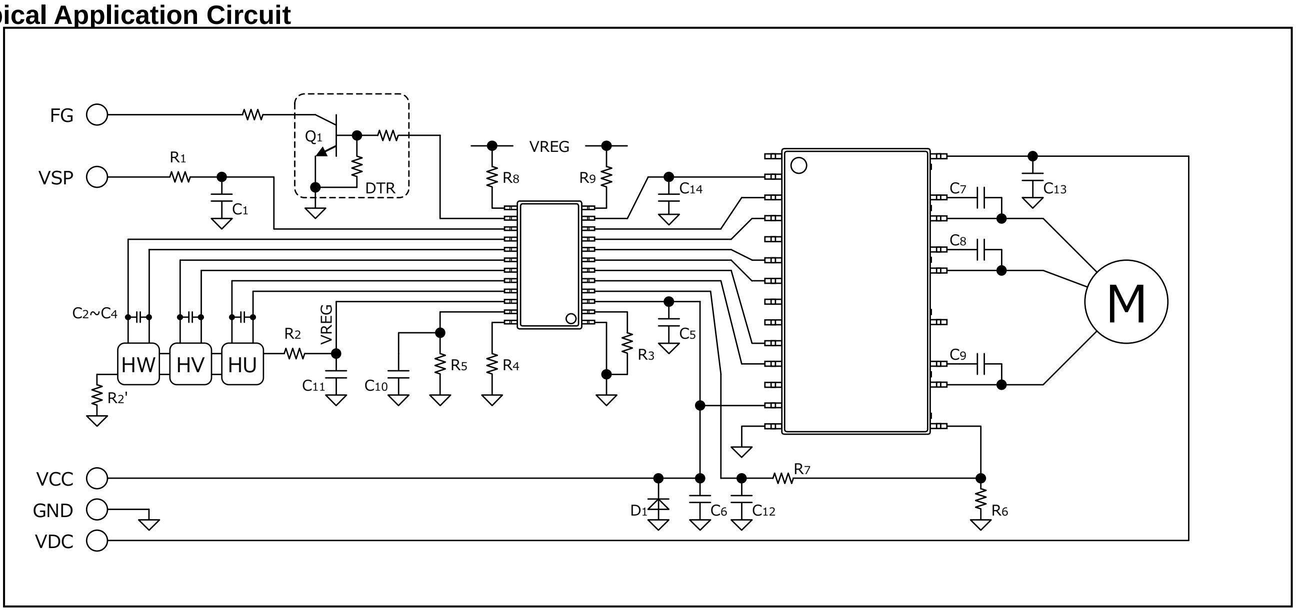


Figure 1. Application Circuit Example

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

Contents

Block Diagram and Pin Configuration

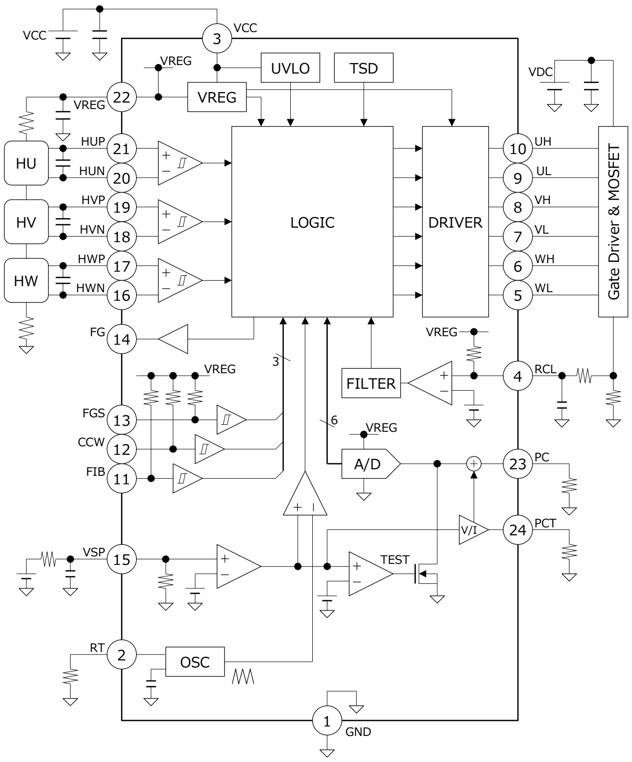


Figure 2. Block Diagram

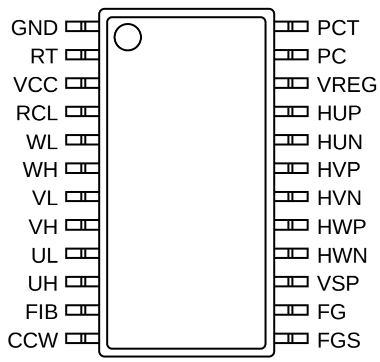


Figure 3. Pin Configuration
(Top View)

Pin Description

No.	Name	Function	No.	Name	Function
1	GND	Signal ground	24	PCT	VSP offset voltage output pin
2	RT	Carrier frequency setting pin	23	PC	Phase control input pin
3	VCC	Power supply	22	VREG	Regulator output
4	RCL	Over current sense pin	21	HUP	Hall input pin phase U+
5	WL	Low side driver output phase W	20	HUN	Hall input pin phase U-
6	WH	High side driver output phase W	19	HVP	Hall input pin phase V+
7	VL	Low side driver output phase V	18	HVN	Hall input pin phase V-
8	VH	High side driver output phase V	17	HWP	Hall input pin phase W+
9	UL	Low side driver output phase U	16	HWN	Hall input pin phase W-
10	UH	High side driver output phase U	15	VSP	Duty control voltage input pin
11	FIB	External fault input (Low active)	14	FG	FG signal output
12	CCW	Direction switch (H:CCW)	13	FGS	FG pulse # switch (H:12, L:4)

Description of Blocks

1. Commutation Logic

When the hall cycle is about 5-Hz or less (e.g. when the motor starts up), the commutation mode is 120° square wave drive with upper and lower switching (no lead angle). The controller monitors the hall cycle, and switches to 150° commutation drive when the hall cycle reaches or exceeds about 5 Hz over four consecutive cycles. Refer to the timing charts in Figures 31 and 32.

Table 1. 120° Commutation (Six-State) Truth Table (CW)

HU	HV	HW	UH	VH	WH	UL	VL	WL
H	L	H	L	PWM	L	H	$\overline{\mathrm{PWM}}$	L
H	L	L	L	L	PWM	H	L	$\overline{\mathrm{PWM}}$
H	H	L	L	L	PWM	L	H	$\overline{\mathrm{PWM}}$
L	H	L	PWM	L	L	$\overline{\mathrm{PWM}}$	H	L
L	H	H	PWM	L	L	$\overline{\mathrm{PWM}}$	L	H
L	L	H	L	PWM	L	L	$\overline{\mathrm{PWM}}$	H

2. Duty Control

The switching duty can be controlled by forcing DC voltage with value from V_{SPMIN} to V_{SPMAX} to the VSP pin. When the VSP voltage is higher than V_{SPTST}, the controller forces PC pin voltage to ground (Testing mode, maximum duty and no lead angle). The VSP pin is pulled down internally by a 200 kΩ resistor. Therefore, note the impedance when setting the VSP voltage with a resistance voltage divider.

3. Carrier Frequency Setting

The carrier frequency setting can be freely adjusted by connecting an external resistor between the RT pin and ground. The RT pin is biased to a constant voltage, which determines the charge current to the internal capacitor. Carrier frequencies can be set within a range from about 16 kHz to 50 kHz. Refer to the formula to the right.

$$f_{OSC}\,[\mathrm{kHz}] = \frac{400}{R_T\,[\mathrm{k\Omega}]}$$

4. FG Signal Output

The FG signal is output from the FG pin. Refer to the timing charts in Figures 31 and 32. The FG signal is generated from the hall signal.
It is recommended to pull up FGS pin to VREG voltage when malfunctioning because of the noise.

FGS	Number of pulse
H	12
L	4

5. Direction of Motor Rotation Setting

The direction of rotation may be switched by the CCW pin. When CCW pin is “H” or open, the motor rotates at CCW direction. When the real direction is different from the setting, the commutation mode is 120° square wave drive (no lead angle). It is recommended to pull up CCW pin to VREG voltage when malfunctioning because of the noise.

CCW	Direction
H	CCW
L	CW

6. Hall Signal Comparator

The hall comparator provides voltage hysteresis to prevent noise malfunctions. The bias current to the hall elements should be set to the input voltage amplitude from the element, at a value higher than the minimum input voltage, $V_{HALLMIN}$. We recommend connecting a ceramic capacitor with value from 100 pF to 0.01 µF, between the differential input pins of the hall comparator. Note that the bias to hall elements must be set within the common mode input voltage range V_{HALLCM}.

Description of Blocks - continued

7. Output Duty Pulse Width Limiter

Pulse width duty is controlled during PWM switching in order to ensure the operation of external power transistor. The controller doesn't output pulse of less than t_{MIN} (0.8µs minimum). Dead time is forcibly provided to prevent external power transistors from turning-on simultaneously in upper and lower side in driver output (for example, UH and UL) of each arm. This will not overlap the minimum time t_{DT} (1.6µs minimum). Because of this, the maximum duty of 120° square wave drive at start up is 90% (typical).

8. Phase Control Setting

The driving signal phase can be advanced to the hall signal for phase control. The lead angle is set by forcing DC voltage to the PC pin. The input voltage is converted digitally by a 6-bit A/D converter, in which internal VREG voltage is assumed to be full-scale, and the converted data is processed by a logic circuit. The lead angle can be set from 0° to +30° at 1° intervals, and updated fourth hall cycle of phase W falling edge. Phase control function only operates at sinusoidal commutation mode. However, the controller forces PC pin voltage to ground (no lead angle) during testing mode. The VSP offset voltage (Figure 27) is buffered to PCT pin, to connect an external resistor between PCT pin and ground. The internal bias current is determined by PCT voltage and the resistor value (V_{PCT} / R_{PCT}), and mixed to PC pin. As a result, the lead angle setting is followed with the duty control voltage, and the performance of the motor can be improved. Select the R_{PCT} value from 50 kΩ to 200 kΩ in the range on the basis of 100 kΩ, because the PCT pin current capability is a 100 µA or less.

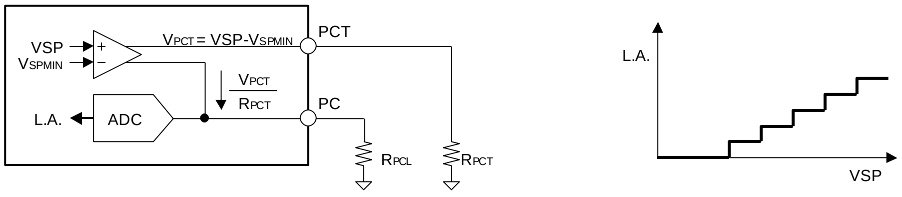


Figure 4. Phase Control Setting Example 1

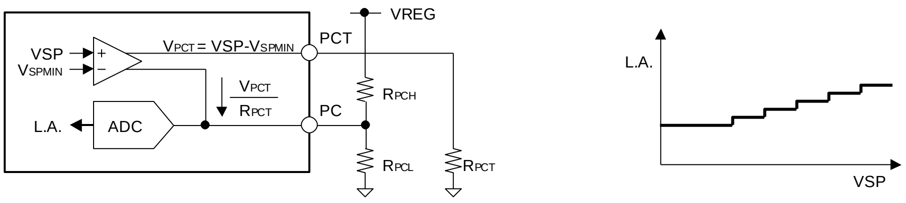


Figure 5. Phase Control Setting Example 2

9. Overcurrent Protection (OCP) Circuit

The over current protection circuit can be activated by connecting a low value resistor for current detection between the external output stage ground and the controller IC ground. When the RCL pin voltage reaches or surpasses the threshold value, the controller forces all the upper switching arm inputs low (UH, VH, WH = L, L, L), thus initiating the overcurrent protection operation. When the RCL pin voltage swings below the ground, it is recommended to insert a resistor (1.5 kΩ or more) between RCL pin and current detection resistor to prevent malfunction. Since this protection circuit is not a latch type, it returns to normal operation (synchronizing with the carrier frequency) once the RCL pin voltage falls below the threshold voltage. A filter is built into the overcurrent detection circuit to prevent malfunctions, and does not activate when a short pulse of less than t_{RCL} is present at the input.

Description of Blocks - continued

10. Under Voltage Lock Out (UVLO) Circuit

To secure the lowest power supply voltage necessary to operate the controller, and to prevent under voltage malfunctions, an UVLO circuit is built into this controller. When the power supply voltage falls to V_{UVL} and below, the controller forces all driver outputs low. When the voltage rises to V_{UVH} and above, the UVLO circuit ends the lock out operation and returns the chip to normal operation.
The voltage monitor circuit (4.0V nominal) is built-in for the VREG voltage. Therefore, the UVLO circuit does not release operation when the VREG voltage rising is delayed behind the VCC voltage rising even if VCC voltage becomes V_{UVH} or more.

11. Thermal Shutdown (TSD) Circuit

The TSD circuit operates when the junction temperature of the controller exceeds the preset temperature (175°C nominal). At this time, the controller forces all driver outputs low. Since thermal hysteresis is provided in the TSD circuit, the chip returns to normal operation when the junction temperature falls below the preset temperature (150°C nominal). The TSD circuit is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation in the presence of extreme heat. Do not continue to use the IC after the TSD circuit is activated, and do not use the IC in an environment where activation of the circuit is assumed.

12. Motor Lock Protection (MLP) Circuit

When the controller detects the motor locking during fixed time of 4 seconds nominal when each edge of the hall signal doesn't input either, the controller forces all driver outputs low under a fixed time 20 seconds nominal, and self-returns to normal operation. This circuit is enabled if the voltage force to VSP is over the duty minimum voltage V_{SPMIN}, and note that the motor cannot start up when the controller doesn’t detect the motor rotation by the minimum duty control.

13. External Fault Signal Input Pin (FIB pin, Low Active)

The FIB pin can force all controller driver outputs low at any time. The FIB pin is pulled up to VREG internally by a 100 kΩ resistor. Therefore, an open drain output can be connected directly. It is recommended to pull up FIB pin to VREG voltage when this function is not used and malfunctioning because of the noise.

14. Hall Signal Wrong Input Detection

Hall element abnormalities may cause incorrect inputs that vary from the normal logic. When all hall input signals go high or low, the hall signal wrong input detection circuit forces all driver outputs low. And when the controller detects the abnormal hall signals continuously for four times or more motor rotation, the controller forces all driver outputs low and latches the state. It is released if the duty control voltage VSP is forced to ground level once.

15. VREG Output

The internal voltage regulator VREG is output for the bias of the hall element and the phase control setting. However, when using the VREG function, be aware of the I_{OMAX} value. If a capacitor is connected to the ground in order to stabilize output, a value of 1 µF or more should be used. In this case, be sure to confirm that there is no oscillation in the output.

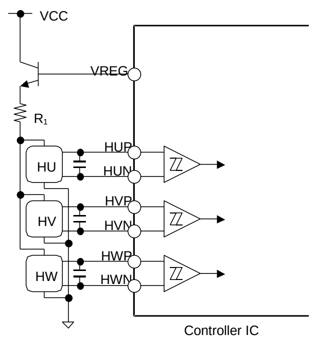


Figure 6. VREG Output Pin Application Example

Controller Outputs and Operation Mode Summary

<table>
<tr><td rowspan="2">Conditions</td><td>Detected direction</td><td colspan="2">Forward (CW:U~V~W, CCW:U~W~V)</td><td colspan="2">Reverse (CW:U~W~V, CCW:U~V~W)</td></tr>
<tr><td>Hall sensor frequency</td><td>< 5Hz</td><td>5Hz ≤</td><td>< 5Hz</td><td>5Hz ≤</td></tr>
<tr><td rowspan="3">Normal operation</td><td>VSP < V_{SPMIN}
(Duty off)</td><td colspan="4">Upper and lower arm off</td></tr>
<tr><td>V_{SPMIN} < VSP < V_{SPMAX}
(Control range)</td><td rowspan="2">120°
Upper and lower switching</td><td>150°
Upper switching</td><td rowspan="2">120°
Upper and lower switching</td><td rowspan="2">120°
Upper switching</td></tr>
<tr><td>V_{SPTST} < VSP
(Testing mode)</td><td>150°
Upper switching
(No lead angle)</td></tr>
<tr><td rowspan="6">Protect operation</td><td>Overcurrent</td><td colspan="2">Upper arm off</td><td colspan="2">Upper and lower arm off</td></tr>
<tr><td>TSD</td><td colspan="4" rowspan="4">Upper and lower arm off</td></tr>
<tr><td>External input</td></tr>
<tr><td>UVLO</td></tr>
<tr><td>Motor lock</td></tr>
<tr><td>Hall sensor abnormally</td><td colspan="4">Upper and lower arm off and latch</td></tr>
</table>

(Note) The controller monitors both edges of three hall sensors for detecting period.
(Note) Phase control function only operates at sinusoidal commutation mode. However, the controller forces no lead angle during the testing mode.

Absolute Maximum Ratings (Tj=25°C)

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	20 *(Note 1)*	V
Duty Control Voltage	V_{SP}	-0.3 to +20	V
All Others	$V_{I/O}$	-0.3 to +5.5	V
Driver Outputs	$I_{OMAX(OUT)}$	±15 *(Note 1)*	mA
Monitor Output	$I_{OMAX(FG)}$	±5 *(Note 1)*	mA
VREG Output	$I_{OMAX(VREG)}$	-40 *(Note 1)*	mA
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

(Note) All voltages are with respect to ground unless otherwise specified.

(Note 1) Do not, however, exceed ASO.

Caution1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 4)*	2s2p *(Note 5)*	
SSOP-A24				
Junction to Ambient	θ_{JA}	104.4	54.1	°C/W
Junction to Top Characterization Parameter *(Note 3)*	Ψ_{JT}	7	6	°C/W

(Note 2) Based on JESD51-2A(Still-Air).
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3.
(Note 5) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70μm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70μm	74.2mm x 74.2mm	35μm	74.2mm x 74.2mm	70μm

Recommended Operating Conditions (Tj=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	10	15	18	V
Junction Temperature	Tj	-40	-	+110	°C

(Note) All voltages are with respect to ground unless otherwise specified.

Electrical Characteristics (Unless otherwise specified V_{CC}=15V and Tj=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Supply						
Supply Current	I_{CC}	1.3	2.5	5.0	mA	
VREG Voltage	V_{REG}	4.5	5.0	5.5	V	I_O=-30mA
Driver outputs						
Output High Voltage	V_{OH}	V_{REG}-0.60	V_{REG}-0.20	V_{REG}	V	I_O=-5mA
Output Low Voltage	V_{OL}	0	0.14	0.60	V	I_O=5mA
Dead Time	t_{DT}	1.6	2.0	2.4	µs	
Minimum Pulse Width	t_{MIN}	0.8	1.0	1.2	µs	
Hall Comparators						
Input Bias Current	I_{HALL}	-2.0	-0.1	+2.0	µA	V_{IN}=0 V
Common Mode Input	V_{HALLCM}	0	-	V_{REG}-1.5	V	
Minimum Input Level	$V_{HALLMIN}$	50	-	-	mV_{p-p}	
Hysteresis Voltage P	$V_{HALLHY+}$	5	13	23	mV	
Hysteresis Voltage N	$V_{HALLHY-}$	-23	-13	-5	mV	
Duty Control						
Input Bias Current	I_{SP}	15	25	35	µA	V_{IN}=5V
Duty Minimum Voltage	V_{SPMIN}	1.8	2.1	2.4	V	
Duty Maximum Voltage	V_{SPMAX}	5.1	5.4	5.7	V	
Testing Operation Range	V_{SPTST}	8.2	-	18	V	
Minimum Output Duty	D_{MIN}	1.2	1.8	2.4	%	f_{OSC}=18kHz
Maximum Output Duty	D_{MAX}	92	95	98	%	f_{OSC}=18kHz
Mode switch and the external input - FGS, CCW and FIB						
Input Bias Current	I_{IN}	-70	-50	-30	µA	V_{IN}=0V
Input High Voltage	V_{INH}	3	-	VREG	V	
Input Low Voltage	V_{INL}	0	-	1	V	
Hysteresis Voltage	V_{INHY}	0.2	0.5	0.8	V	
Monitor Output - FG						
Output High Voltage	V_{MONH}	V_{REG}-0.40	V_{REG}-0.08	V_{REG}	V	I_O=-2mA
Output Low Voltage	V_{MONL}	0	0.06	0.40	V	I_O=2mA
Overcurrent protection						
Input Bias Current	I_{RCL}	-30	-20	-10	µA	V_{IN}=0V
Threshold Voltage	V_{RCL}	0.48	0.50	0.52	V	
Noise Masking Time	t_{RCL}	0.8	1.0	1.2	µs	
Phase Control						
Minimum Lead Angle	P_{MIN}	-	0	1	deg	V_{PC}=0V
Maximum Lead Angle	P_{MAX}	29	30	-	deg	$V_{PC}=1/2 \cdot V_{REG}$
Carrier Frequency Oscillator						
Carrier Frequency	f_{OSC}	16	18	20	kHz	R_T=22kΩ
Under Voltage Lock Out						
Release Voltage	V_{UVH}	8.5	9.0	9.5	V	
Lockout Voltage	V_{UVL}	7.5	8.0	8.5	V	
Hysteresis Voltage	V_{UVHY}	0.5	1.0	1.5	V	

(Note) All voltages are with respect to ground unless otherwise specified.

Typical Performance Curves (Reference Data)

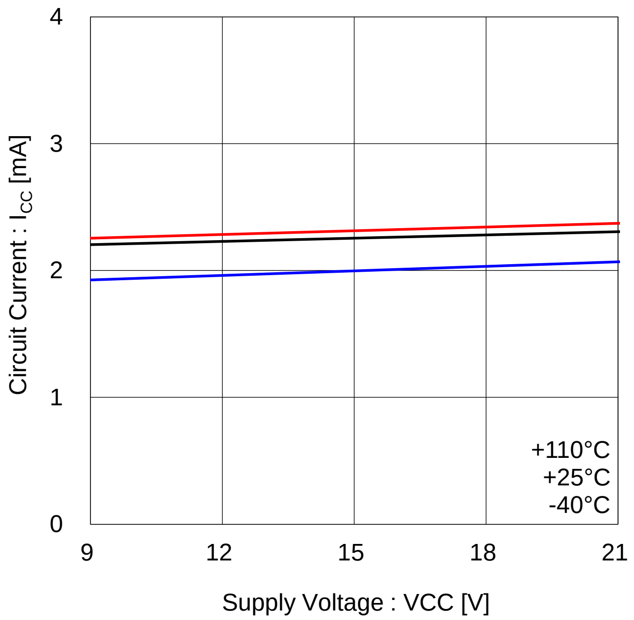


Figure 7. Quiescence Current

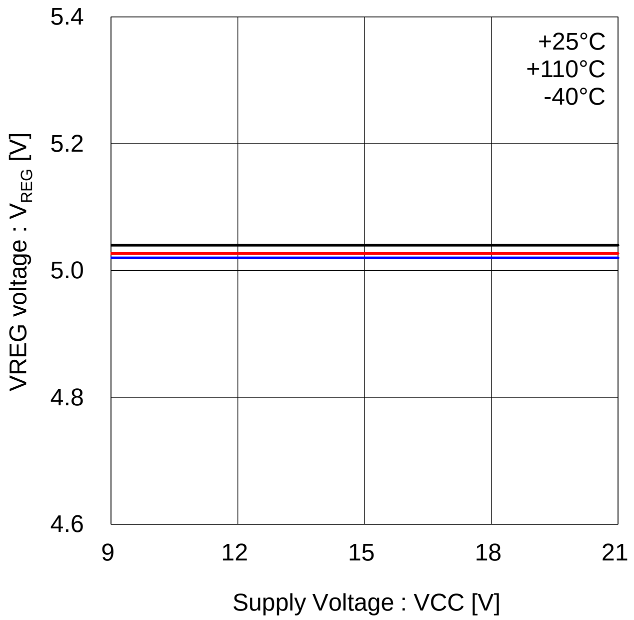


Figure 8. VREG vs VCC

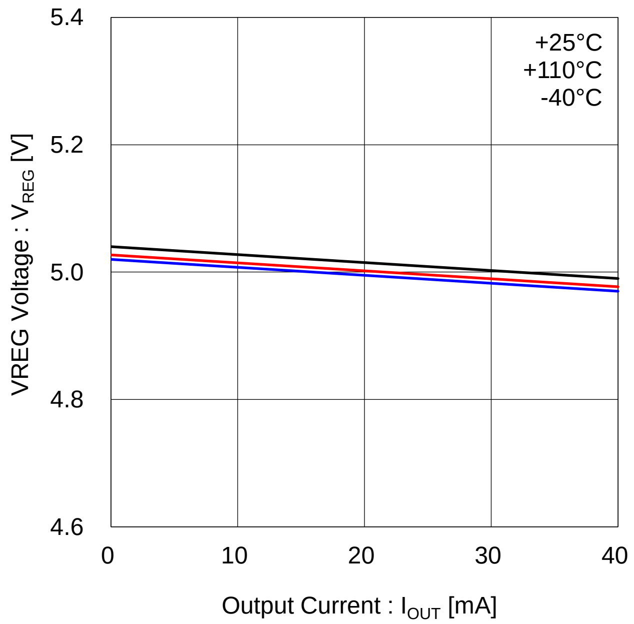


Figure 9. VREG Drive Capability

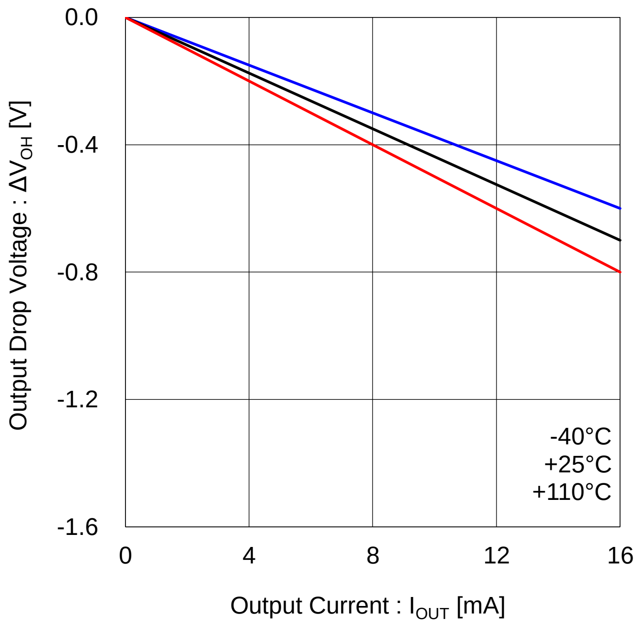


Figure 10. High Side Output Voltage
(XH, XL)

Typical Performance Curves (Reference Data) - continued

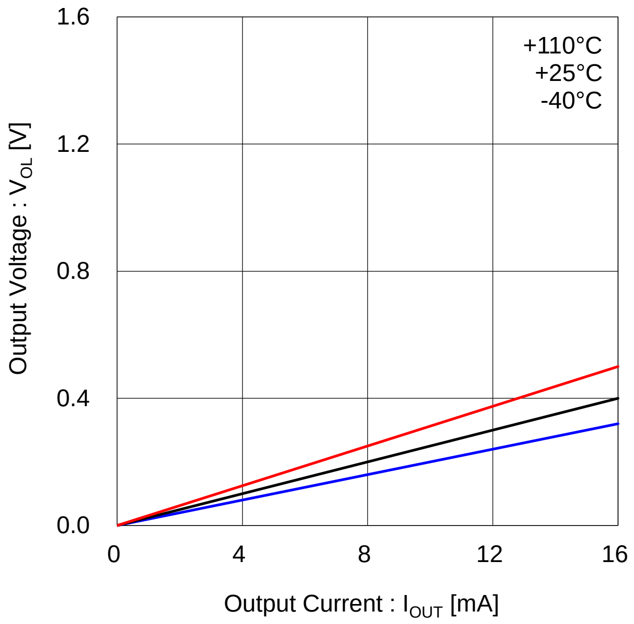


Figure 11. Low Side Output Voltage
(XH, XL)

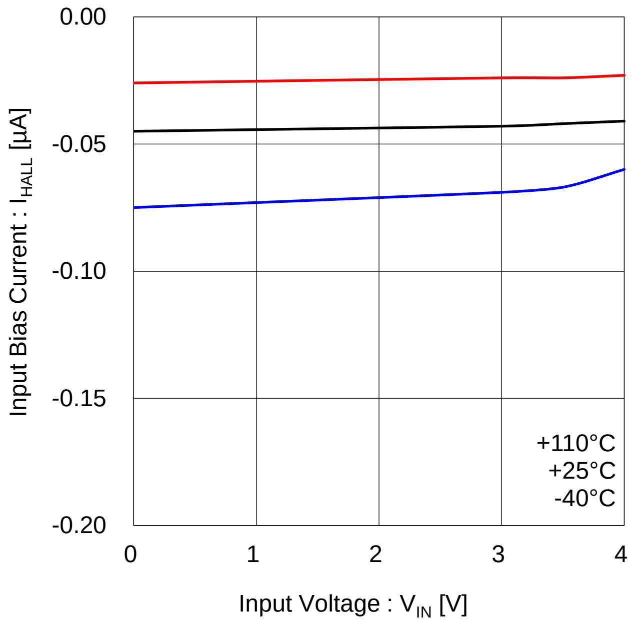


Figure 12. Hall Comparator Input Bias Current
(HXP, HXN)

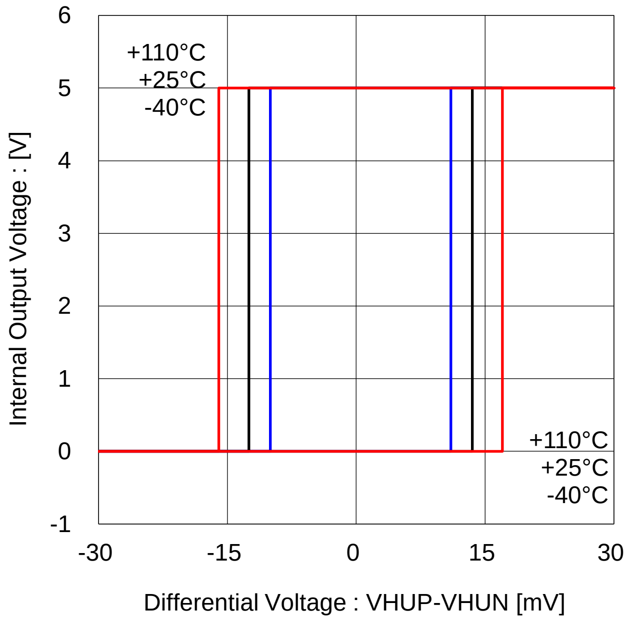


Figure 13. Hall Comparator Hysteresis Voltage

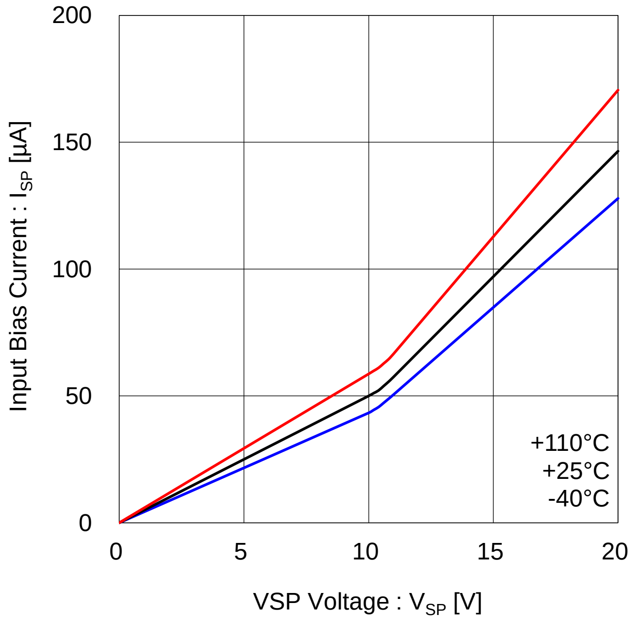


Figure 14. VSP Input Bias Current

Typical Performance Curves (Reference Data) - continued

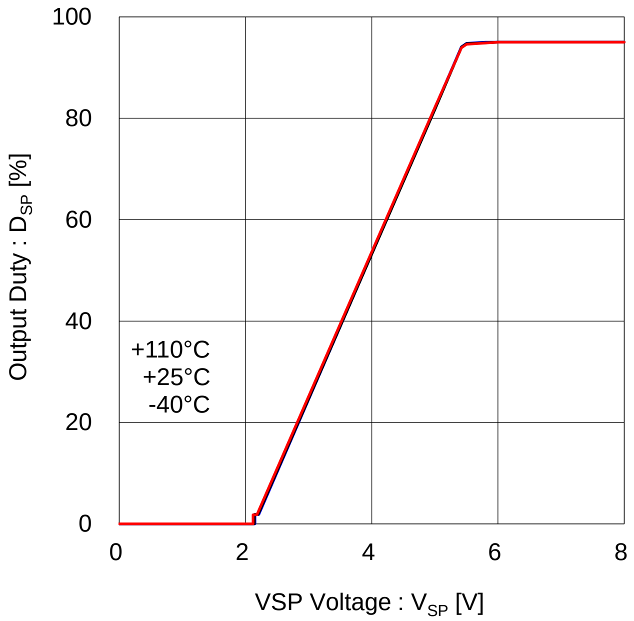


Figure 15. Output Duty vs VSP Voltage

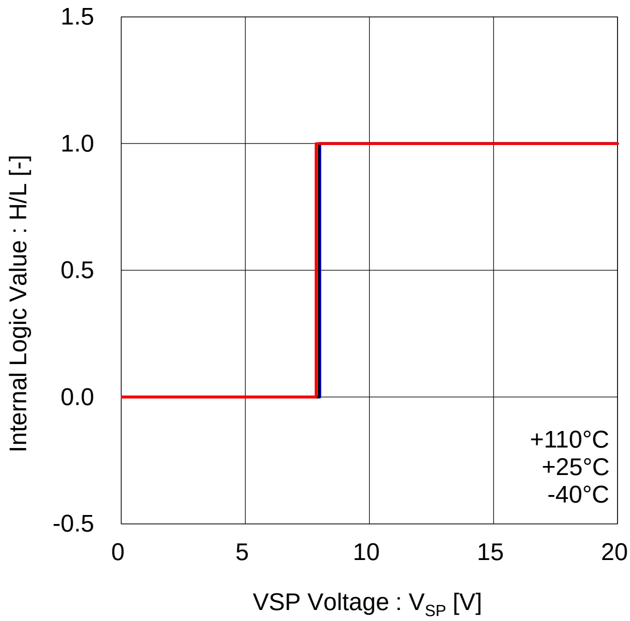


Figure 16. Testing Mode Threshold Voltage

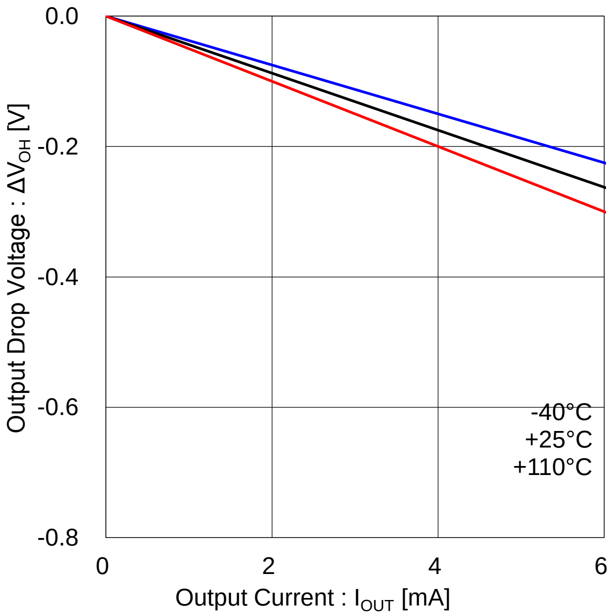


Figure 17. High Side Output Voltage (FG)

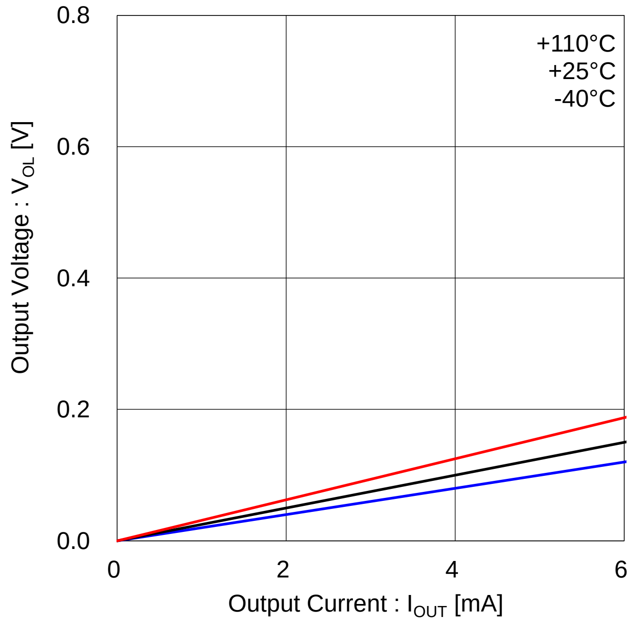


Figure 18. Low Side Output Voltage (FG)

Typical Performance Curves (Reference Data) - continued

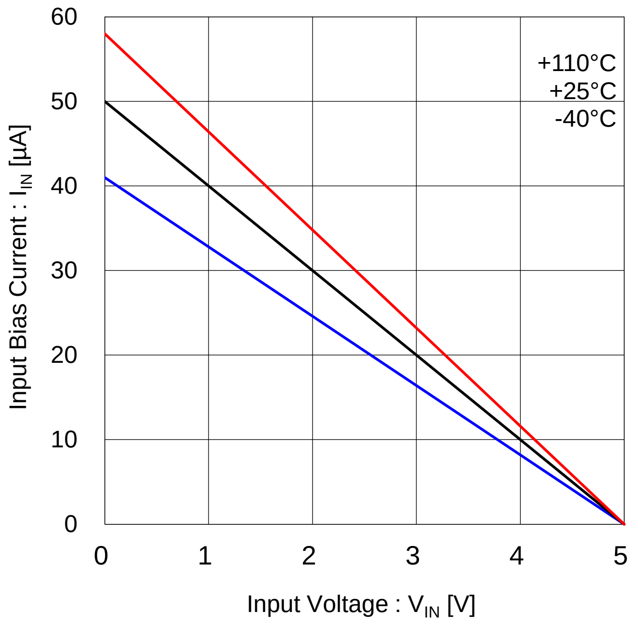


Figure 19. Input Bias Current
(CCW, FIB)

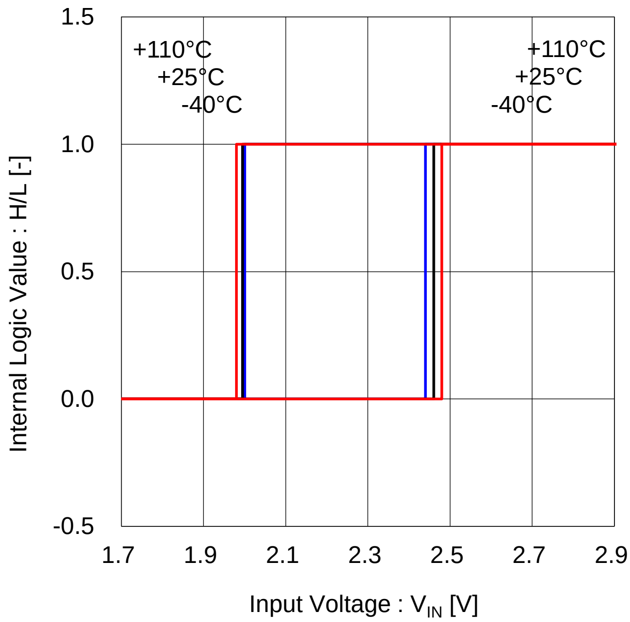


Figure 20. Input Threshold Voltage
(CCW, FIB)

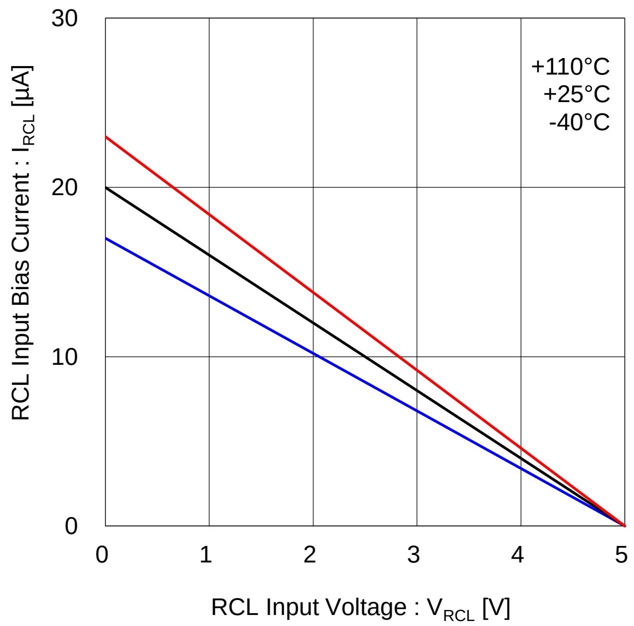


Figure 21. RCL Input Bias Current

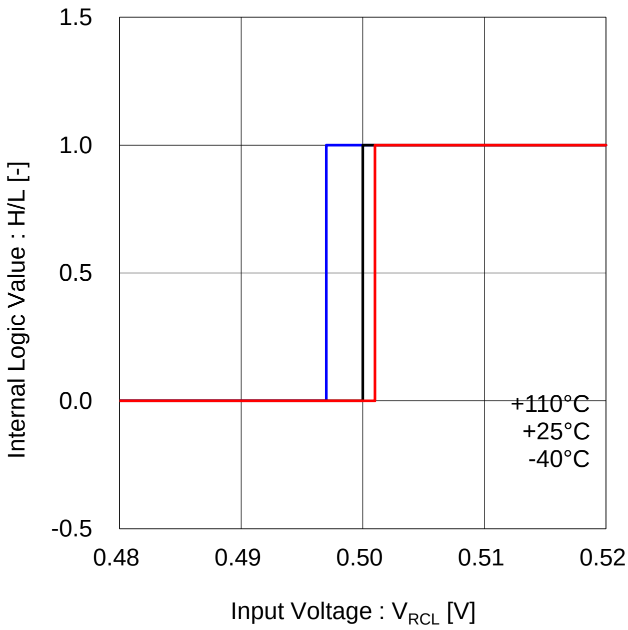


Figure 22. RCL Input Threshold Voltage

Typical Performance Curves (Reference Data) - continued

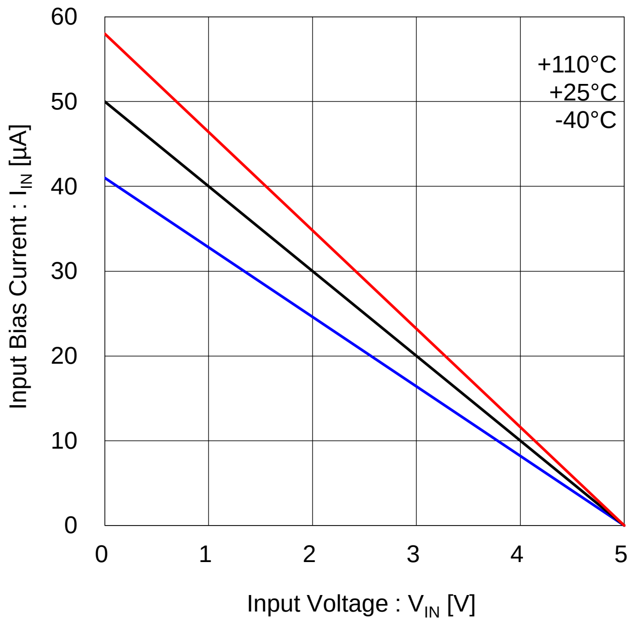


Figure 23. Input Bias Current
(FGS)

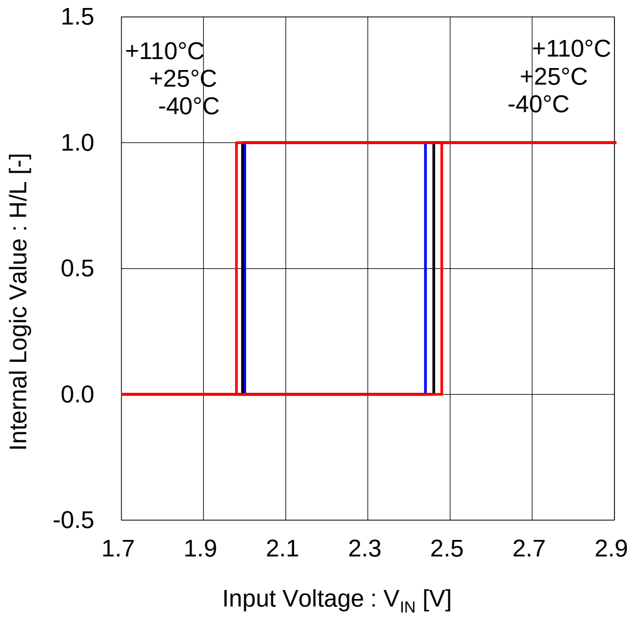


Figure 24. Input Threshold Voltage
(FGS)

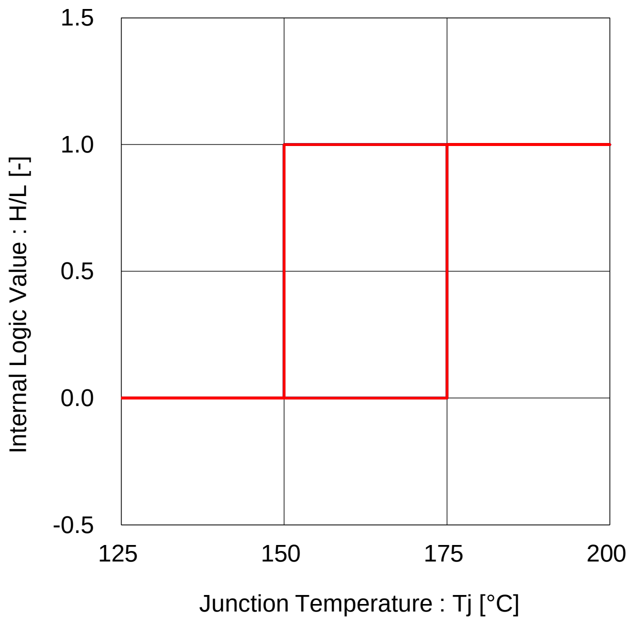


Figure 25. Thermal Shut Down

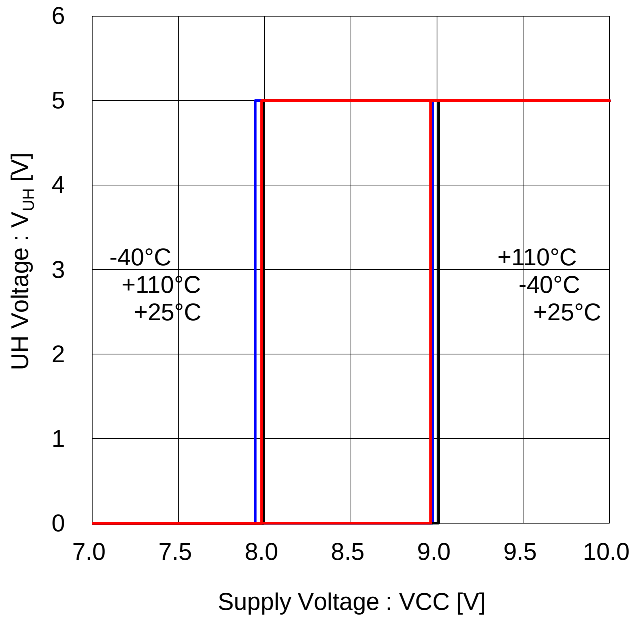


Figure 26. Under Voltage Lock Out
(VCC)

Typical Performance Curves (Reference Data) - continued

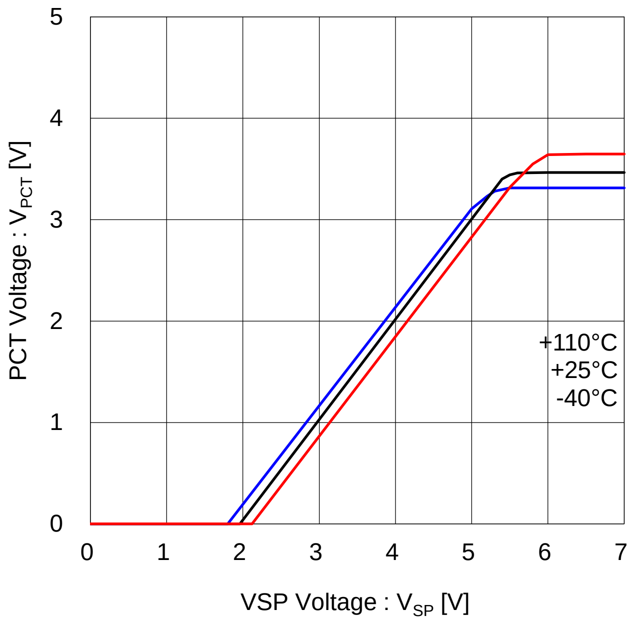


Figure 27. VSP vs PCT Offset Voltage

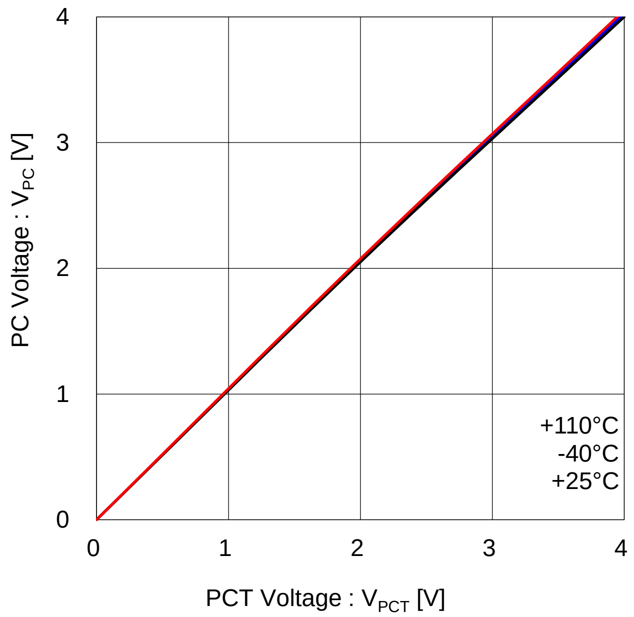


Figure 28. PCT vs PC Linearity
($R_{PCT}=R_{PC}=100k\Omega$)

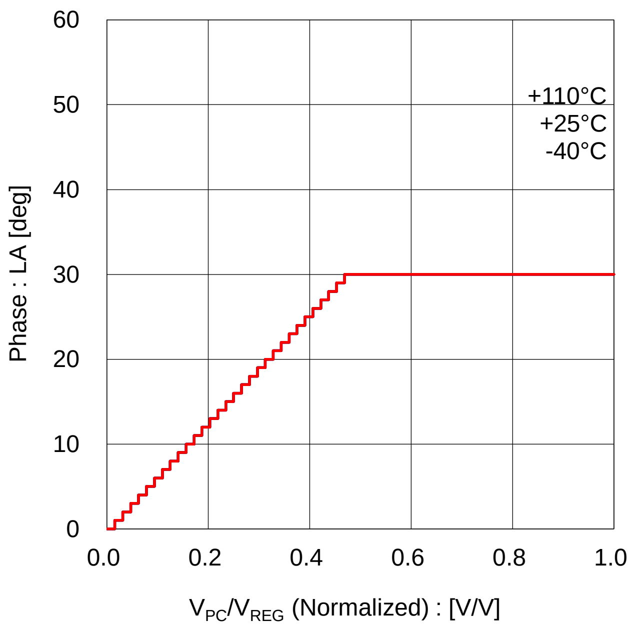


Figure 29. PC Voltage Normalized vs Lead Angle

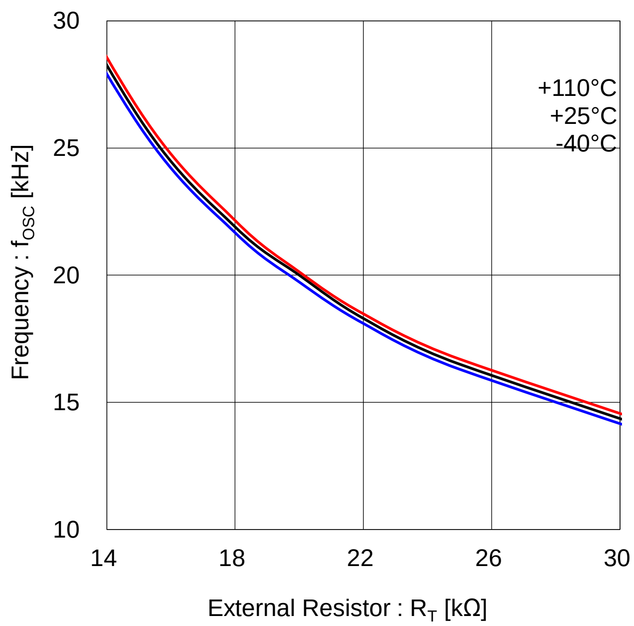


Figure 30. Carrier Frequency vs RT

Timing Chart (CW)

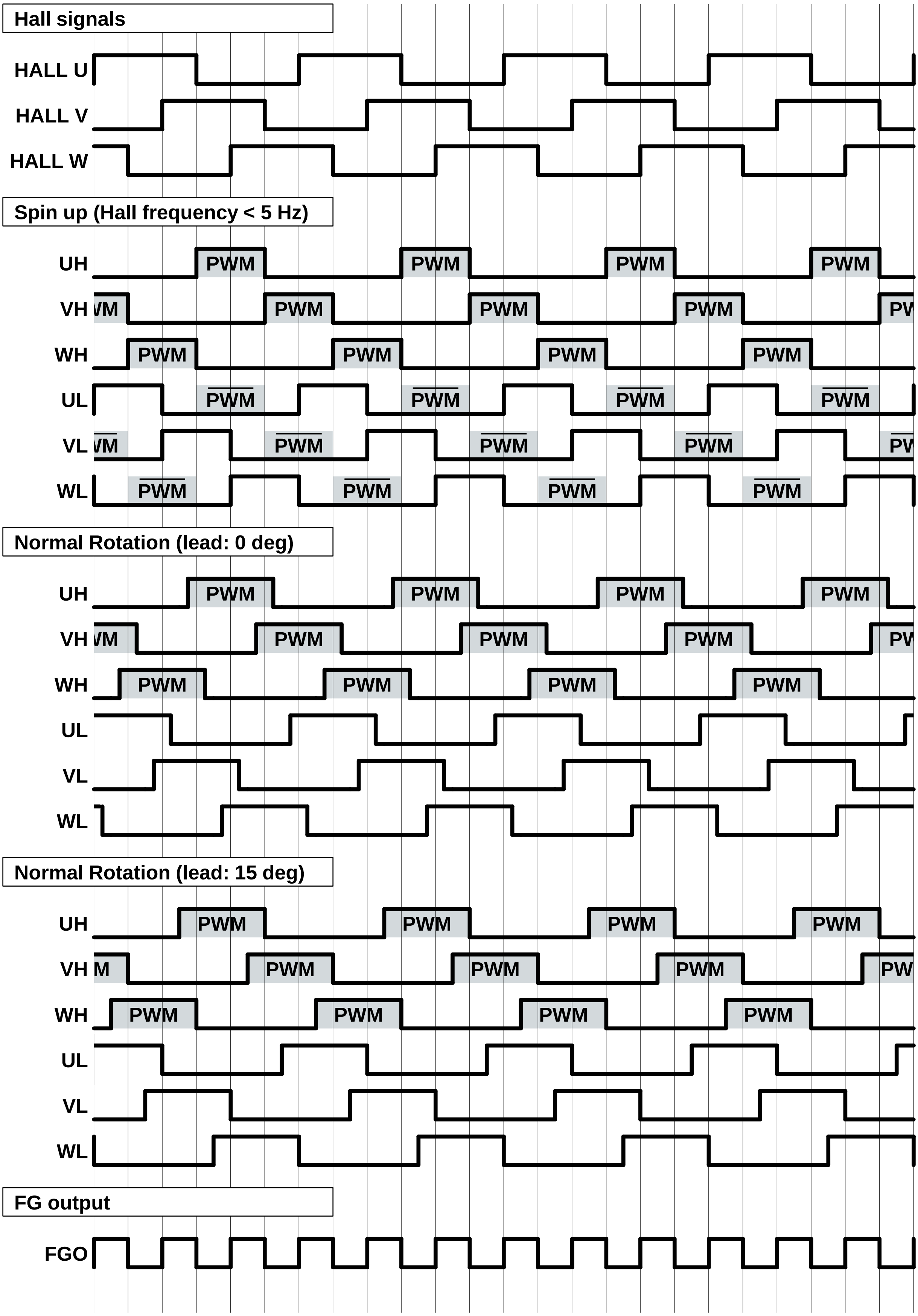


Figure 31. Timing Chart (Clockwise)

Timing Chart (CCW)

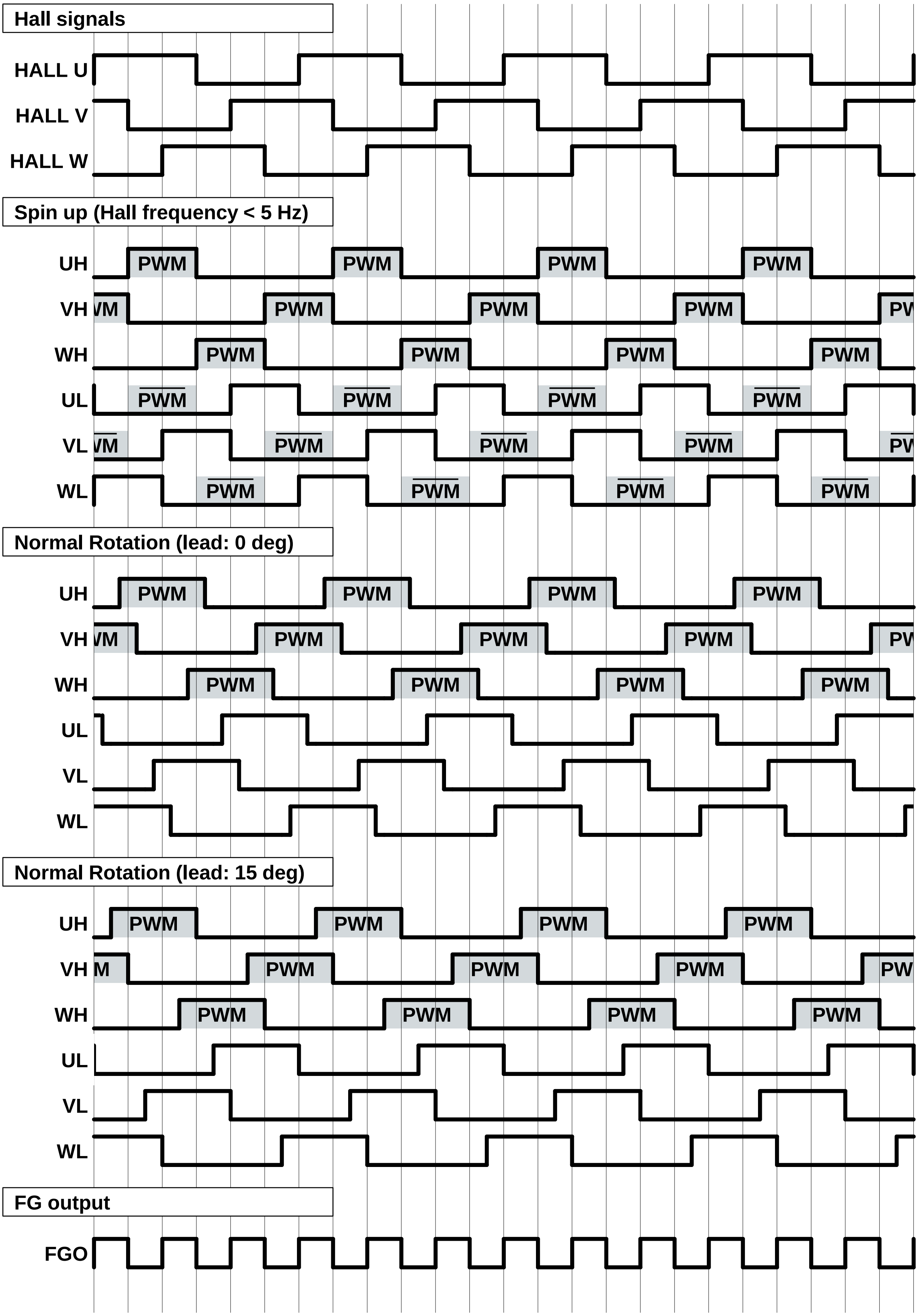


Figure 32. Timing Chart (Counter Clockwise)

Application Example

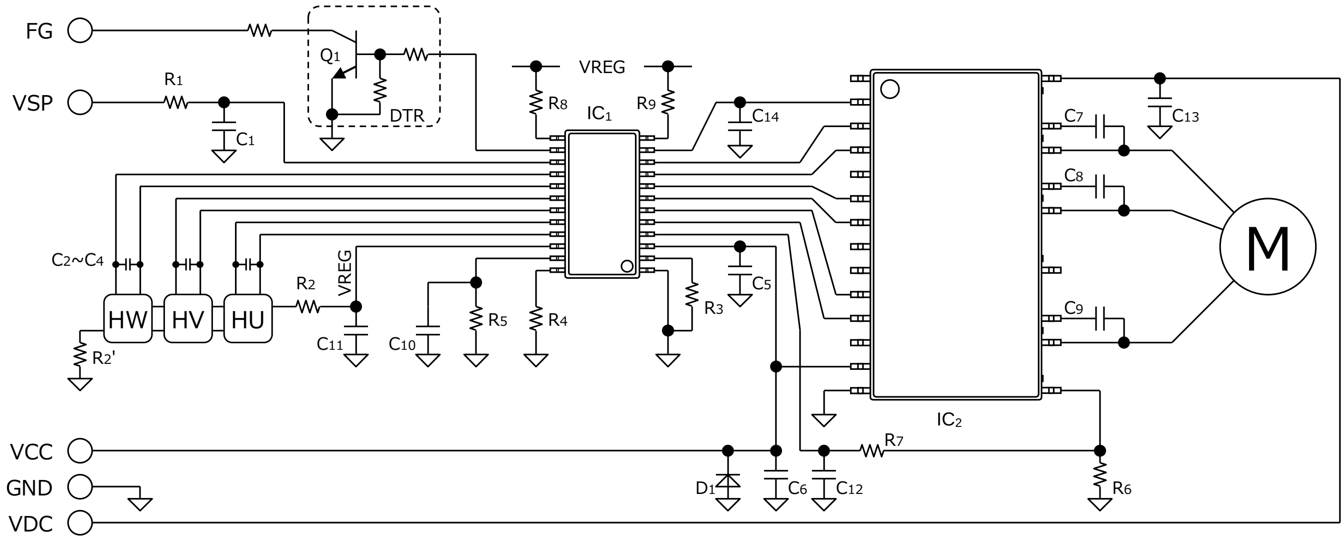


Figure 33. Application Example (150° Commutation Driver, CCW="H", FGS="H")

Parts List

Parts	Value	Manufacturer	Type	Parts	Value	Ratings	Type
IC_1	-	ROHM	BD62012BFS	C_1	0.1µF	50V	Ceramic
IC_2	-	ROHM	BM6242FS	C_2	2200pF	50V	Ceramic
R_1	1kΩ	ROHM	MCR18EZPF1001	C_3	2200pF	50V	Ceramic
R_2	150Ω	ROHM	MCR18EZPJ151	C_4	2200pF	50V	Ceramic
R_3	22kΩ	ROHM	MCR18EZPF2202	C_5	10 µF	50V	Ceramic
R_4	100kΩ	ROHM	MCR18EZPF1003	C_6	10 µF	50V	Ceramic
R_5	51kΩ	ROHM	MCR18EZPF5102	C_7	1µF	50V	Ceramic
R_6	0.5Ω	ROHM	MCR18SEQPJ1R50 // 3	C_8	1µF	50V	Ceramic
R_7	10kΩ	ROHM	MCR18EZPF1002	C_9	1µF	50V	Ceramic
R_8	0Ω	ROHM	MCR18EZPJ000	C_{10}	0.1µF	50V	Ceramic
R_9	0Ω	ROHM	MCR18EZPJ000	C_{11}	1µF	50V	Ceramic
Q_1	-	ROHM	DTC124EU3	C_{12}	100pF	50V	Ceramic
D_1	-	ROHM	KDZV20B	C_{13}	0.1µF	630V	Ceramic
				C_{14}	0.1µF	50V	Ceramic
				HX	-	-	Hall elements

I/O Equivalence Circuits

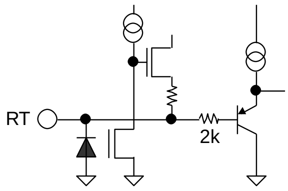


Figure 34. RT

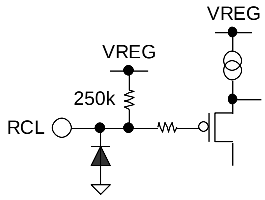


Figure 35. RCL

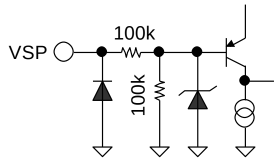


Figure 36. VSP

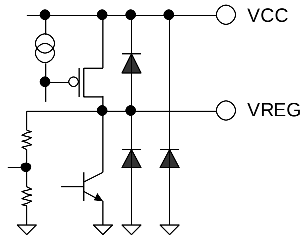


Figure 37. VREG, VCC

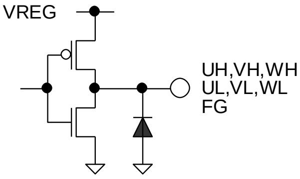


Figure 38. XH, XL, FG

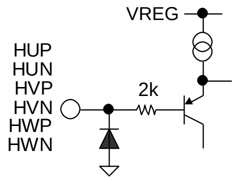


Figure 39. HXP, HXN

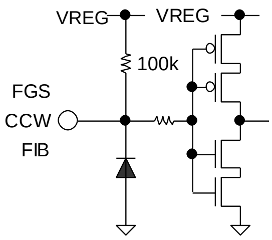


Figure 40. FGS, CCW, FIB

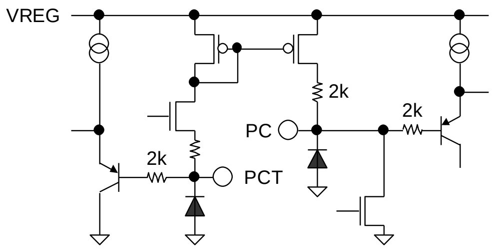


Figure 41. PC, PCT

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

10. Regarding the Input Pin of the IC

Do not force voltage to the input pins when the power does not supply to the IC. Also, do not force voltage to the input pins that exceed the supply voltage or in the guaranteed the absolute maximum rating value even if the power is supplied to the IC.

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

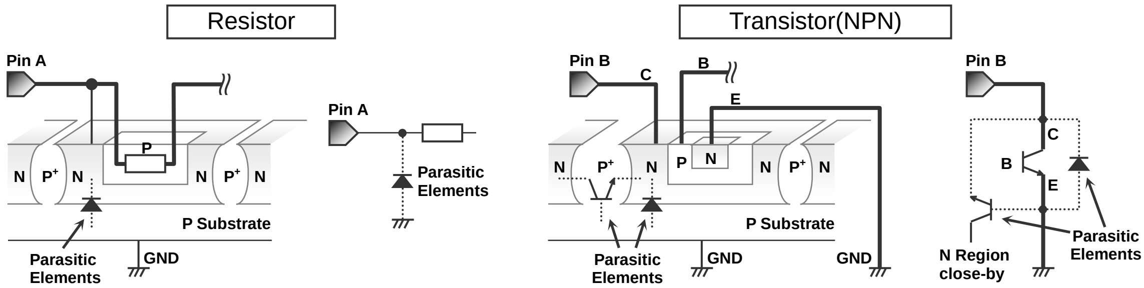


Figure 42. Example of Monolithic IC structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

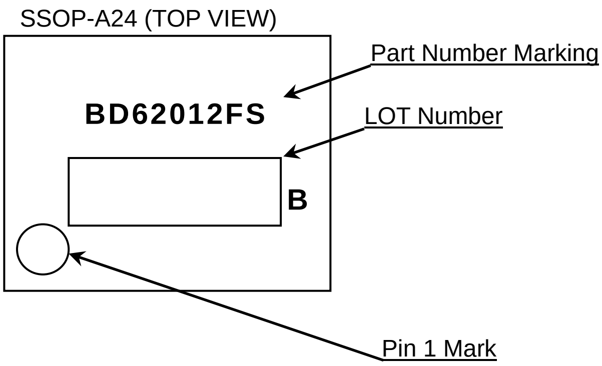
B D 6 2 0 1 2 B F S - E 2

Parts Number

Package
FS : SSOP-A24

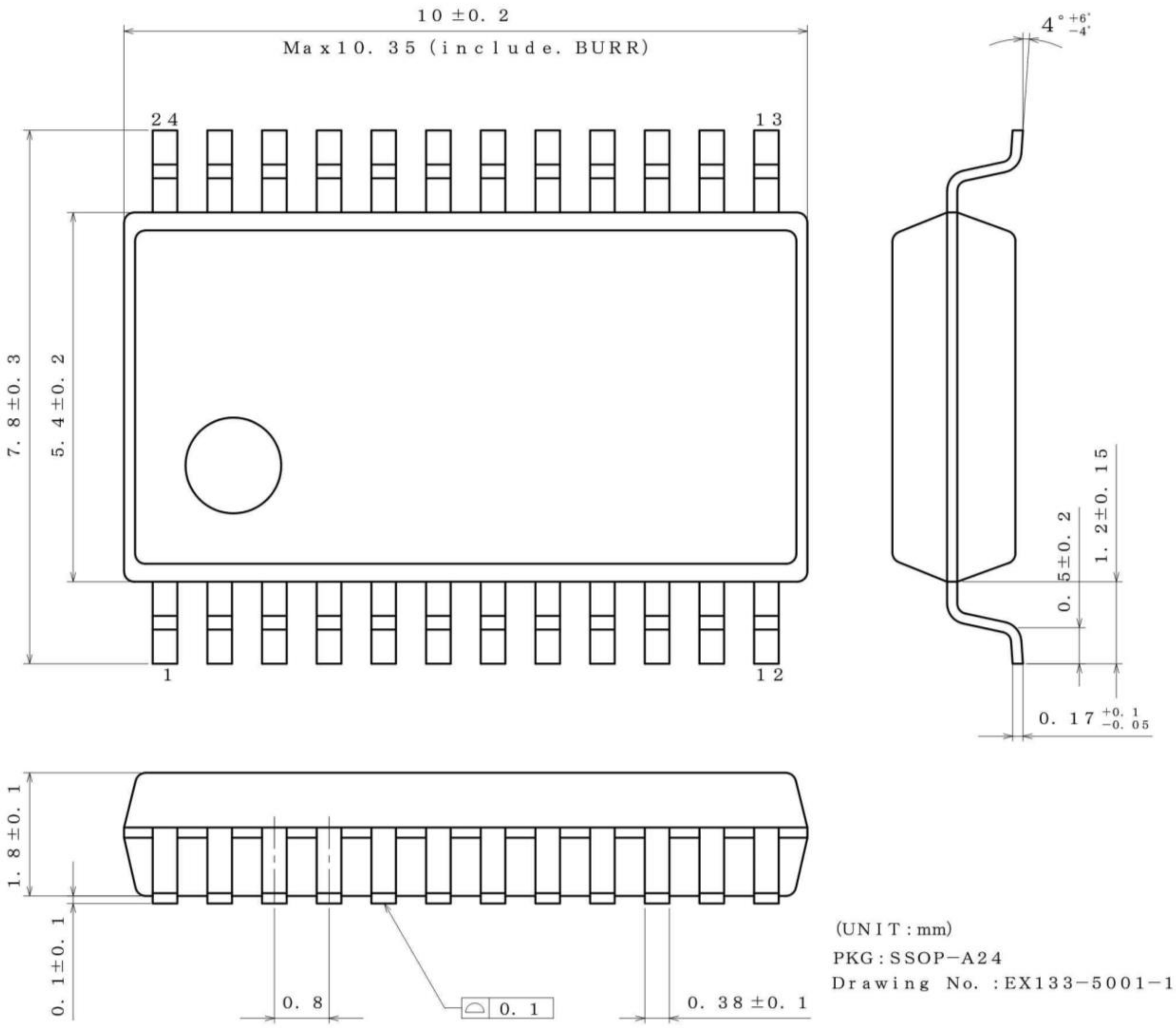
Packaging specification
E2 : Embossed tape and reel

Marking Diagram



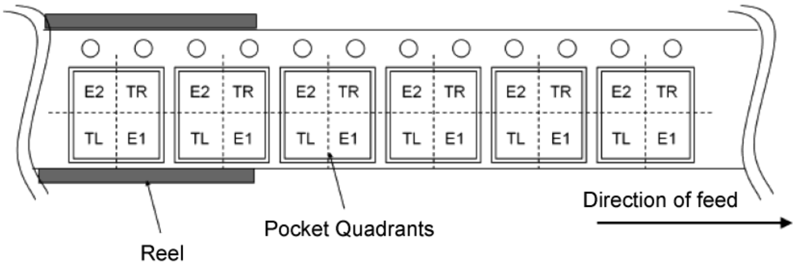
Physical Dimension and Packing Information

Package Name	SSOP-A24



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
21.Jan.2022	001	New Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Precaution for Disposition

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