Automotive IPD Series

1ch High Side Switch

BV1HV050FJ-C

General Description

BV1HV050FJ-C is a 1ch high side switch for automotive application. It has a built in hiccup mode overcurrent protection function, thermal shutdown protection function, open load detection function, under voltage lockout function. It is equipped with diagnostic output function for abnormality detection.

Features

- AEC-Q100 Qualified(Note 1)
- Built in Hiccup Mode Overcurrent Protection Function (OCP)
- Built-in Thermal Shutdown Protection Function (TSD)
- Built-in Open Load Detection Function (OLD)
- Built-in Under Voltage Lockout Function (UVLO)
- Low On-Resistance R_{ON} = 50 mΩ (Typ)
- Monolithic Power Management IC with the Control Block (CMOS) and Power MOSFET Mounted on a Single Chip

(Note 1) Grade1

Application

- Resistance Load, Inductance Load and Capacitance Load for Automotive Application

Key Specifications

- Power Supply Voltage Operating Range: 4.5 V to 28.0 V
- ON-Resistance (Tj = 25 °C): 50 mΩ (Typ)
- Overcurrent Value: 3 A (Min)
- Standby Current (Tj = 25 °C): 10 µA (Typ)
- Active Clamp Energy (Single Pulse): 140 mJ
  (Tj = 25 °C, $I_{OUT(START)}$ = 2 A)

Package

Package	W (Typ) x D (Typ) x H (Max)
SOP-J8	4.9 mm x 6.0 mm x 1.65 mm

SOP-J8

Typical Application Circuit

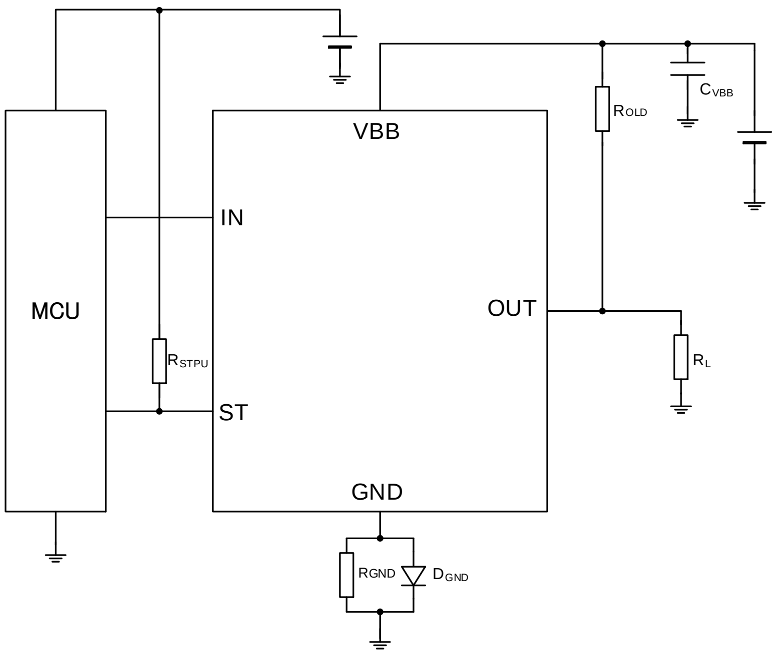


Figure 1. Application Circuit

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Contents

Pin Configuration

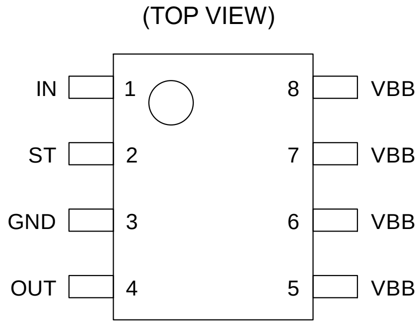


Figure 2. Pin Configuration

Pin Description

Pin Number	Pin Name	Function
1	IN	Input pin. Pull-down resistor is connected internally.
2	ST	Self-diagnostic output pin, which outputs “Low” at overcurrent or overheating, and “High” at open load. It has an n-channel open drain circuit structure.
3	GND	Ground pin
4	OUT	Switch output pin
5 to 8	VBB	Power input pin, Switch input pin

Block Diagram

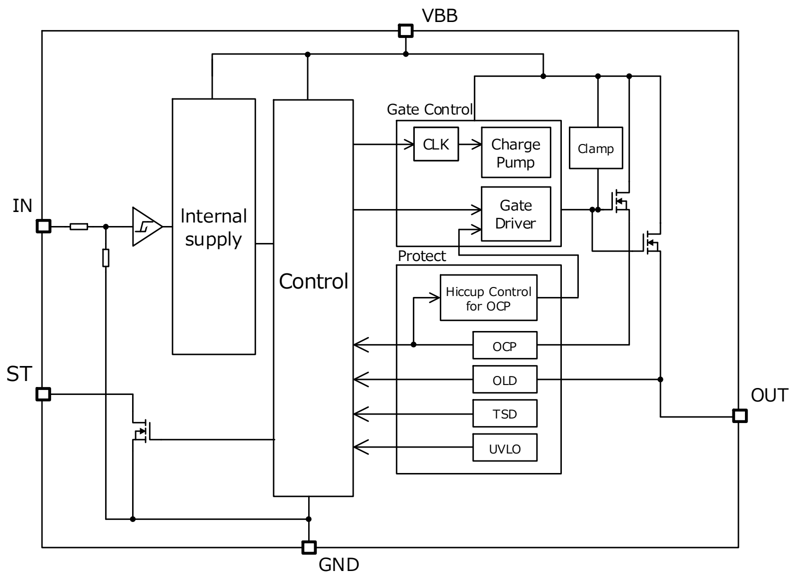


Figure 3. Block Diagram

Definition

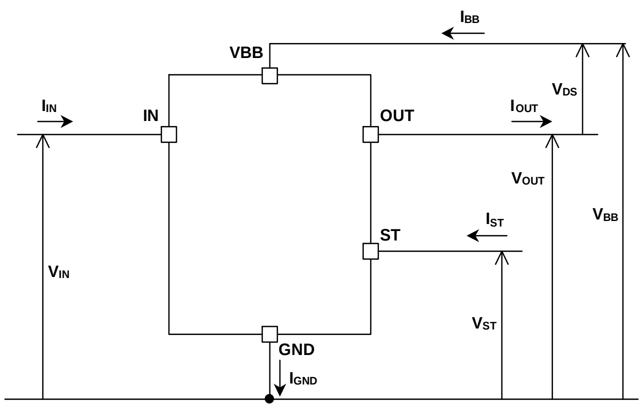


Figure 4. Voltage and Current Definition

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
VBB - OUT Voltage	V_{DS}	-0.3 to Internal clamp*(Note 1)*	V
Power Supply Voltage	V_{BB}	40	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Diagnostic Output Voltage	V_{ST}	-0.3 to +7.0	V
Output Current	I_{OUT}	10 (Overcurrent limit value I_{OC})*(Note 2)*	A
Junction Temperature Width	Tj	-40 to +150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C
Active Clamp Energy (Single Pulse) $Tj_{(START)}$ = 25 °C, $I_{OUT(START)}$ = 2 A *(Note 3)*	$E_{AS(25\ °C)}$	140	mJ
Active Clamp Energy (Single Pulse) $Tj_{(START)}$ = 150 °C, $I_{OUT(START)}$ = 2 A *(Note 3)*	$E_{AS(150\ °C)}$	65	mJ
Supply Voltage for Short Circuit Protection *(Note 4)*	V_{BBLIM}	28	V

(Note 1) Internally limited by output clamp voltage.
(Note 2) When overcurrent flows, output is turned off. Output self-restarts after 2 ms (Typ) .
(Note 3) Maximum active clamp energy using Single Pulse of $I_{OUT(START)}$ = 2 A and V_{BB} = 14 V. Not 100 % tested.
(Note 4) Maximum power supply voltage that can detect short circuit protection.

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*
Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*
Caution 3: *When IC turns off with an inductive load, reverse energy is generated. This energy can be calculated by the following equation:*

$$E_L = \frac{1}{2} L I_{OUT(START)}{}^2 \times \left(1 - \frac{V_{BAT}}{V_{BAT} - V_{OUT(CL)}}\right)$$

Where:
L *is the inductance of the inductive load.*
$I_{OUT(START)}$ *is Output current when the inductive load is turned off.*
$V_{OUT(CL)}$ *is Output Clamp Voltage.*

The BV1HV050FJ-C integrates the active clamp function to internally absorb the reverse energy E_L which is generated when the inductive load is turned off. When the active clamp operates, the thermal shutdown function does not work. Decide a load so that the reverse energy E_L is active clamp energy (Single Pulse) E_{AS} (refer to Figure 5. Active Clamp Energy (Single Pulse) vs Output Current (Start)) or under when inductive load is used.

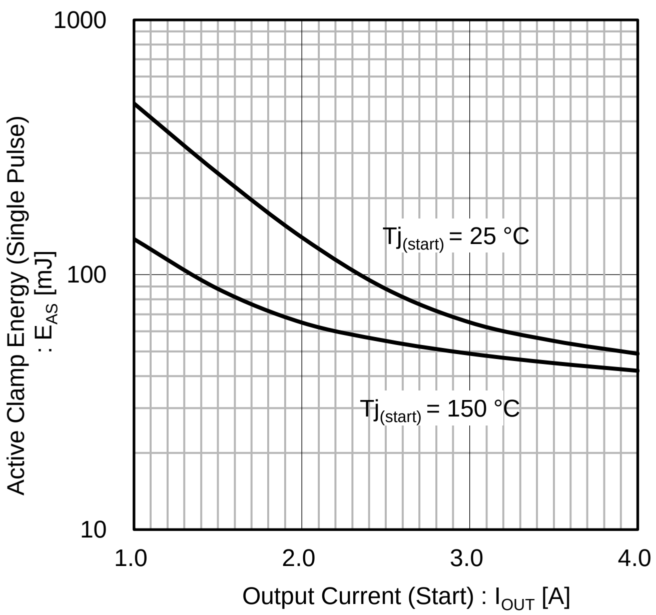


Figure 5. Active Clamp Energy (Single Pulse) vs Output Current (Start)

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Power Supply Voltage	V_{BB}	4.5	14.0	28.0	V
Operating Temperature	Topr	-40	+25	+150	°C
Operating Frequency (VBB = 6 V to 28 V, 50 % Duty)*(Note 1)*	f_{IN}	-	-	1	KHz
Operating Frequency (VBB = 4.5 V to 6 V, 50 % Duty)*(Note 1)*	f_{IN}	-	-	0.5	KHz

(Note 1) If driven at a frequency higher than the maximum value, the output (OUT) voltage may not swing fully and the load may not be driven.

Thermal Resistance*(Note 2)*

Parameter	Symbol	Typ	Unit	Condition
SOP-J8				
Between Junction and Surroundings Temperature Thermal Resistance	θ_{JA}	143.7	°C/W	1s*(Note 3)*
		86.9	°C/W	2s*(Note 4)*
		67.5	°C/W	2s2p*(Note 5)*

(Note 2) The thermal impedance is based on JESD51-2A (Still-Air) standard. It is used the chip of BV1HV050FJ-C.
(Note 3) JESD51-3 standard FR4 114.3 mm x 76.2 mm x 1.57 mm 1-layer (1s)
(Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.)
(Note 4) JESD51-5 standard FR4 114.3 mm x 76.2 mm x 1.60 mm 2-layer (2s)
(Top copper foil: ROHM recommended Footprint + wiring to measure
Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm, copper (top & reverse side) 2 oz.)
(Note 5) JESD51-5 / -7 standard FR4 114.3 mm x 76.2 mm x 1.60 mm 4-layers (2s2p)
(Top copper foil: ROHM recommended Footprint + wiring to measure
2 inner layers and copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm, copper (top & reverse side / inner layers) 2 oz / 1 oz.)

■ PCB Layout 1 layer (1s)

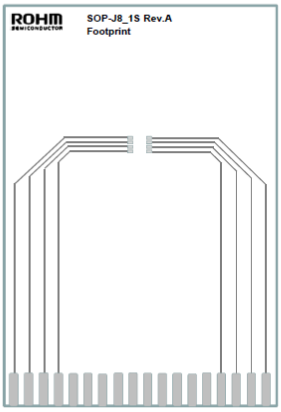


Figure 6. PCB Layout 1 layer (1s)

Dimension	Value
Board finish thickness	1.57 mm ± 10 %
Board dimension	76.2 mm x 114.3 mm
Board material	FR4
Copper thickness (Top/Bottom layers)	0.070 mm (Cu: 2oz)

Thermal Resistance – continued

■ PCB Layout 2 layers (2s)

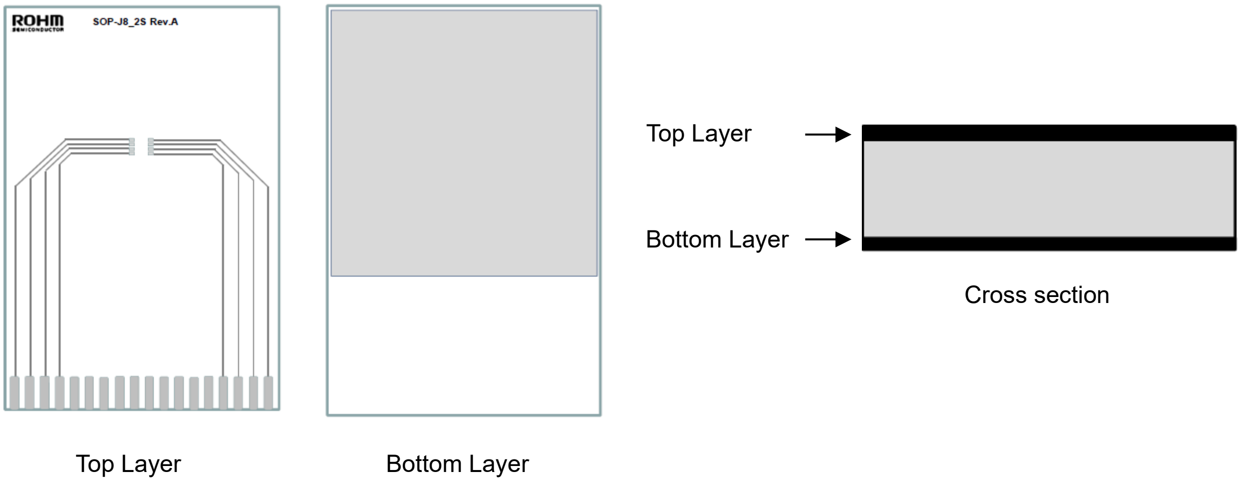


Figure 7. PCB Layout 2 layers (2s)

Dimension	Value
Board finish thickness	1.60 mm ± 10 %
Board dimension	76.2 mm x 114.3 mm
Board material	FR4
Copper thickness (Top/Bottom layers)	0.070 mm (Cu + Plating)

■ PCB Layout 4 layers (2s2p)

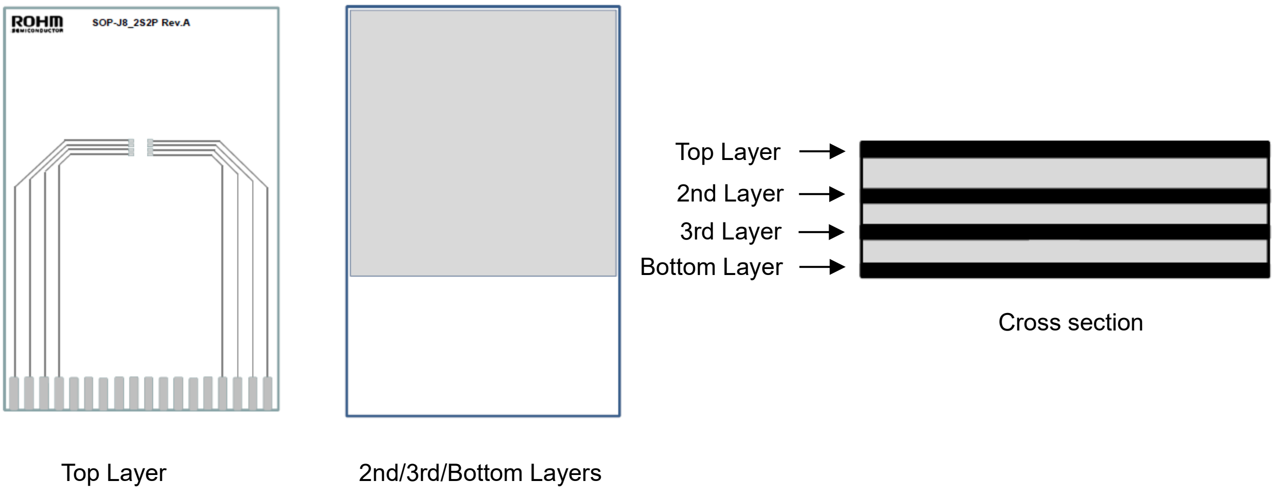


Figure 8. PCB Layout 4 layers (2s2p)

Dimension	Value
Board finish thickness	1.60 mm ± 10 %
Board dimension	76.2 mm x 114.3 mm
Board material	FR4
Copper thickness (Top/Bottom layers)	0.070 mm (Cu + Plating)
Copper thickness (Inner layers)	0.035 mm

Thermal Resistance – continued

■ Transient Thermal Resistance (Single Pulse)

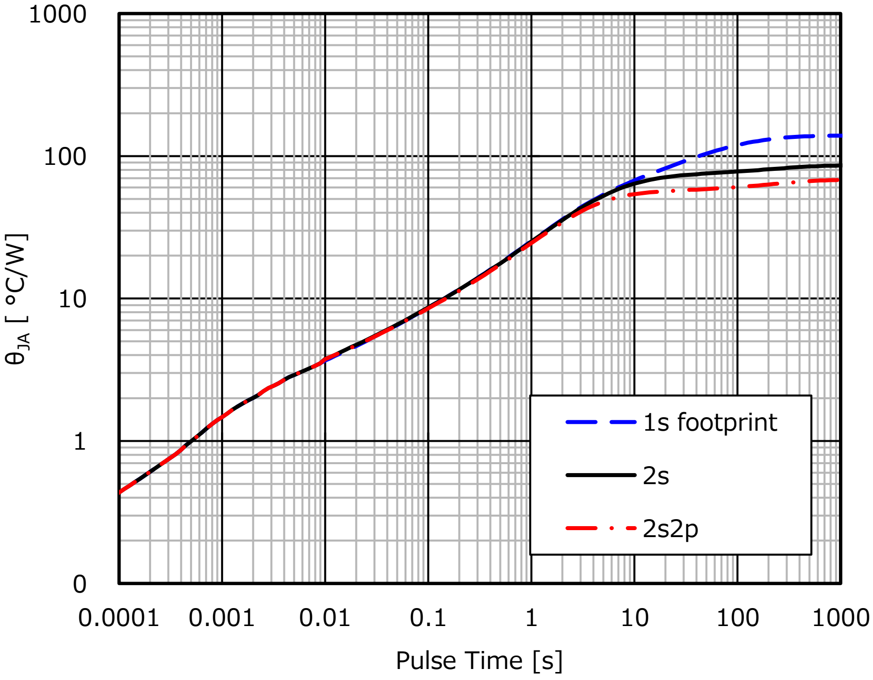


Figure 9. Transient Thermal Resistance

Electrical Characteristics (unless otherwise specified V_{BB} = 4.5 V to 28 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Power Supply]						
Standby Current	I_{BBL}	-	10	20	µA	V_{BB} = 14 V, V_{IN} = 0 V V_{OUT} = 0 V, Tj = 25 °C
		-	-	35	µA	V_{IN} = 0 V V_{OUT} = 0 V, Tj = 25 °C
		-	-	50	µA	V_{BB} = 14 V, V_{IN} = 0 V V_{OUT} = 0 V, Tj = 150 °C
		-	-	100	µA	V_{IN} = 0 V V_{OUT} = 0 V, Tj = 150 °C
Operating Current	I_{BBH}	-	3.5	6	mA	V_{BB} = 14 V, V_{IN} = 5 V, V_{OUT} = open
UVLO Detection Voltage	V_{UVDET}	3.4	3.7	4.0	V	
UVLO Release Voltage	V_{UVREL}	-	-	4.5	V	
UVLO Hysteresis Voltage	V_{UVHYS}	-	-	1.0	V	
[Input (V_{IN})]						
High Level Input Voltage	V_{INH}	3.0	-	-	V	
Low Level Input Voltage	V_{INL}	-	-	1.5	V	
Input Hysteresis Voltage	V_{INHYS}	-	0.5	-	V	
High Level Input Current	I_{INH}	-	50	150	µA	V_{IN} = 5 V
Low Level Input Current	I_{INL}	-10	-	+10	µA	V_{IN} = 0 V
[Power MOS Output]						
Output ON Resistance	R_{ON}	-	50	65	mΩ	V_{BB} = 8 V to 18 V, Tj = 25° C, I_{OUT} = 1 A
		-	-	115	mΩ	V_{BB} = 8 V to 18 V, Tj = 150 °C, I_{OUT} = 1 A
		-	-	180	mΩ	V_{BB} = 4.0 V, I_{OUT} = 1 A
Output Leak Current	I_{OUTL}	-	-	0.5	µA	V_{IN} = 0 V, V_{OUT} = 0 V, Tj = 25 °C
		-	-	10	µA	V_{IN} = 0 V, V_{OUT} = 0 V, Tj = 150 °C
	I_{OUTH}	-60	-30	-	µA	V_{BB} = 14 V V_{IN} = 0 V, V_{OUT} = V_{BB}, Tj = 25 °C
		-80	-40	-	µA	V_{BB} = 14 V V_{IN} = 0 V, V_{OUT} = V_{BB}, Tj = 150 °C
Output Slew Rate when ON	SR_{ON}	0.1	0.3	1.0	V/µs	V_{BB} = 14 V, R_L = 6.5 Ω
Output Slew Rate when OFF	SR_{OFF}	0.1	0.3	1.0	V/µs	V_{BB} = 14 V, R_L = 6.5 Ω
Output Propagation Delay Time when ON	t_{OUTON}	-	60	120	µs	V_{BB} = 14 V, R_L= 6.5 Ω
Output Propagation Delay Time when OFF	t_{OUTOFF}	-	60	120	µs	V_{BB} = 14 V, R_L = 6.5 Ω
Output Clamp Voltage	V_{DSCLP}	45	50	55	V	V_{IN} = 0 V, I_{OUT} = -10 mA
[Diagnostics]						
Diagnostic Output Low Voltage	V_{STL}	-	-	0.5	V	I_{ST} = 1 mA
Diagnostic Output Leak Current	I_{STL}	-	-	10	µA	V_{ST} = 5 V
Diagnostic Output Propagation Delay Time when ON	t_{STON}	-	70	160	µs	V_{BB} = 14 V, R_L = 6.5 Ω
Diagnostic Output Propagation Delay Time when OFF	t_{STOFF}	-	100	250	µs	V_{BB} = 14 V, R_L = 6.5 Ω

Electrical Characteristics (unless otherwise specified V_{BB} = 4.5 V to 28 V, Tj = -40 °C to +150 °C) - continued

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Protection Circuit]						
Overcurrent Detection Current	I_{OC}	3	5.5	10	A	V_{BB} = 14 V, V_{IN} = 5 V, V_{OUT} = 0 V
Overcurrent Detection Peak Current *(Note 1)*	I_{OCPEAK}	3	-	15	A	V_{BB} = 14 V, V_{IN} = 5 V, V_{OUT} = 0 V
Overcurrent Detection ON Time	t_{OCON}	25	55	85	µs	V_{BB} = 14 V, V_{IN} = 5 V, V_{OUT} = 0 V
Overcurrent Detection OFF Time	t_{OCOFF}	1.0	2.0	4.0	ms	V_{BB} = 14 V, V_{IN} = 5 V, V_{OUT} = 0 V
Overcurrent Detection ON Duty	D_{OC}	-	-	7	%	V_{BB} = 14 V, V_{IN} = 5 V, V_{OUT} = 0 V
Open Load Detection Voltage	V_{OLDDET}	2.0	3.0	4.0	V	
Open Load Detection Hysteresis Voltage	V_{OLDHYS}	0.2	0.4	0.8	V	
Open Load Detection Sink Current	I_{OLD}	-30	-10	-	µA	V_{BB} = 6 V to 28 V, V_{IN} = 0 V, V_{OUT} = 5 V
Open Load Detection Diagnostic Output Mask Time	t_{STMASK}	250	500	1000	µs	V_{BB} = 14 V, V_{IN} = 0 V, V_{OUT} = 5 V, Tj = 25 °C
Thermal Shutdown Detection Temperature *(Note 1)*	T_{TSDDET}	150	175	200	°C	
Thermal Shutdown Hysteresis Temperature *(Note 1)*	T_{TSDHYS}	-	15	-	°C	

(Note 1) Not 100 % tested.

Typical Performance Curves

(Unless otherwise specified V_{BB} = 14 V, V_{IN} = 5 V, Tj = 25 °C)

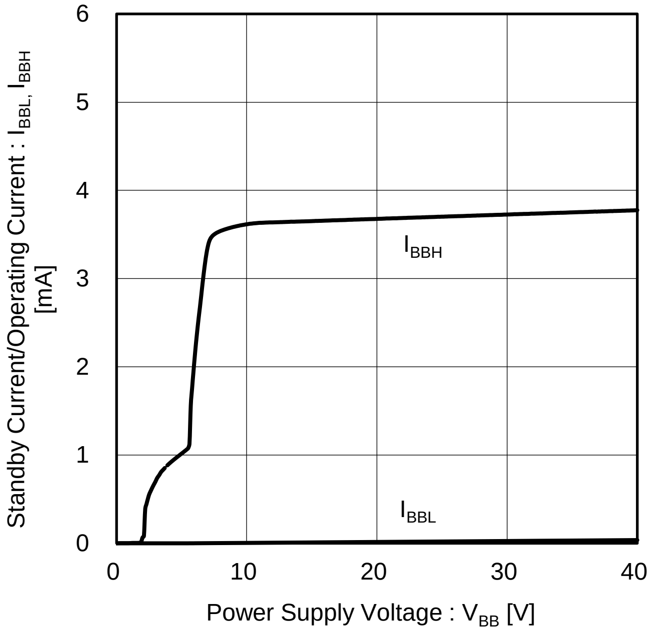


Figure 10. Standby Current/Operating Current vs Power Supply Voltage

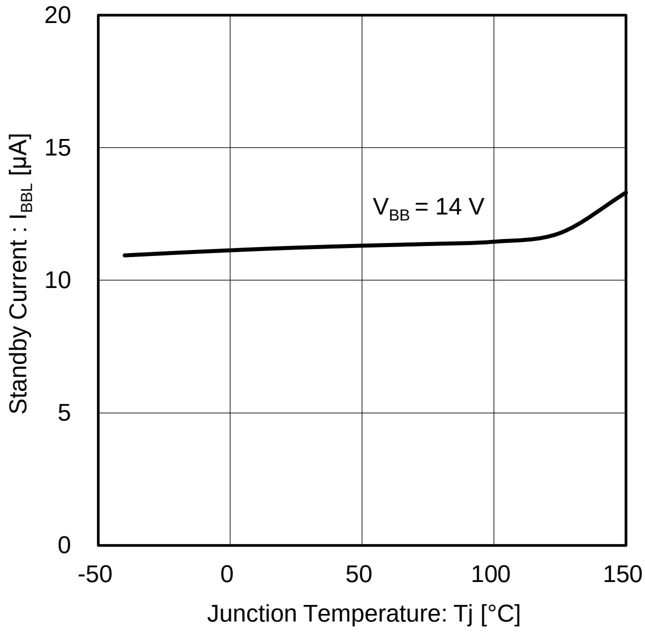


Figure 11. Standby Current vs Junction Temperature

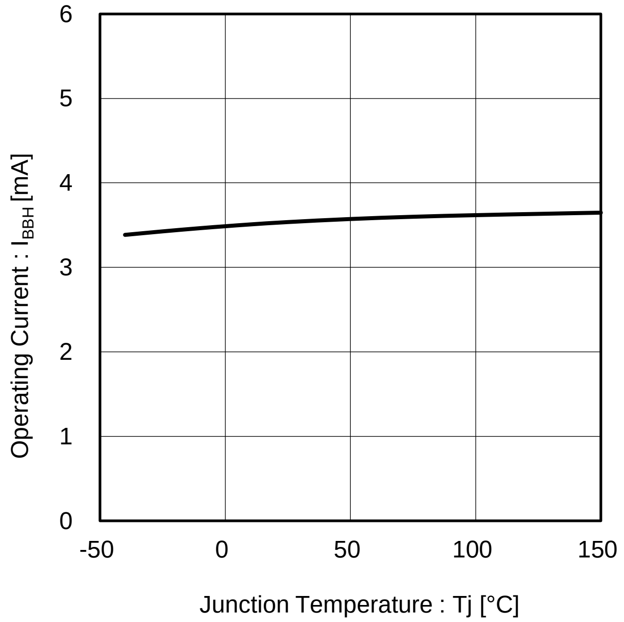


Figure 12. Operating Current vs Junction Temperature

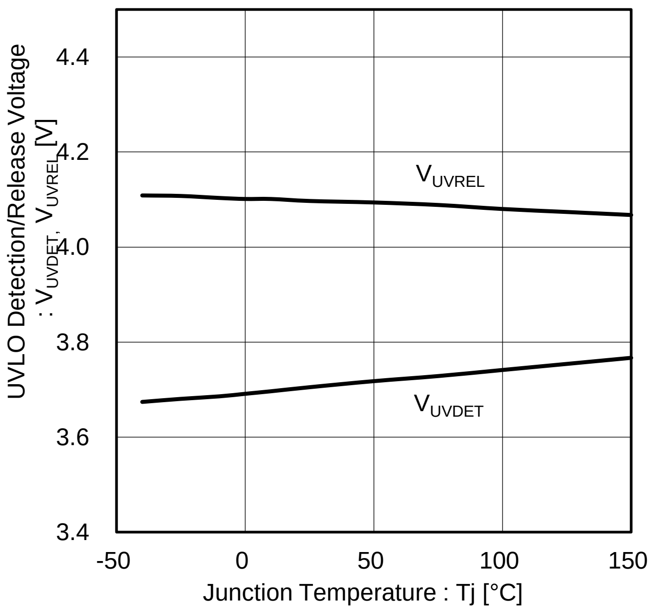


Figure 13. UVLO Detection/Release Voltage vs Junction Temperature

Typical Performance Curves - continued
(Unless otherwise specified V_{BB} = 14 V, V_{IN} = 5 V, Tj = 25 °C)

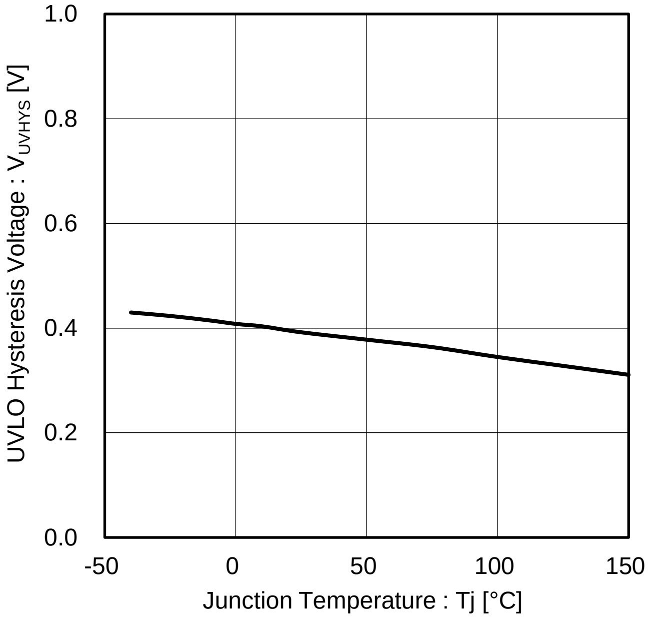


Figure 14. UVLO Hysteresis Voltage vs Junction Temperature

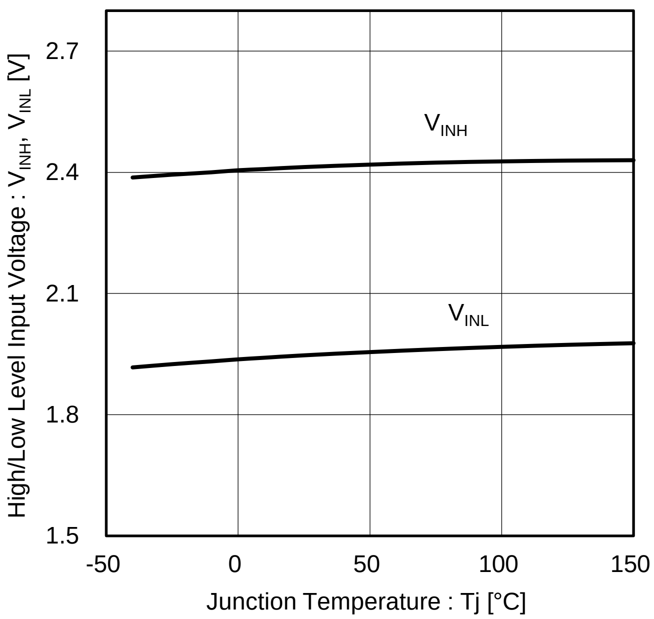


Figure 15. High/Low Level Input Voltage vs Junction Temperature

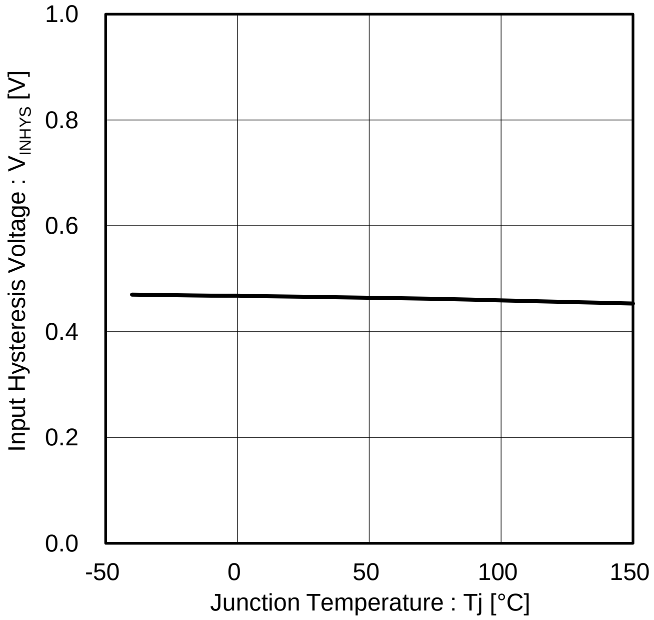


Figure 16. Input Hysteresis Voltage vs Junction Temperature

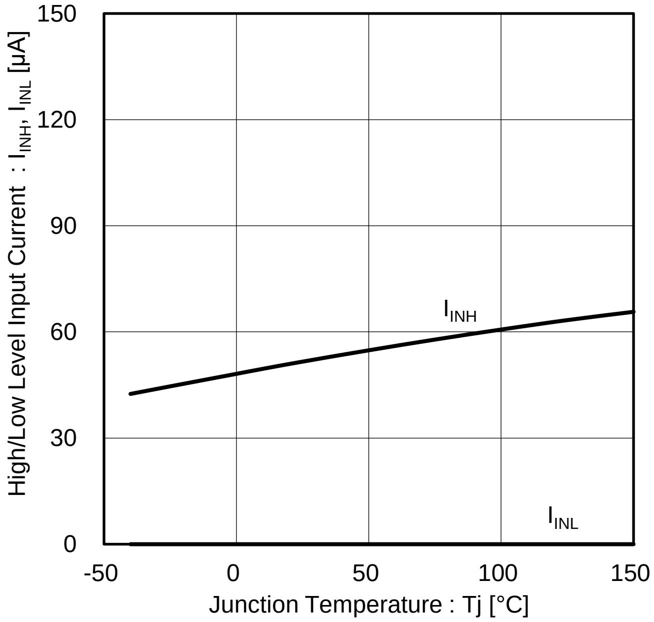


Figure 17. High/Low Level Input Current vs Junction Temperature

Typical Performance Curves - continued
(Unless otherwise specified V_{BB} = 14 V, V_{IN} = 5 V, Tj = 25 °C)

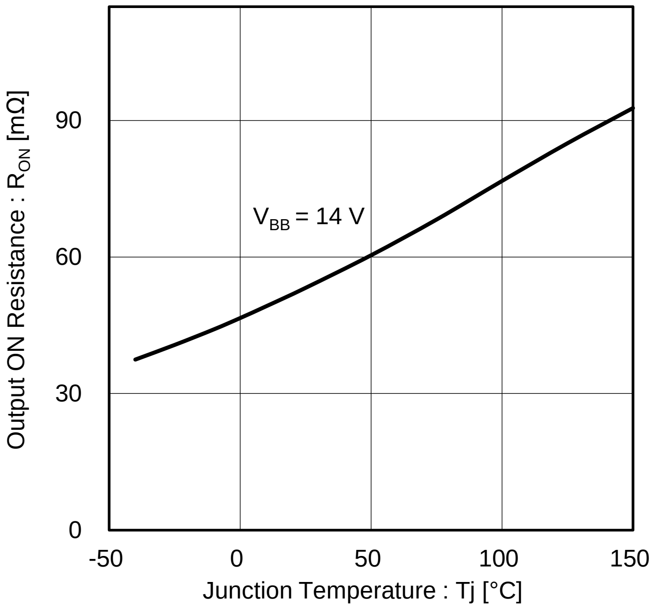


Figure 18. Output ON Resistance vs Junction Temperature

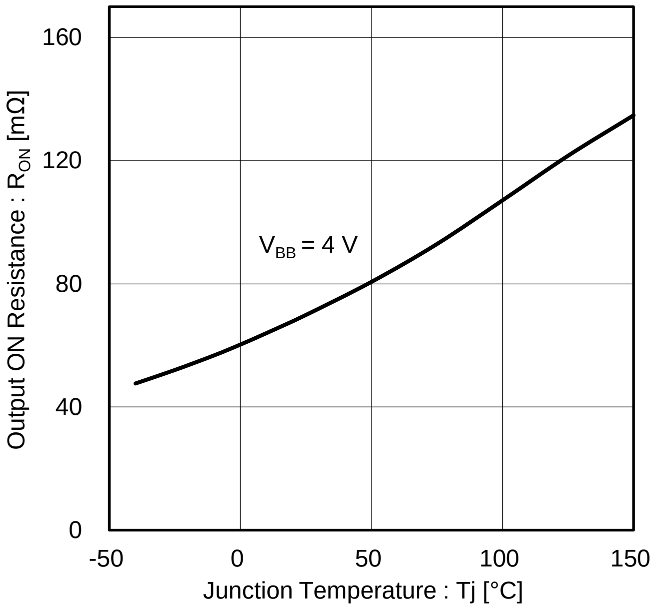


Figure 19. Output ON Resistance vs Junction Temperature

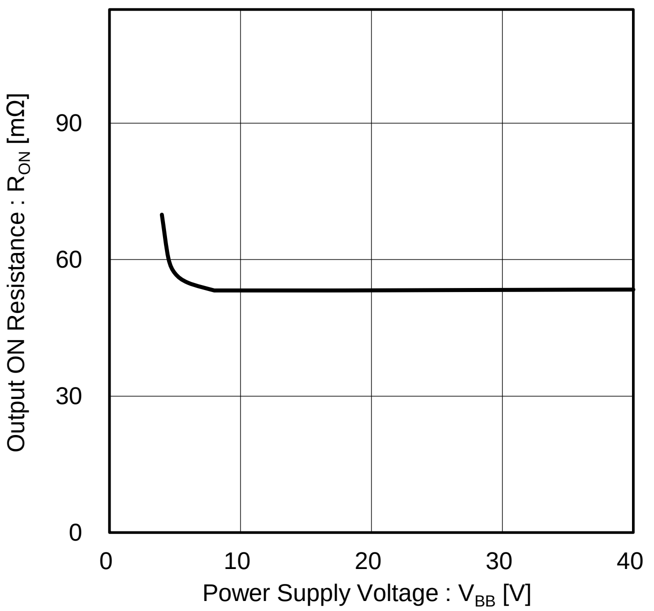


Figure 20. Output ON Resistance vs Power Supply Voltage

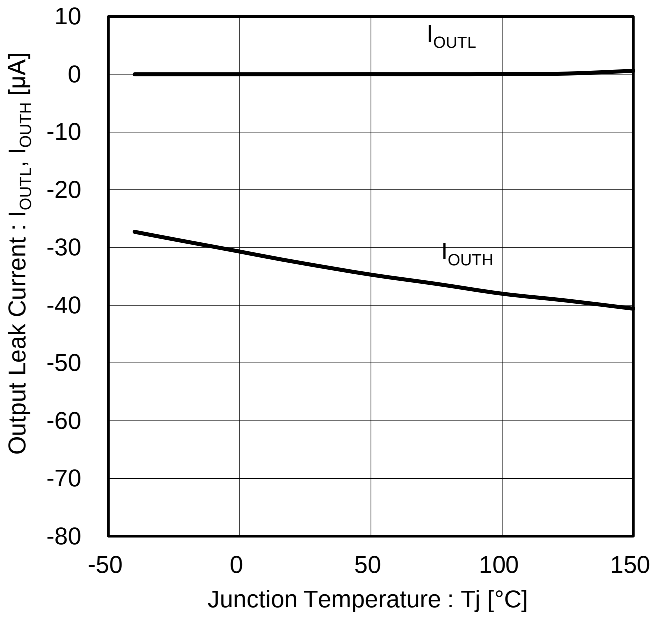


Figure 21. Output Leak Current vs Junction Temperature

Typical Performance Curves - continued
(Unless otherwise specified V_{BB} = 14 V, V_{IN} = 5 V, Tj = 25 °C)

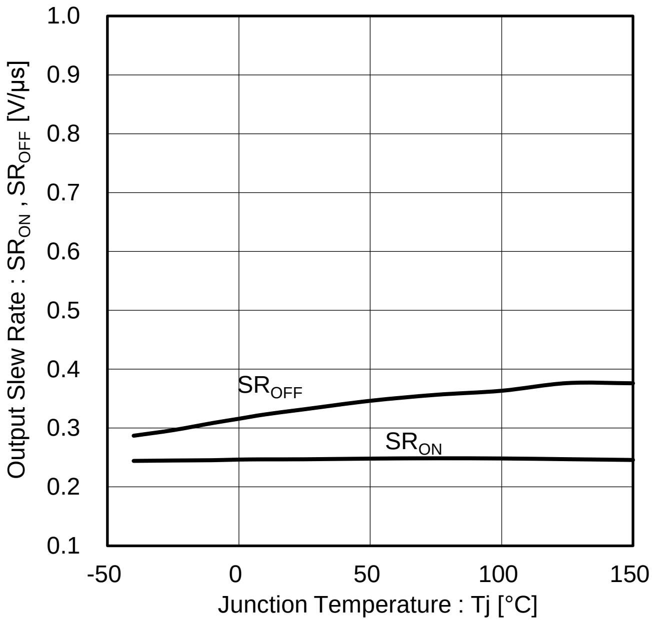


Figure 22. Output Slew Rate vs Junction Temperature

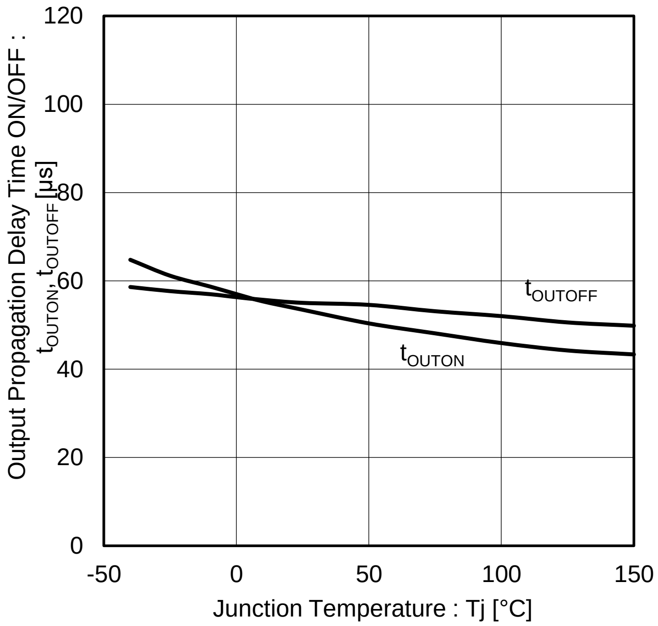


Figure 23. Output Propagation Delay Time ON/OFF vs Junction Temperature

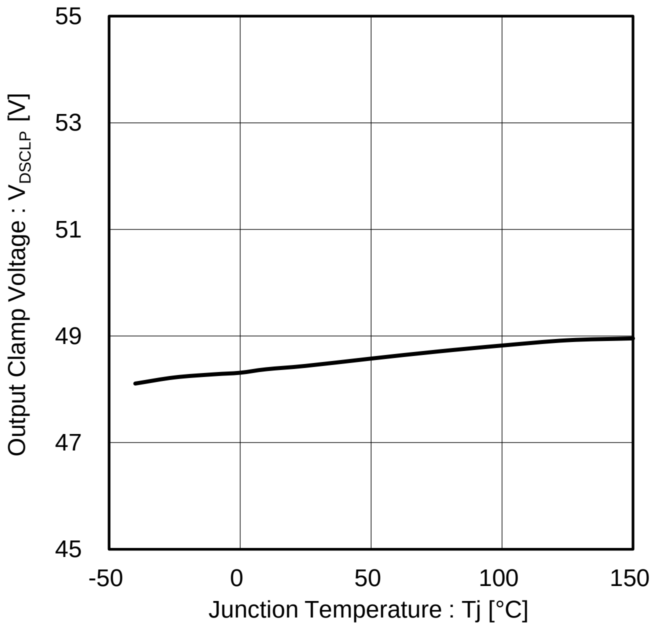


Figure 24. Output Clamp Voltage vs Junction Temperature

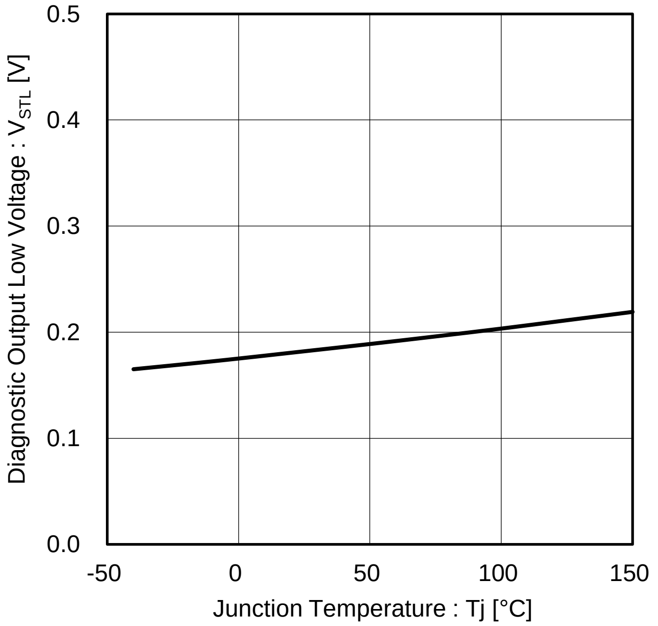


Figure 25. Diagnostic Output Low Voltage vs Junction Temperature

Typical Performance Curves - continued
(Unless otherwise specified V_{BB} = 14 V, V_{IN} = 5 V, Tj = 25 °C)

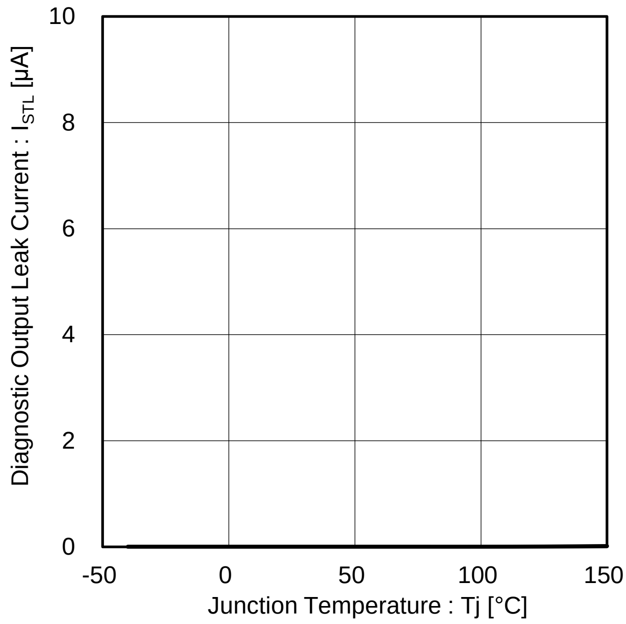


Figure 26. Diagnostic Output Leak Current vs Junction Temperature

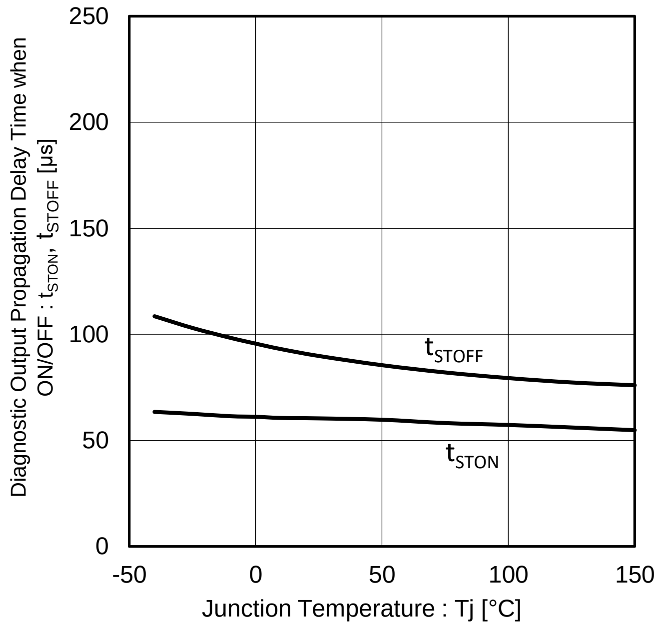


Figure 27. Diagnostic Output Propagation Delay Time when ON/OFF vs Junction Temperature

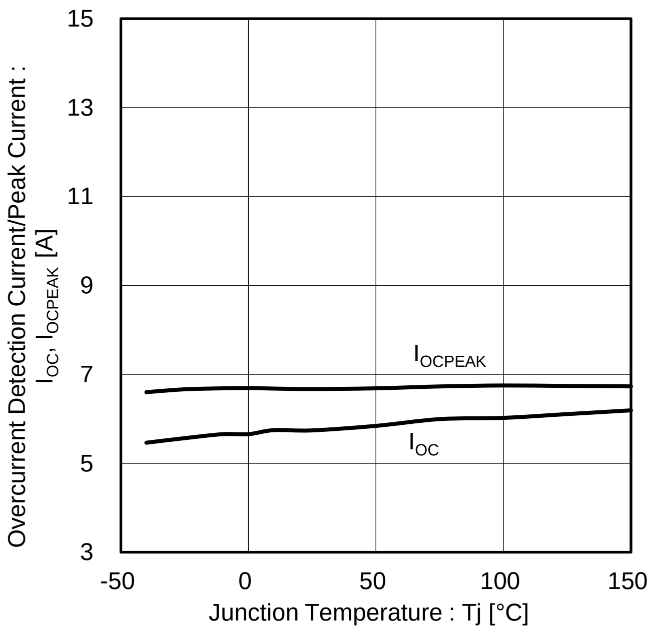


Figure 28. Overcurrent Detection Current/Peak Current vs Junction Temperature

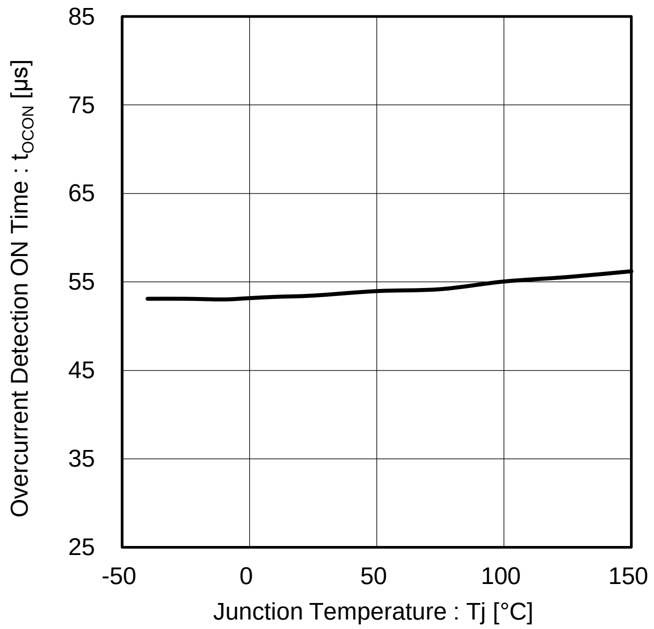


Figure 29. Overcurrent Detection ON Time vs Junction Temperature

Typical Performance Curves - continued
(Unless otherwise specified V_{BB} = 14 V, V_{IN} = 5 V, Tj = 25 °C)

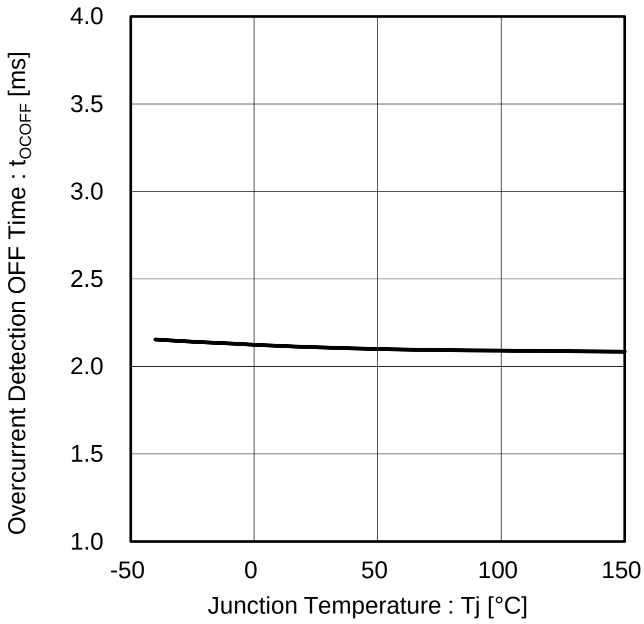


Figure 30. Overcurrent Detection OFF Time vs Junction Temperature

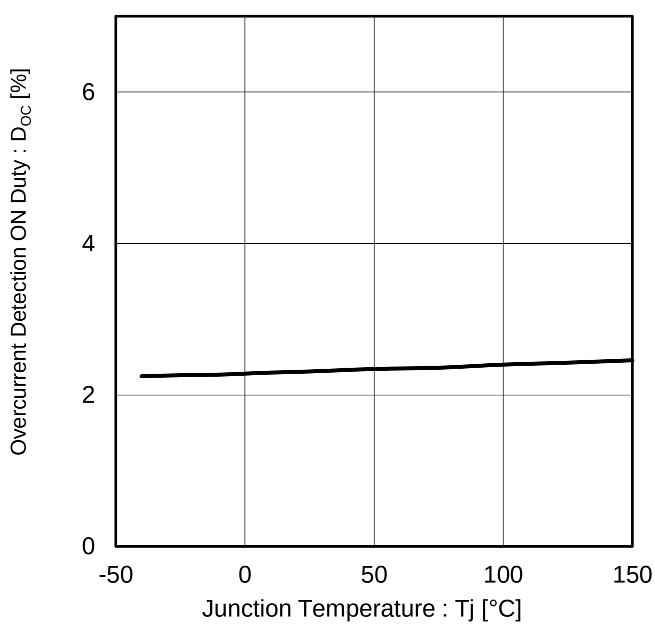


Figure 31. Overcurrent Detection ON Duty vs Junction Temperature

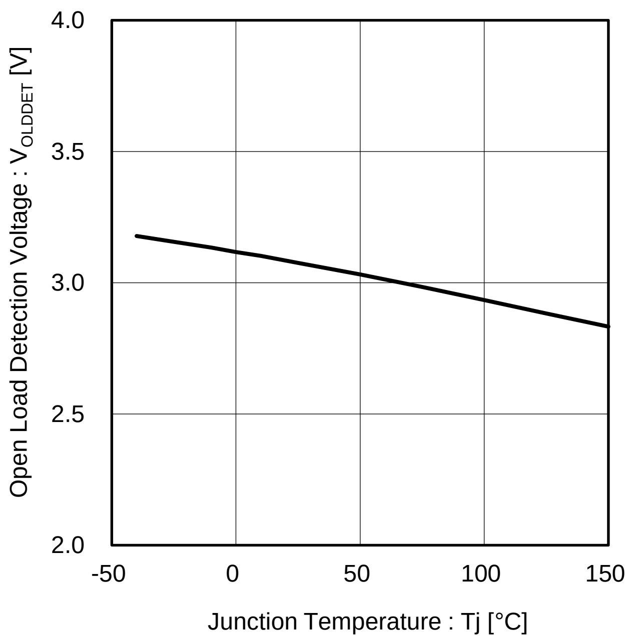


Figure 32. Open Load Detection Voltage vs Junction Temperature

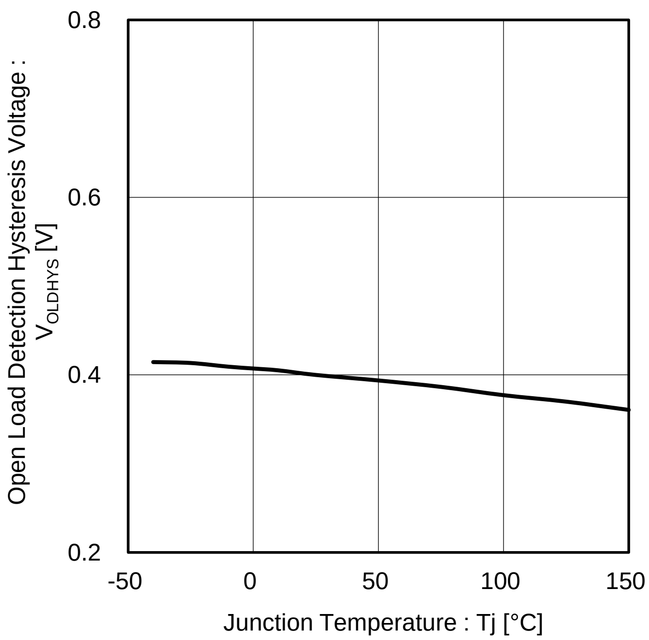


Figure 33. Open Load Detection Hysteresis Voltage vs Junction Temperature

Typical Performance Curves - continued
(Unless otherwise specified V_{BB} = 14 V, V_{IN} = 5 V, Tj = 25 °C)

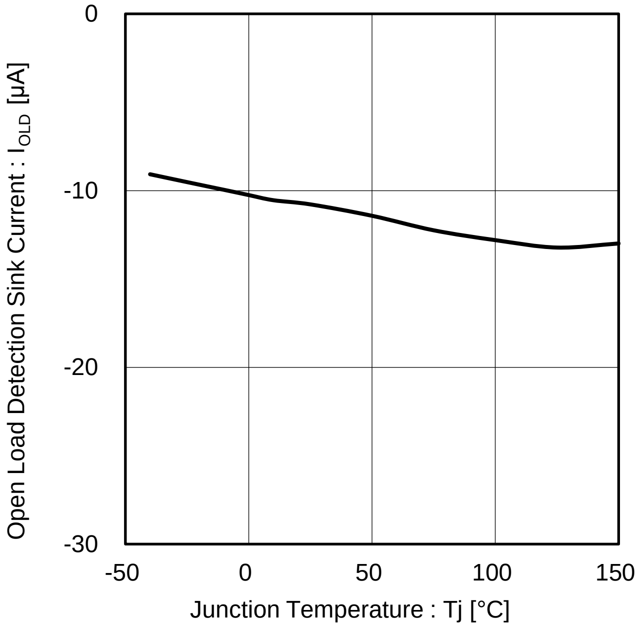


Figure 34. Open Load Detection Sink Current vs Junction Temperature

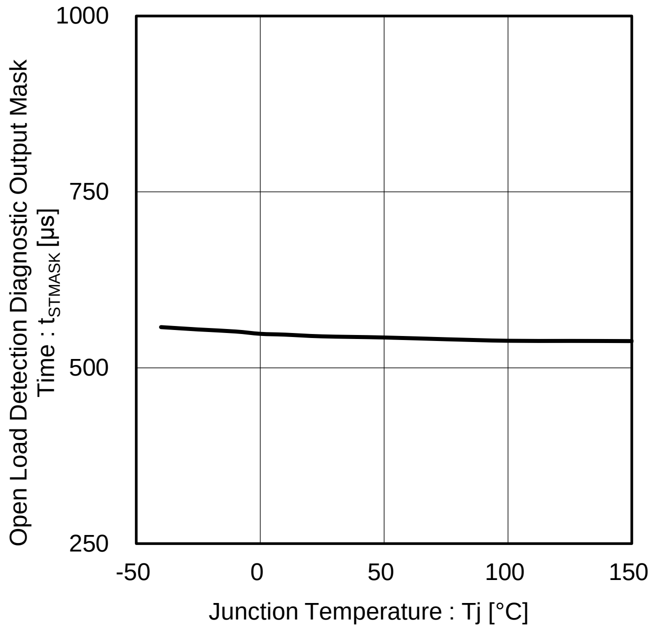


Figure 35. Open Load Detection Diagnostic Output Mask Time vs Junction Temperature

Measurement Circuits

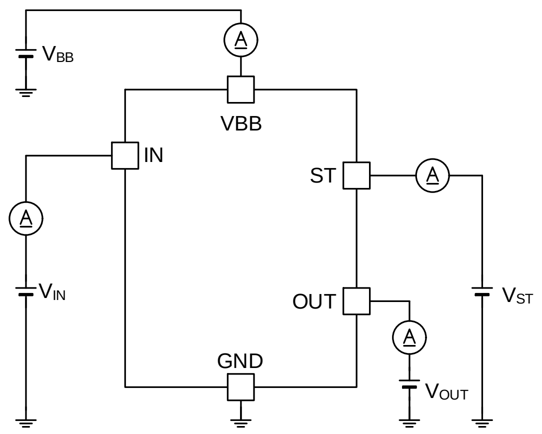


Figure 36. Standby Current
Low Level Input Current
Output Leak Current
Diagnostic Output Leak Current
Overcurrent Detection Current
Overcurrent Detection Peak Current
Overcurrent Detection ON Time
Overcurrent Detection OFF Time
Overcurrent Detection ON Duty

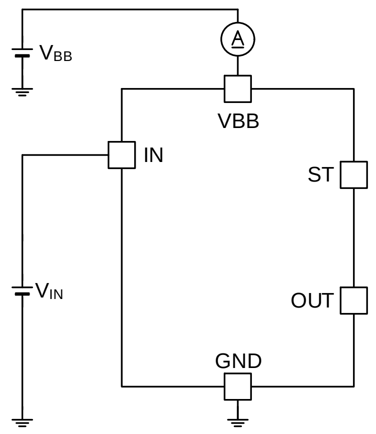


Figure 37. Operating Current

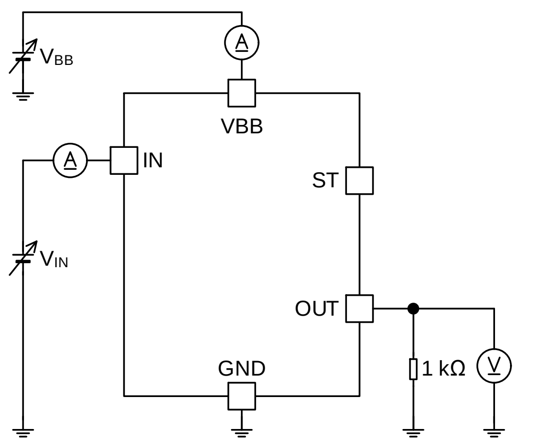


Figure 38. UVLO Detection Voltage
UVLO Release Voltage
UVLO Hysteresis Voltage
High Level Input Voltage
Low Level Input Voltage
Input Hysteresis Voltage
High Level Input Current
Thermal Shutdown Detection Temperature
Thermal Shutdown Hysteresis Temperature

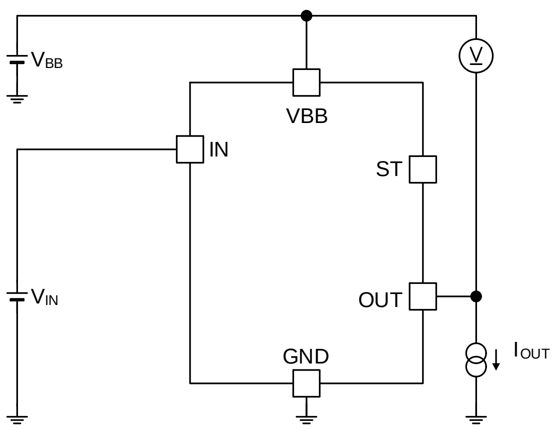


Figure 39. Output ON Resistance
Output Clamp Voltage

Measurement Circuits - continued

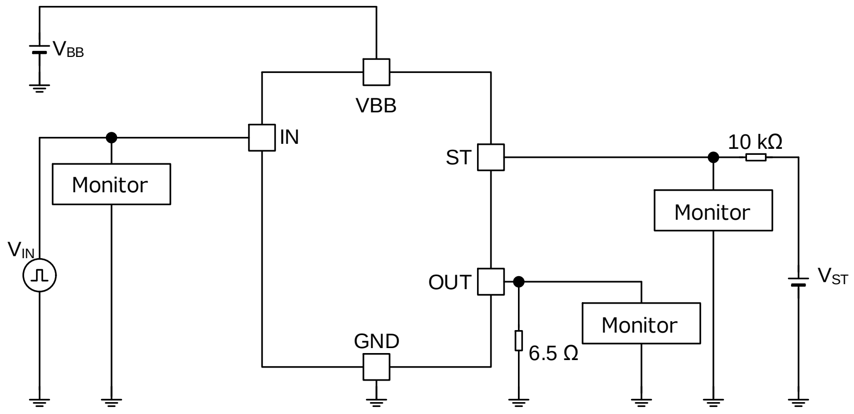


Figure 40. Output Slew Rate when ON
Output Slew Rate when OFF
Output Propagation Delay Time when ON
Output Propagation Delay Time when OFF
Diagnostic Output Propagation Delay Time when ON
Diagnostic Output Propagation Delay Time when OFF

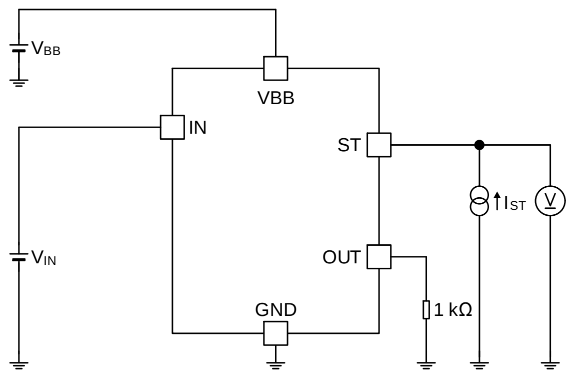


Figure 41. Diagnostic Output Low Voltage

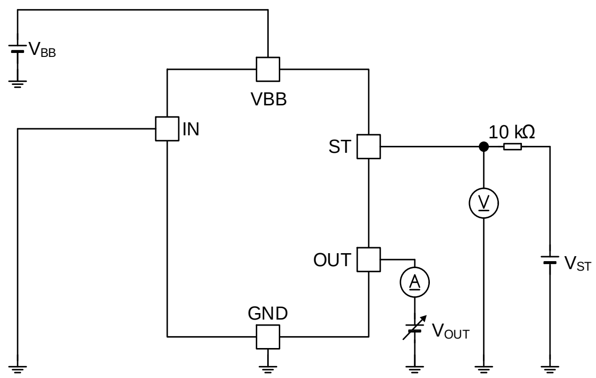


Figure 42. Open Load Detection Voltage
Open Load Detection Hysteresis Voltage
Open Load Detection Sink Current
Open Load Detection Diagnostic Output Mask Time

Measurement Conditions for Time Items

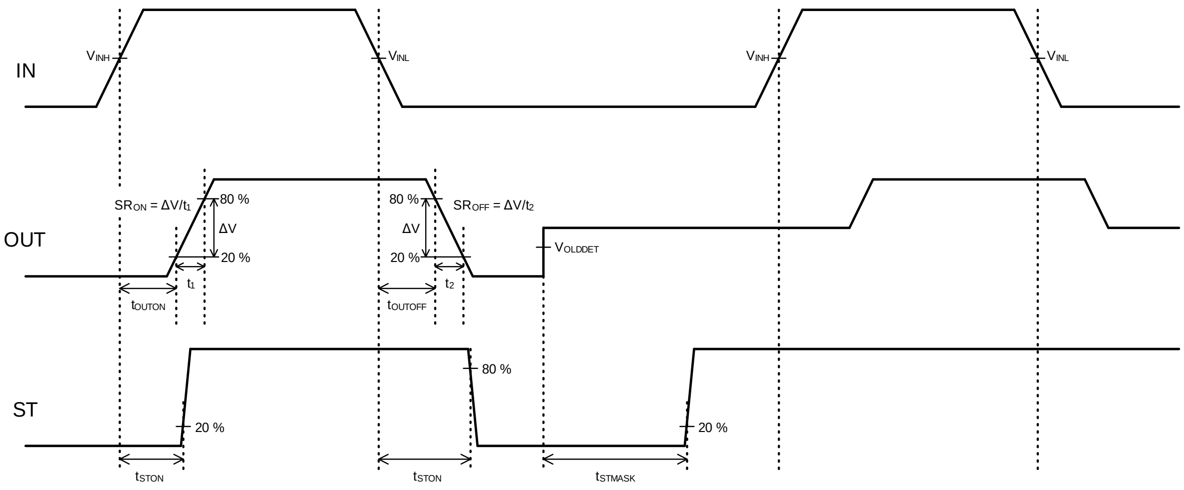


Figure 43. Output Slew Rate when ON
Output Slew Rate when OFF
Output Propagation Delay Time when ON
Output Propagation Delay Time when OFF
Diagnostic Output Propagation Delay Time when ON
Diagnostic Output Propagation Delay Time when OFF
Open Load Detection Diagnostic Output Mask Time

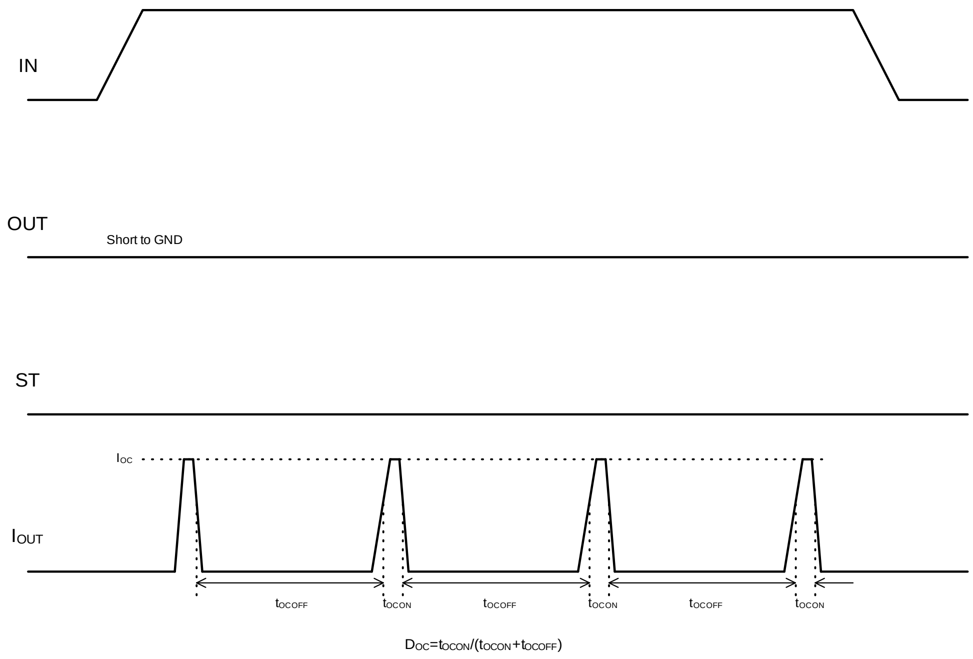


Figure 44. Overcurrent Detection Current
Overcurrent Detection Peak Current
Overcurrent Detection ON Time
Overcurrent Detection OFF Time
Overcurrent Detection ON Duty

Timing Chart

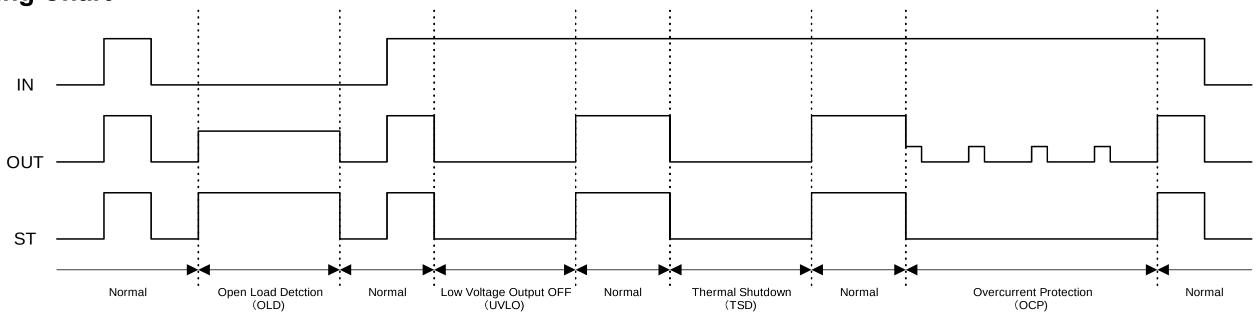


Figure 45. Timing Chart

Description of Blocks

1. Protection Functions

Table 1. Detection and Release Conditions and Diagnostic Output of Each Protection Function

Mode		Detection/Release Conditions	Input IN	Diagnostic Output ST
Normal Condition	Standby	-	Low	Low
	Operating	-	High	High
Open Load Detect (OLD)		Detect V_{OUT} ≥ 3.0 V (Typ)	Low	High
		Release V_{OUT} ≤ 2.6 V (Typ)	Low	Low
Thermal Shutdown Protection (TSD)*(Note 1)*		Detect Tj ≥ 175 °C (Typ)	High	Low
		Release Tj ≤ 160 °C (Typ)	High	High
Overcurrent Protection (OCP) *(Note 2)*		Detect I_{OUT} ≥ 5.5 A (Typ)	High	Low
		Release I_{OUT} < 5.5 A (Typ)	High	High

(Note 1) Thermal shutdown is automatically restored to normal operation.
(Note 2) Overcurrent protection is an intermittent operation to turn the output on and off.

This IC has a built-in protection detection function as mentioned above and outputs the condition with diagnostic output pin ST.
When the output is ON, it switches from Low to High when the output voltage becomes 3.0 V (Typ) or higher.
When the output is OFF, it switches from High to Low when the output voltage falls below 2.6 V (Typ).
Each protection function will automatically recover if the release condition is met after detection, and will operate in the same way as above.

2. Thermal Shutdown Protection

This IC has a built-in overheat protection function.
When the chip temperature of the IC rises above 175 °C (Typ), the output turns off and the diagnostic output (ST) outputs Low. The output is automatically recovered when the chip temperature falls below 160 °C (Typ).

Description of Blocks - continued

3. Overcurrent Protection (Output ground fault detection)

This IC has a built-in overcurrent protection function.
If an overcurrent flows due to an output short to GND, the IC limits the current at 5.5 A (Typ) for 55 µs (Typ). Thereafter, it repeats the intermittent operation of turning the output ON and OFF. The OFF interval is 2 ms (Typ). During intermittent operation due to the output being shorted to GND, the diagnostic output (ST) goes Low (Figure 46), but if the output voltage does not fall below 2.6 V (Typ) due to overcurrent, ST switches in synchronization with the intermittent operation of the output. (Figure 47)

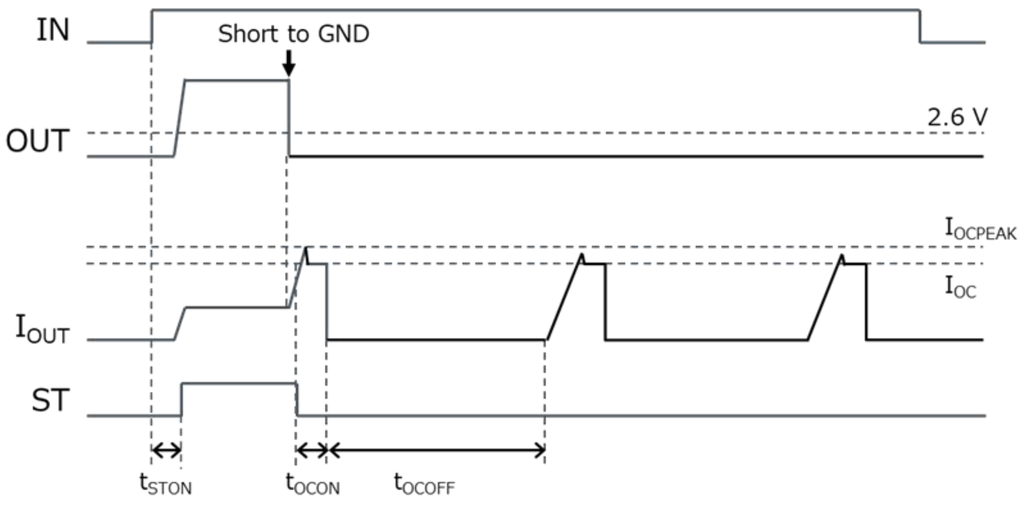


Figure 46. Overcurrent Protection Timing Chart (Short to GND)

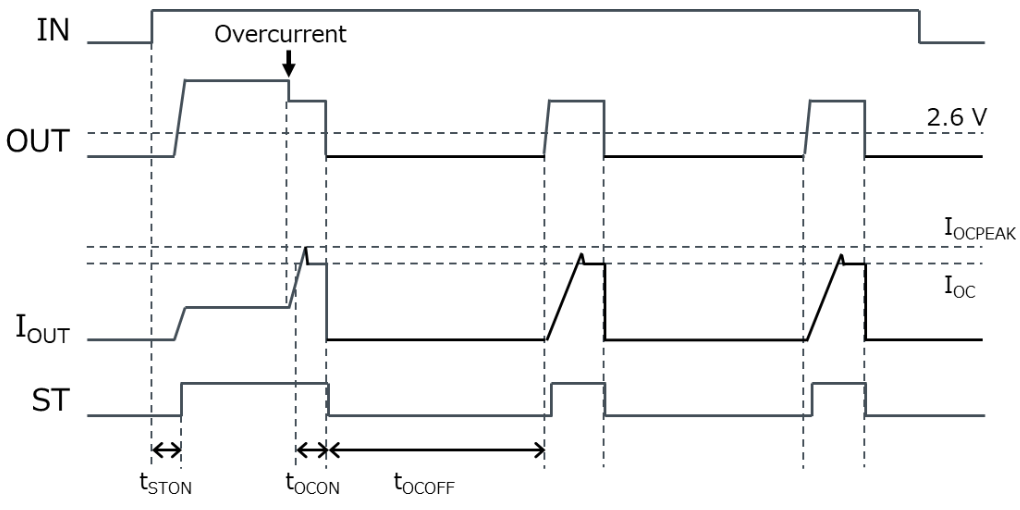


Figure 47. Overcurrent Protection Timing Chart (Overcurrent)

Description of Blocks – continued

4. Open Load Detection

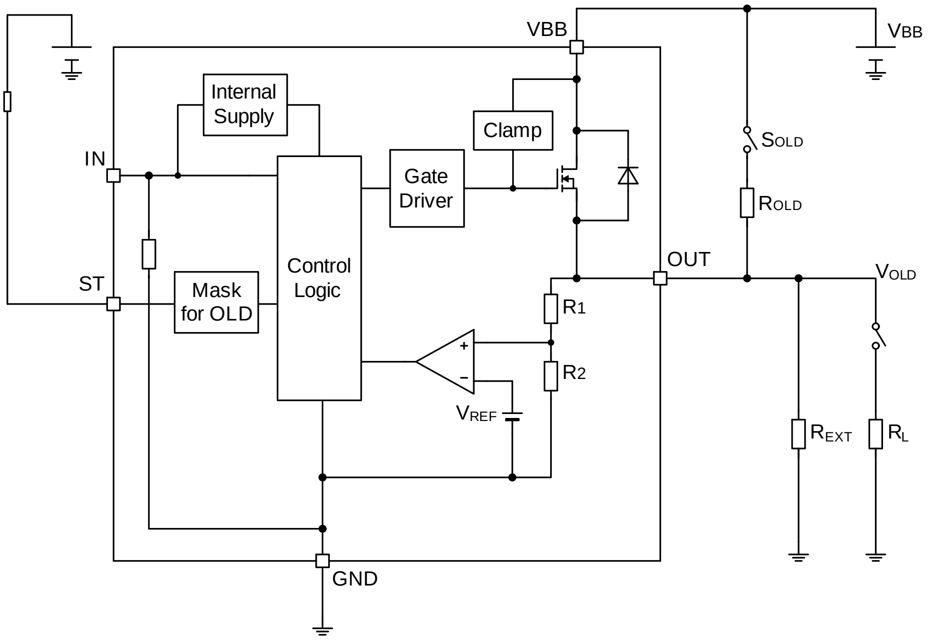


Figure 48. Open Load Detection Block Diagram

This IC can detect load disconnection by inserting an external resistor R_{OLD} between power supply VBB and output OUT.
If the output load is disconnected when input IN is Low, the ST pin outputs High.
Open Load Detection Diagnostic Output Mask Time of 1000 µs (Max) is provided to prevent detection of load open due to noise, etc.
If circuit current reduction during standby is required, it is recommended to insert a switch (S_{OLD}).

The external resistor R_{OLD} value for detecting open load can be calculated by the following formula from the maximum value of Open Load Detection Voltage V_{OLD} and the minimum value of power supply voltage V_{BB} used.
R_{EXT} is the output pull-down resistor other than the load R_L.

$$R_{OLD} < \frac{V_{BB(Min)} \times \left(R_{1(Min)} + R_{2(Min)} \right) // R_{EXT}}{V_{OLD(\mathrm{Max})}} - \left(R_{1(Min)} + R_{2(Min)} \right) // R_{EXT} \quad [\Omega]$$

Substituting constants into the above equation yields the following equation.

$$R_{OLD} < V_{BB(Min)} \times 75 \times 10^3 - 300 \times 10^3 \quad [\Omega]$$

R_{OLD} should be set to less than the resistance calculated by the above formula.

Description of Blocks - continued

5. Other Protection

5.1 GND Open Protection

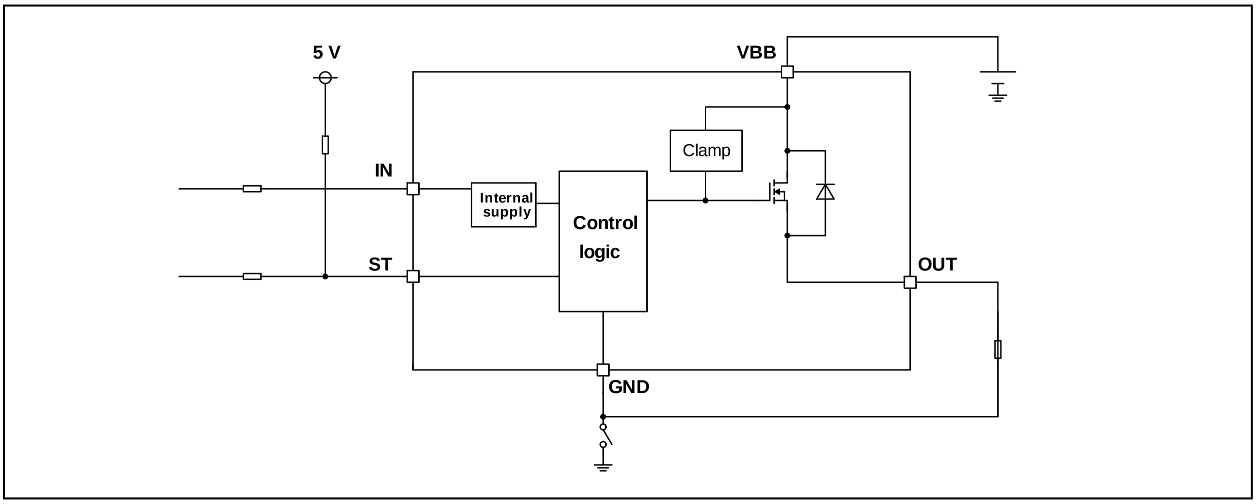


Figure 49. GND Open Protection Block Diagram

When the GND of the IC is open, the output switches to OFF regardless of the IN voltage.
(However, the self-diagnostic output ST is disabled.)
If an inductive load is connected, the GND pin open causes active clamp operation.

5.2 MCU I/O Protection

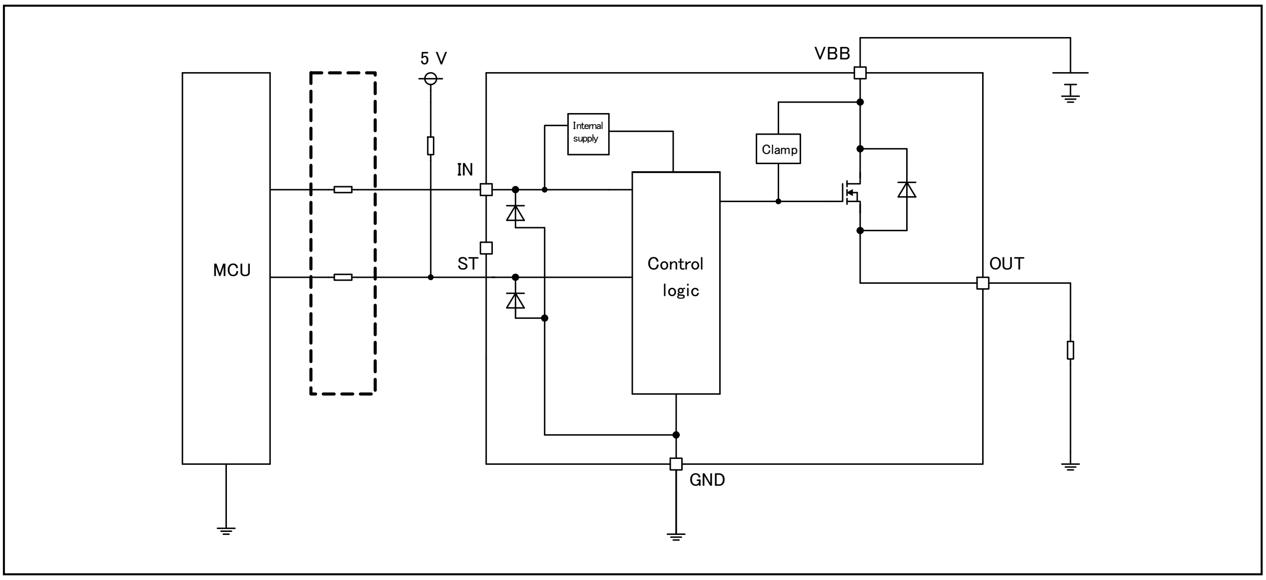
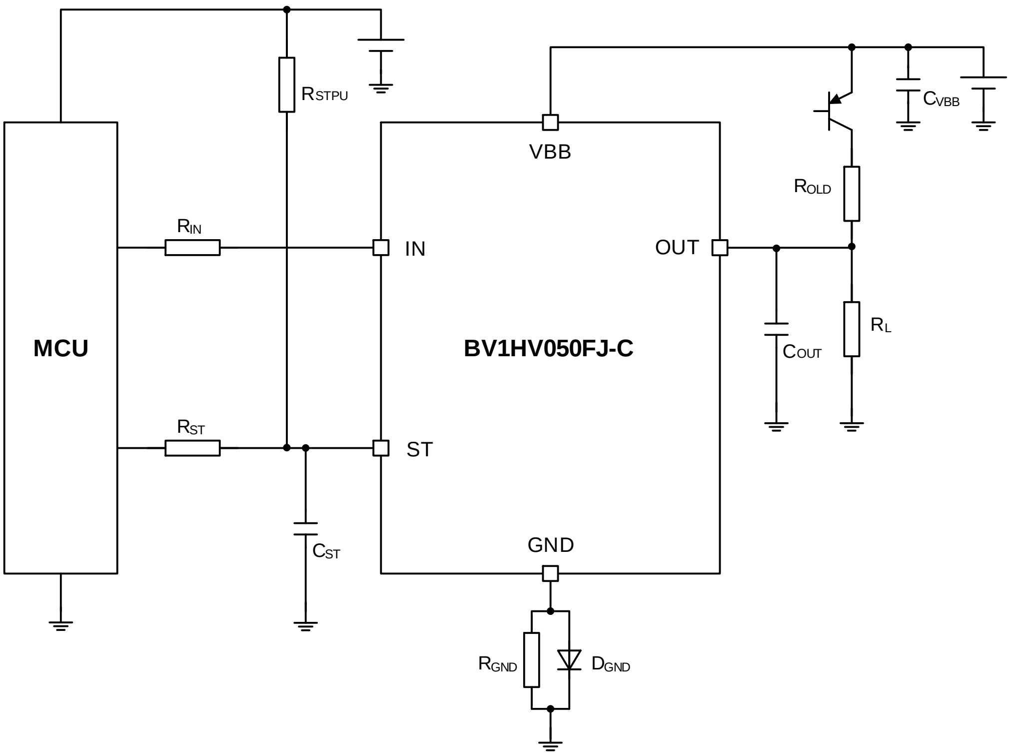


Figure 50. MCU I/O Protection Block Diagram

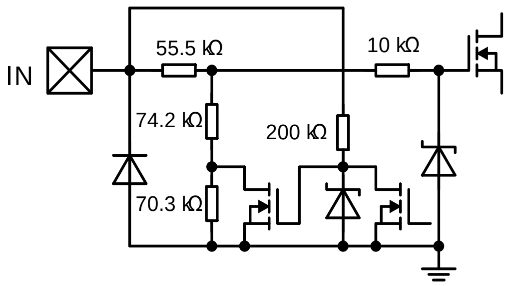
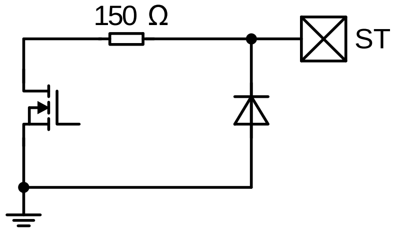
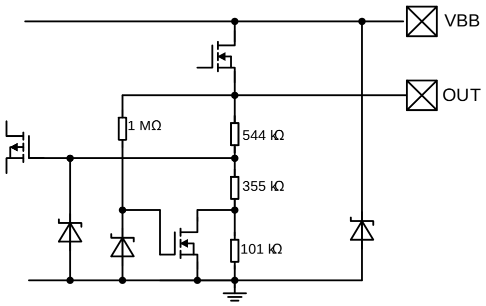
Negative surge voltage to input pin (IN) or diagnostic output pin (ST) may cause damage to the MCU's I/O pins. In order to prevent those damages, it is recommended to insert limiting resistors between IC pins and MCU.

Applications Example



Symbol	Value	Purpose
R_{IN}	1 kΩ	Limit resistance for negative surge
R_{ST}	1 kΩ	Limit resistance for negative surge
R_{STPU}	10 kΩ	Pull up resistance for diagnostic output The ST pin is open drain output and pull up to MCU power supply.
C_{VBB}	10 µF	Filter for battery line voltage spike If a surge is applied to the battery line and a sudden voltage change occurs, the IC may malfunction. If surge of 8 V/µs or more is applied, it is recommended to connect a conductive polymer aluminum electrolytic capacitor of 10 µF or more, which has low ESR even at low temperatures.
R_{GND}	1 kΩ	Current limit resistance for reverse battery connection
D_{GND}	-	Protection diode for BV1HV050FJ-C against reverse battery connection
R_{OLD}	2 kΩ	Resistance for open load detection
C_{OUT}	1000 pF	Filter for radiation noise from outside of BV1HV050FJ-C
C_{ST}	1000 pF	Filter for radiation noise from outside of BV1HV050FJ-C
R_L	-	Output load

I/O Equivalence Circuits

IN	ST
	
OUT	
	

Resistance values shown in the diagrams above represent a typical limit, respectively.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

11. **Thermal Shutdown Function (TSD)**
    This IC has a built-in thermal shutdown function that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD function that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
    Note that the TSD function operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD function be used in a set design or for any purpose other than protecting the IC from heat damage.

Operational Notes – continued

12. **Over Current Protection Function (OCP)**
This IC incorporates an integrated overcurrent protection function that is activated when the load is shorted. This protection function is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection function.

13. **Active Clamp Operation**
The IC integrates the active clamp function to internally absorb the reverse energy E_L which is generated when the inductive load is turned off. When the active clamp operates, the thermal shutdown function does not work. Decide a load so that the reverse energy E_L is active clamp energy (Single Pulse) E_{AS} (refer to Figure 5. Active Clamp Energy (Single Pulse) vs Output Current (Start)) or under when inductive load is used.

14. **Open Power Supply Pin**
When the power supply pin (VBB) becomes open at ON (IN = High), the output is switched to OFF regardless of input voltage. At this time, if an inductive load is connected, the active clamp operates. VBB voltage becomes the ground potential, and the output voltage drops down to (the ground potential – Output Clamp Voltage).

15. **Open GND Pin**
When the GND pin becomes open at ON (IN = High), the output is switched to OFF regardless of input voltage. If an inductive load is connected, the active clamp operates when the GND pin is open.

16. **OUT Pin Voltage**
Ensure that keep OUT pin voltage less than (VBB + 0.3 V) at any time, even during transient condition.

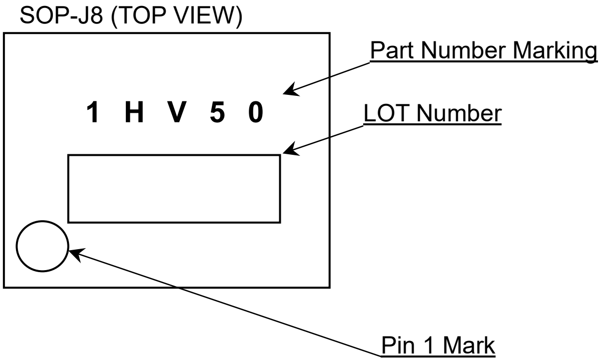
Ordering Information

B V 1 H V 0 5 0 F J - C E 2

Package
FJ: SOP-J8

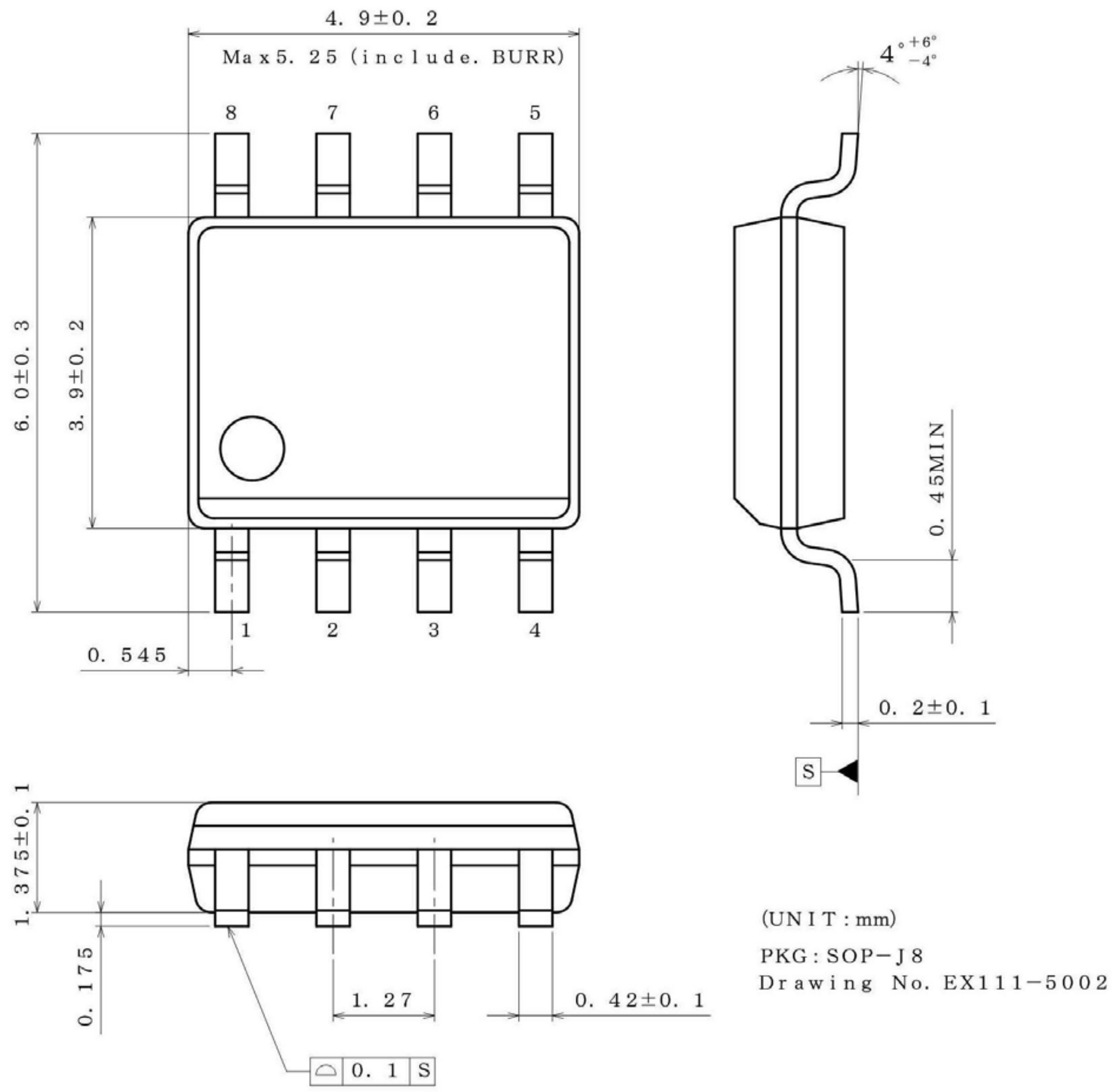
Product Rank
C: Automotive product
Packaging and Forming Specification
E2: Embossed tape and reel

Marking Diagram



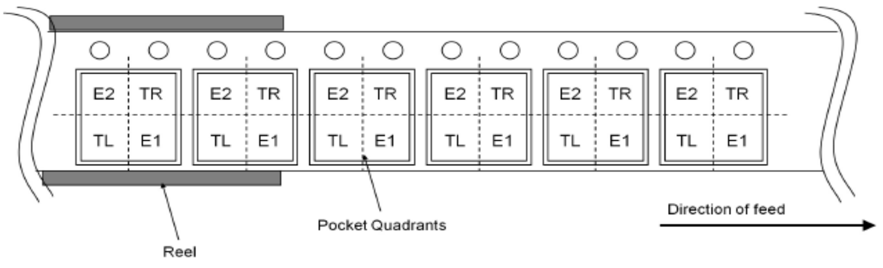
Physical Dimension and Packing Information

Package Name	SOP-J8



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
20.Jan.2023	001	New Release

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   (Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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