Voltage Detector

Voltage Detector ICs with Watchdog Timer for Automotive

BD37BxxFVM-C BD87BxxFVM-C BD87BxxG-C

General Description

BD37BxxFVM-C, BD87BxxFVM-C and BD87BxxG-C integrate a Reset (RESET) that monitors the input voltage of the microcomputer and a Watchdog Timer (WDT) that monitors the clock signal of the microcomputer. Even with its wide input voltage up to 20 V the quiescent current is kept low, making it possible to improve redundancy of various system with low current consumption. The RESET detection voltage can be selected either from fixed type or from variable type just by adjusting the external resister. Also, the RESET delay time and Watchdog monitor time can be adjusted by the external capacitor.

Features

- AEC-Q100 Qualified*(Note 1)*
- Functional Safety Supportive Automotive Products
- Qualified for Automotive Applications
- Integrated Power ON and Under-Voltage Detection Reset
- Integrated Watchdog Timer
- Adjustable Reset Delay Time and Watchdog Monitor Time by External Capacitor
- Adjustable Detection Voltage Power ON and Under-Voltage Detection Reset by External Resister*(Note 2)*

(Note 1) Grade 1
(Note 2) BD87B00FVM-C only

Key Specifications

- Wide Temperature Range (Ta): -40 °C to +125 °C
- Wide Input Voltage Range: -0.3 V to +20 V
- Low Quiescent Current: 3.0 µA (Typ)

Packages	**W (Typ) x D (Typ) x H (Max)**
MSOP8	2.9 mm x 4.0 mm x 0.9 mm
SSOP6	2.9 mm x 2.8 mm x 1.25 mm

MSOP8

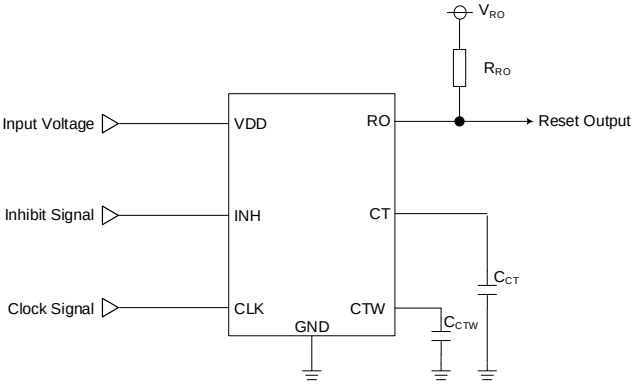
SSOP6

Applications

- Power Train
- Body Control Unit
- Car Infotainment System

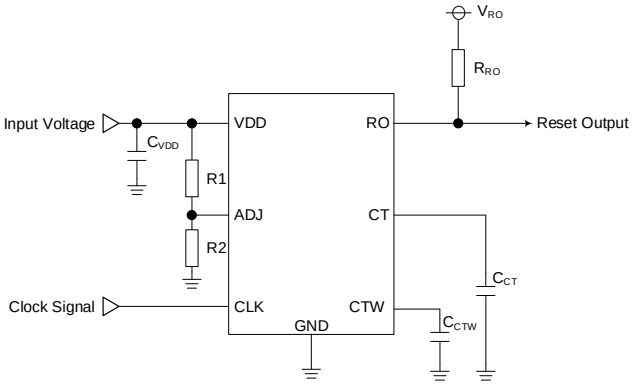
Typical Application Circuits

- External Components
  Capacitor: 0.001 µF ≤ C_{CT} ≤ 47 µF, 0.00047 µF ≤ C_{CTW} ≤ 10 µF
  Resistor: 10 kΩ (Min) ≤ R_{RO}, 10 kΩ ≤ R1 ≤ 200 kΩ, 5 kΩ ≤ R2 ≤ 150 kΩ



BD37BxxFVM-C/BD87BxxFVM-C/BD87BxxG-C*(Note 2)*

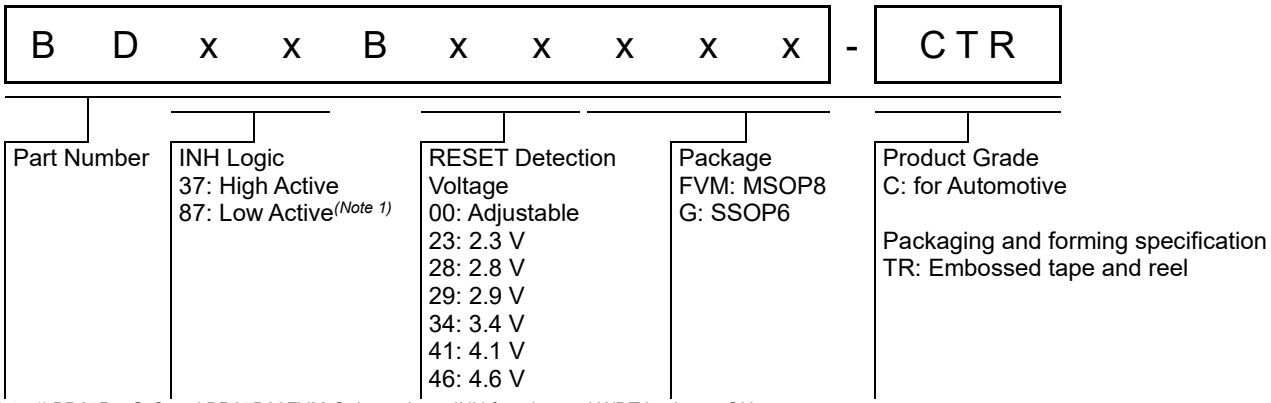
(Note 2) BD87BxxG-C do not have the INH pin, and the WDT is always ON



BD87B00FVM-C

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Ordering Information



(Note 1) BD87BxxG-C and BD87B00FVM-C do not have INH function and WDT is always ON.

Lineup

BD37Bxx

RESET Detection Voltage	INH Logic	Package		Part Number
2.3 V	High Active	MSOP8	Reel of 3000	BD37B23FVM-CTR
2.8 V				BD37B28FVM-CTR
2.9 V				BD37B29FVM-CTR
3.4 V				BD37B34FVM-CTR
4.1 V				BD37B41FVM-CTR
4.6 V				BD37B46FVM-CTR

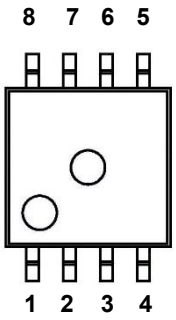
BD87Bxx

RESET Detection Voltage	INH Logic	Package		Part Number
Adjustable	No INH Function (WDT is always ON)	MSOP8	Reel of 3000	BD87B00FVM-CTR
2.3 V	Low Active			BD87B23FVM-CTR
2.8 V				BD87B28FVM-CTR
2.9 V				BD87B29FVM-CTR
3.4 V				BD87B34FVM-CTR
4.1 V				BD87B41FVM-CTR
4.6 V				BD87B46FVM-CTR
2.3 V	No INH Function (WDT is always ON)	SSOP6	Reel of 3000	BD87B23G-CTR
2.8 V				BD87B28G-CTR
2.9 V				BD87B29G-CTR
3.4 V				BD87B34G-CTR
4.1 V				BD87B41G-CTR
4.6 V				BD87B46G-CTR

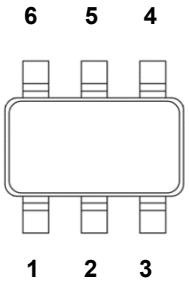
Contents

Pin Configurations

MSOP8
(TOP VIEW)



SSOP6
(TOP VIEW)



Pin Descriptions

BD37BxxFVM-C
BD37B23/28/29/34/41/46FVM-C

Pin No.	Pin Name	Function
1	CLK	Clock Signal Input
2	CT	RESET Delay Time Setting
3	CTW	WDT Monitor Time Setting
4	VDD	Power Input
5	N.C.	-
6	GND	Ground
7	INH	WDT ON/OFF Input
8	RO	RESET Output

BD87BxxG-C
BD87B23/28/29/34/41/46G-C

Pin No.	Pin Name	Function
1	CLK	Clock Signal Input
2	GND	Ground
3	CT	RESET Delay Time Setting
4	CTW	WDT Monitor Time Setting
5	RO	RESET Output
6	VDD	Power Input

BD87BxxFVM-C
BD87B23/28/29/34/41/46FVM-C

Pin No.	Pin Name	Function
1	CTW	WDT Monitor Time Setting
2	CT	RESET Delay Time Setting
3	CLK	Clock Signal Input
4	GND	Ground
5	VDD	Power Input
6	INH	WDT ON/OFF Input
7	N.C.	-
8	RO	RESET Output

BD87BxxFVM-C
BD87B00FVM-C

Pin No.	Pin Name	Function
1	CTW	WDT Monitor Time Setting
2	CT	RESET Delay Time Setting
3	CLK	Clock Signal Input
4	GND	Ground
5	VDD	Power Input
6	ADJ	RESET Detection Voltage Setting
7	N.C.	-
8	RO	RESET Output

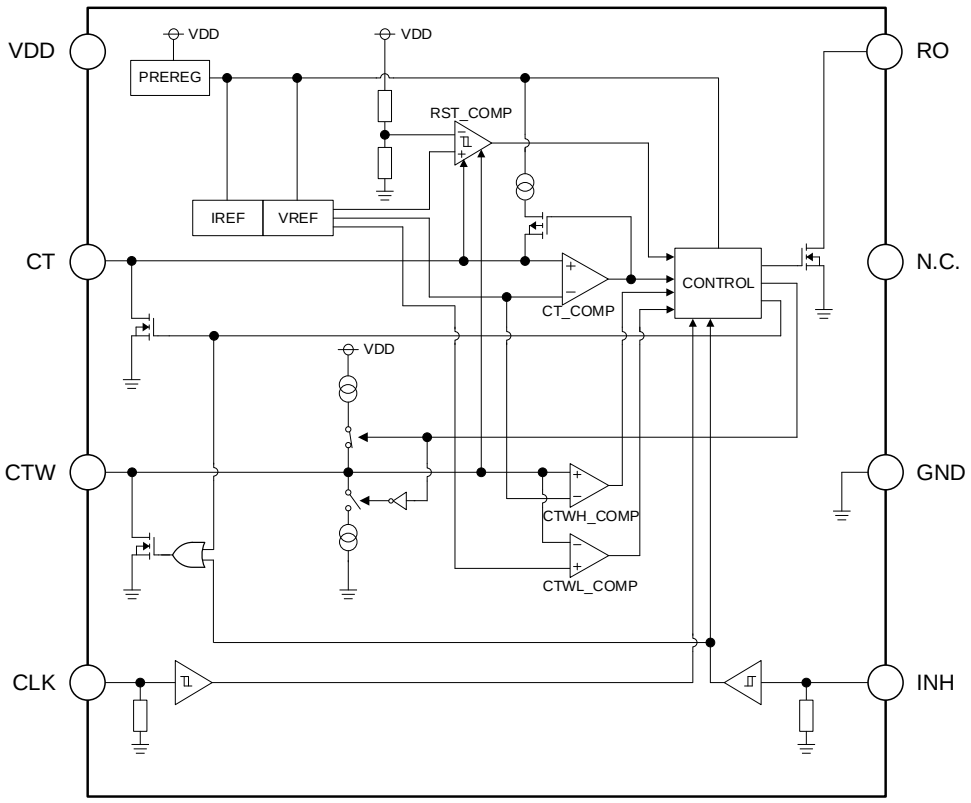
Pin Descriptions - continued

Pin Name	Function	Descriptions	
CLK	Clock Signal Input	This pin is an input of CLK signal(Note 1) from Microcomputer. Pull-down resistors are implemented in the IC. If this pin is open, the input state is kept as low.	
CT	RESET Delay Time Setting	This pin sets RESET Delay Time. It is necessary to connect a capacitor which is from 0.001 µF (Min) to 47 µF (Max) between the CT pin and GND.	
CTW	WDT Monitor Time Setting	This pin sets WDT Monitor Time. It is necessary to connect a capacitor which is from 0.00047 µF (Min) to 10 µF (Max) between the CTW pin and GND.	
VDD	Power Input	This pin is an input of IC to supply the input voltage.	
N.C.	-	This pin is not connected to the chip. It can keep open or it's also possible to connect to GND(Note 2).	
GND	GND	This is Ground pin. It shall be connected to the lowest potential.	
INH	WDT ON/OFF	This pin enables or disables WDT by High/Low input(Note 1). Pull-down resisters are implemented in IC. The input state is low, if this pin is open.	
		BD37BxxFVM-C (High Active) High Voltage: WDT function ON Low Voltage: WDT function OFF	BD87BxxFVM-C (Low Active) High Voltage: WDT function OFF Low Voltage: WDT function ON
RO	RESET Output	This pin is RESET Output. It should connect a resister which is 10 kΩ (Min) or higher between VDD pin and RO pin to pull-up, because the output construction is made by Open - drain. It is also possible to pull-up via resistor to any voltage below the maximum rating.	
ADJ(Note 3)	RESET Detection Voltage Setting	This pin sets RESET Detection Voltage. It is necessary to connect resistors between the VDD pin and the ADJ pin and also between the ADJ pin and GND.	

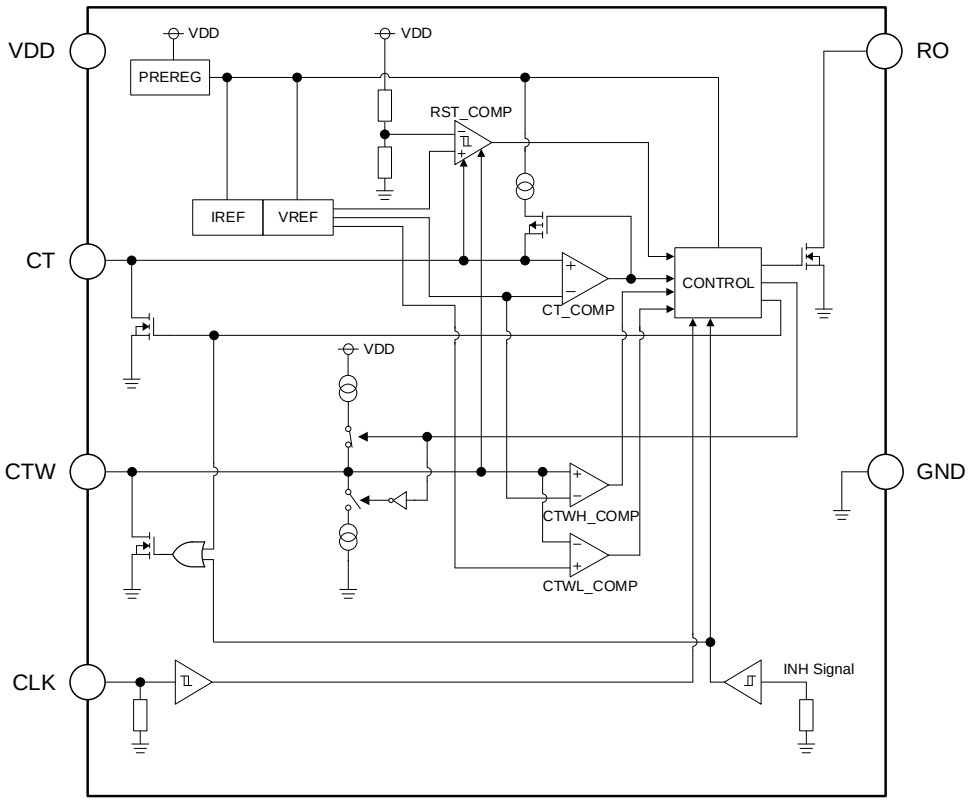
(Note 1) CLK Input High/Low Level Voltage which is described in WDT and RESET Function of Electrical Characteristics should be supplied to the CLK pin.
INH Input High/Low Level Voltage which is also described in WDT and RESET Function of Electrical Characteristics should be supplied to the INH pin.
It is not allowed to supply the input state keeping the midpoint potential voltage which to switch between High and Low.
(Note 2) If N.C. is shorted to GND, confirm if there is any problem with the actual application such as shorting of adjacent pins.
(Note 3) BD87B00FVM-C only.

Block Diagrams

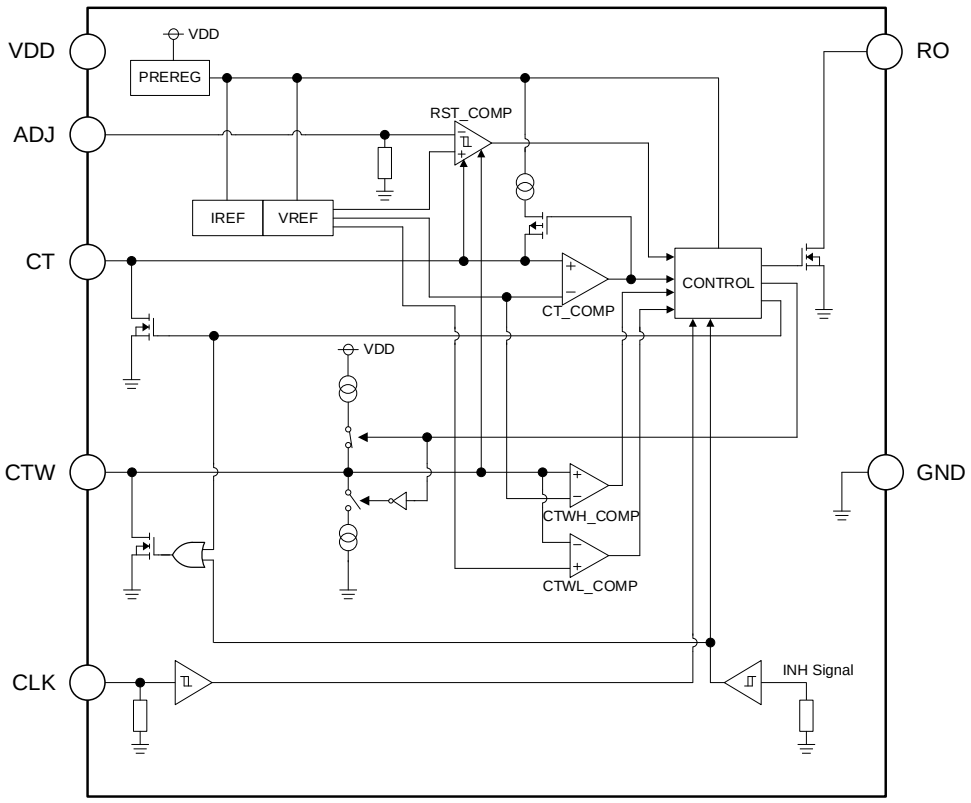
BD37BxxFVM-C, BD87BxxFVM-C (xx: 23/28/29/34/41/46)



BD87BxxG-C (xx: 23/28/29/34/41/46)



Block Diagrams - continued
BD87B00FVM-C



Description of Blocks

Block Name	Description of Blocks
PREREG	Provides Power Supply for the Internal circuit.
IREF	Generates for the Constant Current for the Internal Circuit.
VREF	Generates for the Reference Voltage for the Internal Circuit.
RST_COMP	Outputs a signal compared VDD voltage and the Reference Voltage to the CONTROL Block.
CT_COMP	Outputs a signal compared CT voltage and the Reference Voltage to the CONTROL Block.
CTWH_COMP	Outputs a signal of CTW Upper-side Threshold compared CTW voltage and the Reference Voltage to the CONTROL Block.
CTWL_COMP	Outputs a signal of CTW Lower-side Threshold compared CTW voltage and the Reference Voltage to the CONTROL Block.
CONTROL	Controls Reset and Watchdog operation depending on each state of VDD voltage, CT voltage, CTW voltage, INH voltage and CLK signal.

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	-0.3 to +40.0	V
CT Voltage	V_{CT}	-0.3 to +7.0 (≤ V_{DD} + 0.3)	V
CTW Voltage	V_{CTW}	-0.3 to +20.0(≤ V_{DD} + 0.3)	V
CLK Voltage	V_{CLK}	-0.3 to +7.0(≤ V_{DD} + 0.3)	V
INH Voltage	V_{INH}	-0.3 to +20.0 (≤ V_{DD} + 0.3)	V
RO Voltage	V_{RO}	-0.3 to +20.0	V
ADJ Voltage	V_{ADJ}	-0.3 to +20.0	V
Junction Temperature Range	Tj	-40 to +150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
MSOP8				
Junction to Ambient	θ_{JA}	284.1	135.4	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	21	11	°C/W
SSOP6				
Junction to Ambient	θ_{JA}	376.5	185.4	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	40	30	°C/W

(Note 1) Based on JESD51-2A(Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

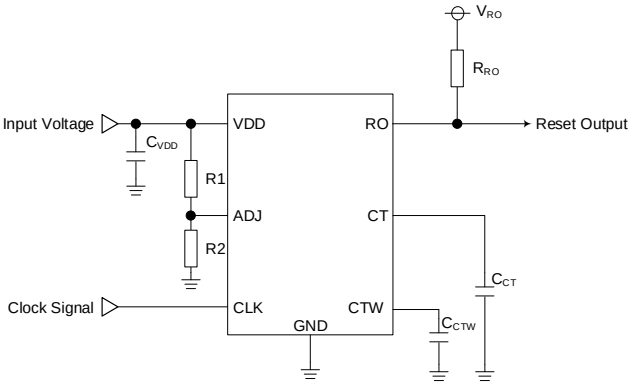
Operating Conditions (-40 °C ≤ Tj ≤ +125 °C)

Parameter	Symbol	Min	Max	Unit
Operating Voltage*(Note 1)*	V_{DD}	2	20	V
CT Capacitor	C_{CT}	0.001	47	µF
CTW Capacitor	C_{CTW}	0.00047	10	µF
RO Pull-up Resister	R_{RO}	10	-	kΩ
Operating Temperature	Ta	-40	+125	°C

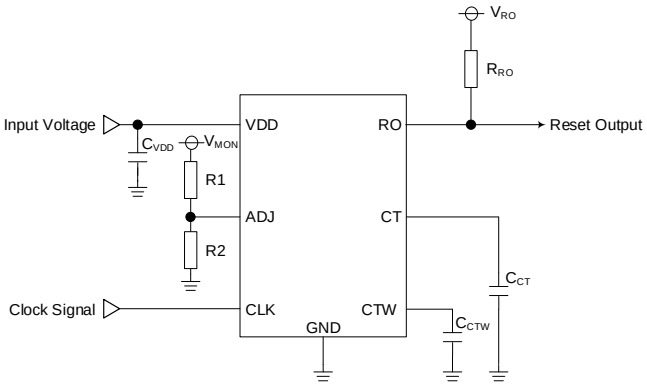
(Note 1) This voltage is the minimum input voltage to be able to start operating RESET function.
The minimum operating voltage of WDT is RESET Detection Voltage (V_{DET}) + RESET Detection Hysteresis (V_{RHY}).

BD87B00FVM-C

Parameter		Symbol	Min	Max	Unit
RESET Detection Voltage Setting Ratings	When monitoring VDD voltage	$V_{ADJDET1}$	2.1	19	V
	When monitoring other voltage than VDD	$V_{ADJDET2}$	0.96	VDD - 1	V
Monitor Voltage Pin - ADJ Pin Connecting Resister		R1	10	200	kΩ
ADJ Pin - GND Connecting Resister		R2	5	150	kΩ



When monitoring VDD voltage



When monitoring other voltage than VDD

Reset Detection Voltage Setting Way

Reset Detection Voltage can be adjusted by connecting external resisters R1 and R2. Refer to the above operating conditions for the range of use of the resisters. And set the resistance value based on the following formula in consideration of component characteristics such as component variation and temperature characteristics.

$$V_{DET} = V_{ADJDET} \times \frac{R1 + R2}{R2}$$

Electrical Characteristics

Unless otherwise specified, -40 °C ≤ Tj ≤ +125 °C, V_{DD} = 5.0 V, V_{INH} = GND (BD37Bxx) / V_{INH} = 5.0 V(BD87Bxx), R_{RO} = 10 kΩ, the typical value is defined at Tj = +25 °C

Parameter		Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
Circuit Current 1 (WDT OFF)		I_{CC1}	-	3.0	-	µA	Tj = +25 °C V_{INH} = GND (BD37Bxx) V_{INH} = 5.0 V (BD87Bxx)
Circuit Current 2 (WDT OFF)		I_{CC2}	-	3.0	9.0	µA	-40 °C ≤ Tj ≤ +125 °C V_{INH} = GND (BD37Bxx) V_{INH} = 5.0 V (BD87Bxx)
Circuit Current 3 (WDT ON)		I_{CC3}	-	4.5	-	µA	-40 °C ≤ Tj ≤ +125 °C V_{INH} = 5.0 V (BD37Bxx) V_{INH} = GND (BD87Bxx) C_{CT} = 0.01 µF, C_{CTW} = 0.0047 µF
RO Leakage Current		I_{LEAK}	-	-	1	µA	V_{DD} = V_{RO} = 5.0 V *(Note 1)*
RO Current Capability 1		I_{OL1}	0.4	-	-	mA	V_{DD} = 1.0 V, V_{RO} = 0.5 V
RO Current Capability 2		I_{OL2}	2.0	-	-	mA	V_{DD} = 2.0 V, V_{RO} = 0.5 V
RESET Detection Voltage	2.3 V	V_{DET}	V_{DET} (Typ) x (-2 %)	2.30	V_{DET} (Typ) x (+2 %)	V	
	2.8 V	V_{DET}	V_{DET} (Typ) x (-2 %)	2.80	V_{DET} (Typ) x (+2 %)	V	
	2.9 V	V_{DET}	V_{DET} (Typ) x (-2 %)	2.90	V_{DET} (Typ) x (+2 %)	V	
	3.4 V	V_{DET}	V_{DET} (Typ) x (-2 %)	3.40	V_{DET} (Typ) x (+2 %)	V	
	4.1 V	V_{DET}	V_{DET} (Typ) x (-2 %)	4.10	V_{DET} (Typ) x (+2 %)	V	
	4.6 V	V_{DET}	V_{DET} (Typ) x (-2 %)	4.60	V_{DET} (Typ) x (+2 %)	V	
RESET Detection Hysteresis		V_{RHY}	V_{RHY} (Typ) x (-45 %)	V_{DET} x (+3.6 %)	V_{RHY} (Typ) x (+45 %)	V	
ADJ Pin RESET Detection Voltage		V_{ADJDET}	0.882	0.900	0.918	V	*(Note 2)*
ADJ Pin RESET Detection Hysteresis		V_{ADJRHY}	17	32	60	mV	*(Note 2)*
ADJ Input Current		I_{ADJ}	-	24	70	nA	V_{ADJ} = 0.95 V *(Note 2)*

(Note 1) V_{RO} is the voltage applied to the RO pin.
(Note 2) BD87B00FVM-C only

Electrical Characteristics - continued

Unless otherwise specified, -40 °C ≤ Tj ≤ +125 °C, V_{DD} = 5.0 V, V_{INH} = GND (BD37Bxx) / V_{INH} = 5.0 V (BD87Bxx), R_{RO} = 10 kΩ, the typical value is defined at Tj = +25 °C

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
CT Threshold	V_{CTTH}	-	0.9	-	V	
CT Charge Current	I_{CT_C}	-	1.3	-	μA	V_{CT} = 0.5 V
CTW Upper-side Threshold	V_{CTWH}	-	0.9	-	V	
CTW Lower-side Threshold	V_{CTWL}	-	0.3	-	V	
CTW Charge Current	I_{CTW_C}	-	0.3	-	μA	V_{CTW} = 0.2 V
CTW Discharge Current	I_{CTW_D}	-	0.9	-	μA	V_{CTW} = 1.0 V
Delay Time L→H	t_D	5.5	6.9	8.3	ms	C_{CT} = 0.01 μF *(Note 1)*
WDT Monitor Time	t_{WH}	7.5	9.4	11.5	ms	C_{CTW} = 0.0047 μF *(Note 1)*
WDT Reset Time	t_{WL}	2.5	3.2	3.9	ms	C_{CTW} = 0.0047 μF *(Note 1)*
CLK Input Current	I_{CLK}	-	0.3	2.0	μA	V_{CLK} = 5.0 V
CLK Input Pulse Width	t_{PCLK}	0.5	-	-	μs	
CLK Input High Level Voltage	V_{HCLK}	V_{DD} x 0.8	-	V_{DD}	V	*(Note 2)*
CLK Input Low Level Voltage	V_{LCLK}	0	-	V_{DD} x 0.2	V	*(Note 2)*
INH Input Current	I_{INH}	-	0.3	2.0	μA	V_{INH} = 5.0 V
INH Input High Level Voltage	V_{HINH}	V_{DD} x 0.8	-	V_{DD}	V	*(Note 2)*
INH Input Low Level Voltage	V_{LINH}	0	-	V_{DD} x 0.2	V	*(Note 2)*

(Note 1) t_D, t_{WH}, and t_{WL} can be adjustable by changing the CT and CTW pins capacitance value.
t_D [s] = 0.69 x C_{CT} [F] x 10^6
t_{WH} [s] = 2 x C_{CTW} [F] x 10^6
t_{WL} [s] = 0.67 x C_{CTW} [F] x 10^6
C_{CT} and C_{CTW} can be used even if they are below the minimum operating conditions, but the t_D, t_{WH}, and t_{WL} settings will increase depending on the delay time inside the circuit.
In addition, the deviation of the external component which are C_{CTW} and C_{CT}, (e.g.) absolute value of capacitance, DC bias, and temperature characteristic, is not considered in these formulas.
(Note 2) When using V_{DD} ≥ 5 V, calculate with V_{DD} = 5 V.

Typical Performance Curves

Unless otherwise specified, V_{DD} = 5 V, V_{INH} = GND (BD37Bxx) / V_{INH} = 5 V (BD87Bxx), R_{RO} = 10 kΩ
V_{DET} = 2.3 V

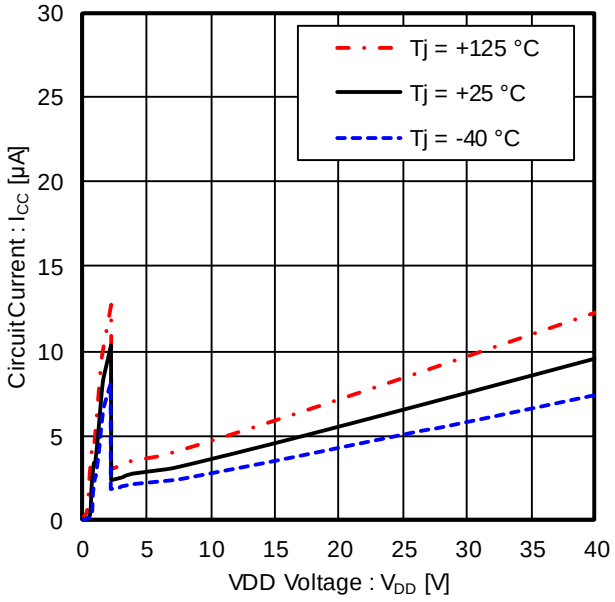


Figure 1. Circuit Current vs VDD Voltage
(V_{DET} = 2.3 V)

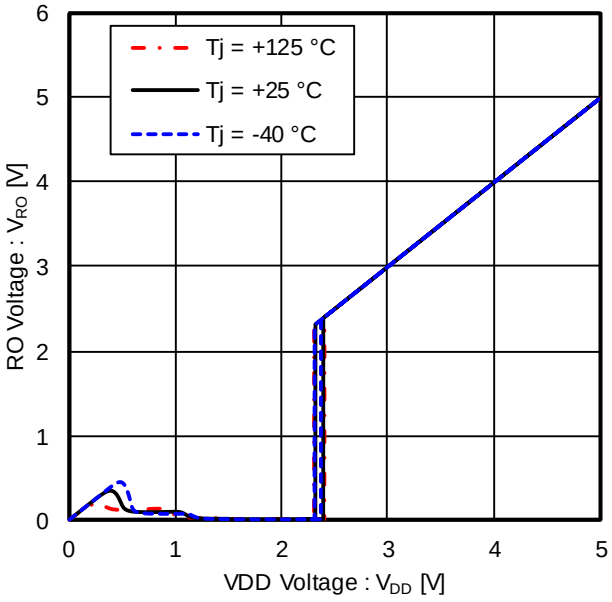


Figure 2. RO Voltage vs VDD Voltage
(Reset Detection Voltage, V_{DET} = 2.3 V)

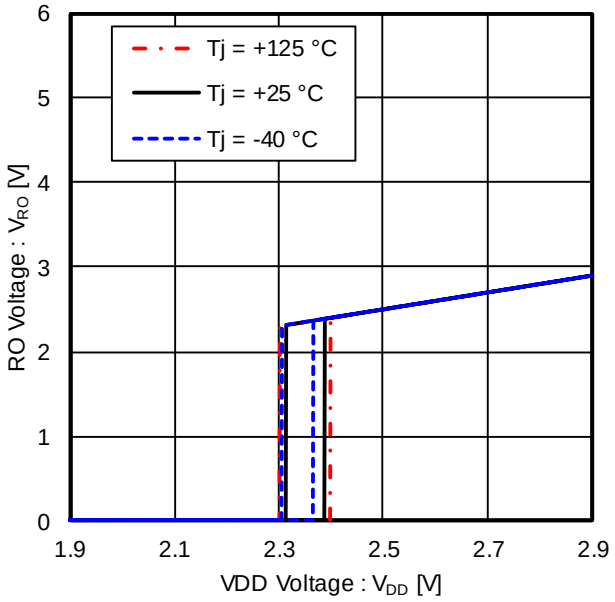


Figure 3. RO Voltage vs VDD Voltage
(Reset Detection Voltage, V_{DET} = 2.3 V, Zoom version)

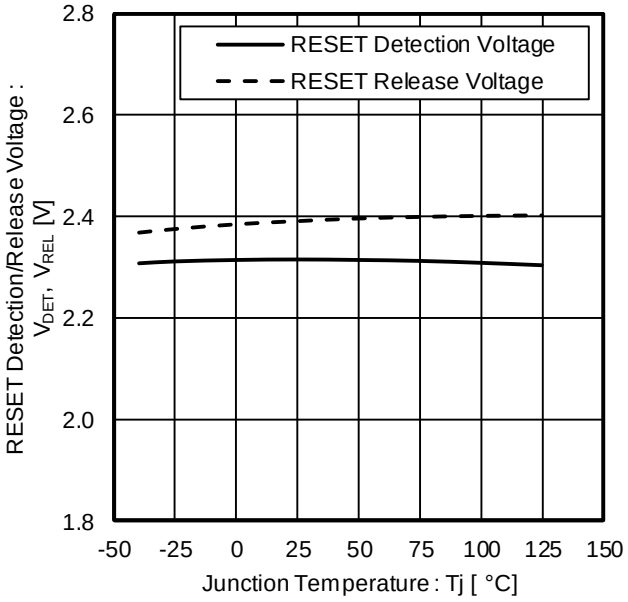


Figure 4. RESET Detection/Release Voltage vs Junction Temperature
(V_{DET} = 2.3 V)

Typical Performance Curve - continued

Unless otherwise specified, V_{DD} = 5 V, V_{INH} = GND (BD37Bxx) / V_{INH} = 5 V (BD87Bxx), R_{RO} = 10 kΩ
V_{DET} = 2.8 V

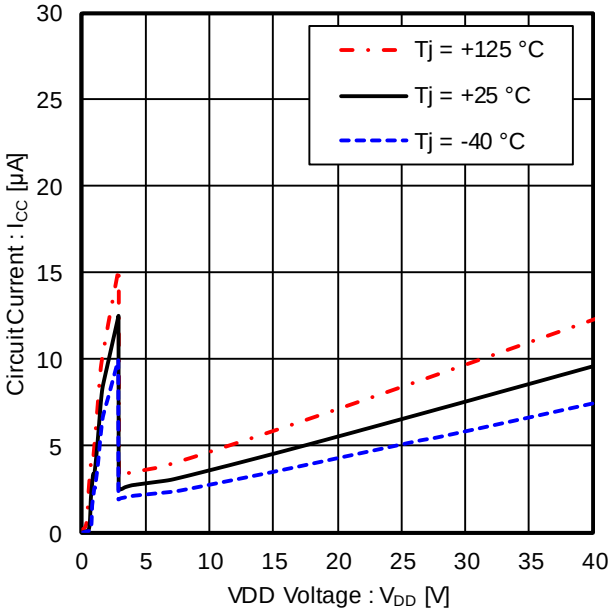


Figure 5. Circuit Current vs VDD Voltage
(V_{DET} = 2.8 V)

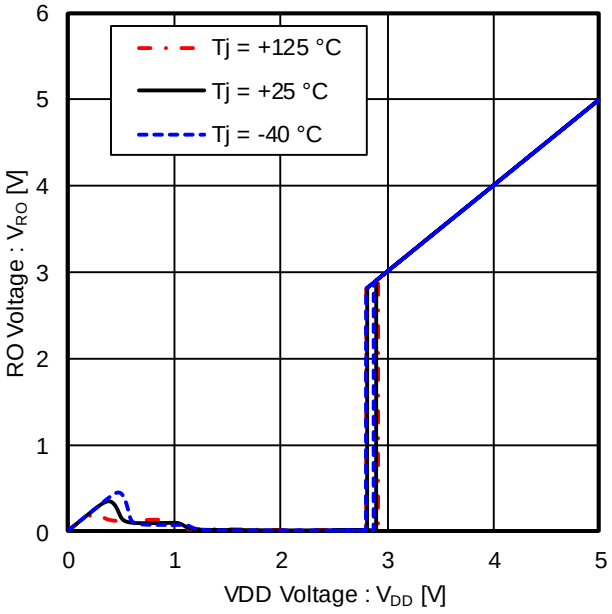


Figure 6. RO Voltage vs VDD Voltage
(Reset Detection Voltage, V_{DET} = 2.8 V)

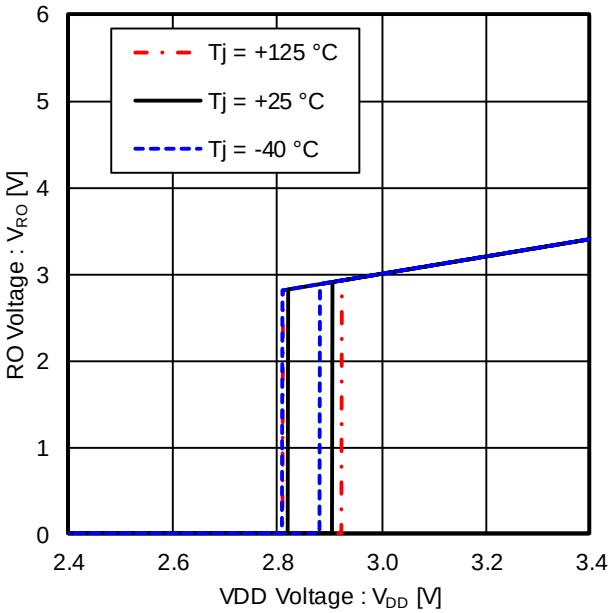


Figure 7. RO Voltage vs VDD Voltage
(Reset Detection Voltage, V_{DET} = 2.8 V, Zoom version)

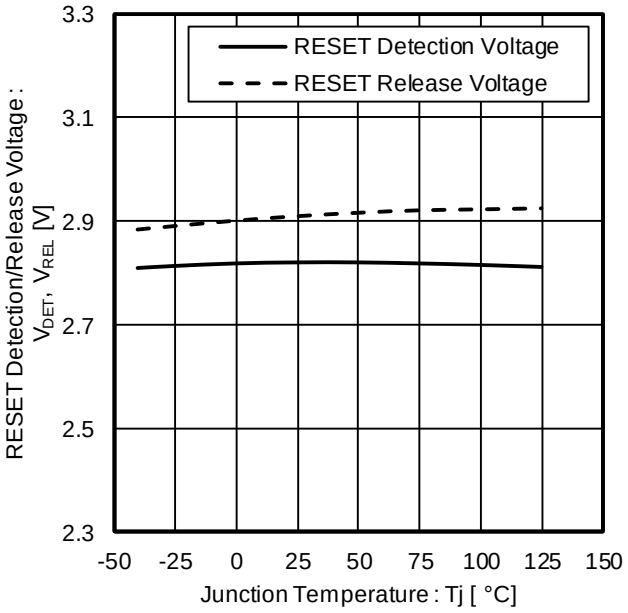


Figure 8. RESET Detection/Release Voltage vs Junction Temperature
(V_{DET} = 2.8 V)

Typical Performance Curve - continued

Unless otherwise specified, V_{DD} = 5 V, V_{INH} = GND (BD37Bxx) / V_{INH} = 5 V (BD87Bxx), R_{RO} = 10 kΩ
V_{DET} = 2.9 V

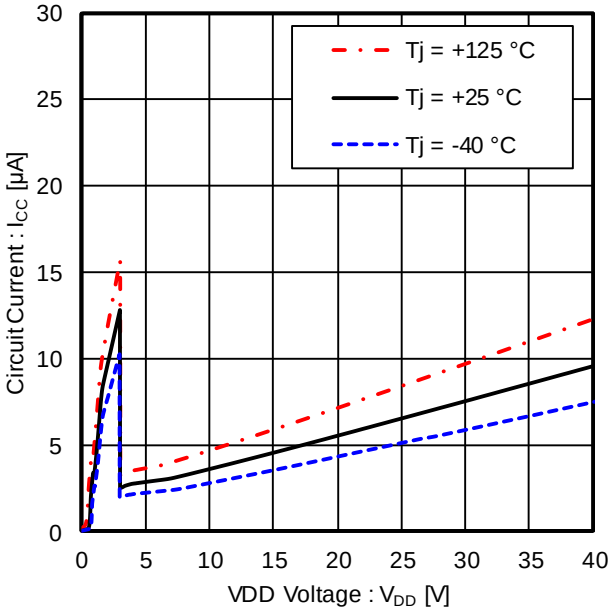


Figure 9. Circuit Current vs VDD Voltage
(V_{DET} = 2.9 V)

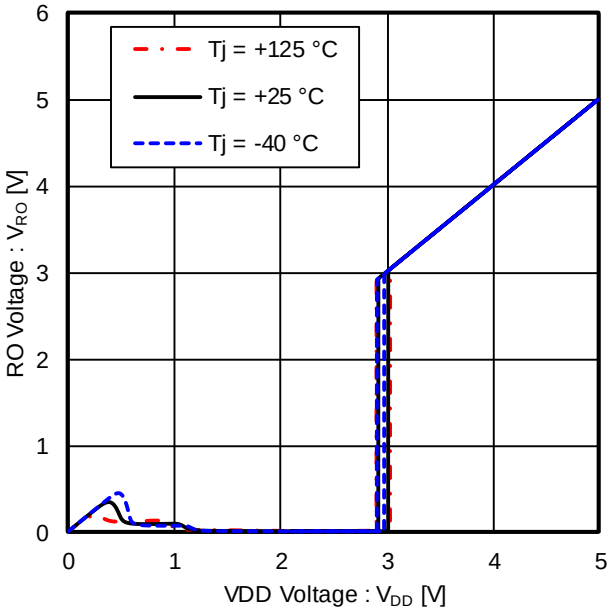


Figure 10. RO Voltage vs VDD Voltage
(Reset Detection Voltage, V_{DET} = 2.9 V)

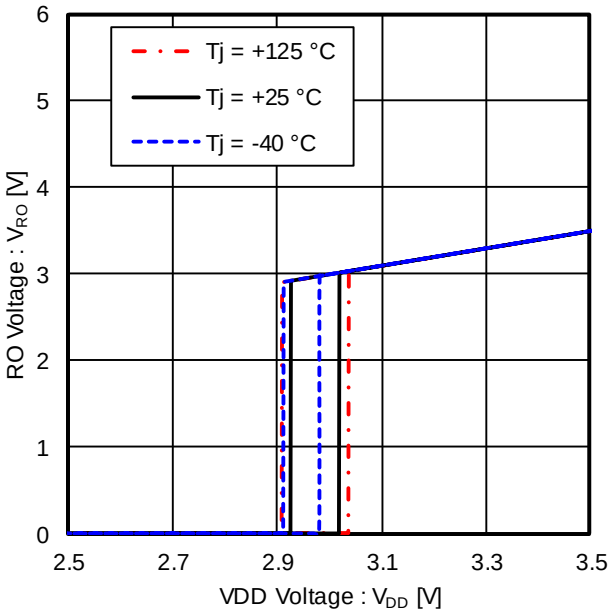


Figure 11. RO Voltage vs VDD Voltage
(Reset Detection Voltage, V_{DET} = 2.9 V, Zoom version)

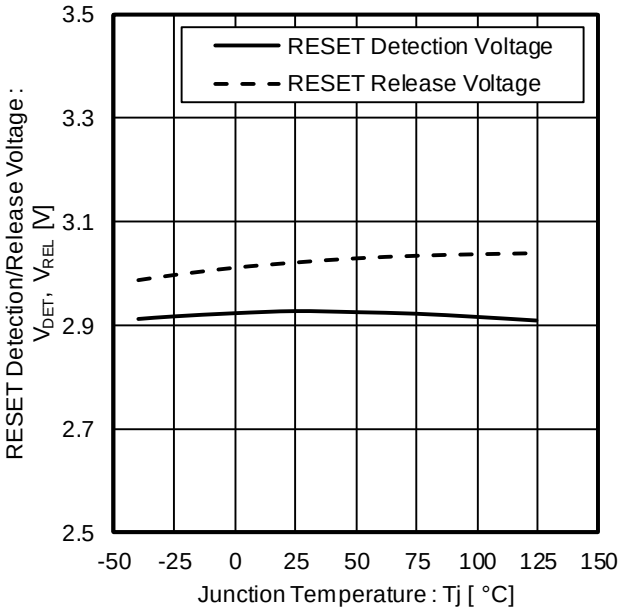


Figure 12. RESET Detection/Release Voltage vs Junction Temperature
(V_{DET} = 2.9 V)

Typical Performance Curve - continued

Unless otherwise specified, V_{DD} = 5 V, V_{INH} = GND (BD37Bxx) / V_{INH} = 5 V (BD87Bxx), R_{RO} = 10 kΩ
V_{DET} = 3.4 V

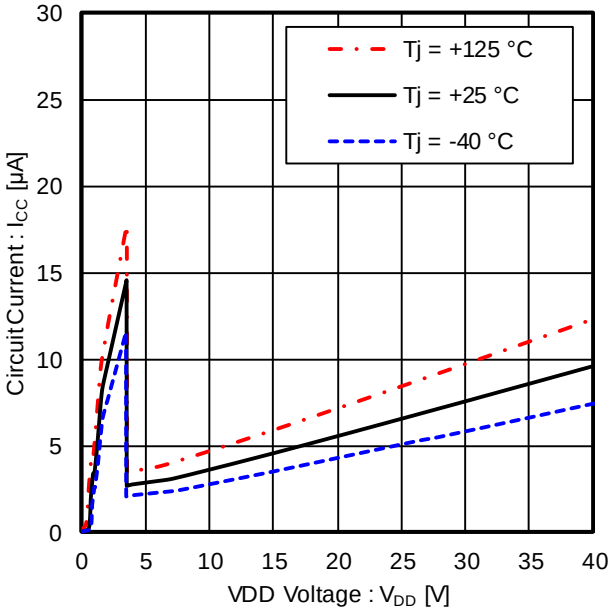


Figure 13. Circuit Current vs VDD Voltage
(V_{DET} = 3.4 V)

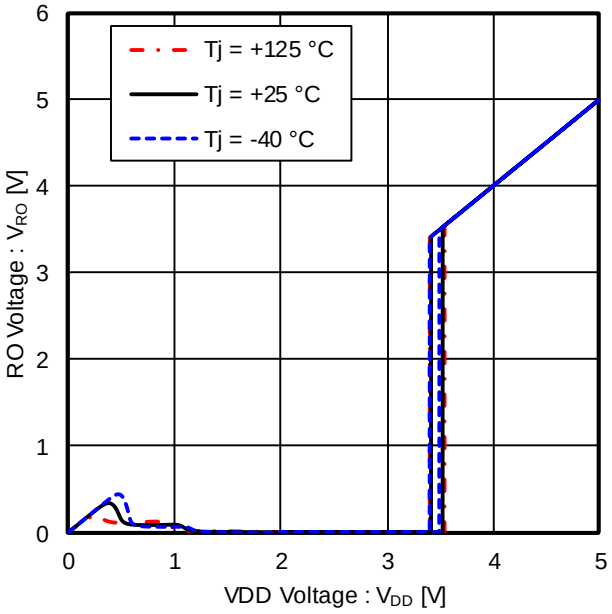


Figure 14. RO Voltage vs VDD Voltage
(Reset Detection Voltage, V_{DET} = 3.4 V)

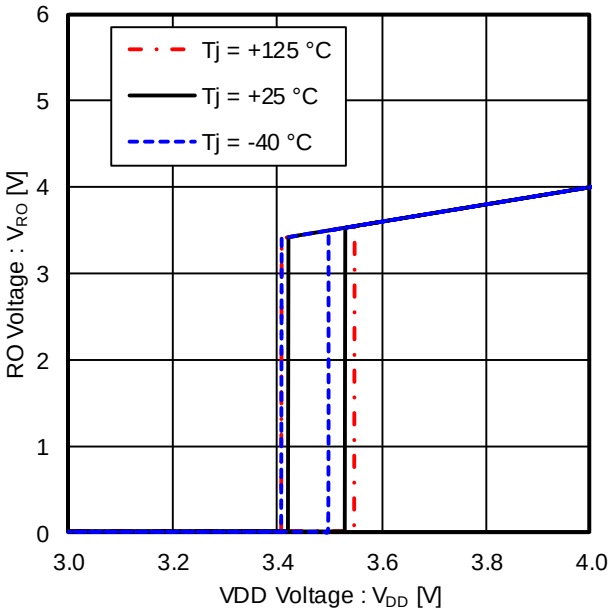


Figure 15. RO Voltage vs VDD Voltage
(Reset Detection Voltage, V_{DET} = 3.4 V, Zoom version)

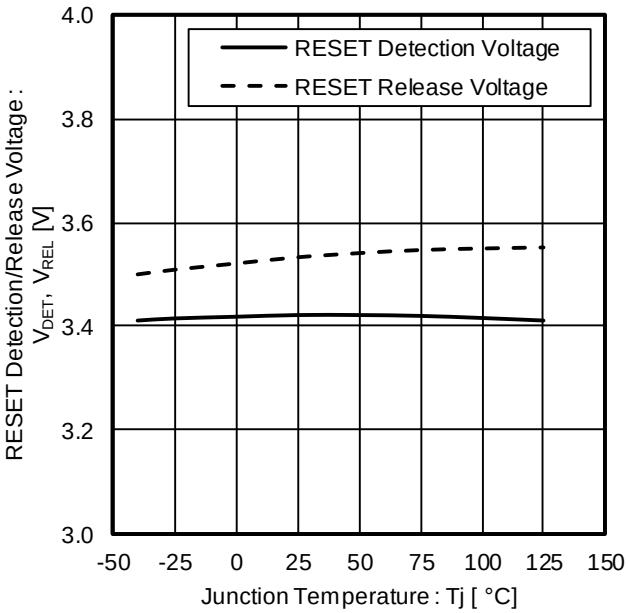


Figure 16. RESET Detection/Release Voltage vs Junction Temperature
(V_{DET} = 3.4 V)

Typical Performance Curve - continued

Unless otherwise specified, V_{DD} = 5 V, V_{INH} = GND (BD37Bxx) / V_{INH} = 5 V (BD87Bxx), R_{RO} = 10 kΩ
V_{DET} = 4.1 V

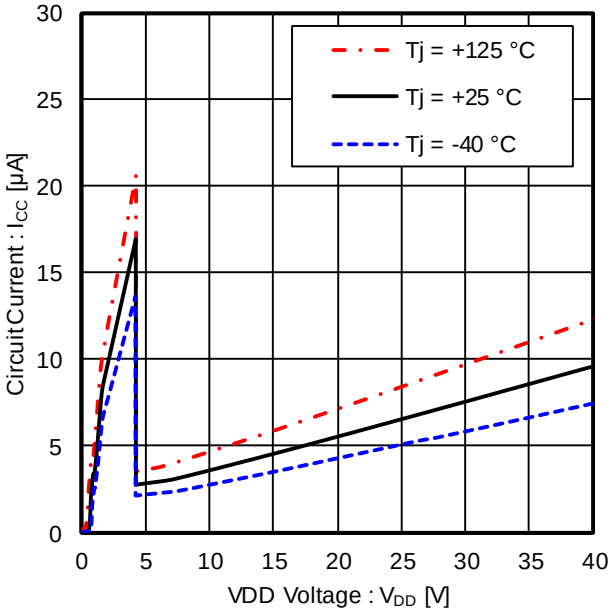


Figure 17. Circuit Current vs VDD Voltage
(V_{DET} = 4.1 V)

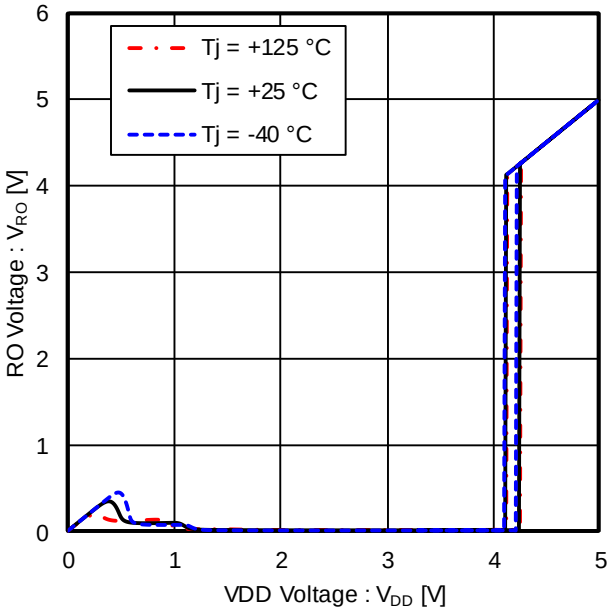


Figure 18. RO Voltage vs VDD Voltage
(Reset Detection Voltage, V_{DET} = 4.1 V)

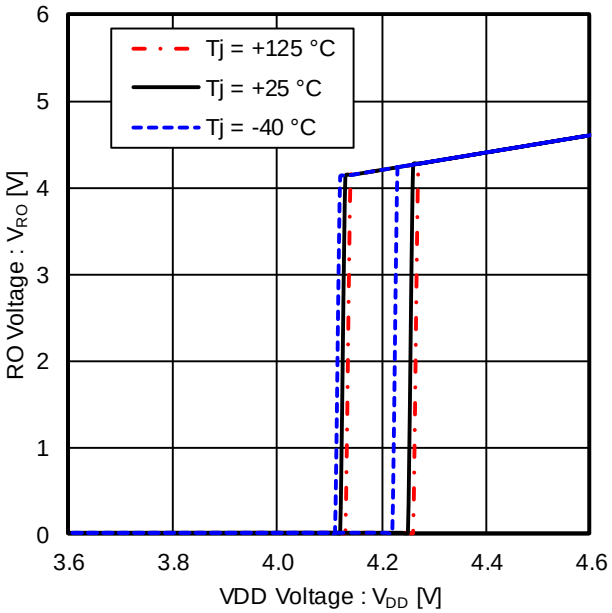


Figure 19. RO Voltage vs VDD Voltage
(Reset Detection Voltage, V_{DET} = 4.1 V, Zoom version)

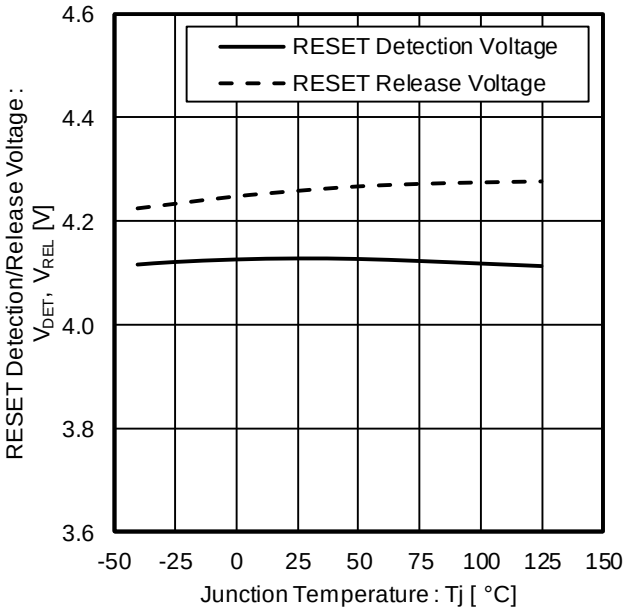


Figure 20. RESET Detection/Release Voltage vs Junction Temperature
(V_{DET} = 4.1 V)

Typical Performance Curve - continued

Unless otherwise specified, V_{DD} = 5 V, V_{INH} = GND (BD37Bxx) / V_{INH} = 5 V (BD87Bxx), R_{RO} = 10 kΩ
V_{DET} = 4.6 V

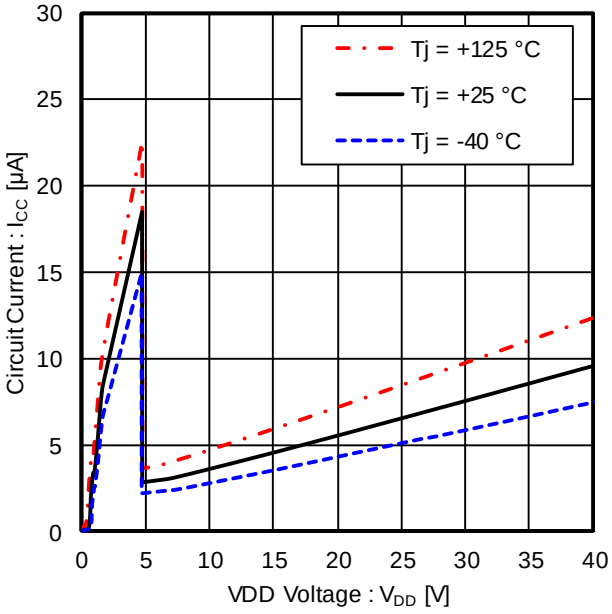


Figure 21. Circuit Current vs VDD Voltage
(V_{DET} = 4.6 V)

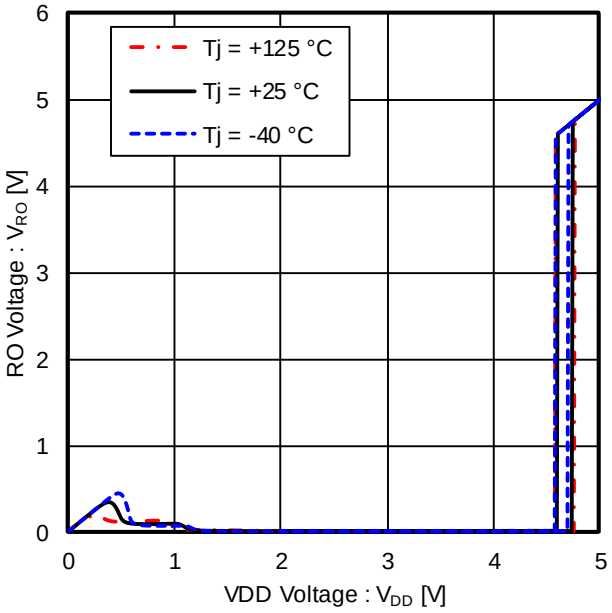


Figure 22. RO Voltage vs VDD Voltage
(Reset Detection Voltage, V_{DET} = 4.6 V)

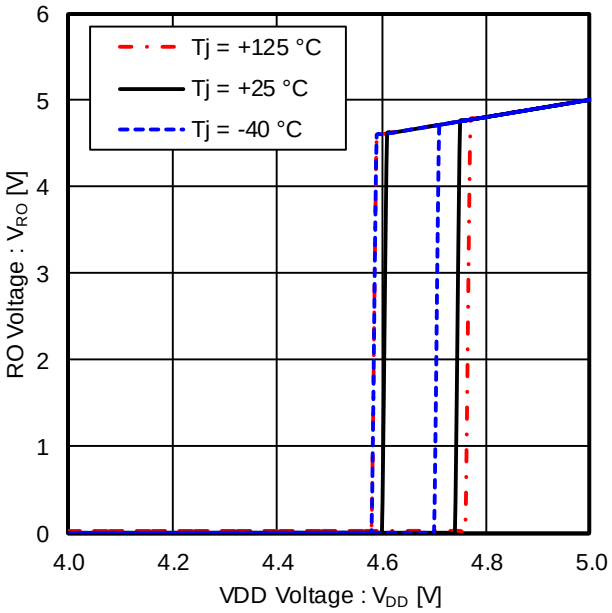


Figure 23. RO Voltage vs VDD Voltage
(Reset Detection Voltage, V_{DET} = 4.6 V, Zoom version)

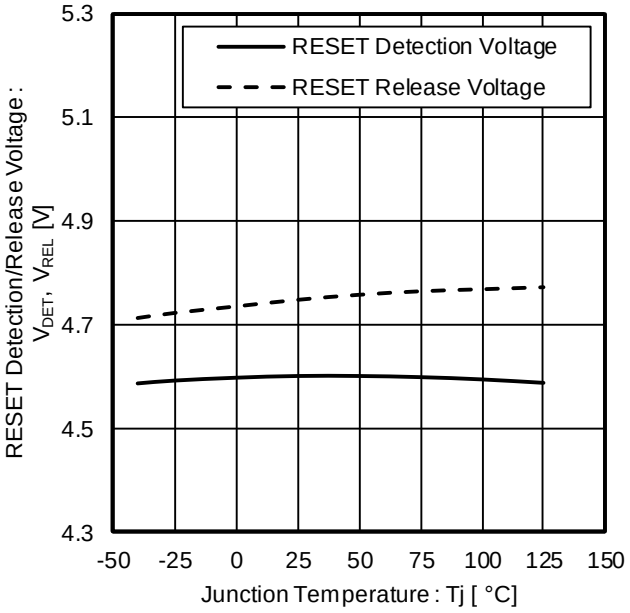


Figure 24. RESET Detection/Release Voltage vs Junction Temperature
(V_{DET} = 4.6 V)

Typical Performance Curve - continued

Unless otherwise specified, V_{DD} = 5 V, R_{RO} = 10 kΩ
V_{DET} = 4.6 V Setting

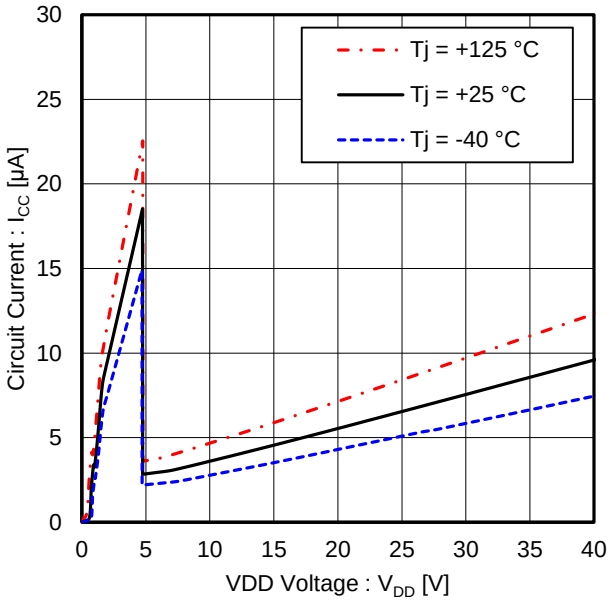


Figure 25. Circuit Current vs VDD Voltage
(BD87B00FVM-C, V_{DET} = 4.6 V Setting)

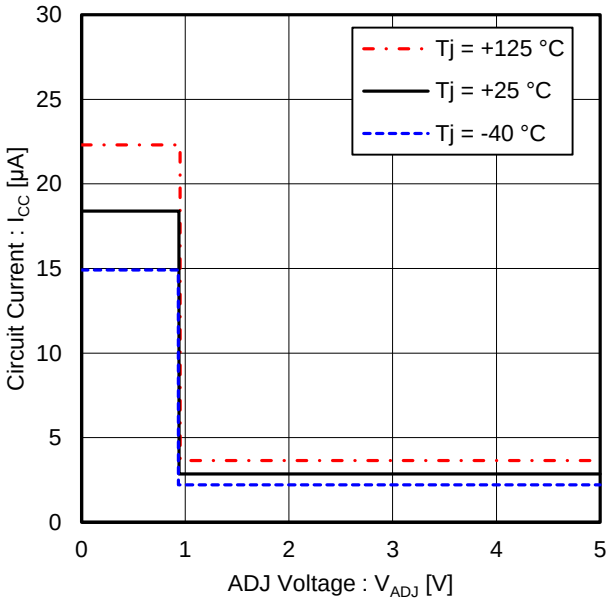


Figure 26. Circuit Current vs ADJ Voltage
(BD87B00FVM-C, V_{DD} = 5 V, V_{ADJ} = Sweep)

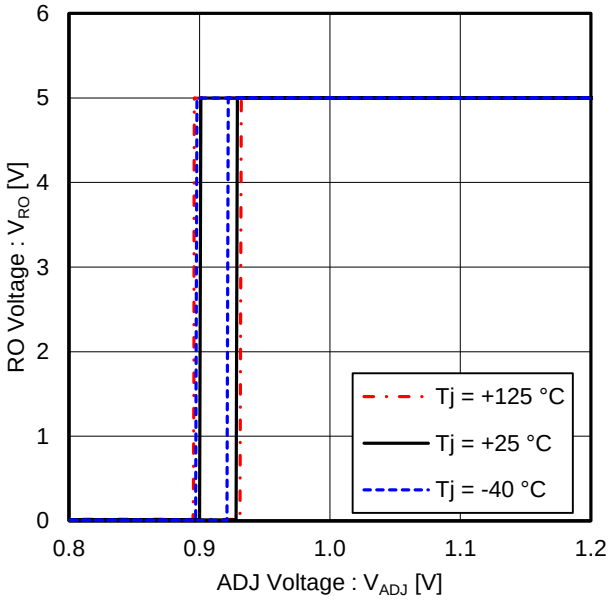


Figure 27. RO Voltage vs ADJ Voltage
(BD87B00FVM-C, V_{DD} = 5 V, V_{ADJ} = Sweep)

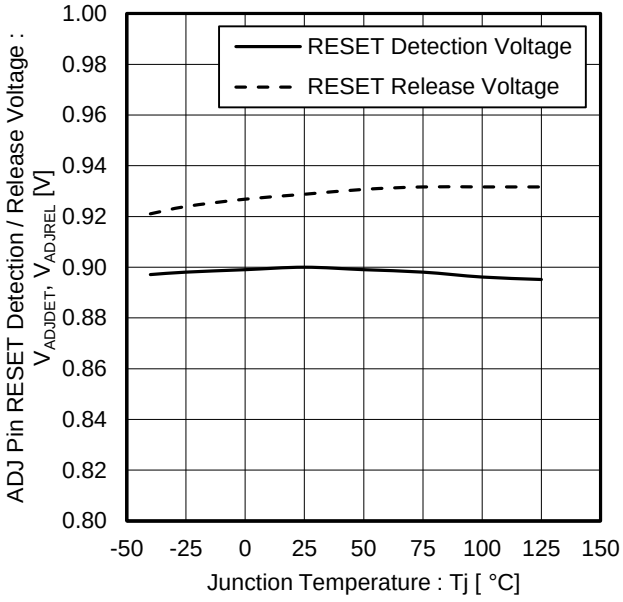


Figure 28. ADJ RESET Detection and Release Voltage vs Junction Temperature
(BD87B00FVM-C, V_{DD} = 5 V, Tj= Sweep)

Typical Performance Curve - continued

Unless otherwise specified, V_{DD} = 5 V, V_{INH} = 5 V (BD37Bxx) / V_{INH} = Open (BD87Bxx)

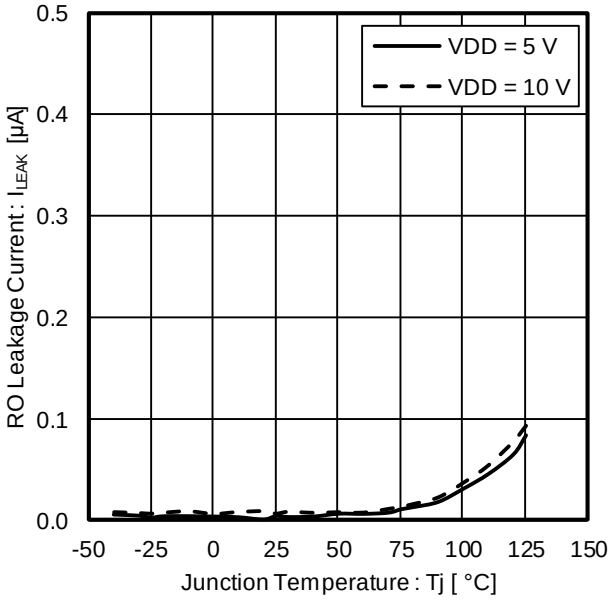


Figure 29. RO Leakage Current vs Junction Temperature
(Short VDD pin and RO pin)

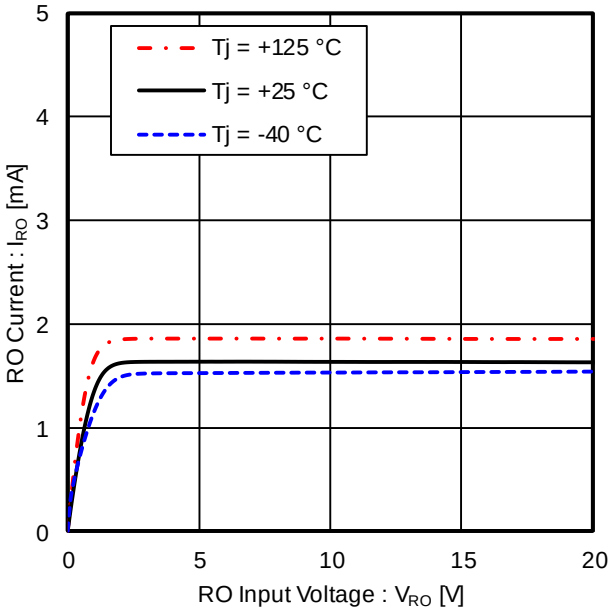


Figure 30. RO Current vs RO Input Voltage
(V_{DD} = 1 V)

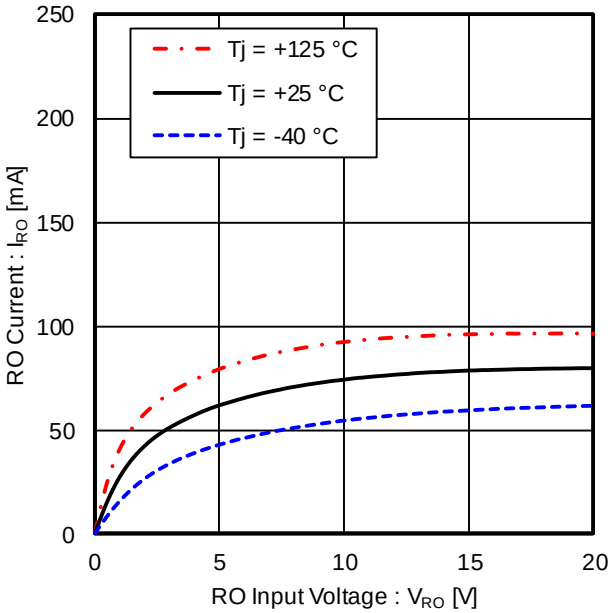


Figure 31. RO Current vs RO Input Voltage
(V_{DD} = 2 V)

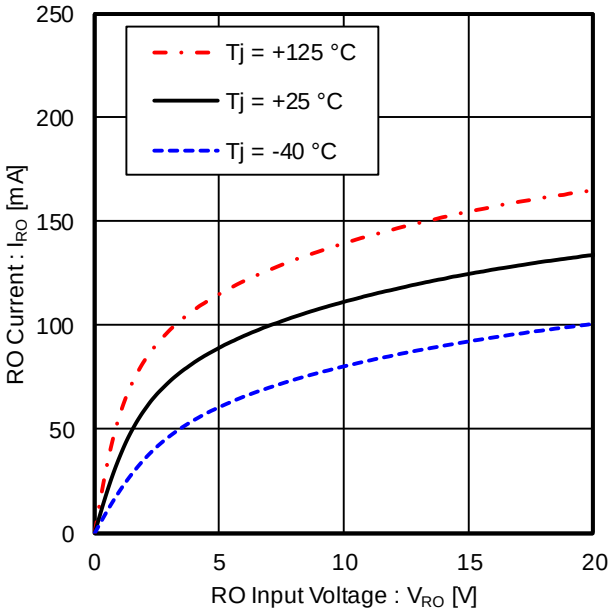


Figure 32. RO Current vs RO Input Voltage
(V_{DD} = 3 V, V_{DET} > 3 V)

Typical Performance Curve - continued

Unless otherwise specified, V_{DD} = 5 V, V_{INH} = 5 V (BD37Bxx) / V_{INH} = Open (BD87Bxx), R_{RO} = 10 kΩ

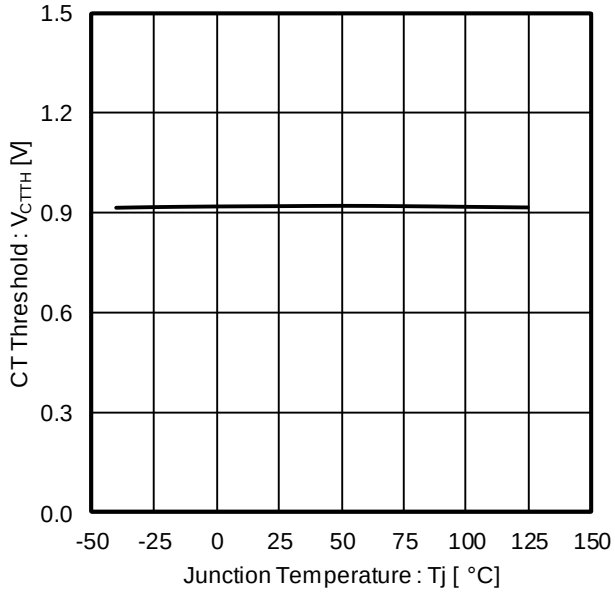


Figure 33. CT Threshold vs Junction Temperature

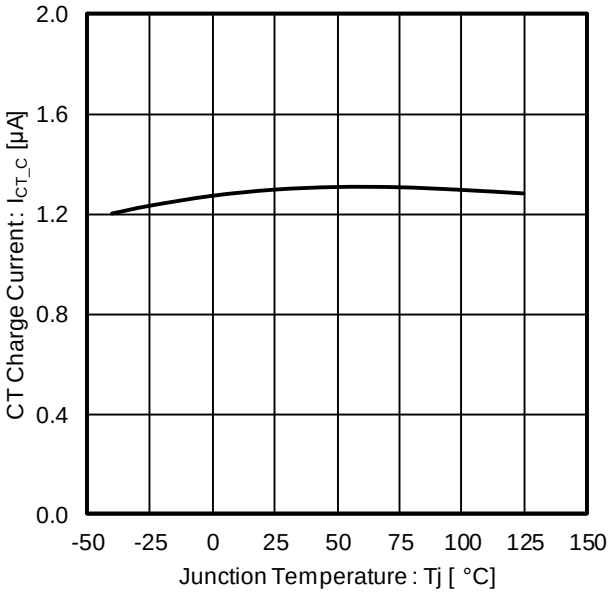


Figure 34. CT Charge Current vs Junction Temperature

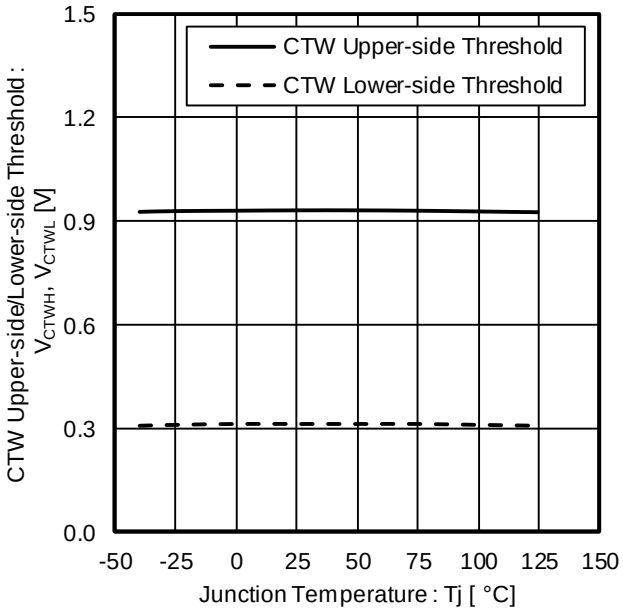


Figure 35. CTW Upper-side/Lower-side Threshold vs Junction Temperature

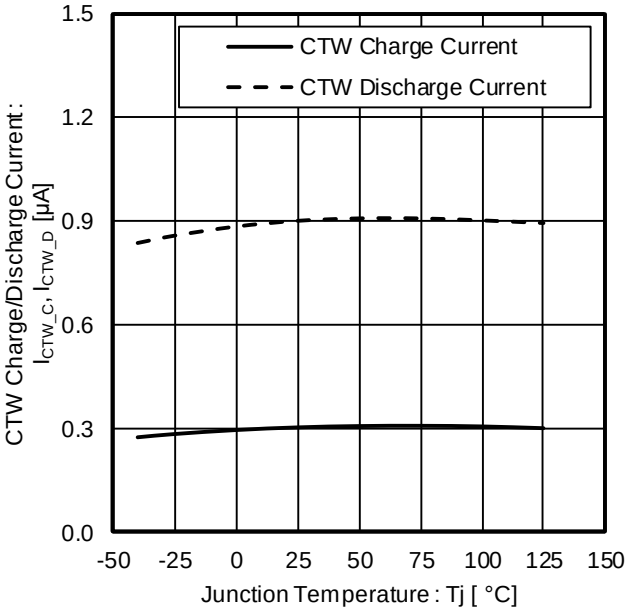


Figure 36. CTW Charge/Discharge Current vs Junction Temperature

Typical Performance Curve - continued

Unless otherwise specified, V_{DD} = 5 V, V_{INH} = 5 V (BD37Bxx) / V_{INH} = Open (BD87Bxx), R_{RO} = 10 kΩ

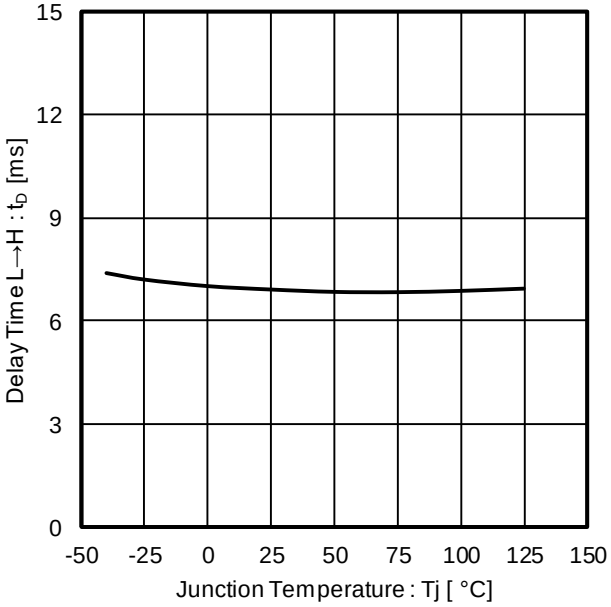


Figure 37. Delay Time L→H vs Junction Temperature

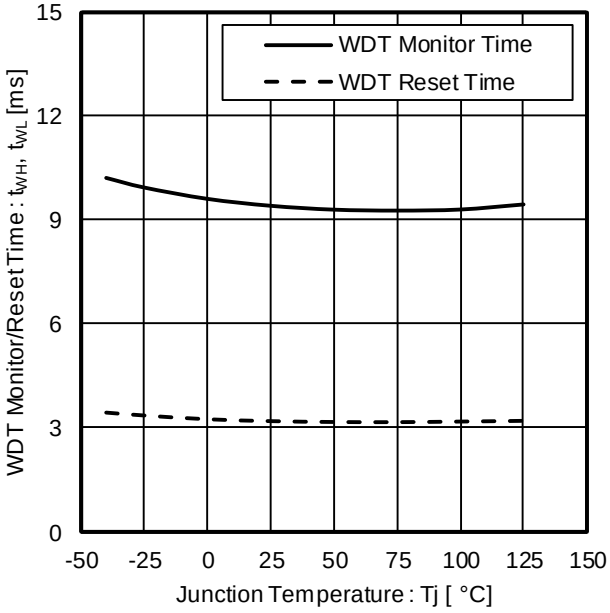


Figure 38. WDT Monitor/Reset Time vs Junction Temperature

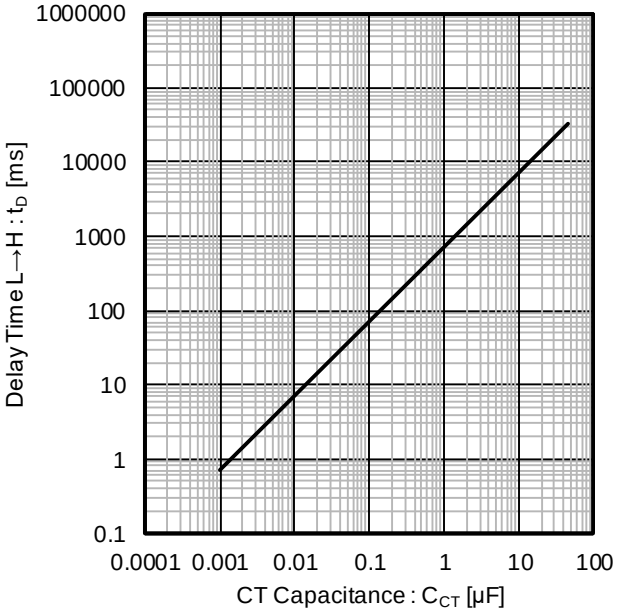


Figure 39. Delay Time L→H vs CT Capacitance
(Tj = +25 °C)

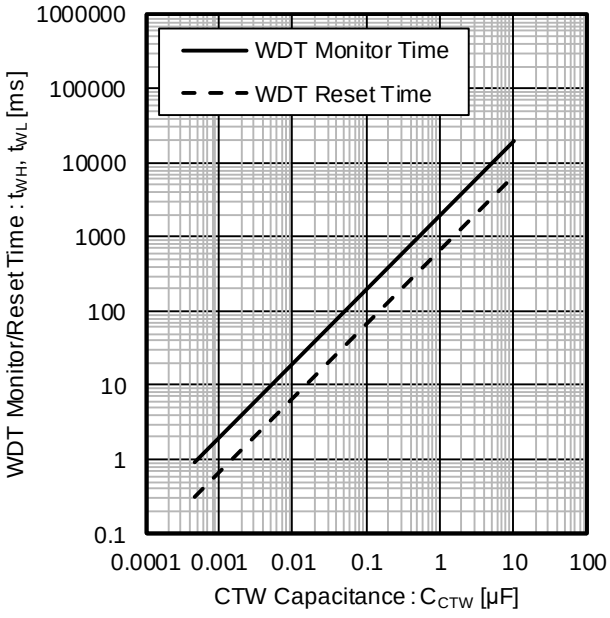


Figure 40. WDT Monitor/Reset Time vs CTW Capacitance
(Tj = +25 °C)

Typical Performance Curve - continued

Unless otherwise specified, V_{DD} = 5 V, R_{RO} = 10 kΩ

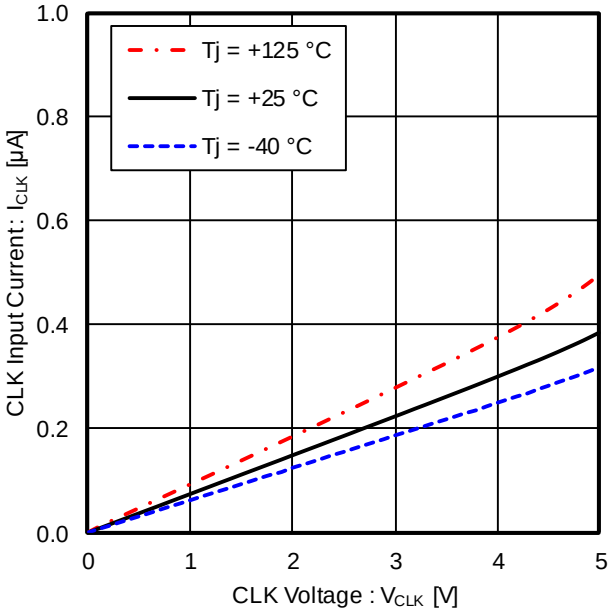


Figure 41. CLK Input Current vs CLK Voltage

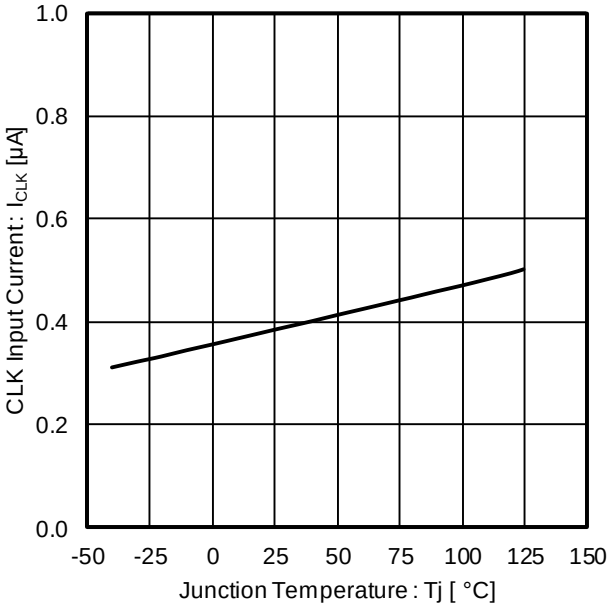


Figure 42. CLK Input Current vs Junction Temperature

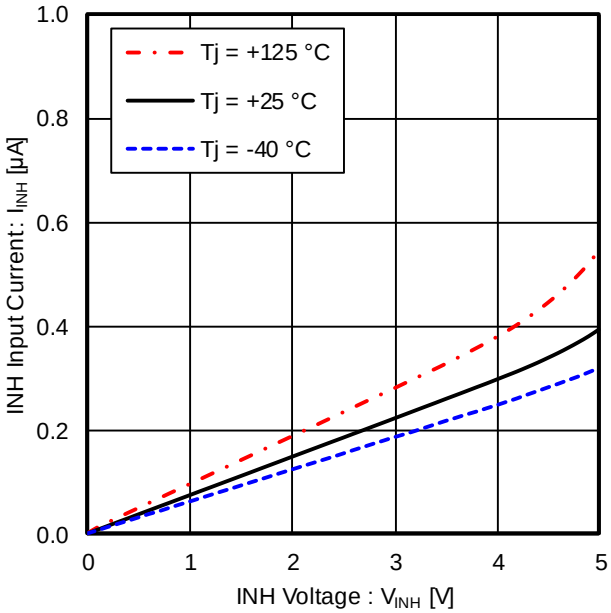


Figure 43. INH Input Current vs INH Voltage

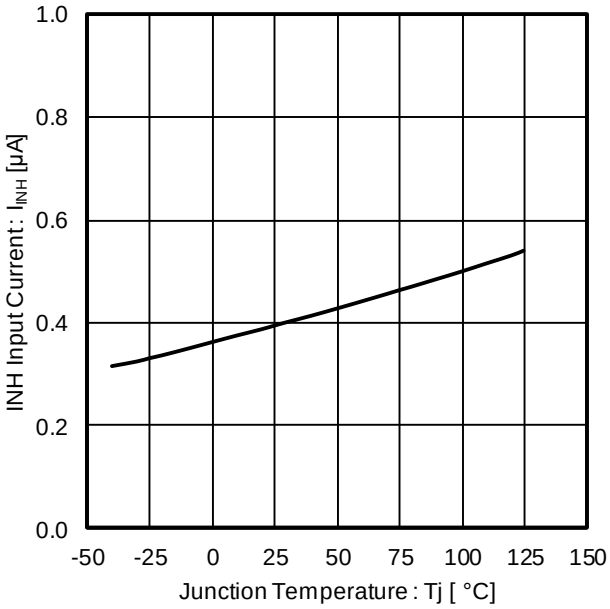


Figure 44. INH Input Current vs Junction Temperature

Typical Performance Curve - continued

Unless otherwise specified, V_{DD} = 5 V, R_{RO} = 10 kΩ, V_{ADJ} = 0.95 V

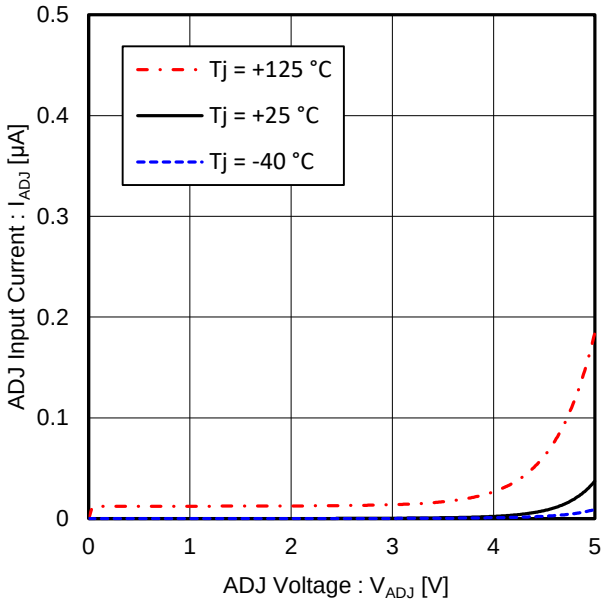


Figure 45. ADJ Input Current vs ADJ Voltage

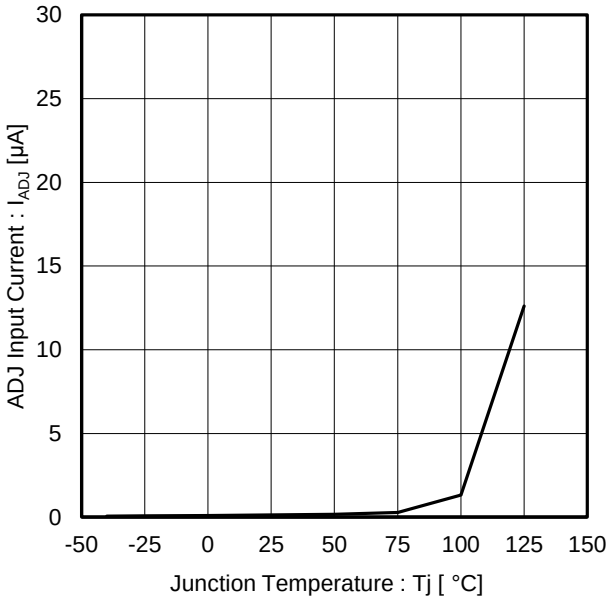
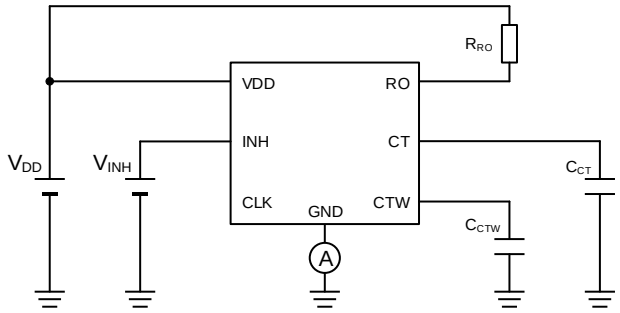


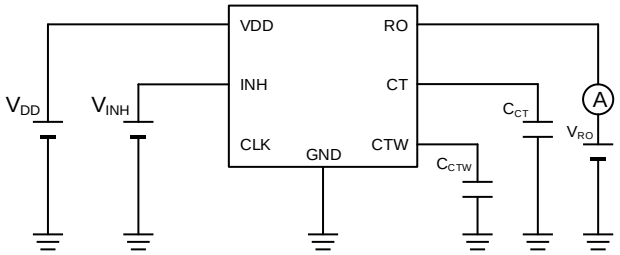
Figure 46. ADJ Input Current vs Junction Temperature

Measurement Setup for Typical Performance Curves

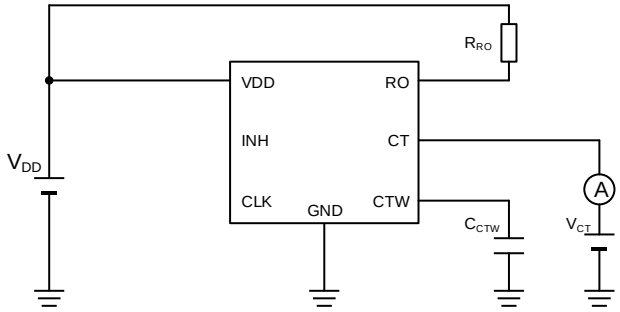
BD87BxxFVM-C



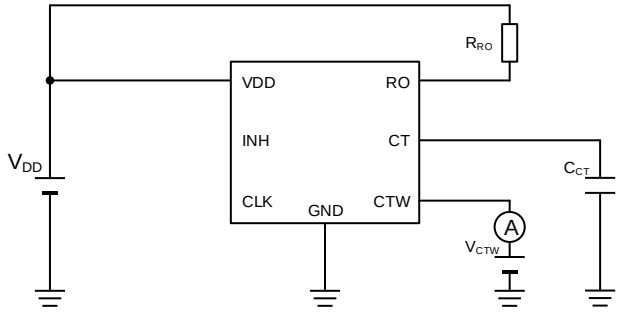
Measurement Setup for
Figure 1 – 24, 37 – 40.



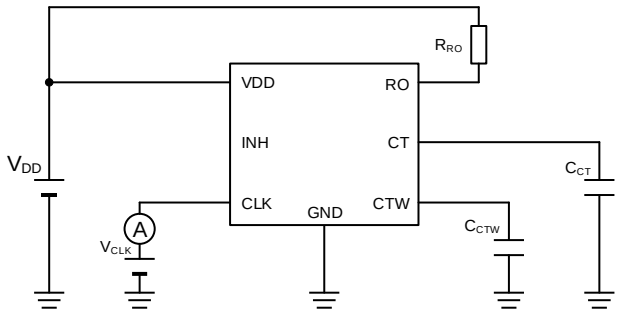
Measurement Setup for
Figure 29 – 32.



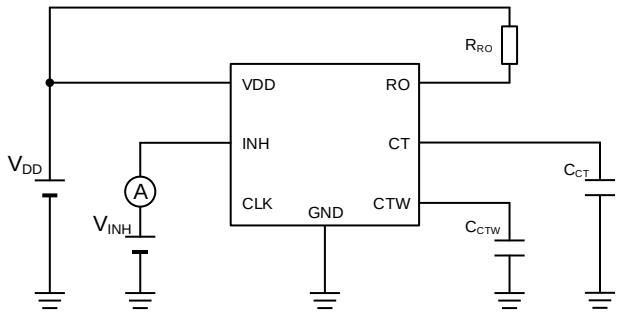
Measurement Setup for
Figure 33, 34.



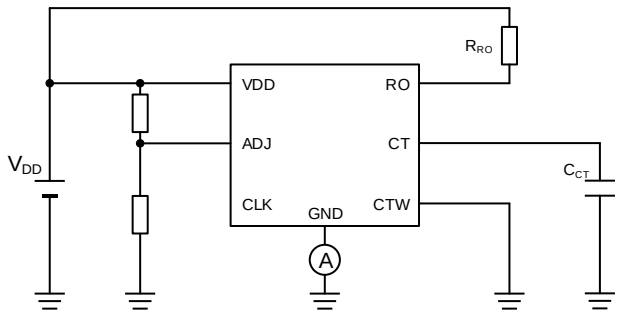
Measurement Setup for
Figure 35, 36.



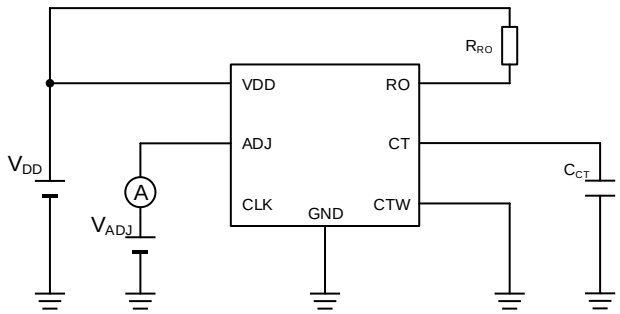
Measurement Setup for
Figure 41, 42.



Measurement Setup for
Figure 43, 44.



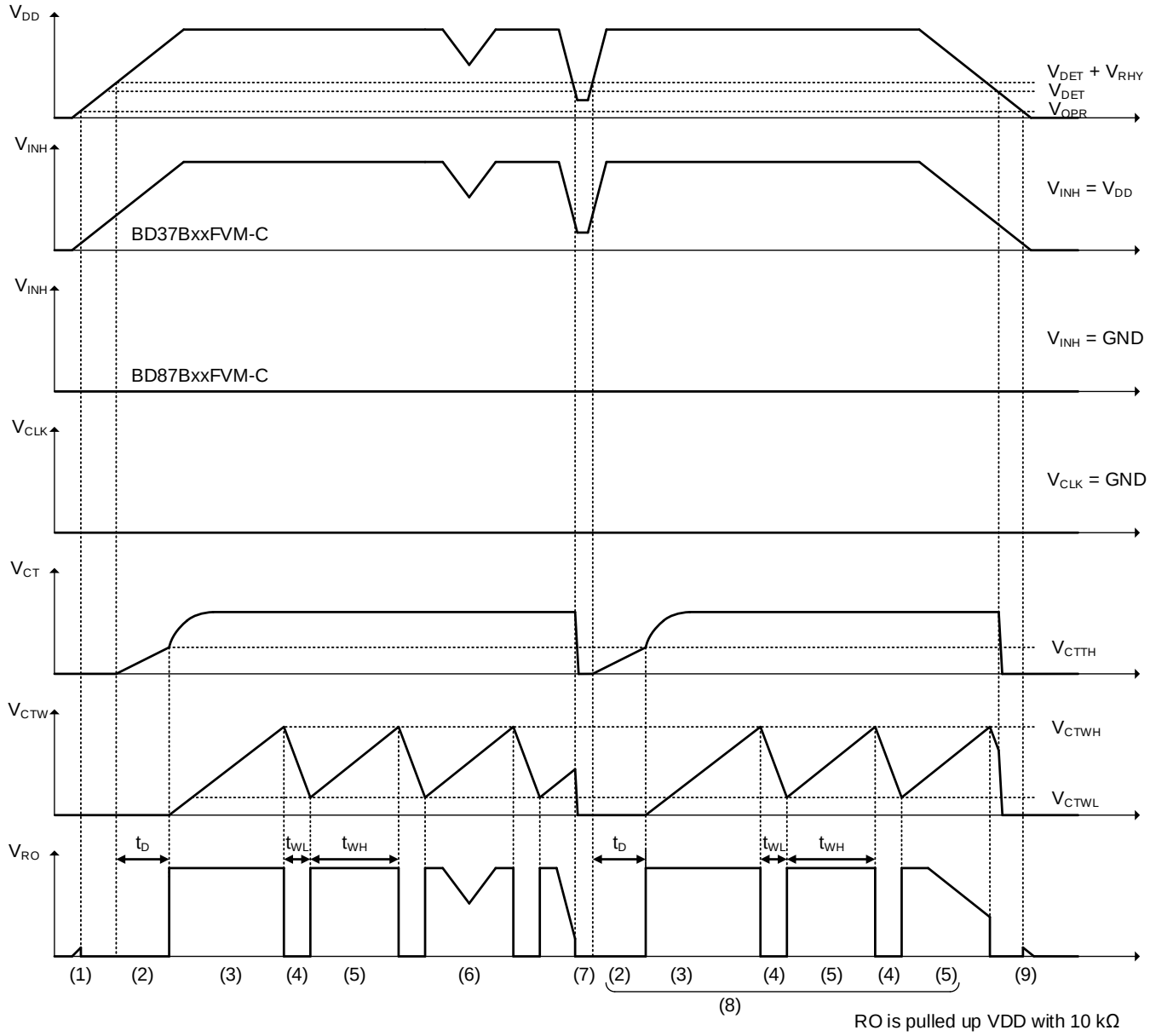
Measurement Setup for
Figure 25.



Measurement Setup for
Figure 26 - 28, 45, 46.

Timing Chart

1. VDD ON/OFF



This page shows the detail of RESET and WDT operation without CLK signal input.

(1) When VDD voltage (V_{DD}) reaches Minimum operating voltage (V_{OPR}), RO outputs Low state.

(2) RESET starts operating when V_{DD} becomes higher than RESET detection voltage (V_{DET}) + RESET detection hysteresis (V_{RHY}), i.e. the reset state caused by low output is removed. When it starts, CT voltage is raised by charging C_{CT}, the external capacitor connected the CT pin, with the internal constant current. If CT voltage reaches to high side threshold voltage, V_{CTTH}, RO outputs High state. The high state voltage level of RO is defined by the pull-up voltage via resistor at the RO pin. This time period described in Timing Chart as (2) is called Delay Time L→H (t_D).

(3) WDT starts operating when V_{CT} reaches CT Threshold (V_{CTTH}). When it starts, CTW voltage is raised by charging the external capacitor connected the CTW pin (C_{CTW}), with the internal constant current. If CTW voltage reaches to CTW Upper-side threshold (V_{CTWH}), the constant current state of CTW is switched from charging to discharging and RO outputs Low state.

(4) Then, if the electron is discharged from C_{CTW}, and V_{CTW} reaches CTW Lower-side Threshold (V_{CTWL}), the constant current of CTW is switched from discharging to charging and RO outputs again High state. This time period described in Timing Chart as (4) is called WDT Reset Time (t_{WL}).

1. VDD ON/OFF - continued

(5) When V_{CTW} reaches V_{CTWH}, the constant current of CTW is switched again from charging to discharging. If the electron is discharged from C_{CTW}, and V_{CTW} reaches V_{CTWL}, RO outputs Low state. This time period described in Timing Chart as (5) is called WDT Monitor Time (t_{WH}).

(6) When VDD voltage changes in the range $V_{DD} > V_{DET}$, RESET function judges the state as not abnormal because VDD voltage is still higher than RESET Detection Voltage, so RO keeps High state.

(7) If VDD voltage changes below the threshold voltage of V_{DET}, the CT and CTW will change its state to rapidly discharging the electron at C_{CT} and C_{CTW}. Regardless of whether the RO state is H or L, CT and CTW will be in this discharging state. RESET function judges the state as abnormal because VDD voltage is lower than RESET Detection Voltage making RO to output Low. It takes time to output Low after detecting this abnormal state, and this time lag is called “reaction time”. Reaction time always exists in electronic circuit operation. For the reason, even with these products, it is necessary to consider reaction time for such following cases.
As a reference, maximum of 150 µs reaction time is required for the RO pin to switch when VDD voltage changes from V_{DET} + 0.5 V to V_{DET} - 0.5 V. Therefore, if instantaneous interruption of VDD voltage is faster than reaction time, for example when voltage drops instantly, RESET may not operate correctly.
If instantaneous interruption may occur, countermeasure such as inputting capacitor in between VDD and GND and filtering faster voltage change than reaction time are recommended. Above mentioned also applies to adjustable detection type BD87B00FVM-C. But because BD87B00FVM-C detects by V_{ADJ}, divided voltage by resistances, and not by V_{DD}, capacitor as a countermeasure against instantaneous interruption must be set in between ADJ and GND.

(8) When RO outputs Low, and V_{CT} and V_{CTW} also become Low state via after (7) operation, and then, if VDD voltage becomes higher than V_{DET} + V_{RHY}, WDT and RESET function restarts operating continuously as following transition, (1) → (2) → (3) → (4) → (5) → (4) → (5) ….

(9) When VDD voltage becomes lower than V_{DET} and then falls to low, the constant current of CT and CTW keep their state of dis-charging in order to make CT and CTW voltages completely low. In this case, RO can keep Low output state until VDD voltage becomes lower than or equal to 1 V (V_{OPR}), i.e. during the condition that $V_{OPR} < V_{DD} < V_{DET}$.

Each period time of t_D, t_{WH} and t_{WL} can be adjusted by CT capacitance, C_{CT} and CTW capacitance, C_{CTW}.

It can be calculated by following formulas.

$$t_D[s] \approx \frac{V_{CTTH}[V] \times C_{CT}[F]}{I_{CT\_C}[A]}$$

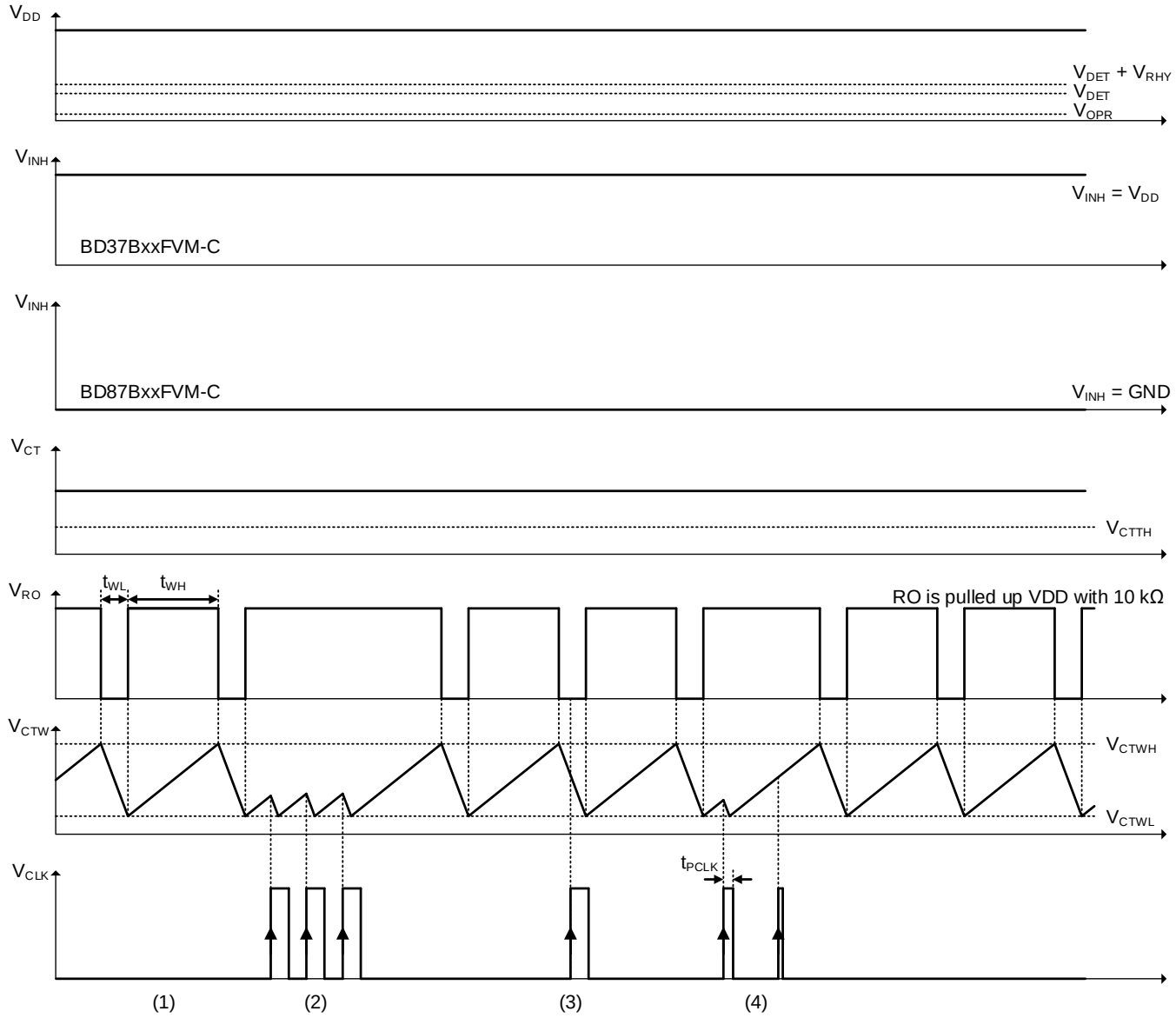
$$t_{WH}[s] \approx \frac{|V_{CTWH} - V_{CTWL}|[V] \times C_{CTW}[F]}{I_{CTW\_C}[A]}$$

$$t_{WL}[s] \approx \frac{|V_{CTWL} - V_{CTWH}|[V] \times C_{CTW}[F]}{I_{CTW\_D}[A]}$$

However, the calculated value using these formulas is just a rough estimation. Therefore the value for CT and CTW capacitances shall be designed by the ratio calculation compared the actual value to the value at the condition of C_{CT} = 0.01 µF and C_{CTW} = 0.0047 µF described in the Electrical Characteristics.

Timing Chart - continued

2. CLK ON/OFF



A WDT behavior on the CLK inputs is described here.

CLK inputs is acceptable only while RO outputs H, i.e. during t_{WH}, for WDT.
When RO outputs Low, i.e. during t_{WL}, t_D and so on, CLK inputs is not allowed.

(1) While RO outputs High, if the input of a rising edge to the CLK pin is not supplied, a charge state at CTW kept. If this state continues until V_{CTW} reaches V_{CTWL}, then the output of RO switches from High to Low. This state is Timeout Failure that WDT does not detect the rising edge of CLK inputs from the microcomputer during the period defined by C_{CTW} capacitance.

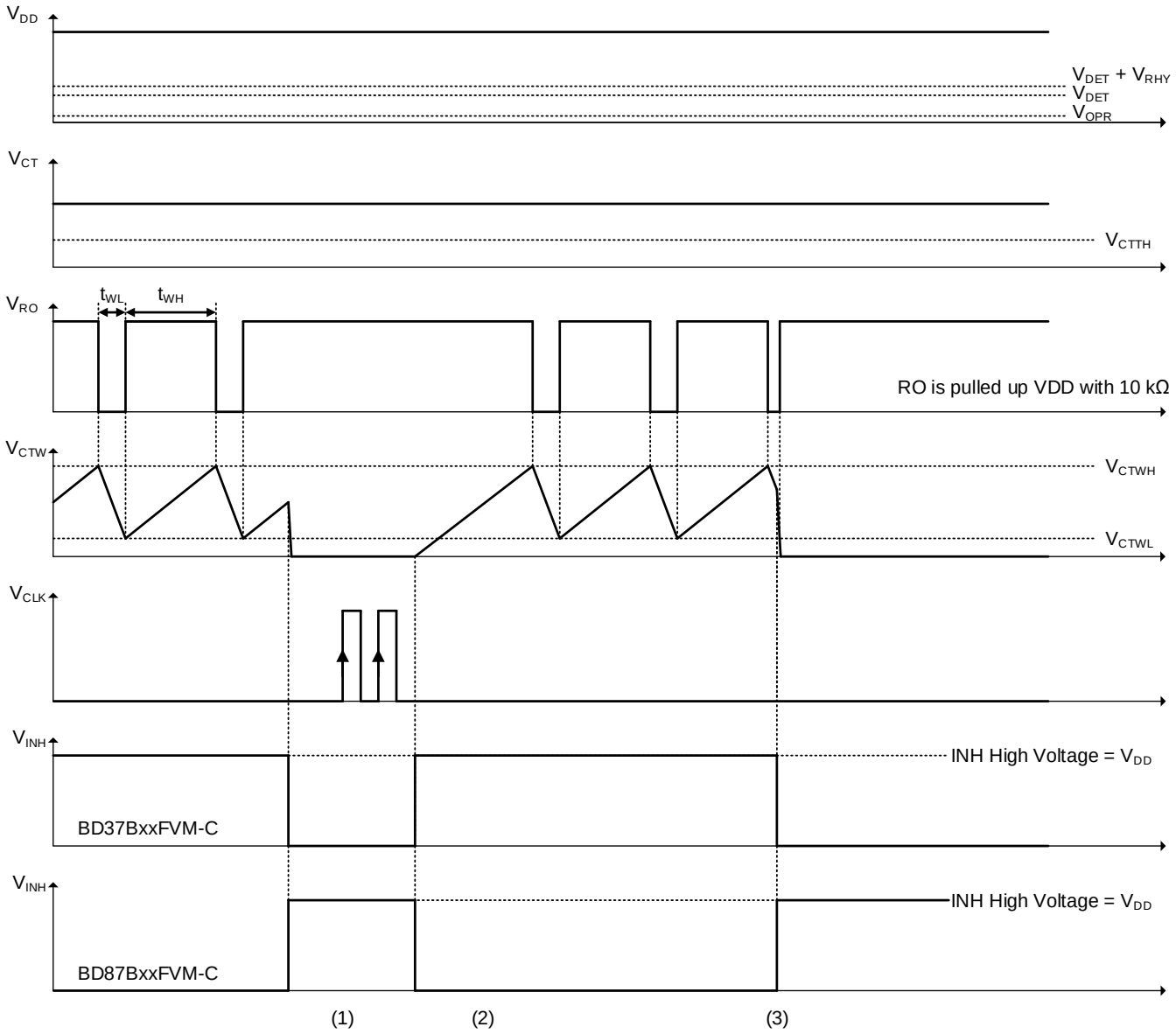
(2) While RO outputs High, if the rising edge supplies to the CLK pin, WDT detects this rising edge and then it changes the charging state at CTW to a discharging state. Then V_{CTW} reaches to V_{CTWL} by discharging constant current to C_{CTW}, CTW state changes back to the charging. RO can keep High output if CLK signal inputs with constant timing that CTW state is the charging as described (2).

(3) While RO outputs Low, even if the rising edge supplies to the CLK pin, WDT does not detect the edge.

(4) The pulse width of CLK inputs, i.e. t_{PCLK}, must be always longer than or equal to 0.5 µs. Otherwise there is a possibility that CTW state cannot change discharging from charging at CLK pulse input.

Timing Chart - continued

3. INH ON/OFF



A disabled WDT behavior on the INH inputs is described here.

INH function expects to use for writing to Micro Computer while stopping WDT function in the factory. Therefore, it can use for the normal operation with the limitation of WDT function, i.e. only using the RESET function.

3.1. In case of BD37BxxFVM-C

(1) If the INH pin is supplied Low input or it keeps open, the CTW pin is pulled down to GND internally. Since V_{CTW} is maintained at lower voltage than or equal to V_{CTWL}, it means WDT does not operate during the condition that $V_{DET} < V_{DD}$, so RO can keep High output state. At this time, if the rising edge is input to the CLK pin, WDT does not detect this edge.

(2) When the High input (around VDD voltage) supplies to the INH pin, the state of CTW is switched from discharging to charging, C_{CTW} is charged with the constant current, and WDT starts operating.

(3) If INH pin is supplied Low input or it keeps open while RO outputs Low state, the CTW pin is pulled down to GND internally. When the electron is discharged from C_{CTW} and V_{CTW} reaches V_{CTWL}, RO outputs again High state. RO can keep High output while the INH pin status does not change.

3. INH ON/OFF - continued

3.2. In case of BD87BxxFVM-C

(1) If the High input (around VDD voltage) supplies to the INH pin, the CTW pin is pulled down to GND internally. Since V_{CTW} is maintained at lower voltage than or equal to V_{CTWL}, it means WDT does not operate during the condition that $V_{DET} < V_{DD}$, so RO can keep High output state. At this time, if the rising edge is input to the CLK pin, WDT does not detect this edge.

(2) When the INH pin is supplied Low input or it keeps open, the state of CTW is switched from discharging to charging, C_{CTW} is charged with the constant current, and WDT starts operating.

(3) If the High input (around VDD voltage) supplies to the INH pin while RO outputs Low state, the CTW pin is pulled down to GND internally. When the electron is discharged from C_{CTW} and V_{CTW} reaches V_{CTWL}, RO outputs again High state. RO can keep High output while the INH pin status does not change.

3.3. In case of BD87BxxG-C

BD87BxxG-C don't have the INH Function, and the WDT is always ON. To stop the WDT behavior, pull down the CTW pin to GND. Pull down resistors can be used 500 kΩ or less.

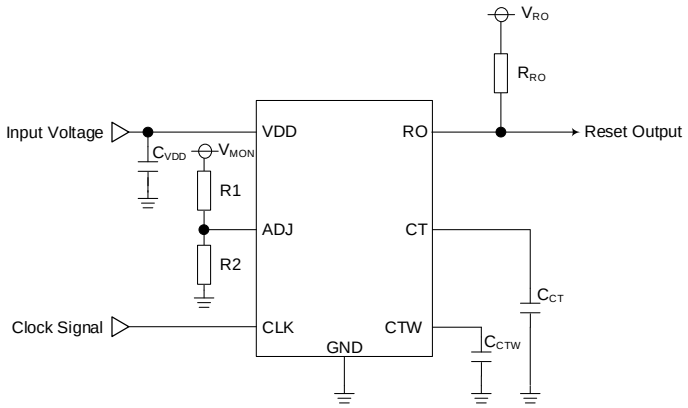
Application Examples

Manual Reset by external processing of the CT pin

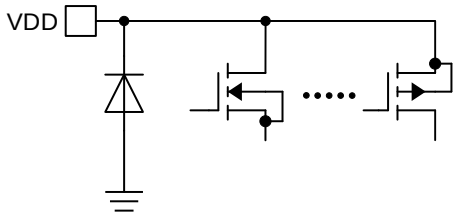
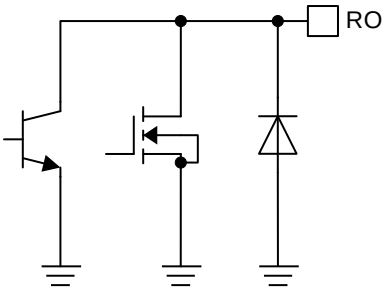
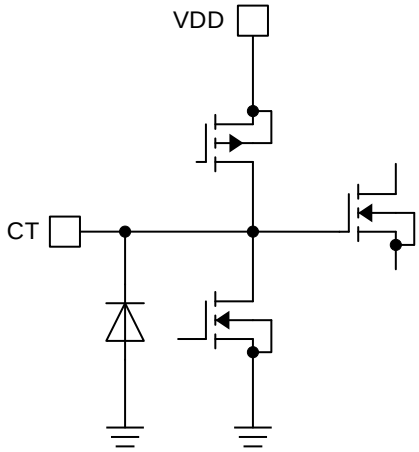
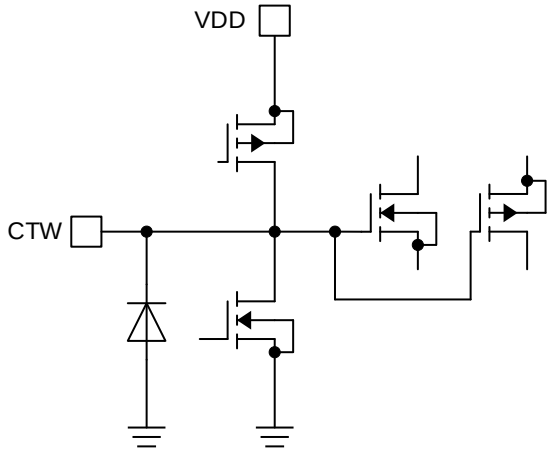
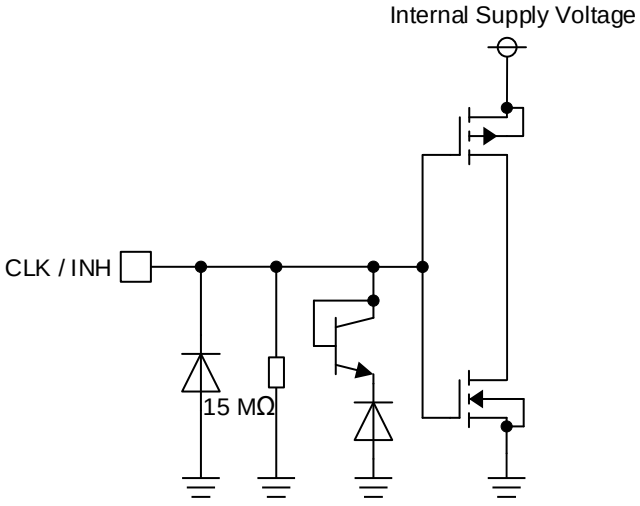
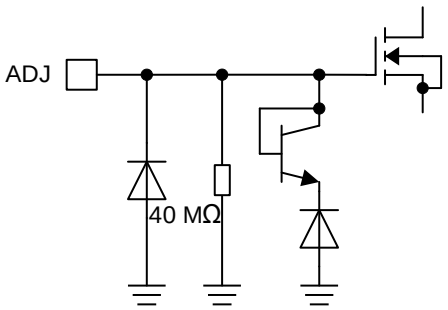
By pulling down the CT pin to GND, it is possible to forcibly output a signal in the reset detection state. Pull down resistors can be used 100 kΩ or less.

Monitoring a voltage other than VDD voltage with BD87B00FVM-C

When monitoring VDD voltage, RESET Detection Voltage cannot be set below the operating voltage of the IC. However, when monitoring a voltage other than VDD voltage as shown the figure below, it can be set up to Min 0.96 V, Which is under operating voltage.



I/O Equivalence Circuits(Note 1)

VDD	RO
	
CT	**CTW**
	
INH/CLK	**ADJ**(Note 2)
	

(Note 1) Listed resistance values are typical value.
(Note 2) BD87B00FVM-C only

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Thermal Consideration**
   If Junction temperature is over Tjmax (= 150 °C), IC characteristics may be worse due to rising chip temperature. Heat resistance in specification is measurement under PCB condition and environment recommended in JEDEC. Ensure that heat resistance in specification is different from actual environment.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

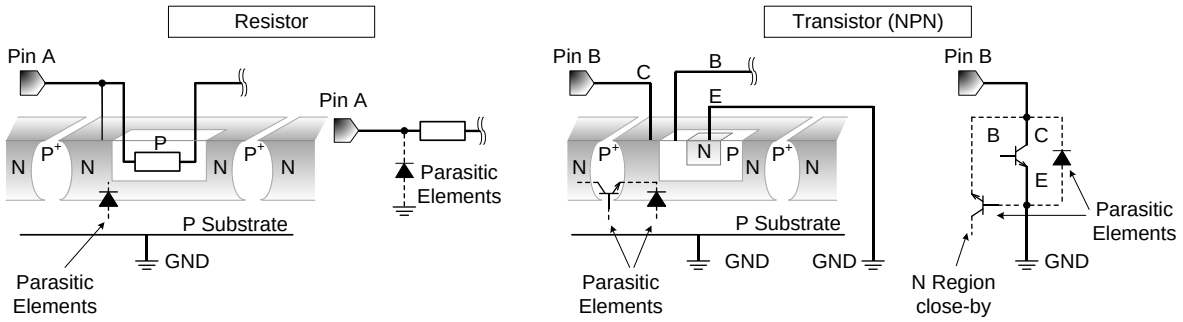


Figure 47. Example of Monolithic IC Structure

12. Ceramic Capacitor

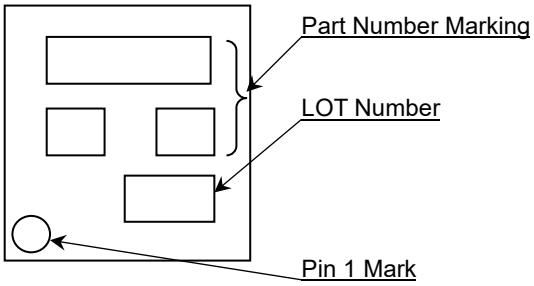
When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.
"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.
"Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.
Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Marking Diagram (MSOP8)

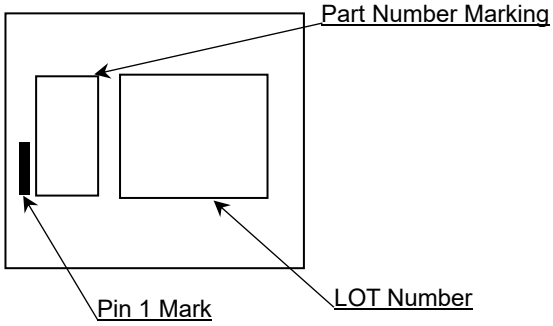
MSOP8 (TOP VIEW)



Marking	RESET Detection Voltage	INH Logic	Part Number
37B23	2.3 V	High Active	BD37B23FVM-CTR
37B28	2.8 V		BD37B28FVM-CTR
37B29	2.9 V		BD37B29FVM-CTR
37B34	3.4 V		BD37B34FVM-CTR
37B41	4.1 V		BD37B41FVM-CTR
37B46	4.6 V		BD37B46FVM-CTR
87B00	Adjustable	No INH Function (WDT is always ON)	BD87B00FVM-CTR
87B23	2.3 V	Low Active	BD87B23FVM-CTR
87B28	2.8 V		BD87B28FVM-CTR
87B29	2.9 V		BD87B29FVM-CTR
87B34	3.4 V		BD87B34FVM-CTR
87B41	4.1 V		BD87B41FVM-CTR
87B46	4.6 V		BD87B46FVM-CTR

Marking Diagram (SSOP6)

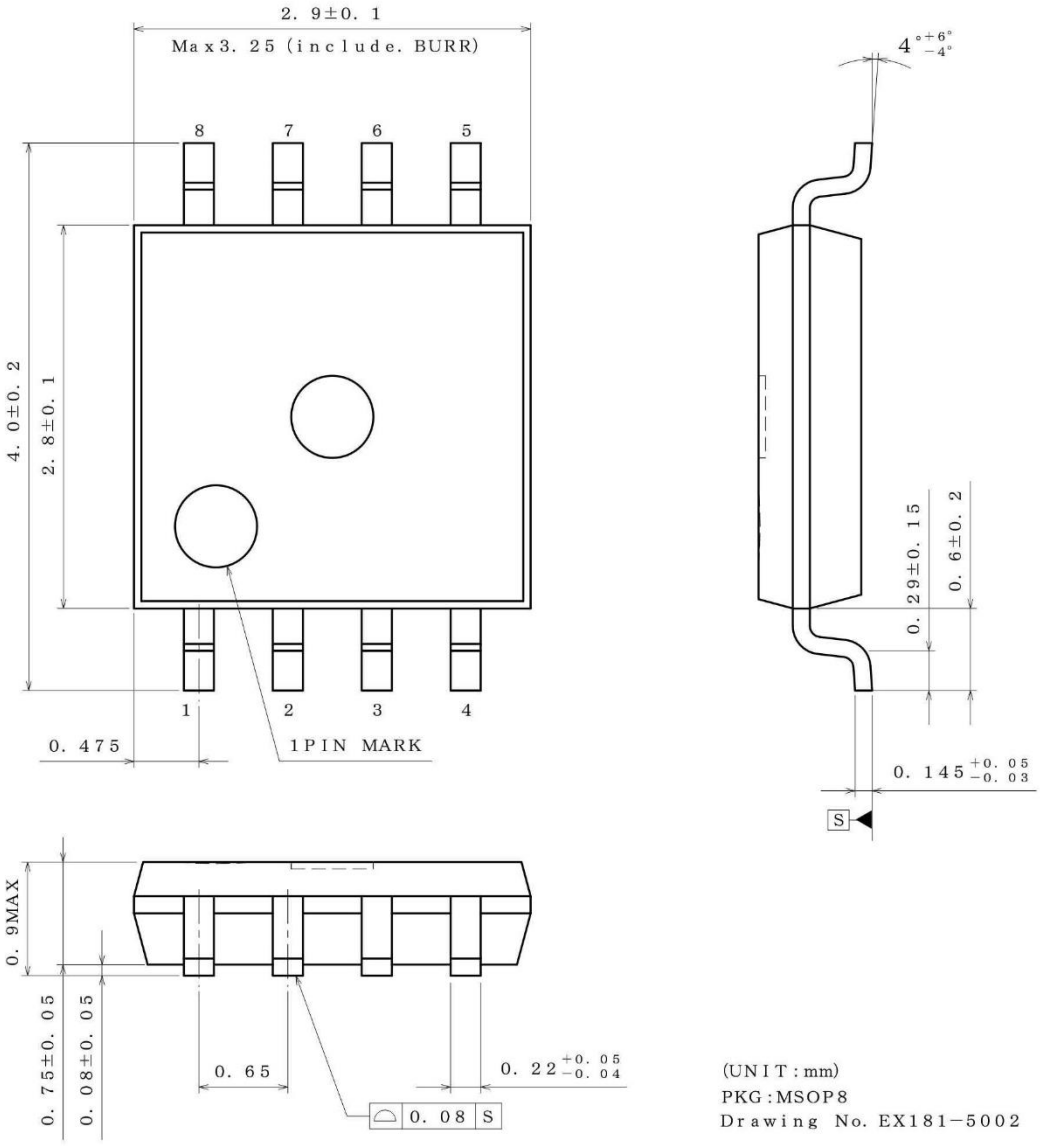
SSOP6 (TOP VIEW)



Marking	RESET Detection Voltage	INH Logic	Part Number
GF	2.3 V	No INH Function (WDT is always ON)	BD87B23G-CTR
GG	2.8 V		BD87B28G-CTR
GH	2.9 V		BD87B29G-CTR
GJ	3.4 V		BD87B34G-CTR
GK	4.1 V		BD87B41G-CTR
GL	4.6 V		BD87B46G-CTR

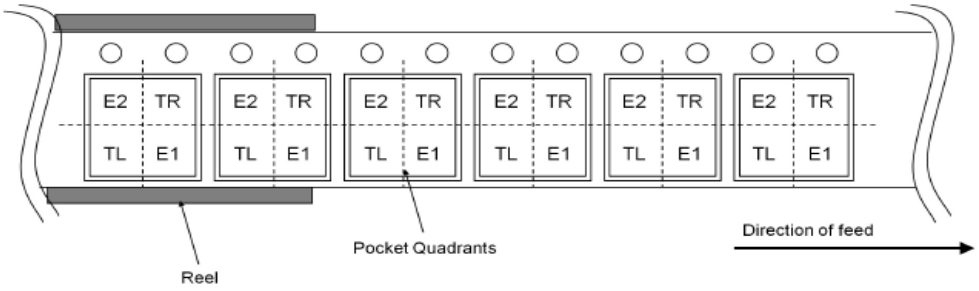
Physical Dimension and Packing Information

Package Name	MSOP8



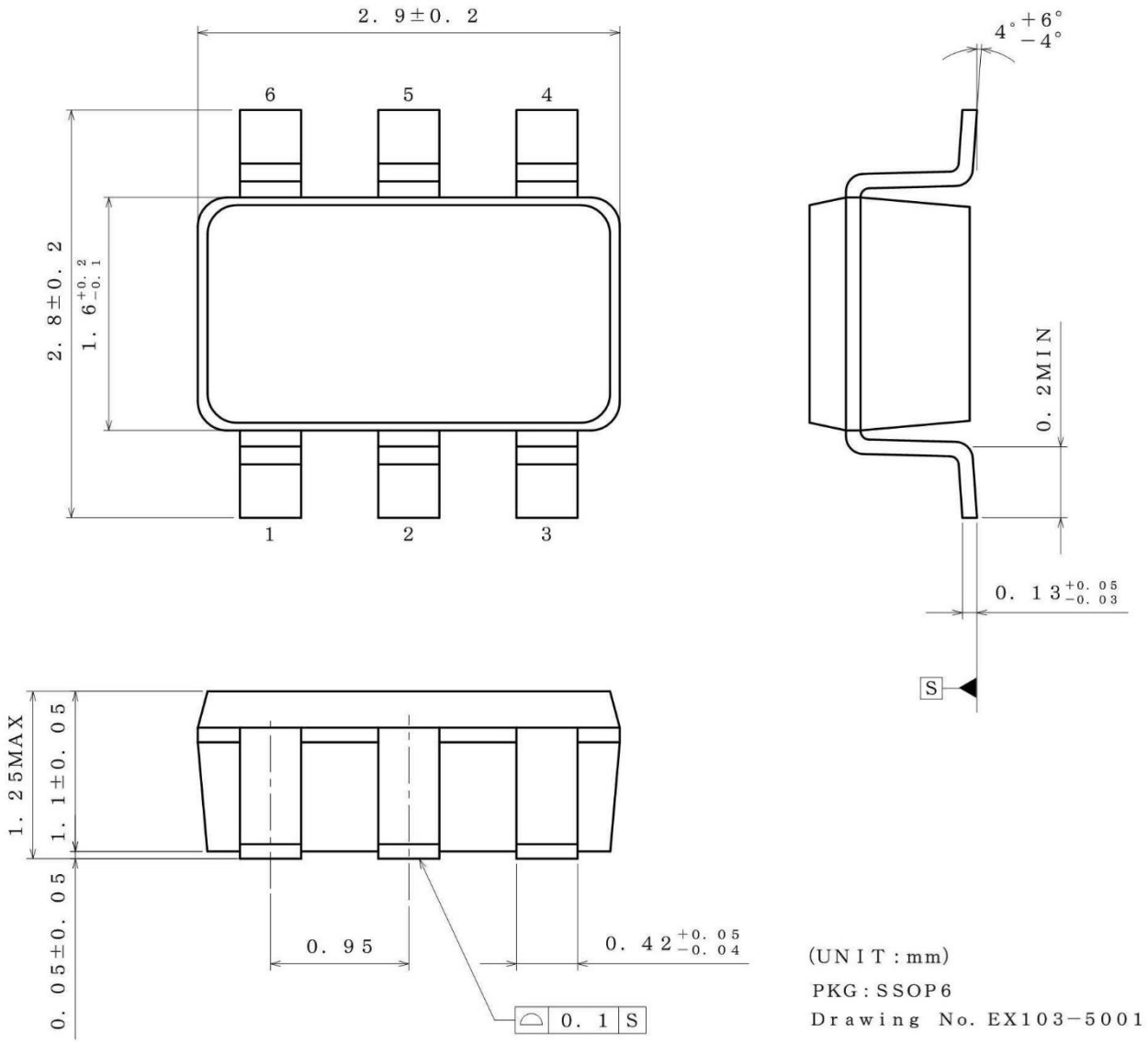
< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



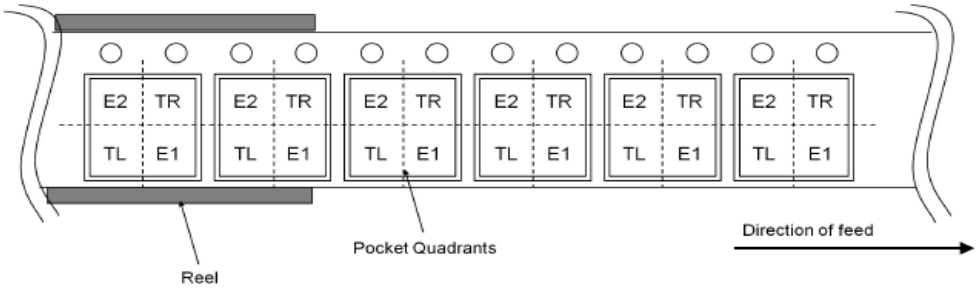
Physical Dimension and Packing Information – continued

Package Name	SSOP6



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
16.Nov.2021	001	New Release
30.Nov.2021	002	Unit Correction “RESET Detection Hysteresis”
28.Dec.2022	003	Added BD87B00FVM-C. Added Notes to conditions of Electrical Characteristics. CLK Input High Level Voltage, CLK Input Low Level Voltage, INH Input High Level Voltage, INH Input Low Level Voltage Added description of Timing Chart VDD ON/OFF.
19.Dec.2023	004	Conditions Correction “CTW Charge Current” and “CTW Discharge Current”. Part Number Correction BD87BxxG-C (xx: 23/28/29/34/41/46). Packaging and forming specification Correction SSOP6.

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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