

MOSFET

OptiMOS™ 7 Power-Transistor, 40 V

Features

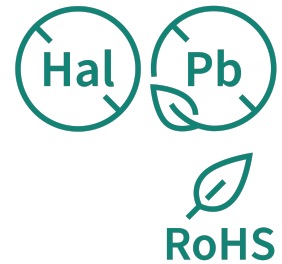
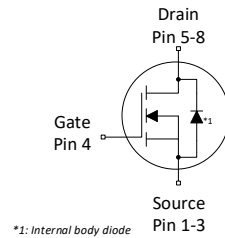
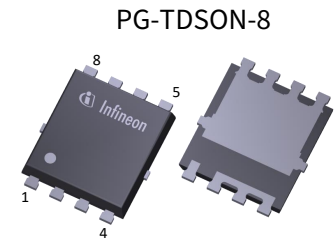
- N-channel
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),max}$	0.42	m Ω
I_D	541	A
Q_{oss}	167	nC
Q_G	79	nC



Type/Ordering Code	Package	Marking	Related Links
ISCH42N04LM7	PG-TDSON-8	42N04LM7	-



Table of Contents

Description	1
Maximum ratings	3
Thermal characteristics	3
Electrical characteristics	4
Electrical characteristics diagrams	6
Package Outlines	10
Revision History	13
Trademarks	13
Disclaimer	13

1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	541 383 323 61	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$ $V_{GS}=10\text{ V}, T_C=100\text{ °C}$ $V_{GS}=4.5\text{ V}, T_C=100\text{ °C}$ $V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=50\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	2164	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	899	mJ	$I_D=50\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	234 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}, R_{thJA}=50\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	0.64	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}	-	-	50	°C/W	-

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	1.5	1.8	V	$V_{DS}=V_{GS}$, $I_D=130\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.39 0.48	0.42 0.59	m Ω	$V_{GS}=10\text{ V}$, $I_D=50\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=25\text{ A}$
Gate resistance	R_G	-	0.9	-	Ω	-
Transconductance	g_{fs}	160	320	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=50\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance ⁶⁾	C_{iss}	-	10000	13000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁶⁾	C_{oss}	-	4600	6000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ⁶⁾	C_{rss}	-	140	240	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	7	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	70	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	22	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

⁶⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁷⁾

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	25	-	nC	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	16	-	nC	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge ⁸⁾	Q_{gd}	-	26	39	nC	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	Q_{sw}	-	35	-	nC	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ⁸⁾	Q_g	-	79	99	nC	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.5	-	V	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ⁸⁾	Q_g	-	156	207	nC	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ⁸⁾	Q_{oss}	-	167	222	nC	$V_{DS}=20\text{ V}$, $V_{GS}=0\text{ V}$

⁷⁾ See "Gate charge waveforms" for parameter definition

⁸⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	235	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	2164	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.76	1.0	V	$V_{GS}=0\text{ V}$, $I_F=50\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time ⁹⁾	t_{rr}	-	55	110	ns	$V_R=20\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ⁹⁾	Q_{rr}	-	70	140	nC	$V_R=20\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery time ⁹⁾	t_{rr}	-	36	72	ns	$V_R=20\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge ⁹⁾	Q_{rr}	-	348	696	nC	$V_R=20\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$

⁹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

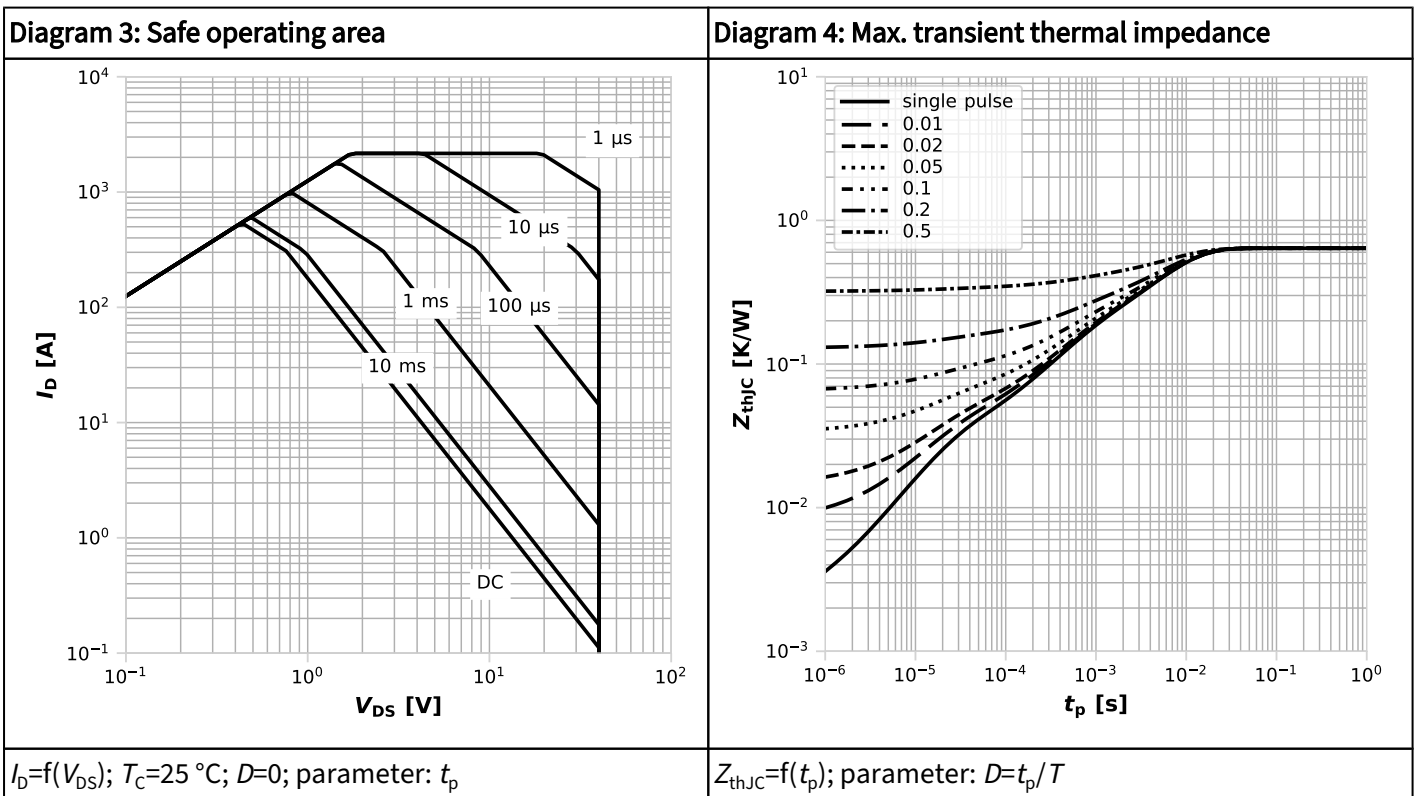
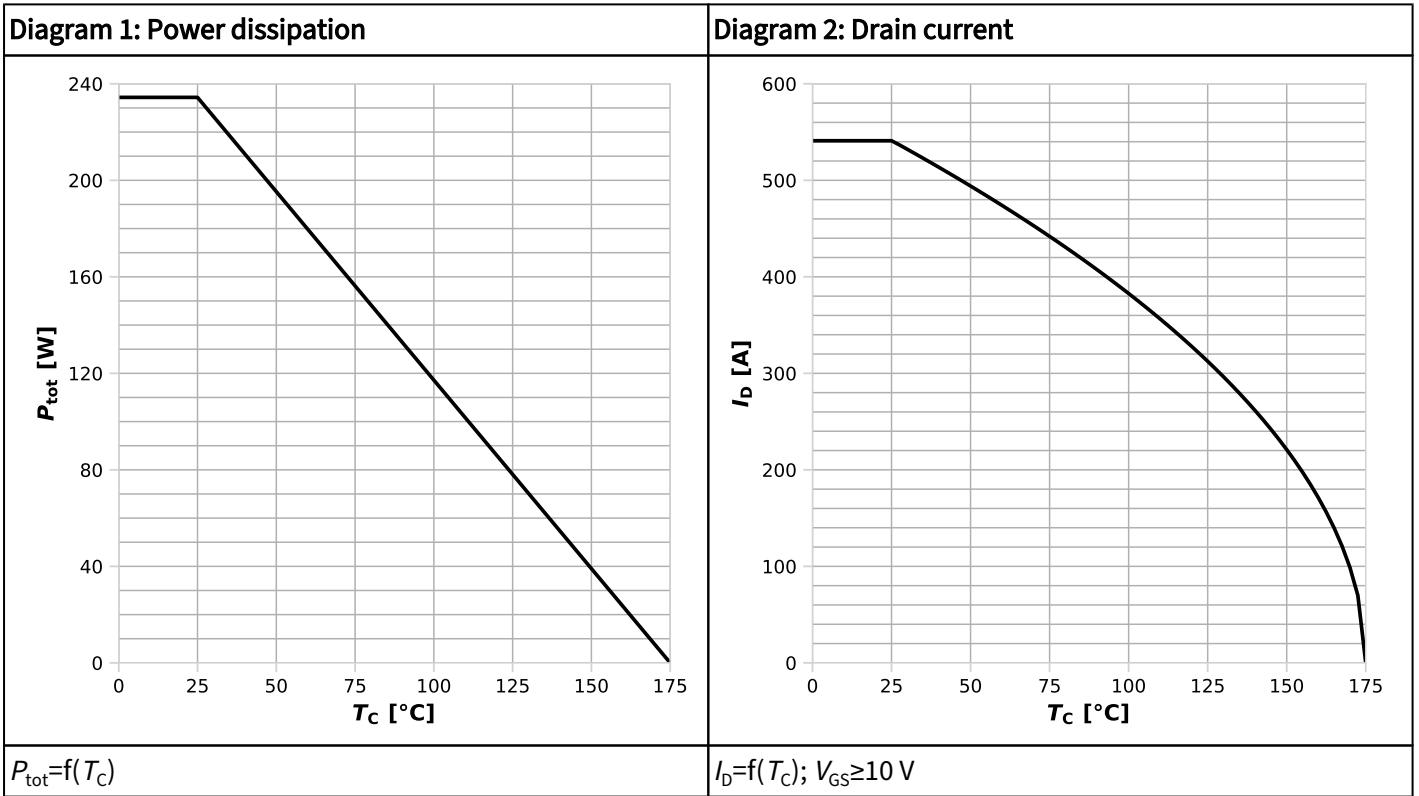
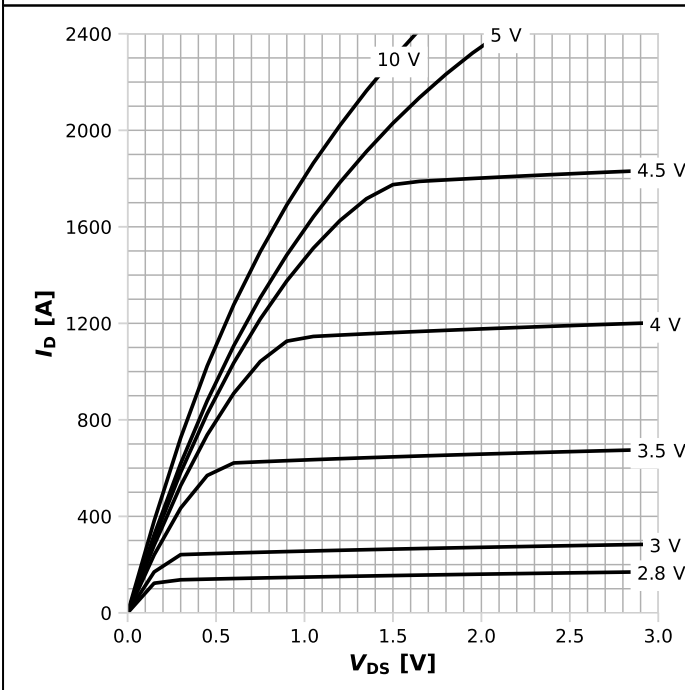
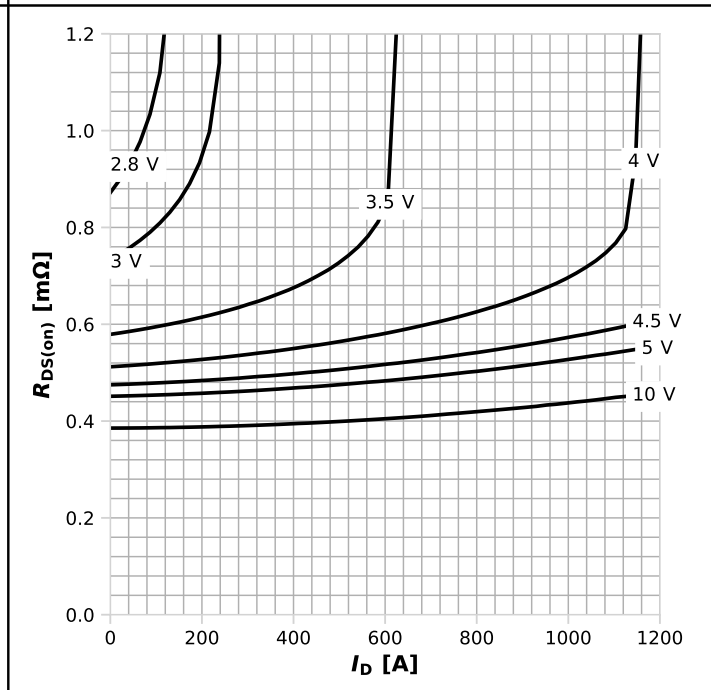


Diagram 5: Typ. output characteristics



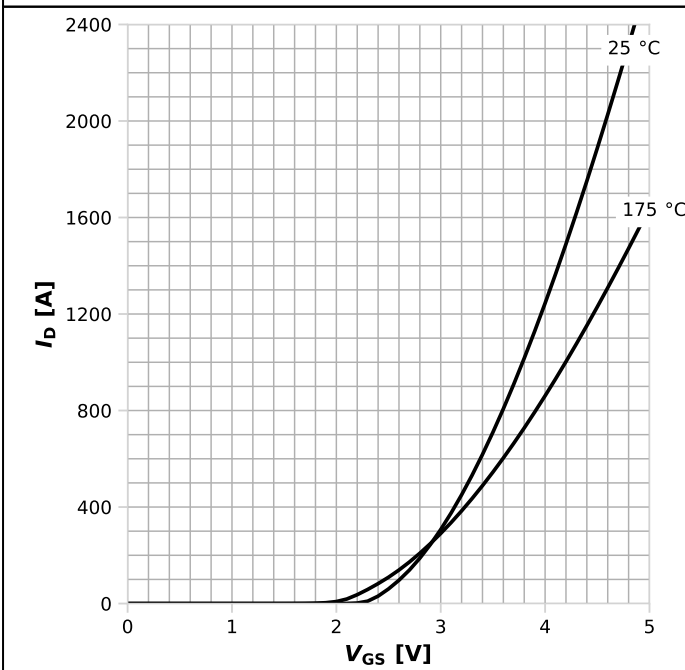
$I_D = f(V_{DS}), T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



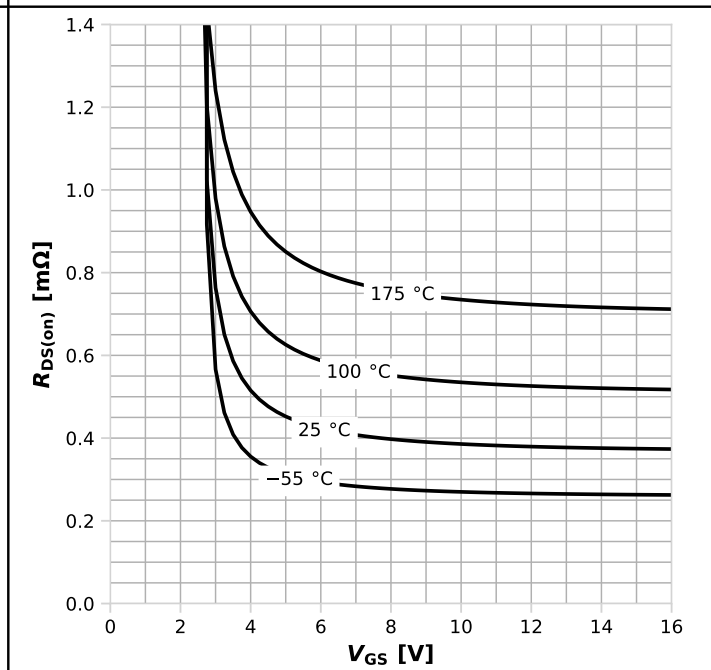
$R_{DS(on)} = f(I_D), T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



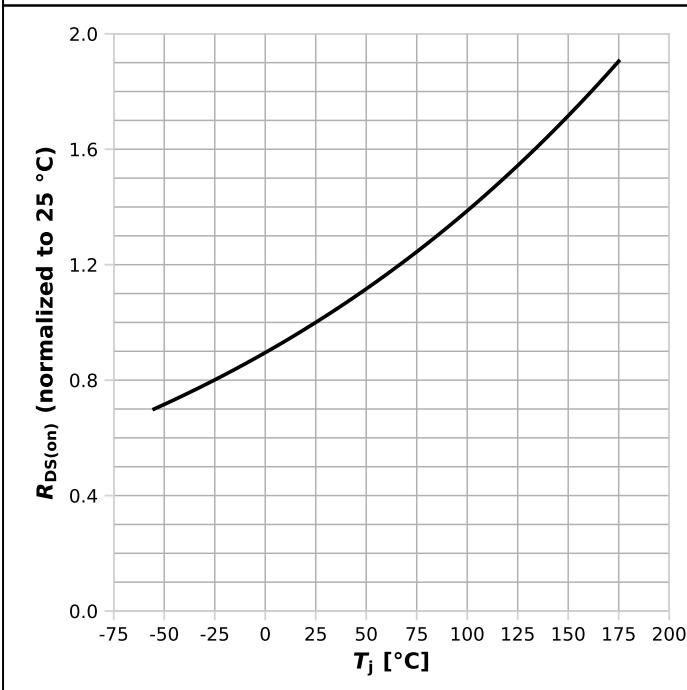
$I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)max};$ parameter: T_j

Diagram 8: Typ. drain-source on resistance



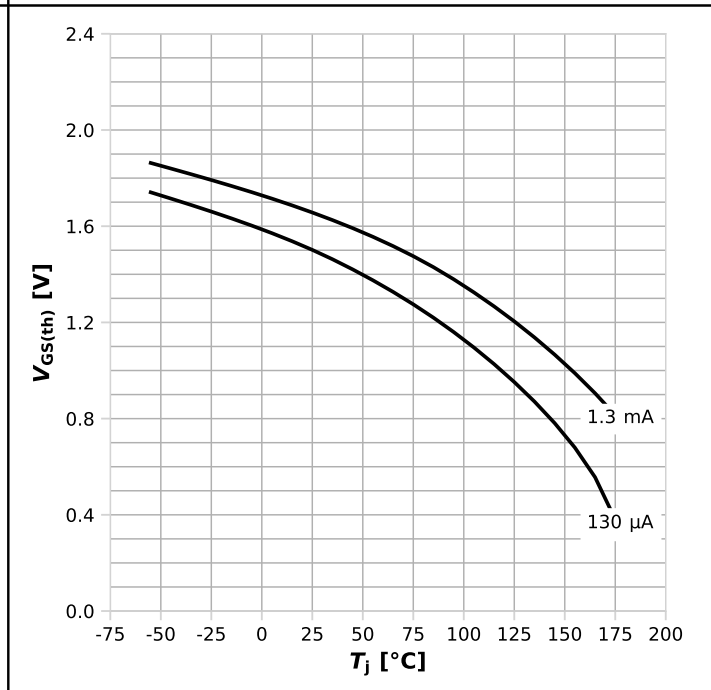
$R_{DS(on)} = f(V_{GS}), I_D = 50\text{ A};$ parameter: T_j

Diagram 9: Normalized drain-source on resistance



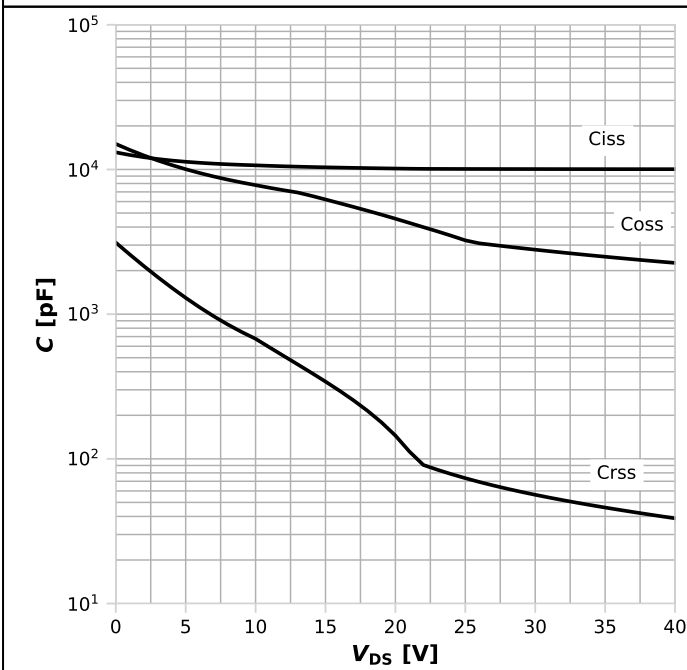
$R_{DS(on)}=f(T_j), I_D=50 \text{ A}, V_{GS}=10 \text{ V}$

Diagram 10: Typ. gate threshold voltage



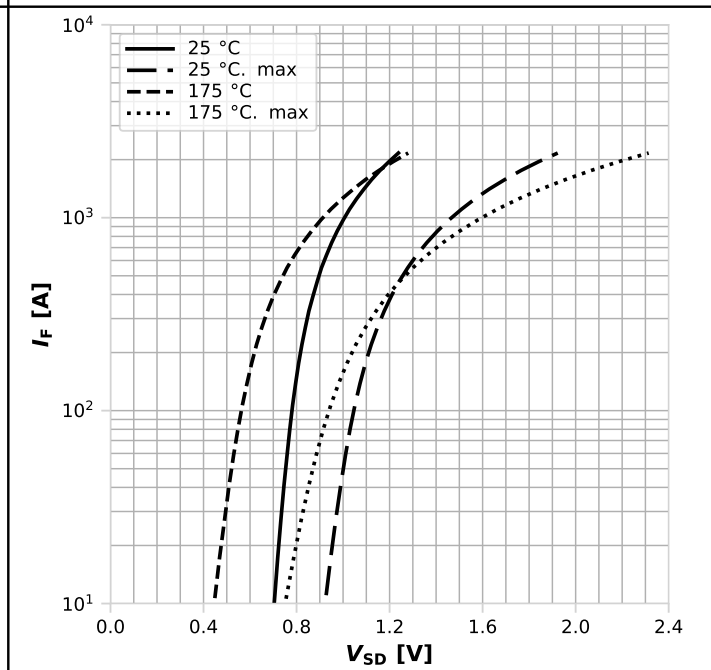
$V_{GS(th)}=f(T_j), V_{GS}=V_{DS}; \text{parameter: } I_D$

Diagram 11: Typ. capacitances



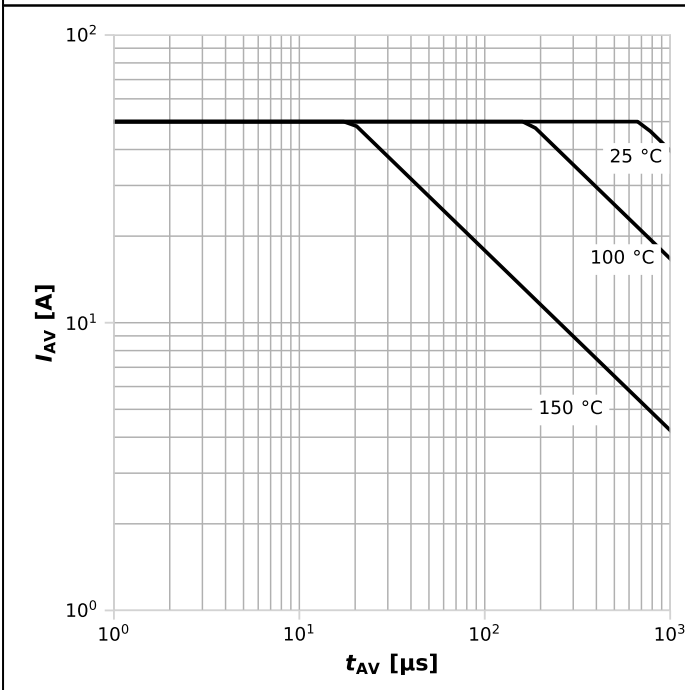
$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



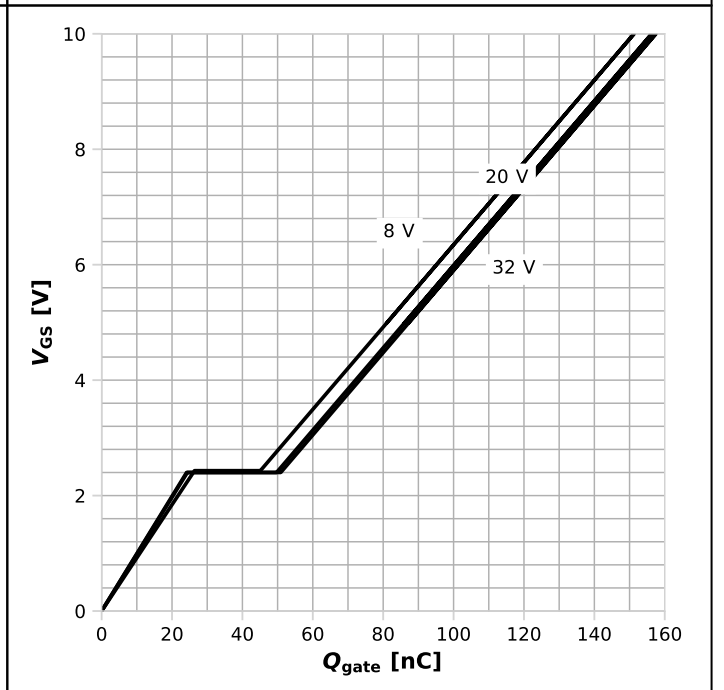
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 13: Avalanche characteristics



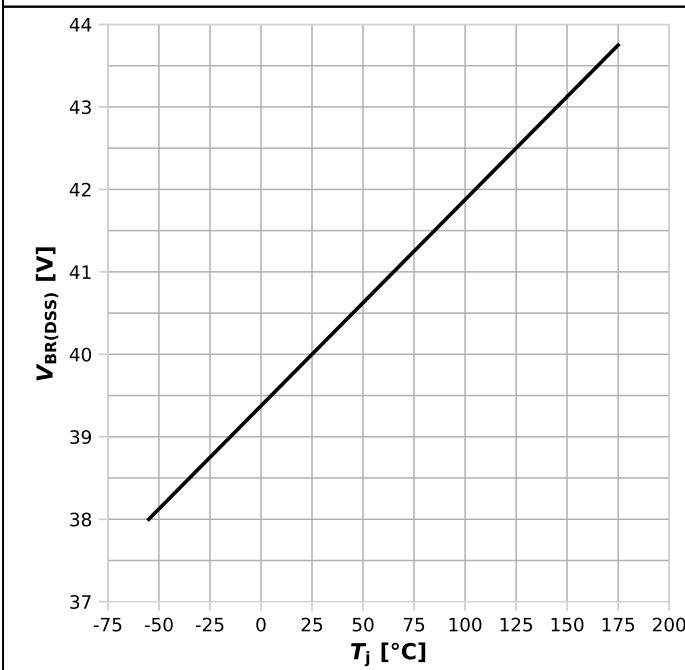
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



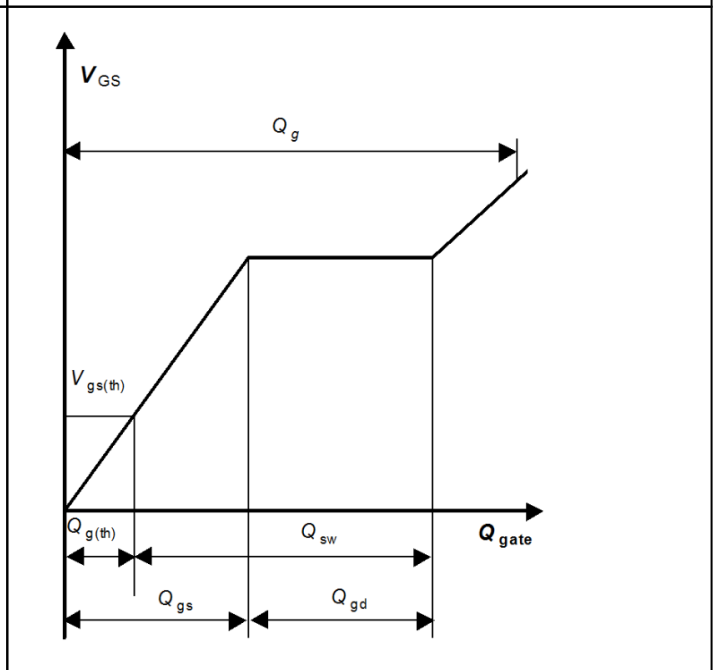
$V_{GS}=f(Q_{gate}), I_D=50 \text{ A pulsed}, T_j=25 \text{ °C}$; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



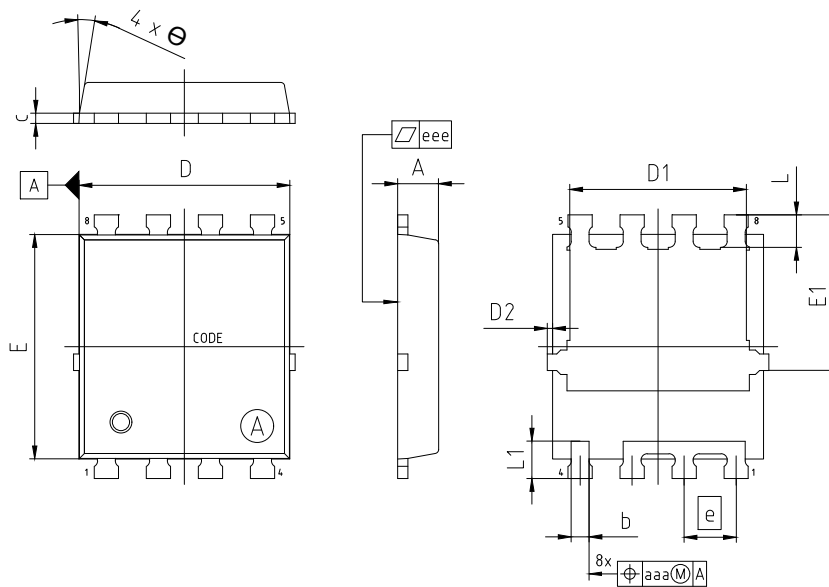
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



-

5 Package Outlines



PACKAGE - GROUP NUMBER: PG-TDSON-8-U02		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.10
b	0.34	0.54
c	0.15	0.35
D	5.05	5.25
D1	4.20	4.40
D2	0.00	0.23
E	5.38	5.58
E1	3.70	3.90
e	1.27	
L	0.70	0.90
L1	0.81	1.01
Θ	8°	12°
aaa	0.25	
eee	0.03	

NOTES:

- 1) EXCLUDED MOLD FLASH
- 2) REMOVAL ON MOLD GATE:
INTRUSION 0.1mm
PROTRUSION 0.1mm
- 3) LEAD LENGTH UP TO ANTI FLASH LINE
- 4) ALL METAL SURFACES ARE PLATED,
EXCEPT AREA OF CUT

Figure 1 Outline PG-TDSON-8, dimensions in mm

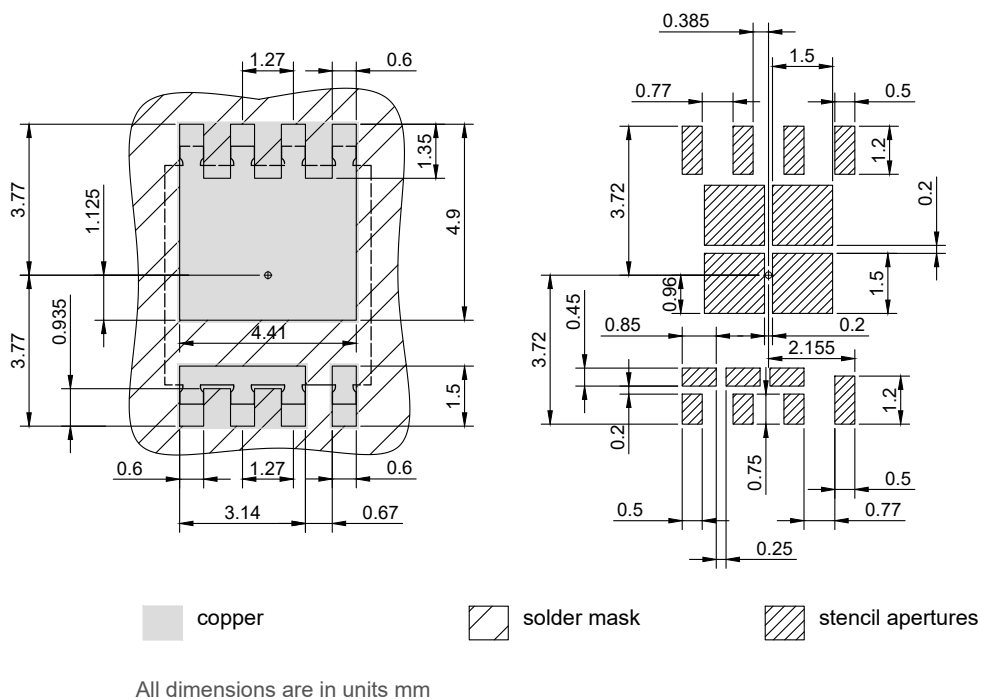


Figure 2 Outline PG-TDSON-8, dimensions in mm

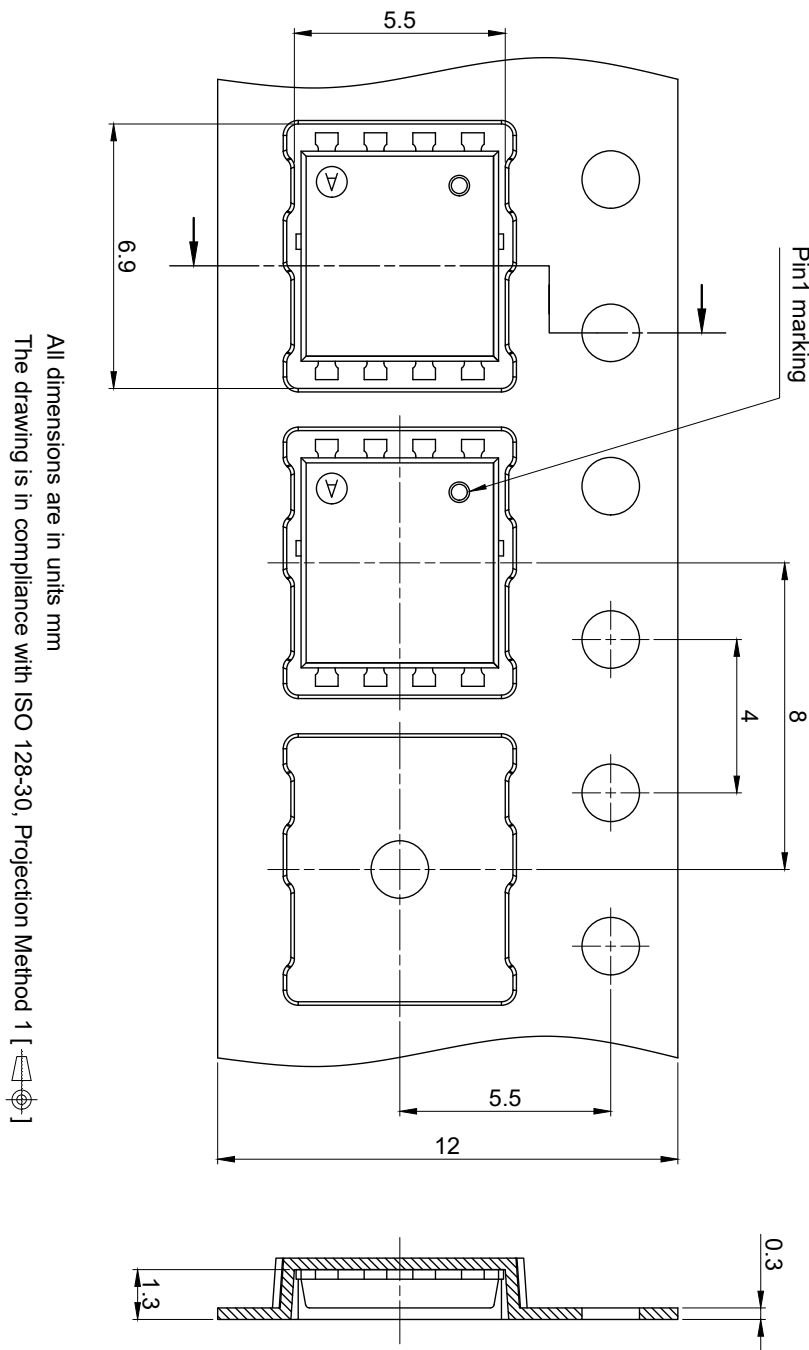


Figure 3 Outline PG-TDSON-8, dimensions in mm

Revision History

ISCH42N04LM7

Revision 2024-04-24, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
0.9	2024-04-08	Release of target version
2.0	2024-04-24	Release of final

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

We Listen to Your Comments Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: erratum@infineon.com

Published by

Infineon Technologies AG
81726 München, Germany
© 2024 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie"). With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.