ANALOG DEVICES

ADPA7005-EVALZ User Guide
UG-1657

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Evaluating the ADPA7005 18 GHz to 44 GHz, GaAs, pHEMT, 32 dBm (>1 W), MMIC Power Amplifier

FEATURES

2-Layer Rogers 4350 evaluation board with heat sink
End launch 2.9 mm RF connectors
Through calibration path

EVALUATION KIT CONTENTS

ADPA7005-EVALZ evaluation board

EQUIPMENT NEEDED

RF signal generator
RF spectrum analyzer
RF network analyzer
5 V, 2 A power supply
−1.5 V, 100 mA power supply

GENERAL DESCRIPTION

The ADPA7005-EVALZ consists of a two-layer printed circuit board (PCB) fabricated from a 10 mil thick, Rogers 4350B, copper clad mounted to an aluminum heat sink. The heat sink assists in providing thermal relief to the device as well as mechanical support to the PCB. Mounting holes on the heat sink allow attachment to larger heat sinks for improved thermal management. The RFIN and RFOUT ports on the ADPA7005-EVALZ are populated by 2.9 mm, female coaxial connectors. The respective RF traces have a 50 Ω characteristic impedance.

The ADPA7005-EVALZ is populated with components suitable for use over the entire −40°C to +85°C operating temperature range of the device. To calibrate board trace losses, a through calibration path is provided between the J1 and the J2 connectors. J1 and J2 must be populated with RF connectors to use the through calibration path. See Table 2 and Figure 3 for the through calibration path performance.

The power voltages, ground voltages, gate control voltages, and detector output voltages are accessed through two 8-pin headers (see Table 1).

The RF traces are 50 Ω, grounded, coplanar waveguide. Package ground leads and the exposed paddle connect directly to the ground plane. Multiple vias are used to connect the top and bottom ground planes with particular focus on the area directly beneath the ground paddle to provide adequate electrical conduction and thermal conduction to the heat sink.

The power supply decoupling capacitors on the ADPA7005-EVALZ represent the configuration that was used to characterize and qualify the device. There may be a scope to reduce the number of capacitors, but the scope varies from system to system. It is recommended to first remove or combine the largest capacitors that are farthest from the device.

TABLE OF CONTENTS

REVISION HISTORY

1/2022—Rev. 0 to Rev. A

Changes to Figure 5 Caption 5

12/2019—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

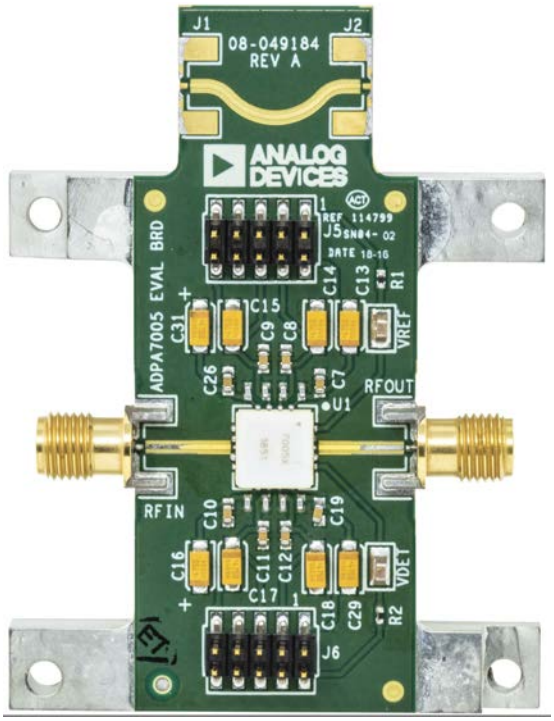

Figure 1. ADPA7005-EVALZ, Top Side

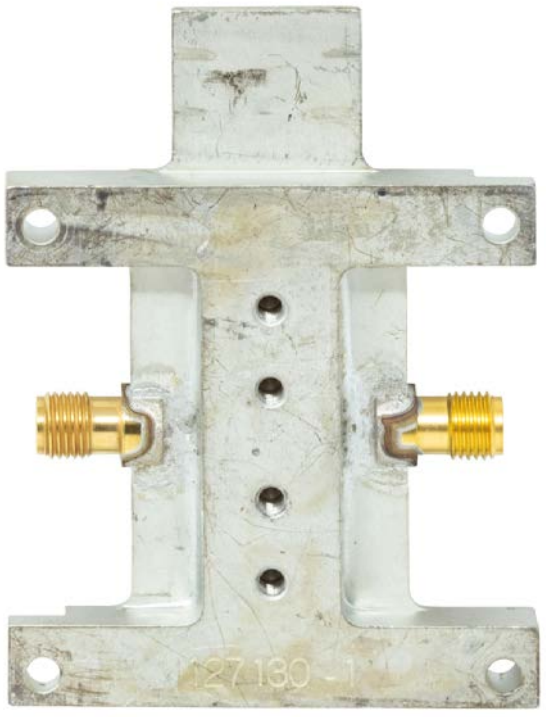

Figure 2. ADPA7005-EVALZ, Bottom Side

OPERATING THE ADPA7005-EVALZ

A 5 V, 2 A power supply is required to provide the main bias to the ADPA7005-EVALZ. Connect the 5 V power supply in parallel to all VDD lines (VDD1, VDD2, VDD3, VDD4, VDD5, and VDD6) through the J5 and J6 headers. A 0 to −1.5 V, 100 mA power supply is required to provide the required gate control voltage. Connect the −1.5 V power supply in parallel to the VGG1 and VGG2 lines through the J5 and J6 headers.

POWER-UP

During power-up, use the following biasing sequence:

1. Connect the ADPA7005 GND pin to the RF ground and dc ground.
2. Initially, set all gate voltages (V_{GG1}, V_{GG2}) and drain voltages (V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{DD5}, and V_{DD6}) to 0 V.
3. Set the ADPA7005 V_{GG1} pin and V_{GG2} pin voltages to −1.5 V.
4. Set all drain bias voltages (V_{DDX} pin voltages) to 5 V.
5. Increase the V_{GG1} pin and V_{GG2} pin voltages to achieve a quiescent drain current of 1.4 A.
6. Apply the RF signal.

POWER-DOWN

During power-down, use the following biasing sequence:

1. Turn off the RF signal.
2. Decrease the V_{GG1} pin and V_{GG2} pin voltages to −1.5 V to achieve I_{DQ} = 0 mA (approximately, where I_{DQ} is quiescent drain current).
3. Decrease all V_{DDX} pin voltages to 0 V.
4. Decrease the V_{GG1} and V_{GG2} pin voltages to 0 V.

Table 1. J5 and J6 Header Connections to ADPA7005

Connector	Header	ADPA7005 Pin
J5	1	VREF (through a 100 kΩ resistor)
J5	2	V_{DD1}
J5	3, 5, 7, 8, 9	GND
J5	4	V_{DD3}
J5	6	V_{DD5}
J5	10	V_{GG1}
J6	1	V_{DD2}
J6	2	VDET (through a 100 kΩ resistor)
J6	3	V_{DD4}
J6	4, 6, 7, 8, 10	GND
J6	5	V_{DD6}
J7	9	V_{GG2}

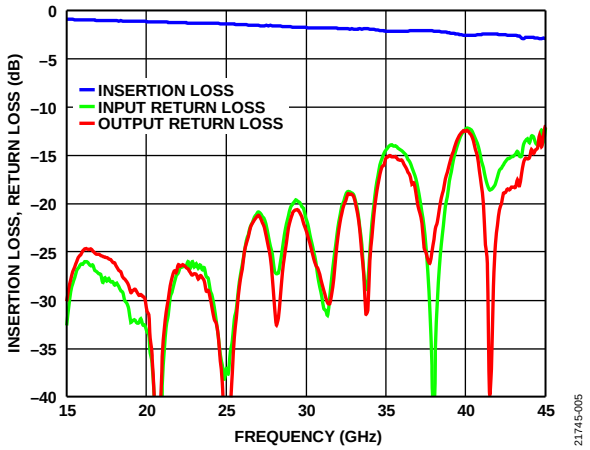

Figure 3. Insertion Loss and Return Loss of Through Calibration Path

Table 2. Insertion Loss and Return Loss of Through Calibration Path

Frequency (GHz)	Insertion Loss (dB)
15	−0.9
17.5	−1.1
20	−1.2
22.5	−1.3
25	−1.4
27.5	−1.6
30	−1.8
32.5	−1.9
35	−2.1
37.5	−2.1
40	−2.6
42.5	−2.5
45	−3

EVALUATION BOARD SCHEMATIC AND ARTWORK

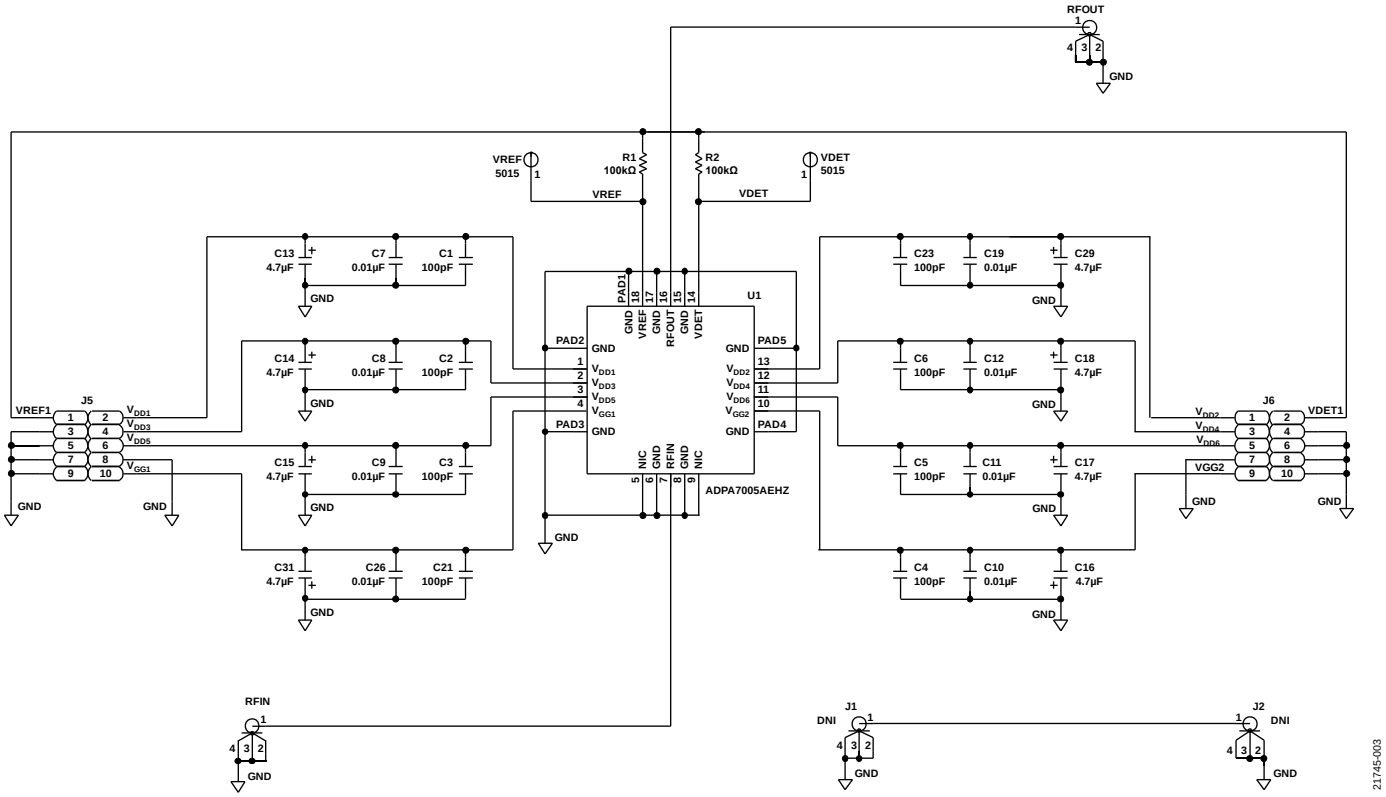

Figure 4. ADPA7005-EVALZ Schematic

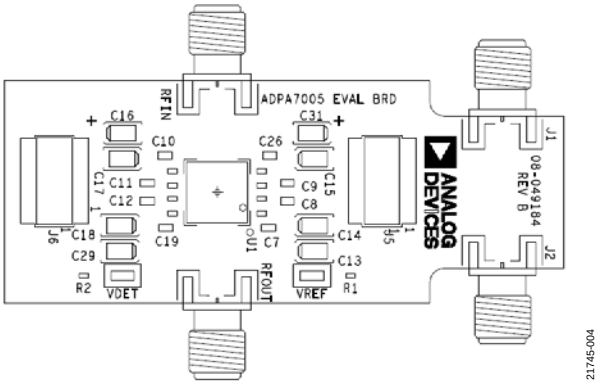

Figure 5. ADPA7005-EVALZ Assembly Drawing (J1 and J2 Not Installed)

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Qty	Reference Designator	Description	Manufacturer	Part Number
8	C1 to C6, C21, C23	Ceramic capacitors, 100 pF	Kemet	C0402C101J5GACTU
8	C7 to C12, C19, C26	Ceramic capacitors, 0.01 µF	Yaego	CC0603KRX7R9BB103
8	C13 to C18, C29, C31	Tantalum capacitors, 4.7 µF	AVX	TAJA475K020RNJ
2	J5, J6	PCB connector headers, 10-position, male, dual-row, 2 mm pitch	Molex	87759-1014
2	R1, R2	Thick film chip resistors, 100 kΩ	Panasonic	ERJ-2RKF1003X
2	RFIN, RFOUT	Connectors, 2.9 mm, jack, PCB mount receptacle	SRI Connector Gage Company	25-146-1000-92
1	U1	18 GHz to 44 GHz, gallium arsenide (GaAs), pseudo morphic high electron mobility transistor (pHEMT), 32 dBm (>1 W), microwave monolithic integrated circuit (MMIC) power amplifier	Analog Devices	ADPA7005AEHZ
2	VDET, VREF	PCB connector surface mount technology (SMT) test points	Keystone Electronics	5015
2	J1, J2	Connectors, 2.9 mm, jack, PCB mount receptacle, do not install (DNI)	SRI Connector Gage Company	25-146-1000-92
	Not applicable	Aluminum heat sink, 2.51 in x 1.9 in	N/A	N/A