EV-SOMCRR-EZLITE ® Manual

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ANALOG DEVICES

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Regulatory Compliance

The *EV-SOMCRR-EZLITE* evaluation board is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer-end product or as a portion of a consumer-end product. The board is an open system design, which does not include a shielded enclosure and, therefore, may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The *EV-SOMCRR-EZLITE* evaluation board contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused boards in the protective shipping package.	

Contents

1 Preface

Thank you for purchasing the Analog Devices, Inc. *EV-SOMCRR-EZLITE* carrier evaluation board.

The evaluation board is designed to be used in conjunction with the CrossCore Embedded Studio® development environment for advanced application code development and debug, with features that enable the ability to:

- Create, compile, assemble, and link application programs written in C++, C, and assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers

Purpose of This Manual

This manual provides instructions for installing the product hardware (board). This manual describes the operation and configuration of board components and provides guidelines for running code on the board.

Manual Contents

The manual consists of:

- ***Using the board***

  Provides basic board information.

- ***Hardware Reference***

  Provides information about the hardware aspects of the board.

- ***Bill of Materials***

  A companion file in PDF format that lists all of the components used on the board is available on the website at http://www.analog.com/EV-SOMCRR-EZLITE.

- ***Schematic***

  A companion file in PDF format documenting all of the circuits used on the board is available on the website at http://www.analog.com/EV-SOMCRR-EZLITE.

Technical Support

You can reach Analog Devices technical support in one of the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:

  http://ez.analog.com/community/dsp

- Submit your questions to technical support directly at:

  http://www.analog.com/support

- E-mail your questions about processors, DSPs, and tools development software from ***CrossCore Embedded Studio*** or ***VisualDSP++***®:

  If using CrossCore Embedded Studio or VisualDSP++ choose ***Help > Email Support***. This creates an e-mail to processor.tools.support@analog.com and automatically attaches your CrossCore Embedded Studio or VisualDSP++ version information and `license.dat` file.

- E-mail your questions about processors and processor applications to:

  processor.support@analog.com

  processor.china@analog.com

- Contact your Analog Devices sales office or authorized distributor. Locate one at:

  http://www.analog.com/adi-sales

Supported Integrated Circuit

This evaluation system supports the Analog Devices ADI IC.

Supported Tools

Information about code development tools for the *EV-SOMCRR-EZLITE* evaluation board and SHARC product family is available at:

http://www.analog.com/EV-SOMCRR-EZLITE

Product Information

Product information can be obtained from the Analog Devices website and the online help system.

Information about the ADI product family is available at:

Analog Devices Website

The Analog Devices website, http://www.analog.com, provides information about a broad range of products - analog integrated circuits, amplifiers, converters, transceivers, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, MyAnalog.com is a free feature of the Analog Devices website that allows customization of a web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the web pages that meet your interests, including documentation errata against all manuals. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

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EngineerZone

EngineerZone is a technical support forum from Analog Devices, Inc. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

2 Using the Board

This chapter provides information on the major components and peripherals on the board, along with instructions for installing and setting up the emulation software.

Product Overview

The board features:

- System-on-Module (SoM) connector
  - Compatible with Analog Devices DSP SoMs
- Audio
  - Analog Devices ADAU1372
  - 3x 3.5mm Stereo connectors: 2 outputs and 4 inputs
- A^2B
  - Two A^2B interface connectors for the A^2B mini modules
- Gigabit ethernet
  - ADIN1300 10/100/1000 Gigabit Ethernet
- USB Interfaces
  - USB3317 USB 2.0 PHY
  - FT4222HQ USB to Quad SPI Interface
- Debug Interface (JTAG)
  - On-Board debug agent
- LEDs
  - 12 LEDs: one power (green), one board reset (red), three general-purpose (amber), six A^2B LEDs, and one RGB LED for on-board debug agent
- Pushbuttons

    - Three pushbuttons: one reset and two IRQ/Flag
- External power supply
    - CE compliant
    - 12V @1.6 Amps

Package Contents

Your *EV-SOMCRR-EZLITE* package contains the following items.

- *EV-SOMCRR-EZLITE* board
- Universal 12V DC power supply
- Two USB 2.0 type A to USB-C cables
- Ethernet Cable

Contact the vendor where you purchased your *EV-SOMCRR-EZLITE* evaluation board or contact Analog Devices, Inc. if any item is missing.

Default Configuration

The ***Default Hardware Setup*** figure shows the default settings for jumpers and switches and the location of the jumpers, switches, connectors, and LEDs. Confirm that your board is in the default configuration before using the board.

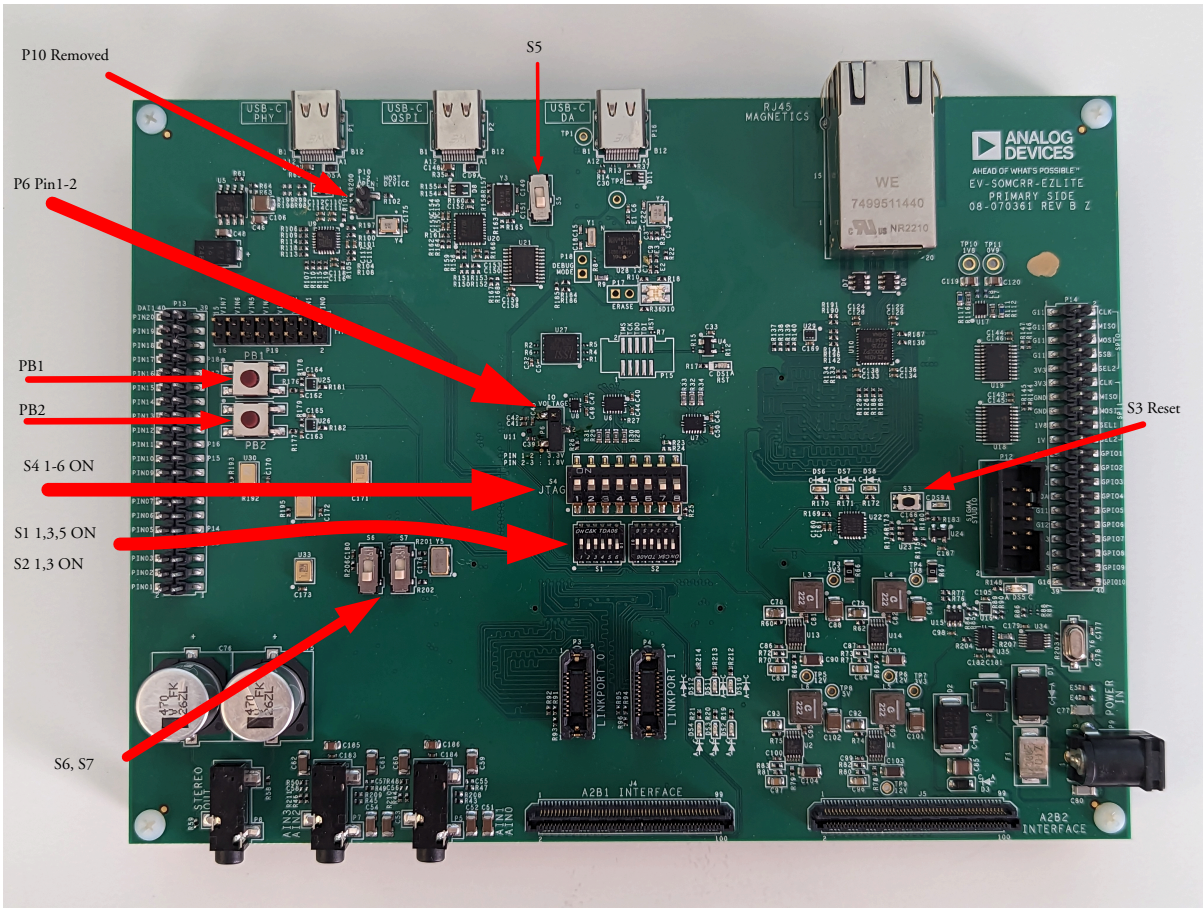

Figure 2-1: Default Hardware Setup

CrossCore Embedded Studio (CCES) Setup

Debug Agent

The *EV-SOMCRR-EZLITE* provides a JTAG connection via an onboard Debug Agent. The Debug Agent uses a USB connection to the PC and allows debugging of Analog Devices DSPs without the need of an external ICE.

Power-On-Self Test

The Power-On-Self-Test Program (POST) tests all the EZ-KIT carrier board peripherals and validates functionality as well as connectivity to the processor. Once assembled, each EZ-KIT carrier board is fully tested for an extended period of time with POST for all the compatible SoM modules. All EZ-KIT carrier boards are shipped with POST preloaded into flash memory. The POST is executed by resetting the board and connecting the USB To UART to your PC with an open terminal window. The POST also can be used as a reference for a custom software design or hardware troubleshooting.

Note that the source code for the POST program is included in the Board Support Package (BSP) along with the readme file that describes how the board is configured to run POST.

Example Programs

Example programs are provided with the *EV-SOMCRR-EZLITE* Board Support Package (BSP) to demonstrate various capabilities of the product. The programs can be found in the `EV-SOMCRR-EZLITE\examples` installation folder. Refer to the readme file provided with each example for more information.

Reference Design Information

A reference design info package is available for download on the Analog Devices Web site. The package provides information on the schematic design, layout, fabrication, and assembly of the board.

The information can be found at:

http://www.analog.com/EV-SOMCRR-EZLITE

Automotive Audio Bus A^{2}B Interface

The Automotive Audio Bus (A^{2}B®) provides a multichannel, I^{2}S/TDM link over distances of up to 15 m between nodes. It embeds bidirectional synchronous pulse-code modulation (PCM) data (for example, digital audio), clock, and synchronization signals onto a single differential wire pair. A^{2}B supports a direct point to point connection and allows multiple, daisy-chained nodes at different locations to contribute and/or consume time division multiplexed channel content.

The A^{2}B Interface connects processor evaluation boards, such as the EV-SOMCRR-EZKIT to A^{2}B daugher cards, such as the ADZS-AD2428MINI board. This allows for an expandable and configurable evaluation system for ADI DSPs and A^{2}B technologies.

ADAU1372 - Quad ADC, Dual DAC, Low Latency, Low Power Codec

The ADAU1372 is a codec with four inputs and two outputs, which incorporates asynchronous sample rate converters. Optimized for low latency and low power, the ADAU1372 is ideal for headsets, handsets, and headphones. The ADAU1372 has built-in programmable gain amplifiers (PGAs); thus, with the addition of just a few passive components and a crystal, the ADAU1372 provides a solution for headset audio needs. Microphone preamplifiers, ADCs, DACs, headphone amplifiers and serial ports for connections to an external DSP.

ADM6315 - Open-Drain Microprocessor Supervisory Circuit

The ADM6315 is a reliable voltage-monitoring device that is suitable for use in most voltage-monitoring applications.

The ADM6315 is designed to monitor as little as a 1.8% degradation of a power supply voltage. The ADM6315 can monitor all voltages (at 100 mV increments) from 2.5 V to 5 V.

Included in this circuit is a debounced manual reset input. RESET can be activated using an ordinary switch (pulling MR low), a low input from another digital device, or a degradation of the supply voltage.

The manual reset function is very useful, especially if the circuit in which the ADM6315 is operating enters into a state that can be detected only by the user. Allowing the user to reset a system manually can reduce the damage or danger that could otherwise be caused by an out-of-control or locked-up system.

ADIN1300CCPZ- 10/100/1000 Ethernet Physical Layer

The ADIN1300 is a low power, single port, Gigabit Ethernet transceiver with low latency and power consumption specifications primarily designed for industrial Ethernet applications).

This design integrates an energy efficient Ethernet (EEE) physical layer device (PHY) core with all associated common analog circuitry, input and output clock buffering, management interface and subsystem registers, and MAC interface and control logic to manage the reset and clock control and pin configuration.

The ADIN1300 is available in a 6 mm × 6 mm, 40-lead lead frame chip scale package (LFCSP). The device operates with a minimum of 2 power supplies, 0.9 V and 3.3 V, assuming the use of a 3.3 V MAC interface supply. For maximum flexibility in system level design, a separate VDDIO supply enables the management data input/output (MDIO) and MAC interface supply voltages to be configured independently of the other circuitry on the ADIN1300, allowing operation at 1.8 V, 2.5 V, or 3.3 V. At power-up, the ADIN1300 is held in hardware reset until each of the supplies has crossed its minimum rising threshold value. Brown-out protection is provided by monitoring the supplies to detect if one or more supply drops below a minimum falling threshold (see Table 19 on the datasheet), and holding the device in hardware reset until the power supplies return and satisfy the power-on reset (POR) circuit.

The MII management interface (also referred to as MDIO interface) provides a 2-wire serial interface between a host processor or MAC (also known as management station (STA)) and the ADIN1300, allowing access to control and status information in the PHY core management registers. The interface is compatible with both the IEEE 802.3 Standard Clause 22 and Clause 45 management frame structures.

The ADIN1300 can support cable lengths up to 150 meters at Gigabit speeds and 180 meters when operating at 100 Mbps or 10 Mbps.

FT4222HQ - USB to Quad SPI

The FT4222HQ is a High/Full Speed USB2.0-to-Quad SPI/I2C device controller in a compact 32-pin QFN package.

- The device requires an external crystal at 12MHz in order for the internal PLL to operate. It supports multi-voltage IO: 1.8/2.5 and 3.3V and provides 128 bytes one-time-programmable (OTP) memory space for storing vendor-specific information. This device contains both SPI and I2C configurable interfaces.
- The SPI interface can be configured as master mode with single, dual and quad bits data width transfer, or slave mode with single bit data width transfer.
- The I2C interface can be configured in master or slave mode. The FT4222HQ is available in in a space saving Pb-free (RoHS compliant) 32-pin QFN package.
- Key Hardware Features
- Single chip USB2.0 Hi-speed to SPI/I2C bridge with a variety of configurations.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- On-chip OTP memory for USB Vendor ID (VID), Product ID (PID), device serial number, product description string and various other vender specific data Configurable industry standard SPI Master/Slave interface controller Support configurable data width with single, dual, quad data width transfer mode in SPI master SCK can support up to 30MHz in SPI master Up to 53.8Mbps data transfer rate in SPI master with quad mode transfer Support single bit data transfer with full-duplex transfer in SPI Slave register.
- Support up to 4 channels slave selection control pins in SPI master application Configurable I2C Master/Slave interface controller conforming to I2C v2.1 and v3.0 specification
- Supports 100kbit/s standard mode (SM), 400kbit/s fast mode (FM), 1 Mbit/s Fast mode plus (FM+), and 3.4 Mbit/s High Speed mode (HS) Configurable GPIOs can be easily controlled by software applications via USB bus
- USB Battery Charger Detection. Allows for USB peripheral devices to detect the presence of a higher current power source to enable faster charging
- Device supplied pre-programmed with unique USB serial number
- USB Power Configurations; supports bus-powered, self-powered and bus-powered with power switching +5V USB VBUS detection engine
- True 3.3V CMOS drive output and TTL input. (operates down to 1V8 with external pull-ups) Configurable I/O pin output drive strength; 4 mA(min) and 16 mA(max) Integrated power-on-reset circuit
- USB2.0 Low operating and suspend current; 68mA (active-type) and 375µA (suspend-type)
- UHCI/OHCI/EHCI host controller compatible
- FTDI Chip's royalty-free Direct (D2XX) drivers for Windows eliminate the requirement for USB driver development in most cases
- Extended operating temperature range; -40°C to 85°C Available in compact Pb-free 32 Pin VQFN packages (RoHS compliant).

USB3317 - Hi-Speed USB 2.0 Transceiver with 1.8v-3.3v ULPI Interface

The USB331x family of Hi-Speed USB 2.0 transceivers provides a highly integrated, small footprint solution designed for portable consumer electronics devices including cell phones, PDAs, portable media players and GPS/ personal navigation devices. The USB331x family eliminates the need for external USB switches and electrostatic discharge (ESD) protection devices, which minimizes eBOM part count and printed circuit board (PCB) area. The USB331x provides an extremely flexible solution which allows the USB connector to act as a single port of connection for high speed data transfer, battery charging and stereo/mono audio accessories.

3 Hardware Reference

This chapter describes the hardware design of the *EV-SOMCRR-EZLITE* carrier board.

System Architecture

The board's configuration is shown in the ***Block Diagram*** figure.

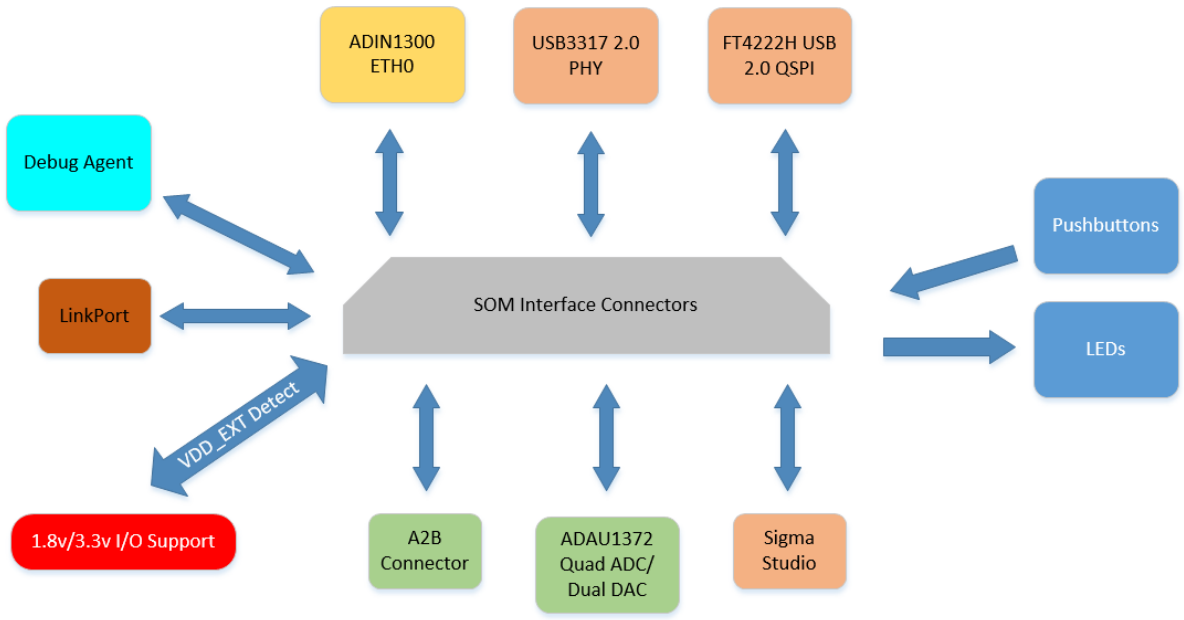

Figure 3-1: Block Diagram

This Carrier board is designed to demonstrate the connected System on Module processor's capabilities. The peripherals help evaluate the processor's features with audio DAC and ADCs, 10/100/1000 ethernet, and A^2B expansion.

User I/O to the processor is provided in the form of two pushbuttons and three LEDs.

The software-controlled switches (SoftConfig) facilitate the switch multi-functionality by disconnecting the pushbuttons from their associated processor pins and reusing the pins elsewhere on the board.

Software-Controlled Switches (SoftConfig)

On the board, most of the traditional mechanical switches and jumpers have been replaced by I^2C software-controlled switches. The remaining mechanical switches are provided for the boot mode and pushbuttons. Reference any `SoftConfig*.c` file found in the installation directory for an example of how to set up the SoftConfig feature of the board through software. The SoftConfig section of this manual serves as a reference to any user that intends to modify an existing software example. If software provided by ADI is used, there should be little need to reference this section.

NOTE: Care should be taken when changing SoftConfig settings not to create a conflict with interfaces. This is especially true when connecting extender cards.

Overview of SoftConfig

In order to further clarify the use of electronic single FET switches and multi-channel bus switches, an example of each is illustrated and compared to a traditional mechanical switching solution. This is a generic example that uses similar FET and bus switch components that are on the board.

After this generic discussion there is a detailed explanation of the SoftConfig interface specific to the *EV-SOMCRR-EZLITE*.

The ***Example of Individual FET Switches*** figure shows two individual FET switches (Pericom PI3A125CEX) with reference designators `UA` and `UB`. Net names `ENABLE_A` and `ENABLE_B` control `UA` and `UB`. The default FET switch enable settings in this example are controlled by resistors `RA` and `RB` which pull the enable pin 1 of `UA` and `UB` to ground (low). In a real example, these enable signals are controlled by the IO expander. The default pull-down resistors connects the signals `EXAMPLE_SIGNAL_A` and `EXAMPLE_SIGNAL_B` and also connects signals `EXAMPLE_SIGNAL_C` and `EXAMPLE_SIGNAL_D`. To disconnect `EXAMPLE_SIGNAL_A` from `EXAMPLE_SIGNAL_B`, the IO expander is used to change `ENABLE_A` to a logic 1 through software that interfaces with the Microchip. The same procedure for `ENABLE_B` disconnects `EXAMPLE_SIGNAL_C` from `EXAMPLE_SIGNAL_D`.

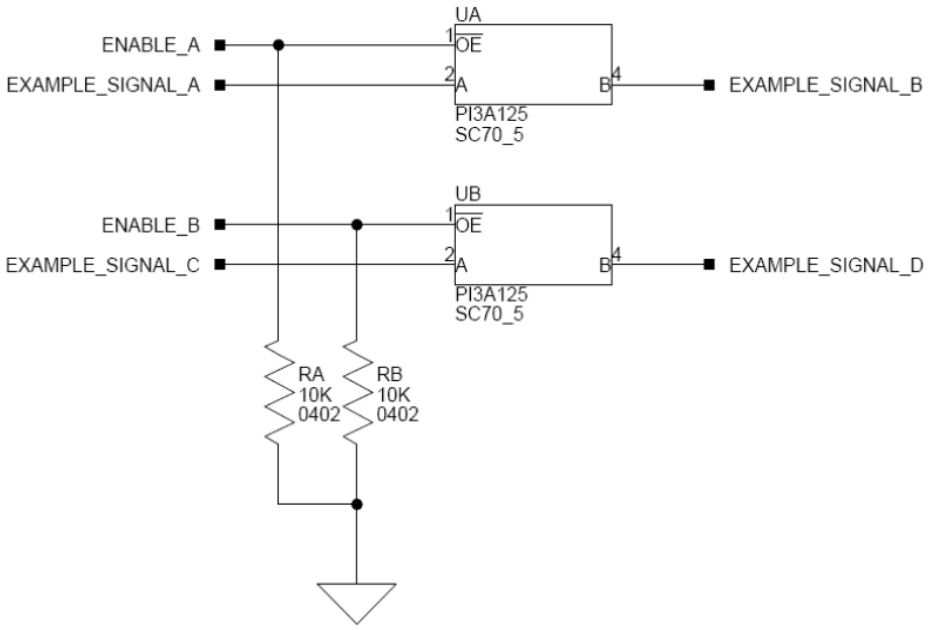

Figure 3-2: Example of Individual FET Switches

The following figure shows the equivalent circuit to the ***Example of Individual FET Switches*** figure but utilizes mechanical switches that are in the same package. Notice the default is shown by black boxes located closer to the ***ON*** label of the switches. In order to disconnect these switches, physically move the switch to the OFF position.

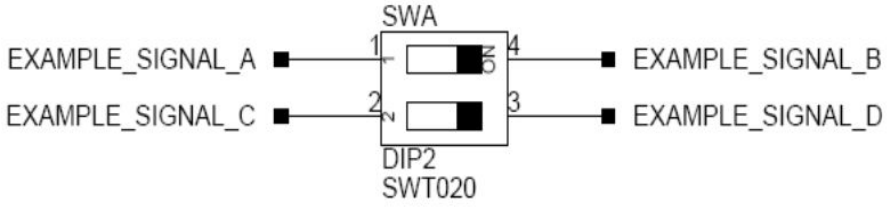

Figure 3-3: Example of a Mechanical Switch (Equivalent to Example of Individual FET Switches Figure)

The ***Example of Bus Switch*** figure shows a bus switch example, reference designator `UC` (Pericom PI3LVD512ZHE), selecting between lettered functionality and numbered functionality. The signals on the left side are multiplexed signals with naming convention letter_number. The right side of the circuit shows the signals separated into letter and number, with the number on the lower group (`0B1`) and the letter on the upper group (`0B2`). The default setting is controlled by the signal `CONTROL_LETTER_NUMBER` which is pulled low. This selects the number signals on the right to be connected to the multiplexed signals on the left by default. In this example, the IO expander is not shown but controls the signal `CONTROL_LETTER_NUMBER` and allows the user to change the selection through software.

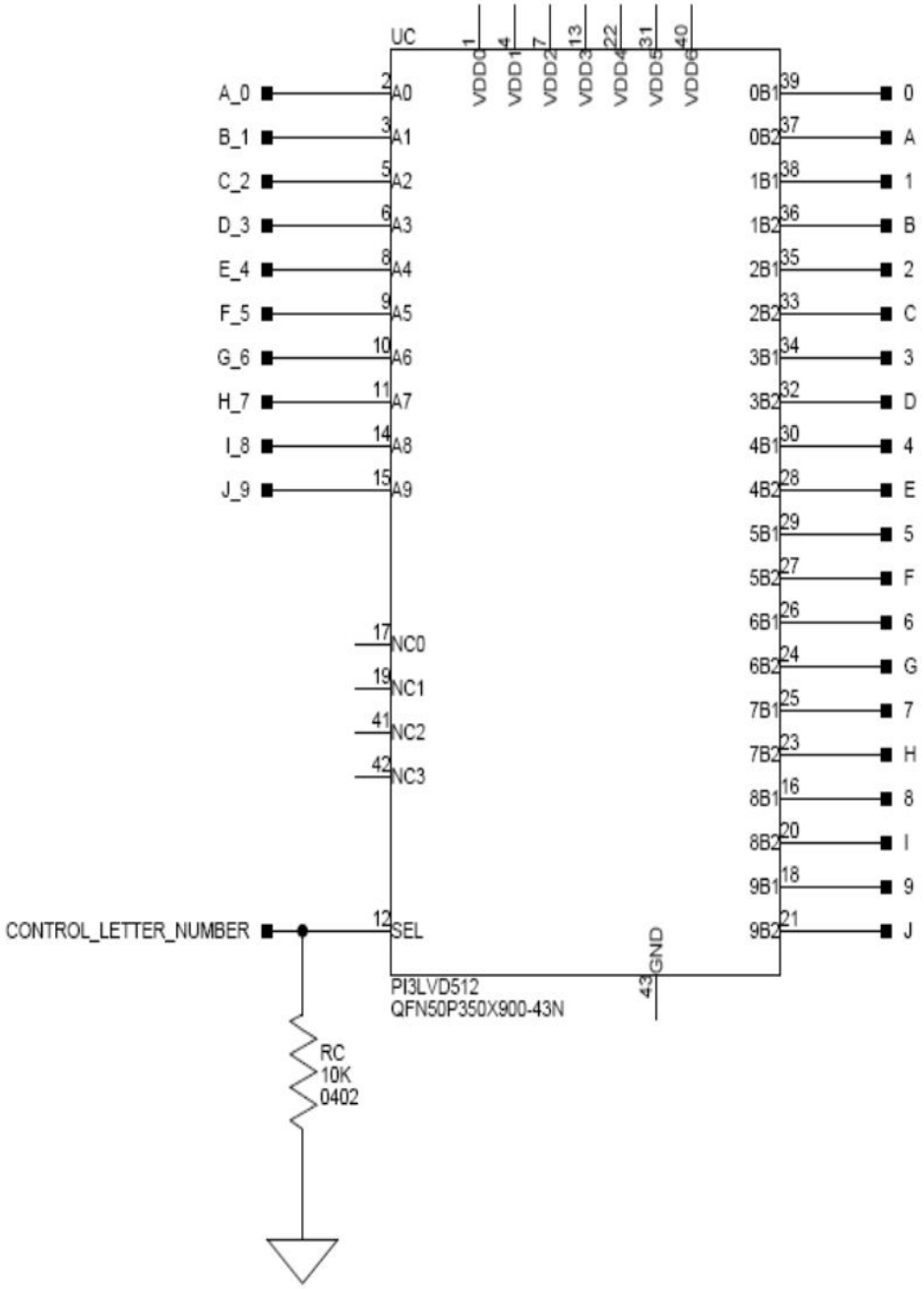

Figure 3-4: Example of a Bus Switch

The following figure shows the equivalent circuit to the ***Example of Bus Switch*** figure but utilizes mechanical switches. Notice the default for reference designators SWC and SWD is illustrated by black boxes located closer to the ***ON*** label of the switches to enable the number signals by default. Also notice the default setting for reference designators SWE and SWF is OFF. In order to connect the letters instead of the numbers, the user physically changes all switches on SWC and SWD to the OFF position and all switches on SWE and SEF to the ON position.

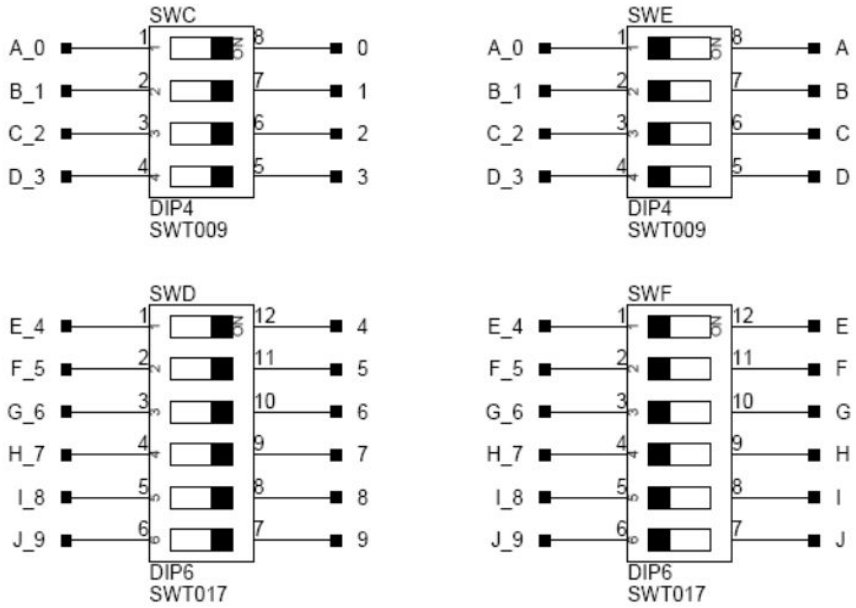

Figure 3-5: Example of a Mechanical Switch (Equivalent to Example of Bus Switch)

Programming SoftConfig Switches

On the board, an ADI ADP5587-1 devices exist. The ADP5587 can be configured as a GPIO extender or a keypad interface. It is used as a GPIO Extended on the System on Module evaluation board.

Refer to the ASP5587-1 datasheet for programming information. https://www.analog.com/media/en/technical-documentation/data-sheets/adp5587.pdf

Each example in the Board Support Software (BSP) includes source files that program the soft switches, even if the default settings are being used. The `README` for each example identifies only the signals that are being changed from their default values. The code that programs the soft switches is located in the `SoftConfig_XXX.c` file in each example where XXX is the name of the baord.

The part number of the ADP5587-1 determines the address of the IC. The ADP5587ACPZ has (***I^2C Hardware Address 0x68*** and the ADP5587ACPZ-1 has ***I^2C Hardware Address 0x60***).

Table below ***Output Signals of ADP5587-1 GPIO Expander (U24)*** show the output signals of the ADI GPIO extender (***U24***), with a TWI address of `0110 100X`, where `X` represents the read or write bit. The signals that control an individual FET have an entry in the ***FET*** column. The ***Component Connected*** column shows the board IC that is connected if the FET is enabled. The (`U24`) is controlling the enable signal of a FET switch. Also note that if a particular functionality of the processor signal is being used, it is in ***bold*** font in the ***Processor Signal*** column.

Table 3-1: Output Signals of ADP5587-1 GPIO Extender (U24)

Connection	*Signal Name*	*Description*	*FET*	*Processor Signal (if applicable)*	*Connected*	*Default*
C9	DS6	GPIO LED		None	DS6	Low
C8	DS7	GPIO LED		None	DS7	Low
C7	DS8	GPIO LED		None	DS8	Low
C6	Pushbutton_EN	Enabled Pushbuttons	U36	Processor Dependent	PB1,PB2	High
C5	$\overline{\text{ADAU1372\_PWRDN}}$	Shudown ADAU1372		Processor Dependent	U12	High
C4	ETH0_RESET	ADIN1300 Reset		Processor Dependent	U10	High
C3	$\overline{\text{USB\_QSPI\_REST}}$	Reset FT4222H USB-QSPI		FT4222H Reset	U20	High
C2	$\overline{\text{USB\_QSPI\_EN}}$	Enable FT4222H USB-QSPI		Processor Dependent	U21	High
C1	$\overline{\text{USBI\_SPI1\_EN}}$	Enables SPI1 on SigmaStudio Connector		SPI1	U18	High
C0	$\overline{\text{USBI\_SPI0\_EN}}$	Enables SPI0 on SigmaStudio Connector		SPI0	U19	Low
R6	A2B2_IRQ	A2B2 IRQ Signal		A2B Interface 2 IRQ		Low
R5	A2B2_RESET	A2B2 Reset Signal		A2B Interface 2 Reset		Low
R4	A2B1_IRQ	A2B1 IRQ Signal		A2B Interface 1 IRQ		Low
R3	A2B1_RESET	A2B1 Reset Signal		A2B Interface 1 Reset		Low
R2	A2B1_IO1	A2B1 IO1 Signal		A2B Interface 1 IO1		Low
R1	A2B1_IO2	A2B1 IO7 Signal		A2B Interface 1 IO2		Low
R0	A2B1_IO7	A2B1 IO7 Signal		A2B Interface 1 IO7		Low

SoftConfig on the Board

The Analog Devices ADP5587-1 GPIO extenders provide control for individual electronic switches. The TWI interface of the processor communicates with the GPIO extender devices. There are individual switches with default settings that enable basic board functionality.

The ***Default Processor Interface Availability*** table lists the processor and board interfaces that are available by default. Note that only interfaces affected by software switches are listed in the table.

Table 3-2: Default Processor Interface Availability

Interface	*Availability by Default*
Pushbutton_EN	Pushbuttons Enabled
USB to QSPI	USB to QSPI Interface Disabled
ADAU1372	Audio Codec Enabled
LEDs	Enabled

Switches

This section describes operation of the switches. The switch locations are shown in the ***Switch/Jumper Locations*** figure.

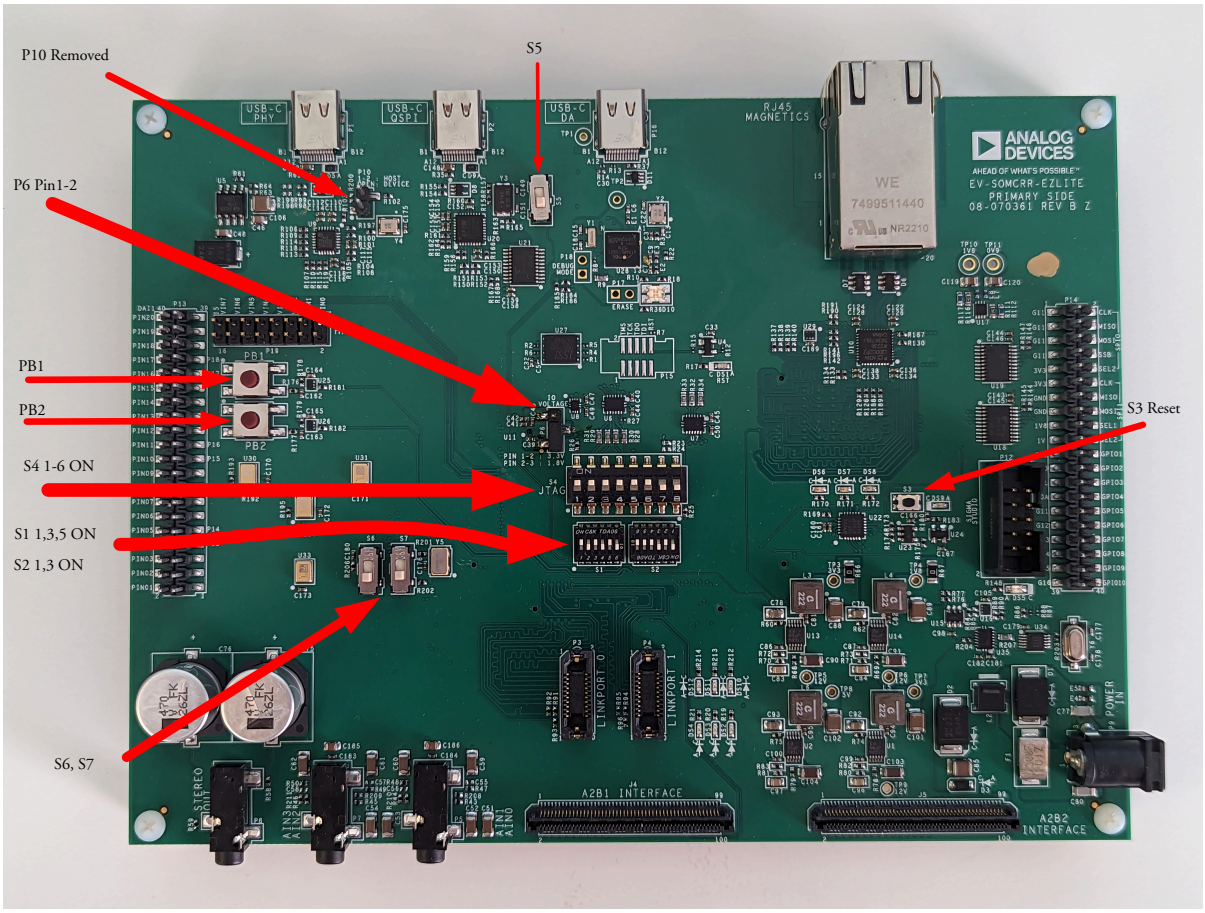

Figure 3-6: Switch/Jumper Locations

Reset Pushbutton (S3)

The reset pushbutton resets the ADI processor. The reset signal also is connected to the SoM interface connectors via the SYS_HWRST signal. Reset (DS9) is used to indicate when the board is in reset.

GPIO Pushbuttons (PB1 and PB2)

The GPIO pushbuttons are connected to the processor's signals GPIO1 and GPIO2, respectively.

The GPIO pushbuttons can be disconnected from the processor by setting SoftConfig. See Software-Controlled Switches (SoftConfig) for more information.

JTAG Interface (S4 S1, S2)

The JTAG Interface switch enables/disables the on-board debug agent. When in the disabled configuration, an ICE can be attached to the JTAG header on the SoM module to provide on-chip debug capabilities.

Table 3-3: Debug Agent Enable

Location	Position
S4.1	ON
S4.2	ON
S4.3	ON
S4.4	ON
S4.5	ON
S4.6	ON
S4.7	OFF
S4.8	OFF

Table 3-4: Debug Agent Disable

Location	Position
S4.1	OFF
S4.2	OFF
S4.3	OFF
S4.4	OFF
S4.5	OFF
S4.6	OFF
S4.7	OFF
S4.8	OFF

Table 3-5: JTAG Over LinkPort Settings - Default Local JTAG

Location	Position
S1.1	ON

Table 3-5: JTAG Over LinkPort Settings - Default Local JTAG (Continued)

Location	Position
S1.2	OFF
S1.3	ON
S1.4	OFF
S1.5	ON
S1.6	OFF
S2.1	ON
S2.2	OFF
S2.3	ON
S2.4	OFF
S2.5	OFF
S2.6	OFF

Jumpers

This section describes the functionality of the configuration jumpers. The ***Switch/Jumper Locations*** figure shows the jumper locations.

HADC ( )

The HADC jumper is used to connect the HADC of the processor to various voltages on the board for monitoring.

P19 Jumper	Voltage
1 and 2	GND
3 and 4	GND
5 and 6	GND
7 and 8	GND
9 and 10	GND
11 and 12	GND
13 and 14	GND
15 and 16	GND

LEDs

This section describes the on-board LEDs. The ***LED Locations*** figure shows the LED locations.

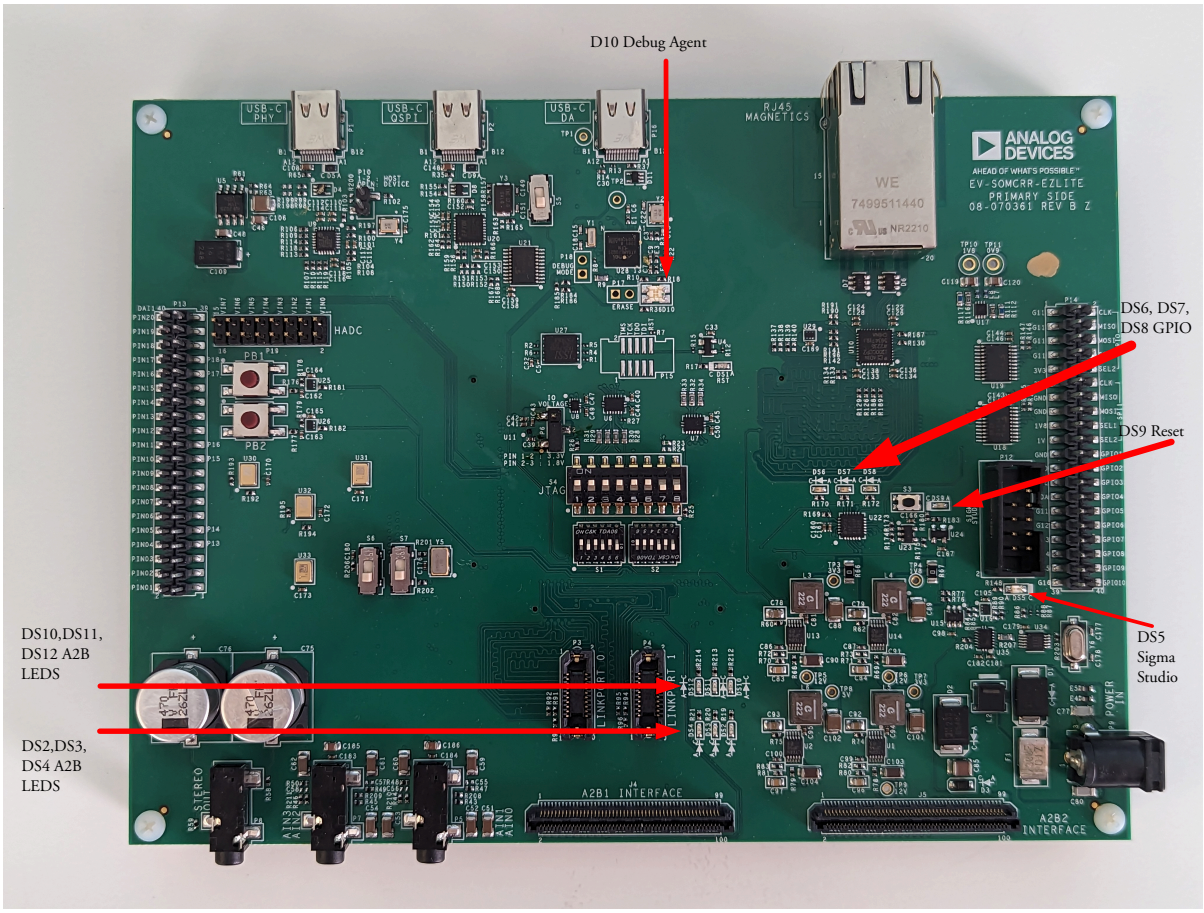

Figure 3-7: LED Locations

A²B Interface LEDs (`LED1, LED2, LED3, LED13, LED14, LED15`)

The A²B Interface LEDs are driven by the connected A2B daughter card on the A2B Interface Connectors. These are connected to A2B IRQ and GPIO signals. Refere to the schematics of the connected A2B or related daughter card for more information.

Power (`LED8`)

When ON (green), it indicates that power is being supplied to the board properly.

GPIO (`DS6, DS7, DS8`)

Three LEDs are connected to the general-purpose I/O pins of the processor (see the ***GPIO LEDs*** table). The LEDs are active high and are turned ON (amber) by writing a 1 to the correct processor signal.

Table 3-6: GPIO LEDs

Reference Designator	*Programmable Flag Pin*
LED7	LED3_KIT
LED9	LED1_KIT
LED10	LED2_KIT

Reset (DS9)

When ON (red), it indicates that the board is in reset. A master reset is asserted by pressing S3, which activates the LED. For more information, see Reset Pushbutton (S3).

Connectors

This section describes connector functionality and provides information about mating connectors. The connector locations are shown in the ***Connector Top*** and ***Connector Bottom*** figures.

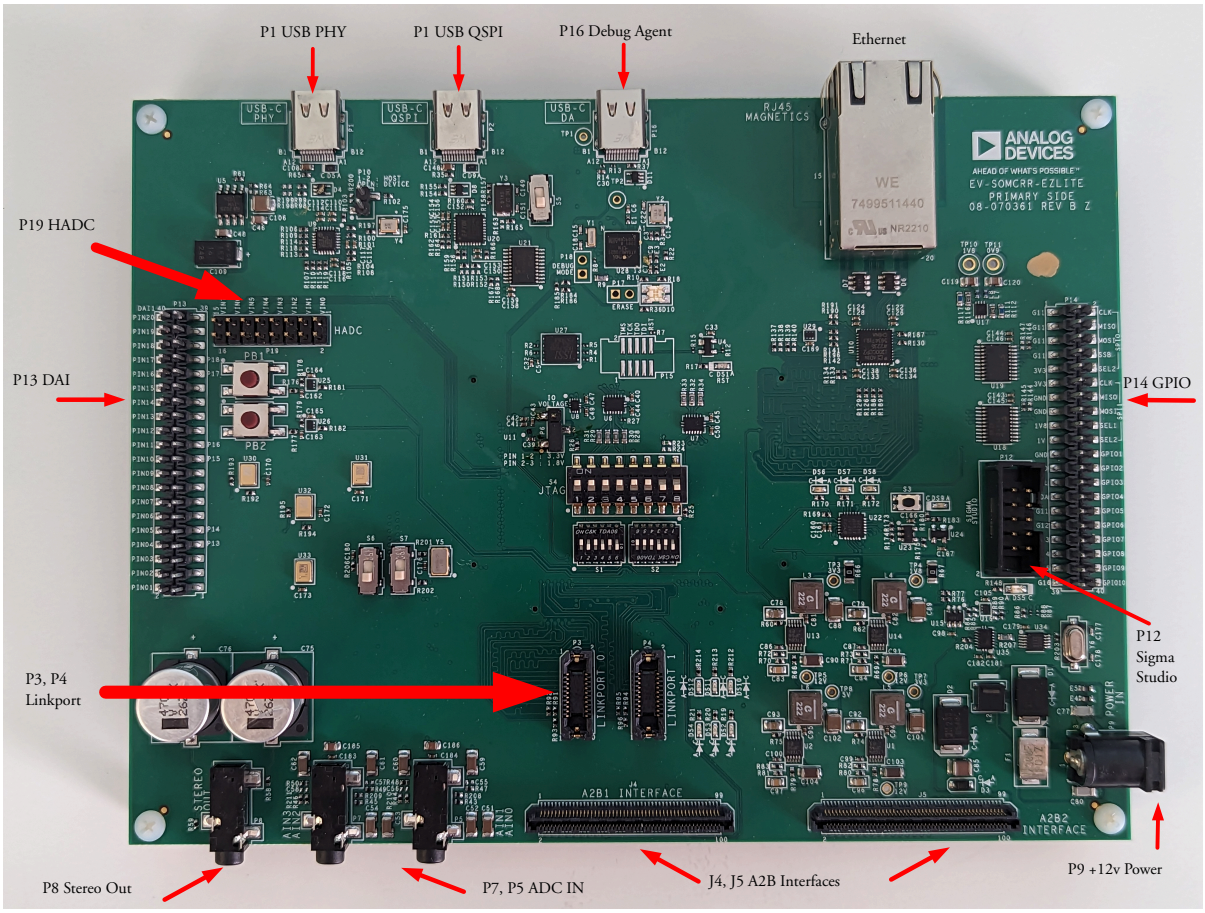

Figure 3-8: Connector Top

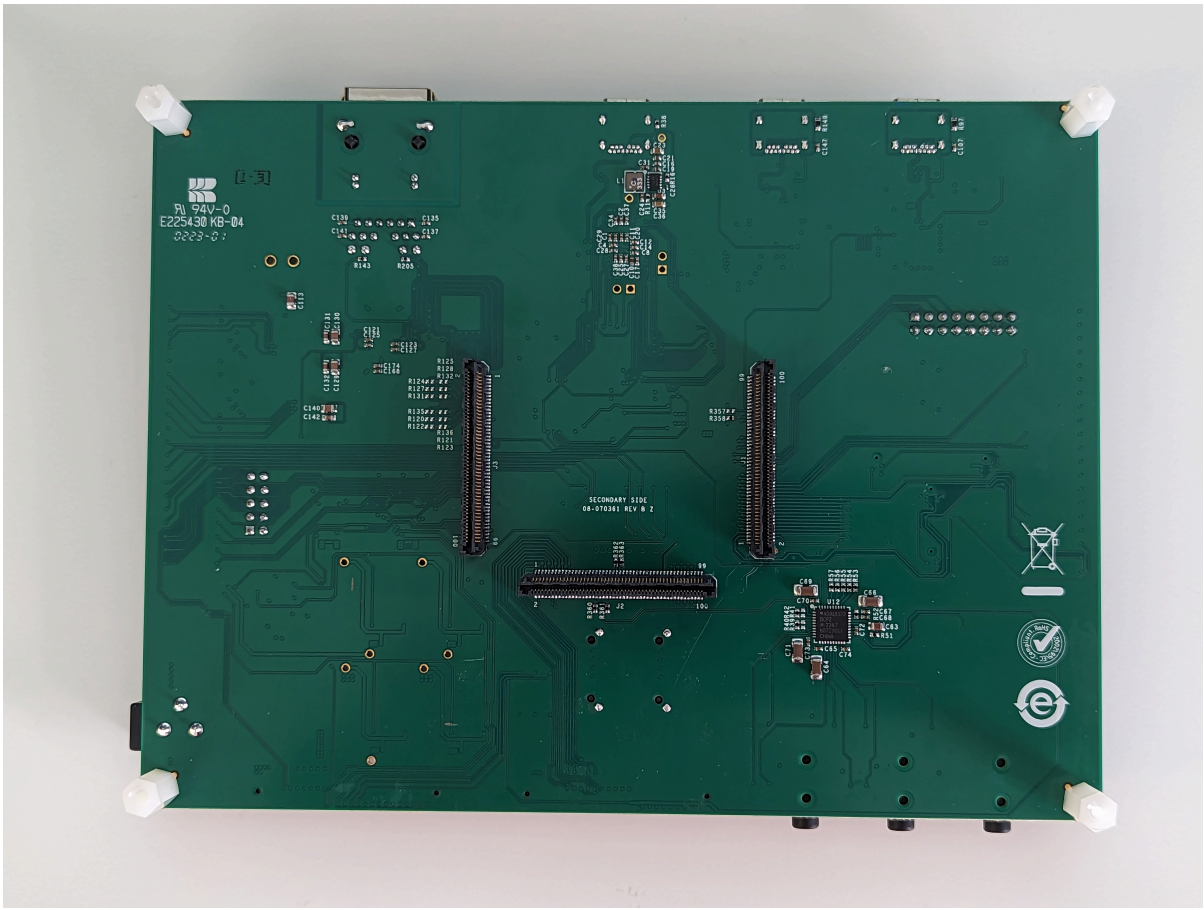

Figure 3-9: Connector Bottom

Audio Input/Output (P5 and P7)

Part Description	*Manufacturer*	*Part Number*
3.5mm Stereo female	CUI	SJ-3523-SMT
Mating Cable		
Standard 3.5mm stereo cable		

Audio Output (P8)

Part Description	*Manufacturer*	*Part Number*
3.5mm Stereo female	CUI	SJ-3523-SMT
Mating Cable		
Standard 3.5mm stereo cable		

Audio and GPIO Connectors (P13 P14)

The EV-SOMCRR-EZLITE contains two 40 pins headers that breakout the unused DAI and GPIO signals from a connector SOM module. The following tables show the pin out of the connectors. Refer to the schematics for the EV-SOMCRR-EZLITE and the SOM module for full signal naming.

Table 3-7: DAI Connector (`P13`)

Pin	Signal	Pin	Signal
1	GND	21	DAI0_PIN16
2	DAI1_PIN01	22	DAI1_PIN11
3	GND	23	GND
4	DAI1_PIN02	24	DAI1_PIN12
5	GND	25	GND
6	DAI1_PIN03	26	DAI1_PIN13
7	DAI0_PIN13	27	GND
8	DAI1_PIN04	28	DAI0_PIN14
9	DAI0_PIN14	29	GND
10	DAI1_PIN05	30	DAI1_PIN15
11	GND	31	DAI0_PIN17
12	DAI1_PIN06	32	DAI1_PIN16
13	GND	33	DAI0_PIN18
14	DAI1_PIN07	34	DAI1_PIN17
15	GND	35	GND
16	DAI1_PIN08	36	DAI1_PIN18
17	GND	37	GND
18	DAI1_PIN09	38	DAI1_PIN19
19	DAI0_PIN15	39	GND
20	DAI1_PIN10	40	DAI1_PIN20

Table 3-8: GPIO Connector (`P14`)

Pin	Signal	Pin	Signal
1	VDDIO	21	GND
2	SPI0_CLK	22	GPIO_01
3	VDDIO	23	GND
4	SPI0_MISO	24	GPIO_02
5	GND	25	TWI2_SCL
6	SPI0_MOSI	26	GPIO_03

Table 3-8: GPIO Connector (P14) (Continued)

Pin	Signal	Pin	Signal
7	GND	27	TWI2_SDA
8	SPI0_SSB	28	GPIO_04
9	3V3	29	GPIO_11
10	SPI0_SEL2*	30	GPIO_05
11	3V3	31	GPIO_12
12	SPI1_CLK	32	GPIO_06
13	GND	33	GPIO_13
14	SPI1_MISO	34	GPIO_07
15	GND	35	GPIO_14
16	SPI1_MOSI	36	GPIO_08
17	GND	37	GPIO_15
18	SPI1_SEL1*	38	GPIO_09
19	VDD1V8	39	GPIO_16
20	SPI1_SEL2*	40	GPIO_10

Table 3-9: Connector

Part Description	*Manufacturer*	*Part Number*
40-pin, 2.54 mm	SAMTEC	TSM-120-01-T-DV

Sigma Studio (P12)

This connector interfaces with SigmaStudio® through the EVAL-ADUSB2EBZ board. The connector is a 0.1" header. The pinout can be found in the schematic.

A2B (J4 and J5)

Part Description	*Manufacturer*	*Part Number*
100-pin, 0.64mm	SAMTEC	LSS-150-01-L-DV-A-K
Mating Connector		
100-pin, 0.64mm	SAMTEC	LSS-150-01-L-DV-A-K

Link Port/JTAG (P3, P4)

Part Description	*Manufacturer*	*Part Number*
ERF8 10X2, female	Samtec	ERF8-010-05.0-D-DV-L
Mating Cable		
6" coax cable assembly	Samtec	ERCD-010-06.00-TED-TEU-1-D

Ethernet 1000 (RJ45)

Part Description	*Manufacturer*	*Part Number*
RJ45	Assmann	A-2004-2-4-LPS-N-R
Mating Cable		
Standard CAT5e Ethernet cable		

Power Plug (P9)

Part Description	*Manufacturer*	*Part Number*
2.1 mm power jack	CUI	PJ-102AH
Mating Cable		
12.0VDC@1.5A power supply	CUI	EMSA120150-P5RP-SZ

SoM Interface Connection (J1, J2, J3)

The SoM Interface consists of three SAMTEC high speed connectors that provide the DSP peripheral signals for use with a plug in SoM module. These signals are based upon the peripheral signal needs, which allows multiple processors to be used with this connection. These connectors are self-mating, and the pinout here reflects the connectors of the associated SoM board.

The *SoM Interface A Connector (J5)*, *SoM Interface B Connector (J3)*, and *SoM Interface C Connector (J6)* tables show the signal associated with each pin on the connectors.

Table 3-10: SoM Interface A Connector (J5)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND1	21	DAI0_PIN10	41	DAI0_PIN20	61	USB0_ID	81	GPIO3
2	GND2	22	DAI1_PIN10	42	DAI1_PIN20	62	USB_D2	82	$\overline{\text{USB\_RESET}}$
3	DAI0_PIN01	23	DAI0_PIN11	43	GND3	63	USB0_VBUS	83	GPIO4
4	DAI1_PIN01	24	DAI1_PIN11	44	GND4	64	USB_D3	84	GPIO6
5	DAI0_PIN02	25	DAI0_PIN12	45	GND5	65	USB0_VBC	85	GPIO5
6	DAI1_PIN02	26	DAI1_PIN12	46	GND6	66	USB_D4	86	GPIO7

Table 3-10: SoM Interface A Connector (J5) (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
7	DAI0_PIN03	27	DAI0_PIN13	47	HADC_VIN0	67	USB1_DP	87	GND9
8	DAI1_PIN03	28	DAI0_PIN13	48	HADC_VIN4	68	USB_D5	88	GPIO8
9	DAI0_PIN04	29	DAI0_PIN14	49	HADC_VIN1	69	USB1_DM	89	MLB_CLKP
10	DAI1_PIN04	30	DAI1_PIN14	50	HADC_VIN5	70	USB_D6	90	GPIO9
11	DAI0_PIN05	31	DAI0_PIN15	51	HADC_VIN2	71	USB1_ID	91	MLB_CLKN
12	DAI1_PIN05	32	DAI1_PIN15	52	HADC_VIN6	72	USB_D7	92	GPIO10
13	DAI0_PIN06	33	DAI0_PIN16	53	HADC_VIN3	73	USB1_VBUS	93	MLB_SIGP
14	DAI1_PIN06	34	DAI1_PIN16	54	HADC_VIN7	74	USB_NXT	94	GND10
15	DAI0_PIN07	35	DAI0_PIN17	55	GND7	75	USB1_VBC	95	MLB_SIGN
16	DAI1_PIN07	36	DAI1_PIN17	56	GND8	76	USB_STP	96	MLB_CLK
17	DAI0_PIN08	37	DAI0_PIN18	57	USB0_DP	77	GPIO1	97	MLB_DATP
18	DAI1_PIN08	38	DAI1_PIN18	58	USB_D0	78	USB_DIR	98	MLB_SIG
19	DAI0_PIN09	39	DAI0_PIN19	59	USB0_DM	79	GPIO2	99	MLB_DATN
20	DAI1_PIN09	40	DAI1_PIN19	60	USB_D1	80	USB_CLK	100	MLB_DAT

Table 3-11: SoM Interface B Connector (J3)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND1	21	OSPI_D7	41	TWI2_SDA	61	MSI_D3	81	LINKPORT0_D7
2	GND2	22	SPI1_SEL2b	42	UART2_RXb	62	GND8	82	LINKPORT1_D7
3	SP2_OSPI_MISO	23	SPI2_SEL2b	43	UART0_TXb	63	MSI_D4	83	LINKPORT0_D6
4	SPI0_CLK	24	GND3	44	UART2_RTSb	64	CAN0_TX	84	LINKPORT1_D6
5	SP2_OSPI_MOSI	25	GND4	45	UART0_RXb	65	MSI_D5	85	LINKPORT0_D5
6	SPI0_MISO	26	NU	46	UART2_CTSb	66	CAN0_RX	86	LINKPORT1_D5
7	SPI2_OSPI_D2	27	NU	47	UART0_RTSb	67	MSI_D6	87	LINKPORT0_D4
8	SPI0_MOSI	28	NU	48	GND6	68	GND	88	LINKPORT1_D4
9	SP2_OSPI_D3	29	NU	49	UART0_CTSb	69	MSI_D7	89	LINKPORT0_D3
10	SPI0_SSb	30	NU	50	GPIO1	70	CAN1_TX	90	LINKPORT1_D3
11	SP2_OSPI_CLK	31	TWI0_SCL	51	GND5	71	GND7	91	LINKPORT0_D2
12	SPI0_SEL2b	32	UART1_TXb	52	GPIO2	72	CAN1_RX	92	LINKPORT1_D2
13	SP2_OSPI_SSb	33	TWI0_SDA	53	NU	73	NU	93	LINKPORT0_D1
14	SPI1_CLK	34	UART1_RXb	54	NU	74	NU	94	LINKPORT1_D1
15	OSPI_D4	35	TWI1_SCL	55	MSI_D0	75	NU	95	LINKPORT0_D0

Table 3-11: SoM Interface B Connector (J3) (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
16	SPI1_MISO	36	UART1_RTSb	56	MSI_CLK	76	NU	96	LINKPORT1_D0
17	OSPI_D5	37	TWI1_SDA	57	MSI_D1	77	NU	97	LINKPORT0_ACK
18	SPI1_MOSI	38	UART1_CTSb	58	MSI_CMD	78	NU	98	LINKPORT1_ACK
19	OSPI_D6	39	TWI2_SCL	59	MSI_D2	79	GND9	99	LINKPORT0_CLK
20	SPI1_SSb	40	UART2_TXb	60	MSI_CDb	80	GND10	100	LINKPORT1_CLK

Table 3-12: SoM Interface C Connector (J6)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND1	21	ETH0_ RXCLK_REFCLK	41	GND7	61	PPI_D05	81	PPI_D15
2	GND2	22	GND4	42	CLK1	62	PPI_D17	82	GPIO3
3	ETH0_MDIO	23	ETH0_RXCTL_CRS	43	PPI_CLK	63	PPI_D06	83	PPI_D16
4	ETH1_MDIO	24	ETH0_PTPCLKIN0	44	CLK2	64	PPI_D18	84	GPIO4
5	ETH0_MDC	25	GND3	45	PPI_FS1	65	PPI_D07	85	GND11
6	ETH1_MDC	26	ETH0_PTPAUX-IN0	46	GND8	66	PPI_D19	86	GPIO5
7	ETH0_MD_INT	27	ETH0_TXD3	47	PPI_FS2	67	PPI_D08	87	VDD_EXT
8	ETH0_RXD1	28	ETH0_PTPPPS0	48	JTG0_TMS/ SWDIO	68	PPI_D20	88	GPIO6
9	ETH0_GPIO_1	29	ETH0_TXD2	49	PPI_FS3	69	PPI_D09	89	VDD_VREF
10	ETH0_RXD0	30	ETH0_PTPPPS1	50	JTG0_TCK/ SWCLK	70	PPI_D21	90	GND12
11	ETH0_GPIO_2	31	ETH0_TXD1	51	PPI_D00	71	PPI_D10	91	VDD_A
12	ETH0_TXEN	32	ETH0_PTPPPS2	52	JTG0_TDO/SW0	72	PPI_D22	92	VDD_DMC
13	ETH0_RXD3	33	ETH0_TXD0	53	PPI_D01	73	PPI_D11	93	VDD_INT
14	ETH0_TXD0	34	ETH0_PTPPPS3	54	JTG0_TDI	74	PPI_D23	94	$\overline{\text{SYS\_HWRST}}$
15	ETH0_RXD2	35	ETH0_TCLK	55	PPI_D02	75	PPI_D12	95	PWR_SEQ_GOOD
16	ETH0_TXD1	36	GND5	56	$\overline{\text{JTG0\_TRST}}$	76	GND10	96	$\overline{\text{SoM\_Reset}}$
17	ETH0_RXD1	37	ETH0_TXEN	57	PPI_D03	77	PPI_D13	97	VDD1
18	ETH1_CRS	38	SYS_CLKOUT	58	$\overline{\text{TARGET\_RESET}}$	78	GPIO1	98	VSS1
19	ETH0_RXD0	39	GND6	59	PPI_D04	79	PPI_D14	99	VDD2

Table 3-12: SoM Interface C Connector (J6) (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
20	ETH1_INTb	40	AUDIO_CLK	60	GND9	80	GPIO2	100	VSS2

Table 3-13: Mating Connector

Part Description	*Manufacturer*	*Part Number*
100-pin, 0.64 mm	SAMTEC	LSS-150-02-L-DV-A-K
Mating Connector		
100-pin, 0.64 mm	SAMTEC	LSS-150-01-L-DV-A-K