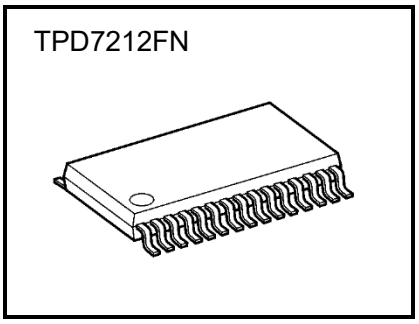
Toshiba Intelligent Power Device Silicon Monolithic Power MOS Integrated Circuit

TPD7212FN

Power MOSFET Gate Driver for 3-Phase brushless DC Motor

1. Description

The TPD7212F is a power MOSFET gate driver for 3-phase full-bridge circuits by the BiCD process. The inclusion of a charge pump circuit for drivers inside the IC makes it easy to configure a 3-phase full-bridge circuit.



SSOP30-P-300-0.65

2. Applications

- 3-Phase brushless DC motor for Automotive
- Electric power steering
- Power sliding door
- Transmission
- Automotive pumps
- Automotive fans
- HVAC

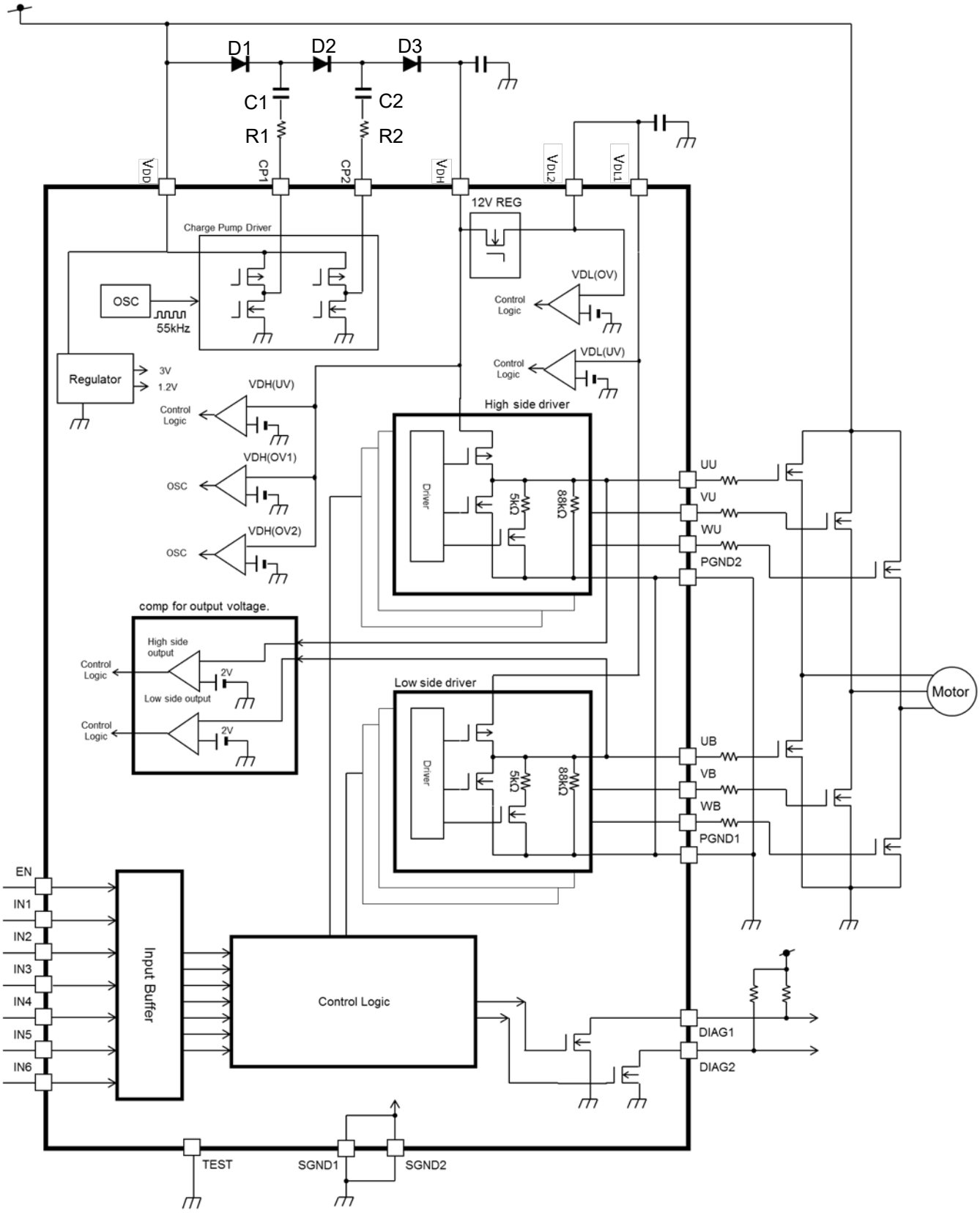
3. Features

- Built-in diagnostic functions for driver power supply and output voltage.
- Built-in charge pump circuit.
- SSOP30 package for surface mounting.
- AEC-Q100 qualified.

Note: This product has a MOS structure and is sensitive to electrostatic discharge.

Start of commercial production
2020-08

4. Block Diagram



Note: Some of the functional blocks, circuits, constants, etc. in the block diagram are omitted or simplified.

Figure 4.1 Block Diagram

5. Pin Assignments

(TOP VIEW)

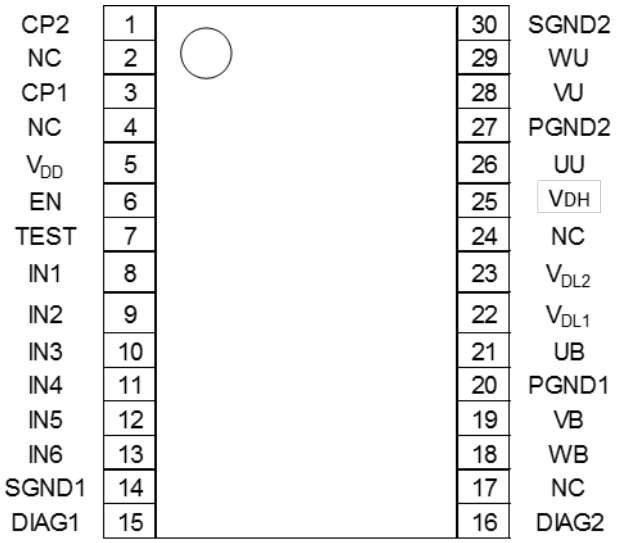


Figure 5.1 Pin Assignments

6. Pin Description

Table 6.1 Pin Description

Pin No.	Symbol	I/O	Pin Description
1	CP2	OUT	Capacitor pin for charge pump
2	NC	-	No-Connect pin.
3	CP1	OUT	Capacitor pin for charge pump
4	NC	-	No-Connect pin.
5	V_{DD}	-	Power supply pin
6	EN	IN	Inhibit pin (high active). Built in pull down resistor (400kΩtyp.).
7	TEST	IN	For internal test. Please connect to GND during normal operation.
8	IN1	IN	Input pin: It controls for UU. Built in pull down resistor (100kΩ typ.).
9	IN2	IN	Input pin: It controls for VU. Built in pull down resistor (100kΩ typ.).
10	IN3	IN	Input pin: It controls for WU. Built in pull down resistor (100kΩ typ.).
11	IN4	IN	Input pin: It controls for UB. Built in pull down resistor (100kΩ typ.).
12	IN5	IN	Input pin: It controls for VB. Built in pull down resistor (100kΩ typ.).
13	IN6	IN	Input pin: It controls for WB. Built in pull down resistor (100kΩ typ.).
14	SGND1	-	Signal block GND pin: shared internally with SGND2.
15	DIAG1	OUT	Diagnosis detection pin. Nch open drain.
16	DIAG2	OUT	Diagnosis detection pin. Nch open drain.
17	NC	-	No-Connect pin.
18	WB	OUT	Drives the power MOSFET connected to the low side of the W phase.
19	VB	OUT	Drives the power MOSFET connected to the low side of the V phase.
20	PGND1	-	Power block GND pin: shared internally with PGND2.
21	UB	OUT	Drives the power MOSFET connected to the low side of the U phase.
22	V_{DL1}	-	Power supply pin for low side drive. Connect to V_{DL2} pin outside.
23	V_{DL2}	-	Power supply pin for low side drive. Connect to V_{DL1} pin outside.
24	NC	-	No-Connect pin.
25	V_{DH}	-	Output pin for charge pump.
26	UU	OUT	Drives the power MOSFET connected to the high side of the U phase.
27	PGND2	-	Power block GND pin: shared internally with PGND1.
28	VU	OUT	Drives the power MOSFET connected to the high side of the V phase.
29	WU	OUT	Drives the power MOSFET connected to the high side of the W phase.
30	SGND2	-	Signal block GND pin: shared internally with SGND1.

7. Operational Description

7.1. Driver power supply voltage characteristic (Charge pump voltage characteristic)

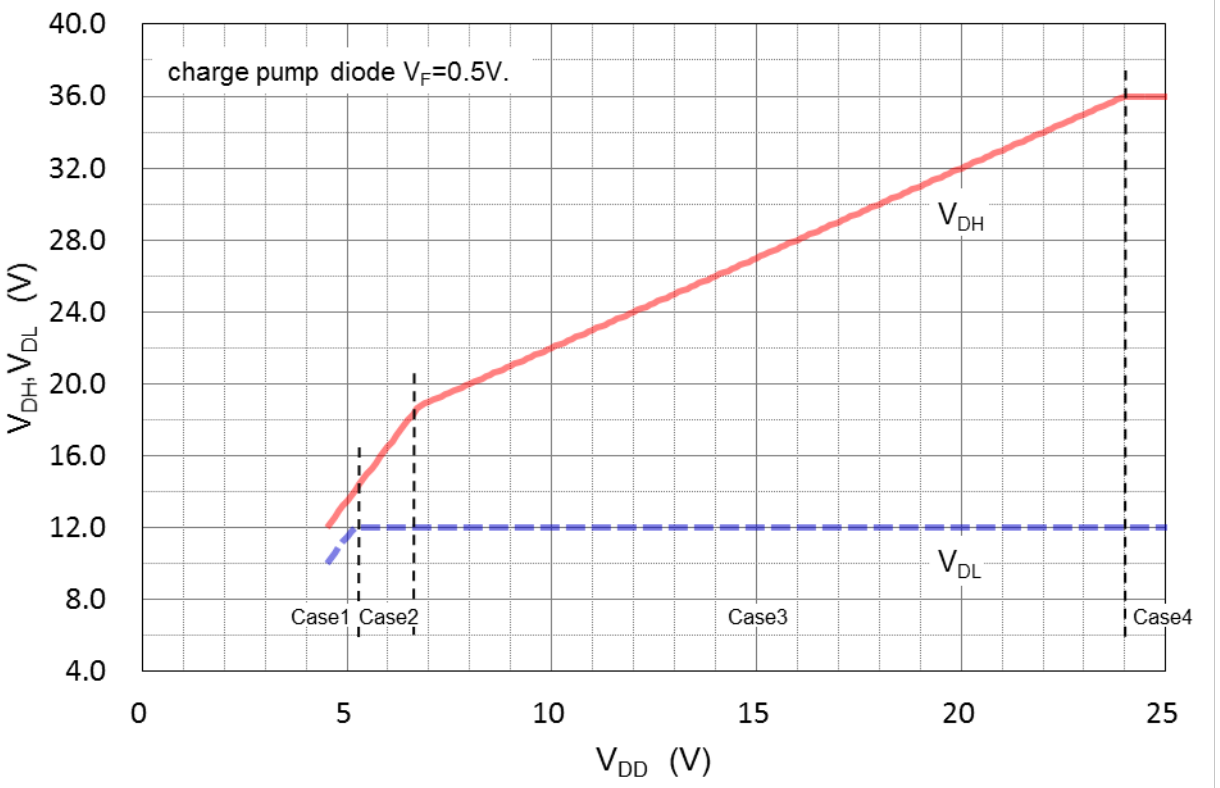


Figure 7.1 Charge pump voltage characteristic

In the graph above, V_{DH} is the charge pump output voltage and the power supply voltage for the high side driver. V_{DL} is the power supply voltage for the low side driver. This IC generates the V_{DL} voltage from the V_{DH} voltage by the regulator to keep the V_{DL} voltage constant even when the V_{DD} voltage is low. V_{DH} and V_{DL} have the following characteristics.

- Case1) $V_{DH} = 3\times(V_{DD}-V_F)$
  $V_{DL} = V_{DH}-2V$
- Case2) $V_{DH} = 3\times(V_{DD}-V_F)$
  $V_{DL} = 12V$
- Case3) $V_{DH} = V_{DD}+12V$
  $V_{DL} = 12V$
- Case4) $V_{DH} = 36V$
  $V_{DL} = 12V$

7.2. Diagnosis of the driver power supply voltage

If at least one of V_{DH} and V_{DL} is abnormal, DIAG2 becomes H. Under some conditions, the low-side output (UB, VB, WB) goes L.
All of these recover by themselves when the voltage returns to normal.

7.2.1. V_{DH} under voltage detection

If $V_{DH} \leq V_{DD}+4.5V$ (Typ.), it is judged as abnormal and DIAG2 becomes H.

7.2.2. V_{DL} under voltage detection

If $V_{DH} \leq 4.5V$ (typ.), It is judged as abnormal and DIAG2 becomes H.

7.2.3. V_{DL} over voltage detection

If $V_{DL} \geq 18V$ (Typ.), it is judged as abnormal, and low side output (UB, VB, WB) becomes L and DIAG2 becomes H.

Note1: Driver power supply (V_{DH} and V_{DL}) is boosted by the charge pump. Boost operation will start with V_{DD}> 4.5V.

Note2: In order to prevent a malfunction, please enter the signal to IN1 to 6 after checking the DIAG2 = "L".

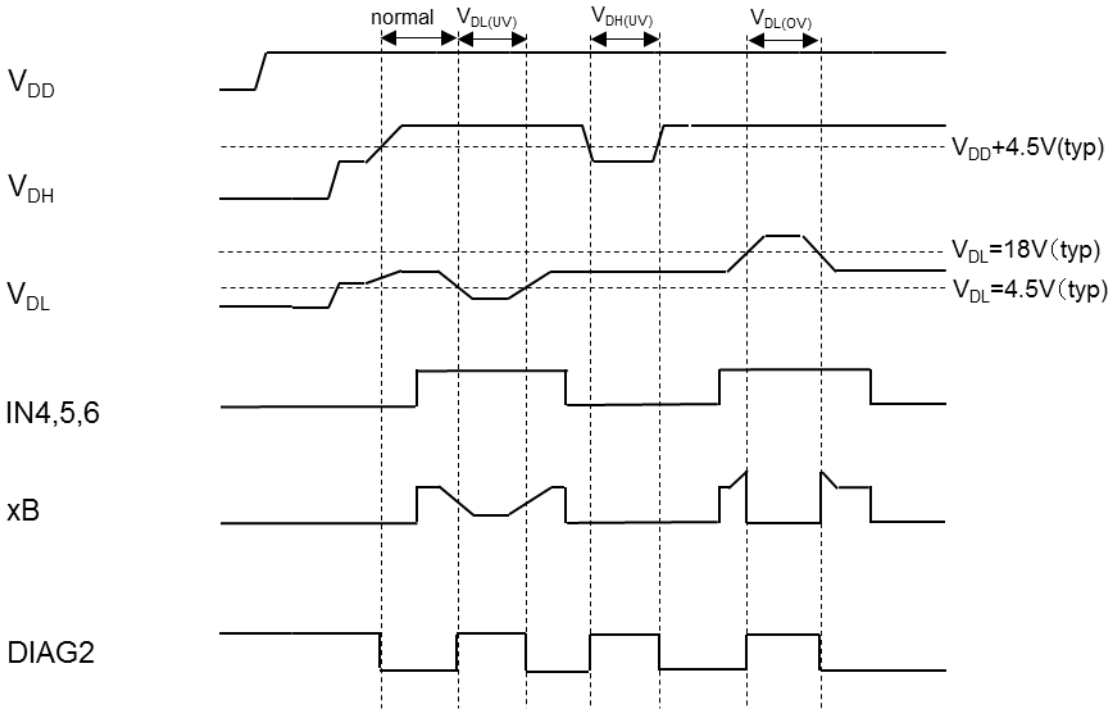


Figure 7.2 Diagnosis of power supply for driver

7.3. Normal operation, Top and bottom short circuit input mode

Table 7.1 Truth table

EN	IN1 (IN2,3)	IN4 (IN5,6)	Charge pump circuit	Output voltage		DIAG1 output	DIAG2 output	Remarks
				UU output (VU,WU)	UB output (VB,WB)			
L	*	*	Operate	L	L	H	L	–
H	L	L	Operate	L	L	H	L	–
H	H	L	Operate	H	L	H	L	–
H	L	H	Operate	L	H	H	L	–
H	H	H	Operate	L(self-return)	L(self-return)	L(self-return)	L	Top and bottom short circuit input mode

* : Don't care

When at least one of the paired high-side output control input and low-side output control input (IN1 and IN4, IN2 and IN5, IN3 and IN6) is H, the top and bottom short circuit input mode is selected, and all outputs are L DIAG1 is also L.
These self-return will be carried out if the corresponding input is out of the Top and bottom short circuit input mode.

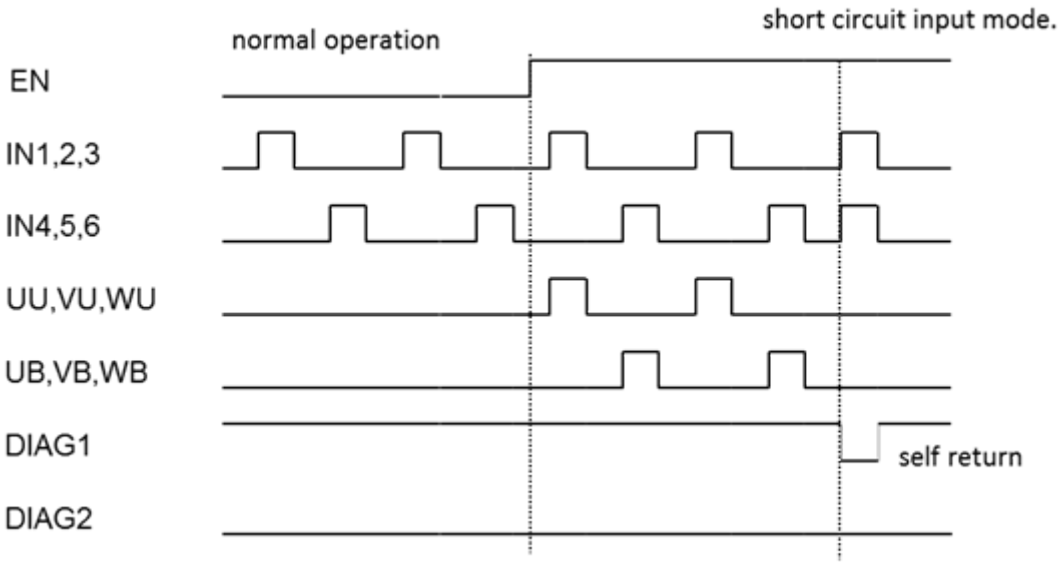


Figure 7.3 Normal operation, Top and bottom short circuit input mode

7.4. Abnormal diagnosis of output voltage (VDD short, GND short)

Output voltage diagnosis operates for abnormal output voltage when the input signal changes, and for abnormal output voltage when the input is stable. The criterion for diagnosing an error is the output judgment voltage (V_{OM}). When the input signal is H, it is output voltage <V_{OM}, and when the input signal is L, the output voltage ≧V_{OM}. If it is diagnosed as abnormal, turn off all outputs and pull down to GND with an internal resistance (5 kΩ). Also latch DIAG1 at L. These are canceled at the rising edge of EN signal (L to H).

7.4.1. Abnormal diagnosis of output voltage when input signal changes

For output abnormality when the input signal changes, after a certain mask time (t_{mask}), turn off all outputs and pull down to GND with an internal resistance (5 kΩ). Also latch DIAG1 at L. These are canceled at the rising edge of EN signal (L to H).

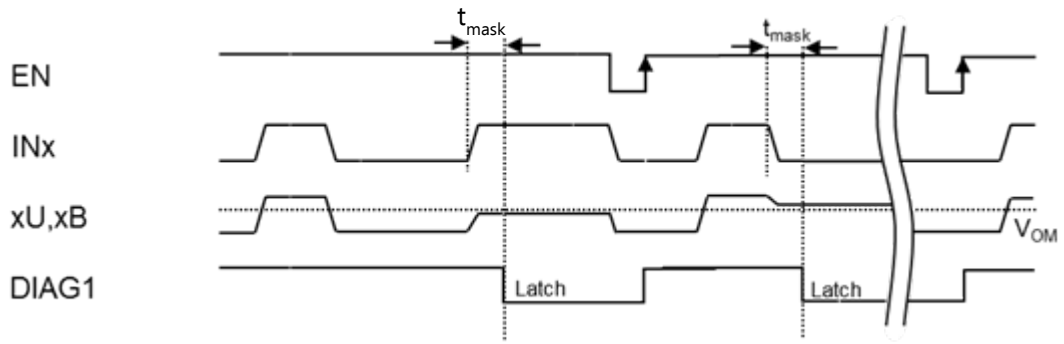


Figure 7.4 Abnormal diagnosis of output voltage when input signal changes

7.4.2. Abnormal diagnosis of output voltage when input signal is stable

For output abnormalities when the input signal is stable, without mask time (t_{mask}), immediately turn off all outputs and pull down to GND with internal resistance (5kΩ). Also latch DIAG1 at L. These are canceled at the rising edge of EN signal (L to H).

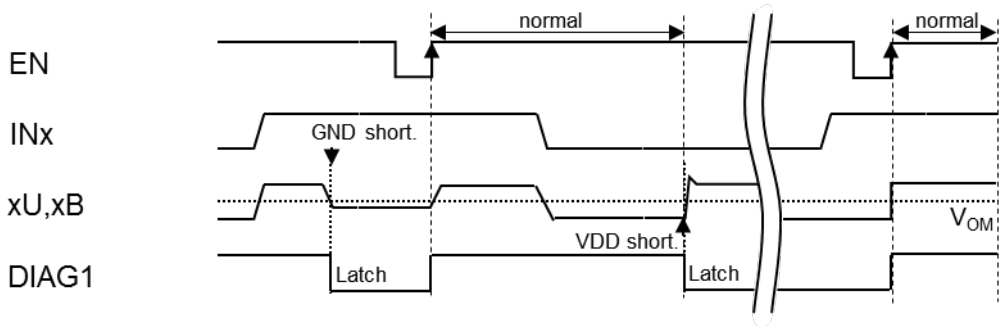


Figure 7.5 Abnormal diagnosis of output voltage when input signal is stable

Note: INx: IN1,IN2,IN3,IN4,IN5,IN6 xU: UU,VU,WU xB: UB,VB,WB

8. Absolute Maximum Ratings

Table 8.1 Absolute Maximum Ratings

(T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Rating	Unit	Note
Supply voltage	**DC**	$V_{DD(DC)}$	-0.3 to 25.0	V	-
	pulse	$V_{DD(Pulse)}$	-0.3 to 40.0	V	t≦300ms
PGND voltage		V_{PGND}	-0.3 to 0.3	V	Standard in SGND
Output voltage	**High side**	V_{xU}	-0.3 to V_{DH}+0.3	V	UU,VU,WU pin
	Low side	V_{xB}	-0.3 to V_{DL}+0.3	V	UB,VB,WB pin
Output current	**Source current**	I_{xU}	-1.0	A	-
	Sink current	I_{xB}	+1.5	A	-
Input voltage	**IN1 to IN6**	V_{IN}	-0.3 to 6.0	V	-
	EN	V_{EN}	-0.3 to 25.0	V	-
Diagnosis output voltage		V_{DIAG}	-0.3 to 6.0	V	-
Diagnosis output current		I_{DIAG}	5	mA	-
Power dissipation		P_D	2.6	W	-
Operating temperature		T_{opr}	-40 to 150	°C	-
Junction temperature		T_j	175	°C	-
Storage temperature		T_{stg}	-55 to 175	°C	-

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

8.1. Thermal Resistance

Table 8.2 Thermal resistance

Charateristics	Symbol	Rating	unit
Thermal resistance (junction-to-ambient)	$R_{th\ (j-a)}$	56	°C / W

Note: Glass epoxy board
Material: FR-4(4 layer)
Board size: 76.2mmx114.3mmx1.6mm

9. Operating Ranges

Table 9.1 Operating supply voltage

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Operating supply voltage	$V_{DD(opr)}$	T_j = -40 to 150°C	4.5	12.0	18.0	V

10. Electrical Characteristics

Table 10.1 Electrical Characteristics

(T_j = −40 to 150°C, V_{DD} = 5 to 18V unless otherwise specified)

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Supply current		I_{DD}	V_{EN}=H,V_{INx}=L, V_{DD}=4.5 to 18.0V Note2	-	3.9	8.0	mA
Input threshold voltage(IN)	High level	V_{INxH}	-	2.0	-	-	V
	Low level	V_{INxL}	-	-	-	1.0	V
Input threshold voltage(EN)	High level	V_{ENH}	-	2.0	-	-	V
	Low level	V_{ENL}	-	-	-	1.0	V
Input current(IN)	High level	I_{INxH}	V_{INx}=5V	-	50	100	V
	Low level	I_{INxL}	V_{INx}=0V	-1	0	1	μA
Input current(EN)	High level	I_{ENH}	V_{EN}=5V	-	12	30	μA
	Low level	I_{ENL}	V_{EN}=0V	-1	0	1	μA
Output voltage	High level	V_{OHxU1}	V_{DD}=4.5V,I_o=-1mA, Note2	V_{DD}+6	V_{DD}+7	-	μA
		V_{OHxU2}	V_{DD}=7 to 18V,Io=-1mA, Note2	V_{DD}+10	V_{DD}+12	V_{DD}+16	V
		V_{OHxB1}	V_{DD}=4.5V,I_O=-1mA, Note2	7	10	-	V
		V_{OHxB2}	V_{DD}=7 to 18V,I_O=-1mA, Note2	10	13	16	V
	Low level	V_{OLxU1}	V_{DD}=4.5V,I_O=1mA	-	-	0.5	V
		V_{OLxU2}	V_{DD}=5 to 18V,I_O=1mA	-	-	0.5	V
		V_{OLxB1}	V_{DD}=4.5V,I_O=1mA	-	-	0.5	V
		V_{OLxB2}	V_{DD}=5 to 18V,I_O=1mA	-	-	0.5	V
Output detection voltage		V_{OM}	V_{DD}=5 to 18V, V_{PGND}=V_{SGND}=0V	2.0	2.5	3.5	V
Mask time for monitoring output detection voltage.		t_{mask}	V_{DD}=5 to 18V	1.0	3.0	5.0	μs
Output pull down resistance	Normal mode	R_{pd1}	-	45	88	135	kΩ
	Hiz mode	R_{pd2}	I_O=+0.5mA,V_{DD}=5 to 18V	3.5	5.0	6.5	kΩ
Driver on resistance	Source side DMOS	$R_{DS(ON)HS}$	I_O=-0.1A,V_{DD}=5 to 18V	-	1.3	3.0	Ω
	Sink side DMOS	$R_{DS(ON)LS}$	I_O=+0.1A,V_{DD}=5 to 18V	-	0.7	2.0	Ω

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Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Diagnosis output voltage	Low level	V_{DIAG}	I_{DIAG}=0.5mA,V_{DD}=5 to 18V	-	-	0.5	V
Diagnosis output leakage current.	High level	I_{DIAG}	V_{DIAG}=6V,V_{DD}=5 to 18V	-	-	10	μA
V_{DH} drop detection		$V_{DH(UV)}$	V_{DD}=5 to 18V	V_{DD}+4	V_{DD}+4.5	V_{DD}+6	V
V_{DL} drop detection		$V_{DL(UV)}$	-	4.0	4.5	6.0	V
V_{DL} over voltage detection		$V_{DL(OV)}$	-	-	18	-	V
Delay time	V_{OUT}=L to H	$t_{d(ON)}$	V_{DD}=V_{DH}=V_{DL}=12V	-	0.21	0.40	μs
	V_{OUT}=H to L	$t_{d(OFF)}$	R_L=25Ω,C_L=20000pF	-	0.21	0.40	μs
Slew Rate (rise)		$dv/dt_{(ON)}$	-	-	75	-	V/μs
Slew Rate (fall)		$dv/dt_{(OFF)}$	-	-	75	-	V/μs
Propagation delay time	Same output	$\Delta t_{d(OFF-ON)1}$	-	-0.2	-	0.2	μs
	Top and bottom output	$\Delta t_{d(OFF-ON)2}$	-	-0.2	-	0.2	μs
Dead time		t_{dead}	V_{DD}=12V, V_{th}=2.0V	-	0.64	1.00	μs
Charge pump frequency		f_{osc}	V_{DD}=5 to 18V	30	55	80	kHz

Note 1: Typical value if not specified is the 12V condition.
Note 2: In Figure 4.1, D1,D2,D3 = CRH01, R1,R2 = 10Ω, C1,C2 = 2.2μF

11. Test Circuit

11.1. Slew Rate

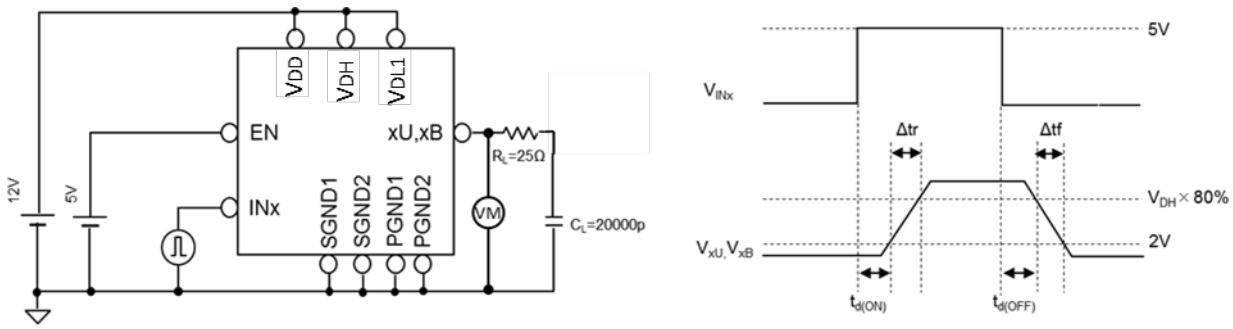


Figure 11.1 Slew Rate

11.2. Dead time

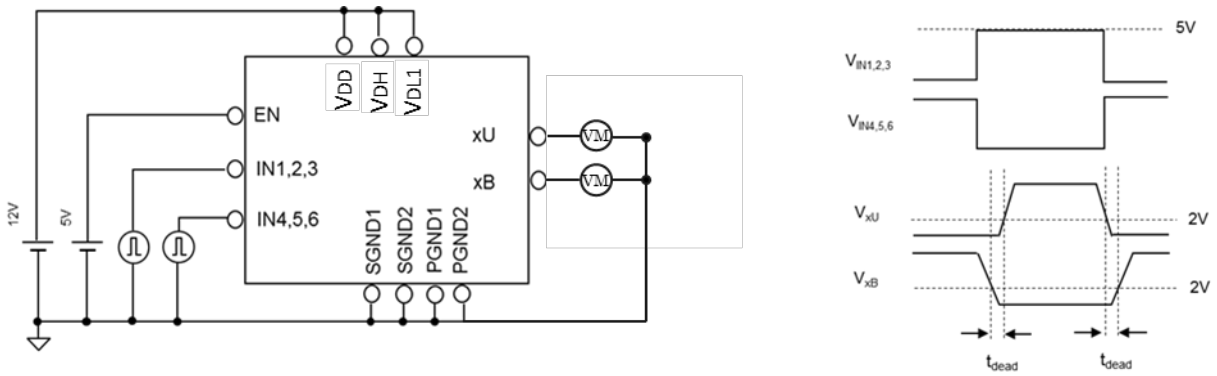


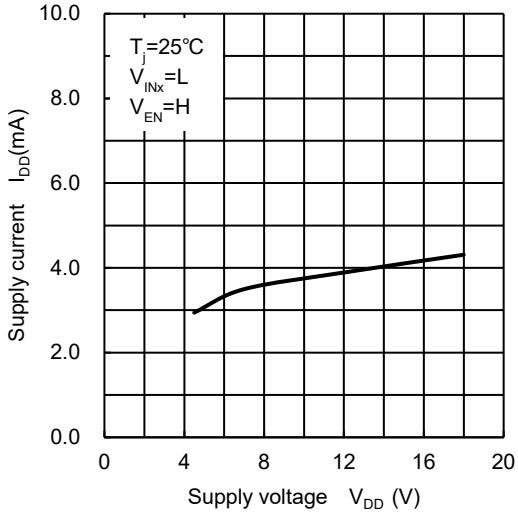
Figure 11.2 Dead time

Note: INx: IN1,IN2,IN3,IN4,IN5,IN6 xU: UU,VU,WU xB: UB,VB,WB

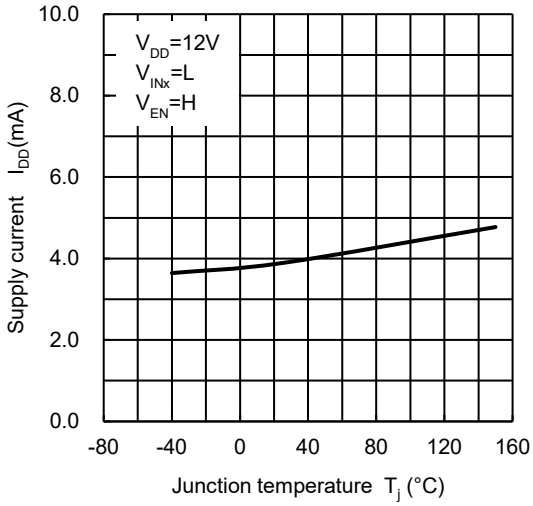
12. Characteristic curves

The below characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

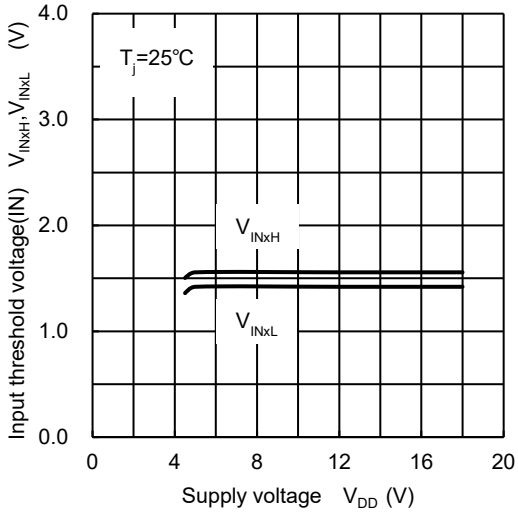
I_{DD} - V_{DD}



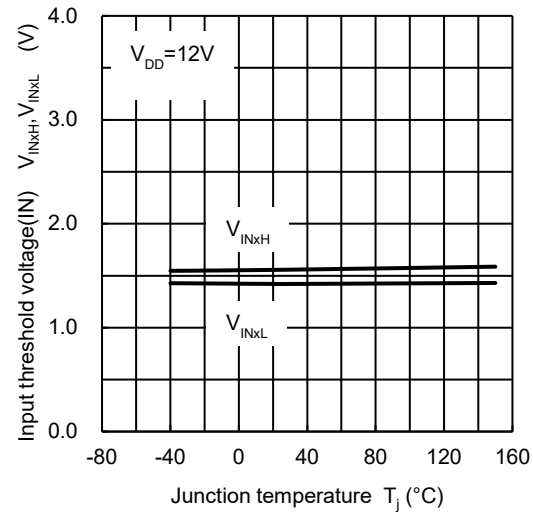
I_{DD} - T_j



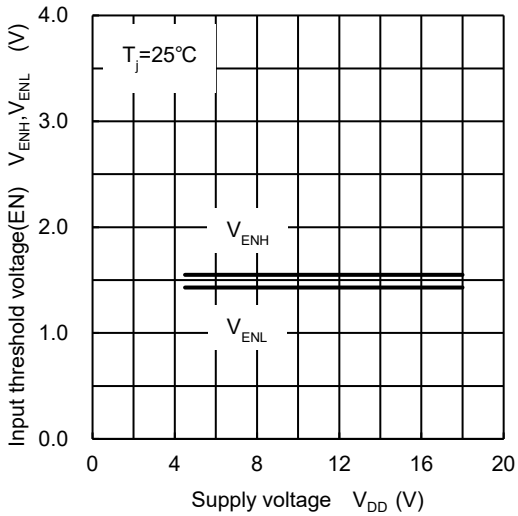
V_{INxH},V_{INxL} - V_{DD}



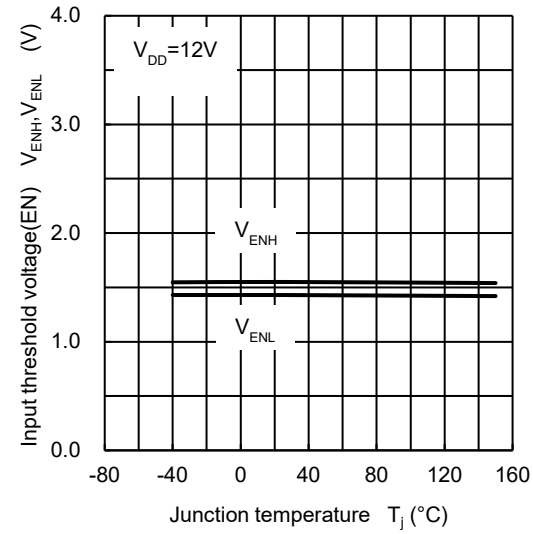
V_{INxH},V_{INxL} - T_j



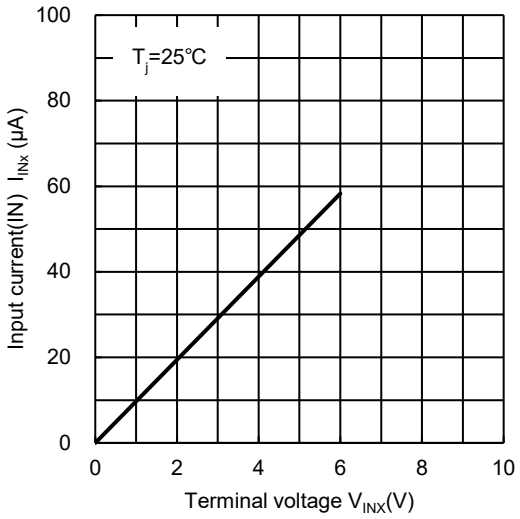
V_{ENH},V_{ENL} - V_{DD}



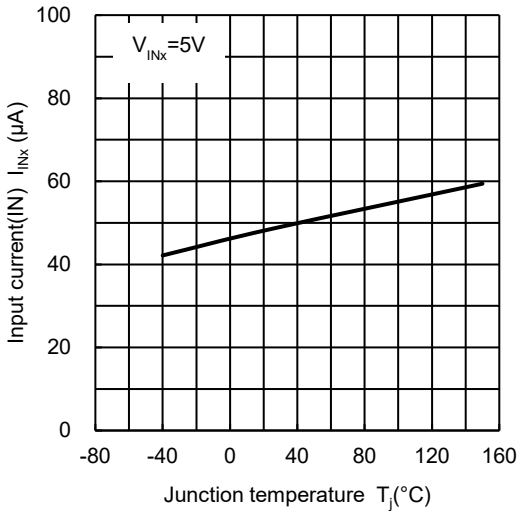
V_{ENH},V_{ENL} - T_j



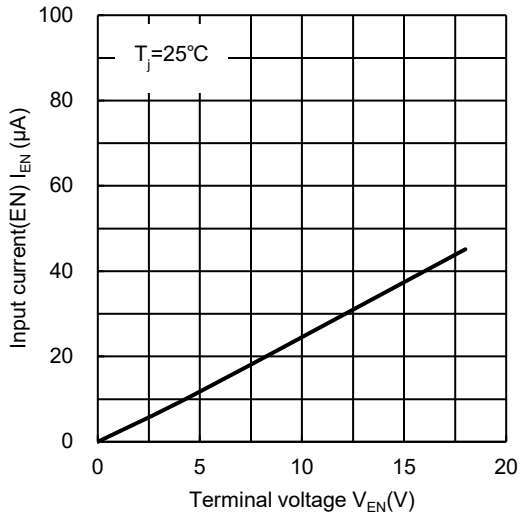
I_{INx} - V_{INx}



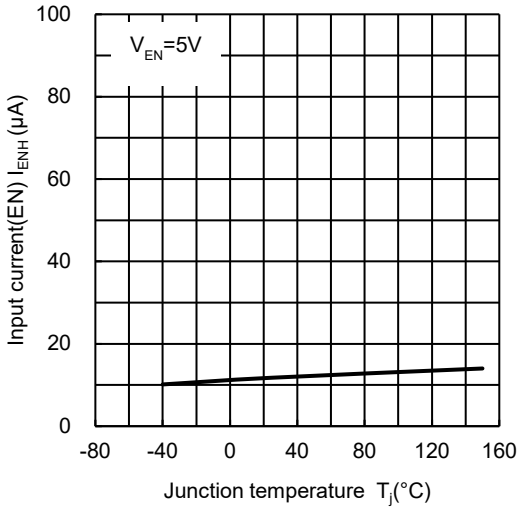
I_{INx} - T_j



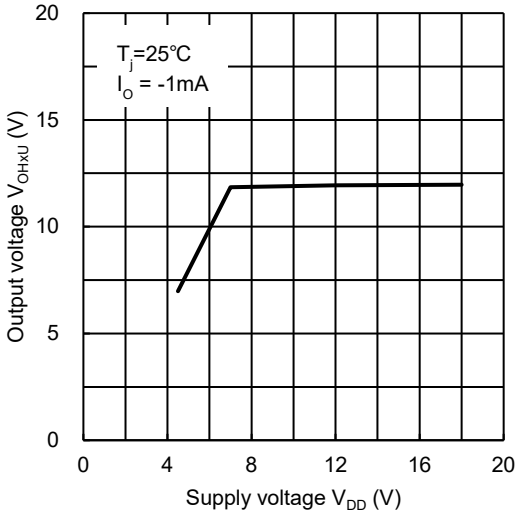
I_{EN} - V_{EN}



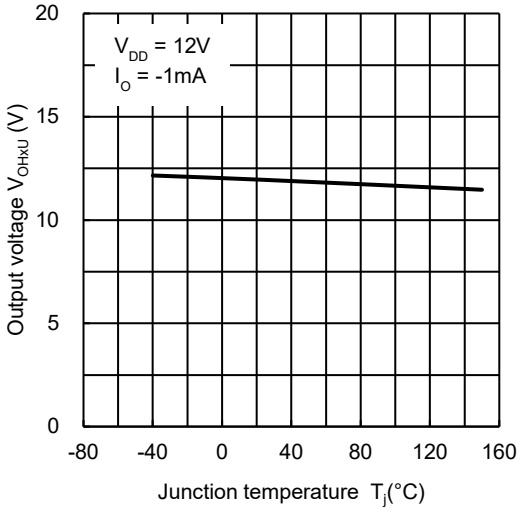
I_{ENH} - T_j



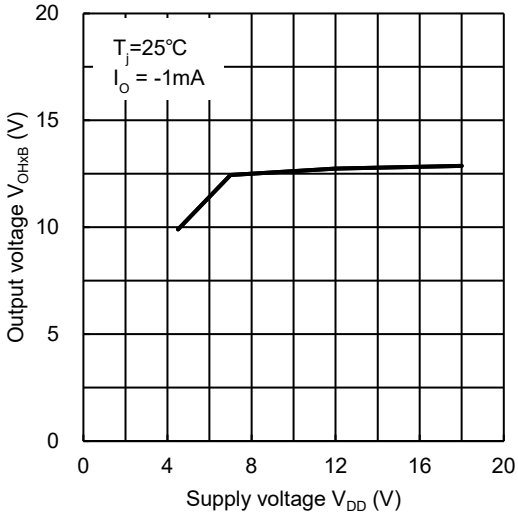
V_{OHxU} - V_{DD}



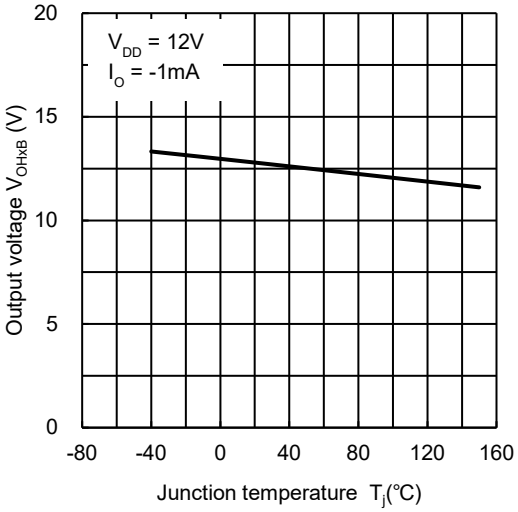
V_{OHxU} - T_j



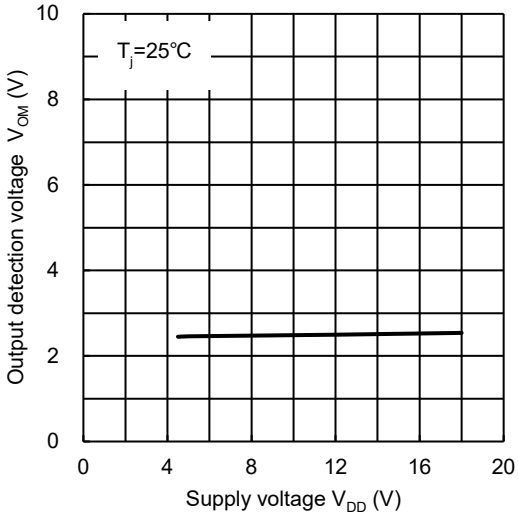
V_{OHxB} - V_{DD}



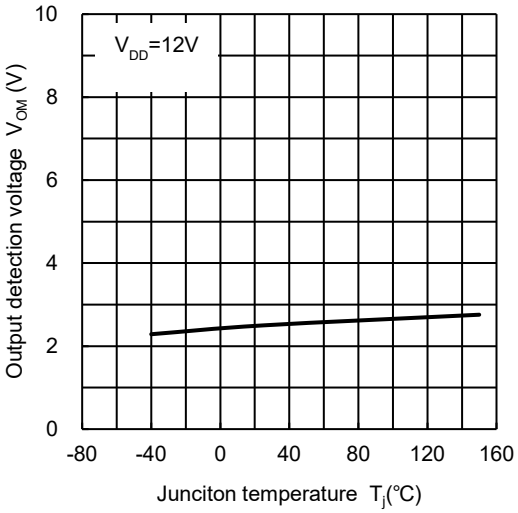
V_{OHxB} - T_j



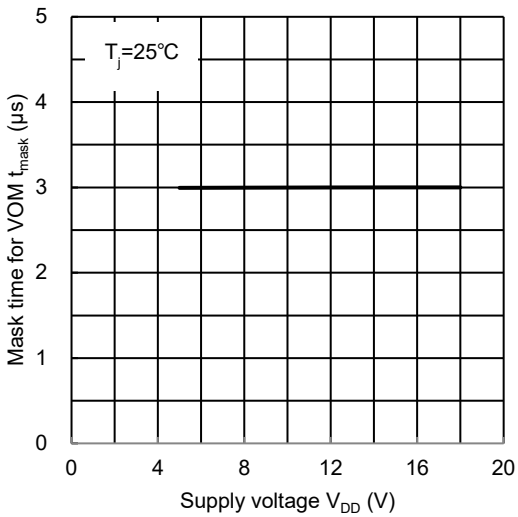
V_{OM} - V_{DD}



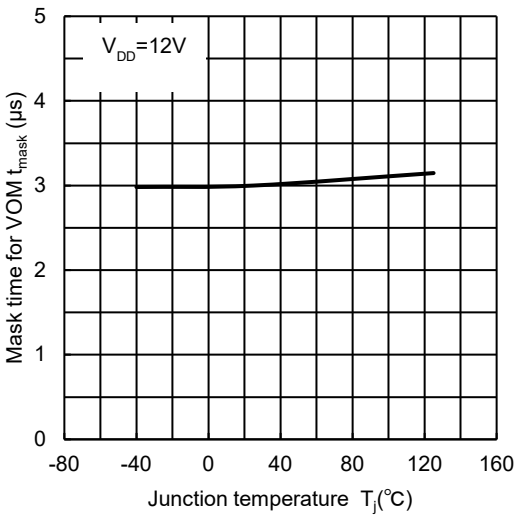
V_{OM} - T_j



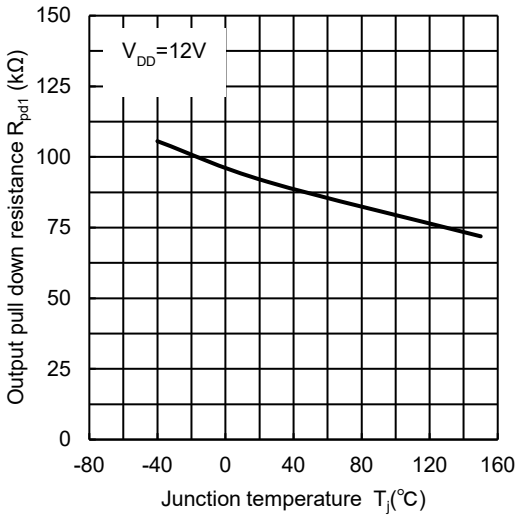
t_{mask} - V_{DD}



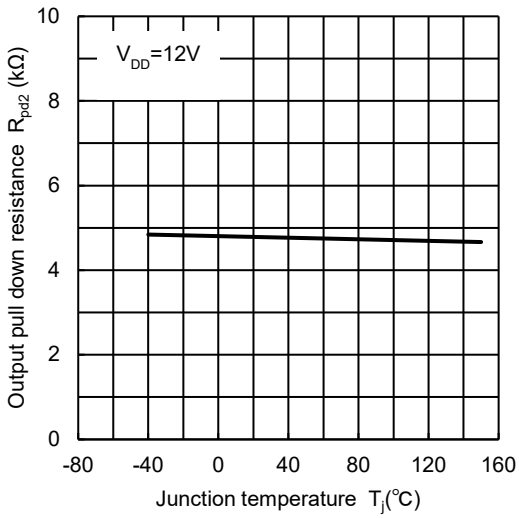
t_{mask} - T_j



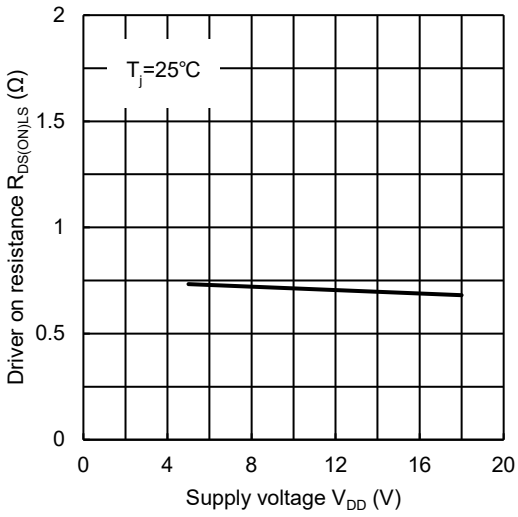
R_{pd1} - T_j



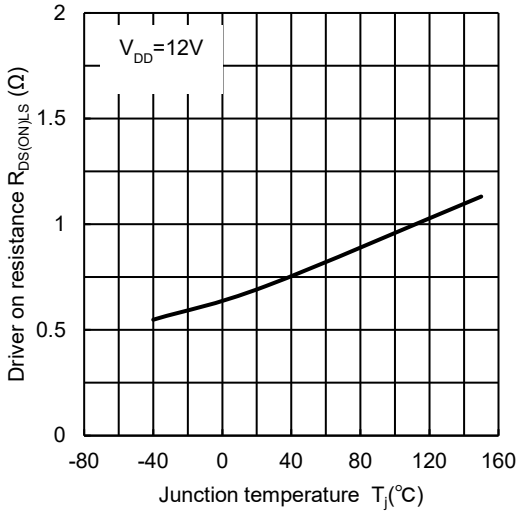
R_{pd2} - T_j



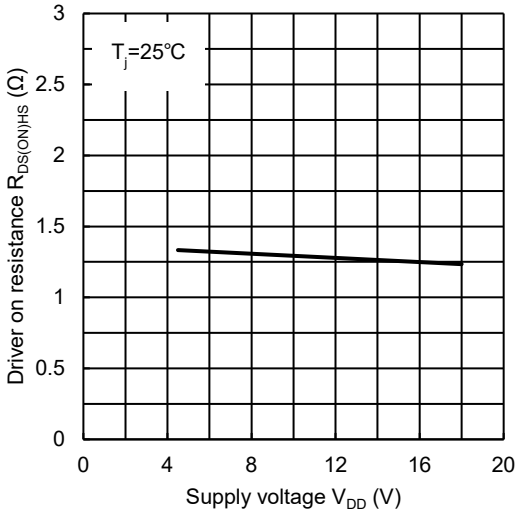
$R_{DS(ON)LS}$ - V_{DD}



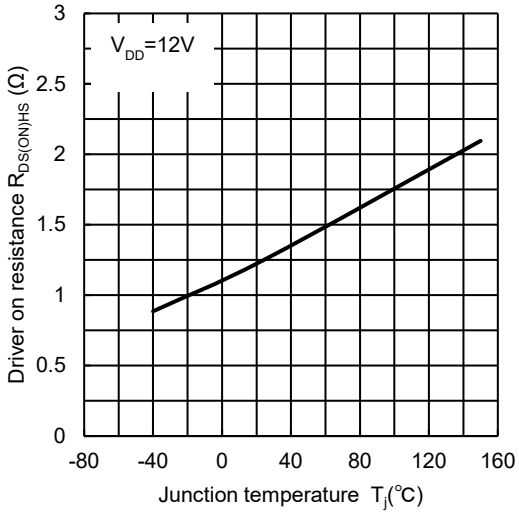
$R_{DS(ON)LS}$ - T_j



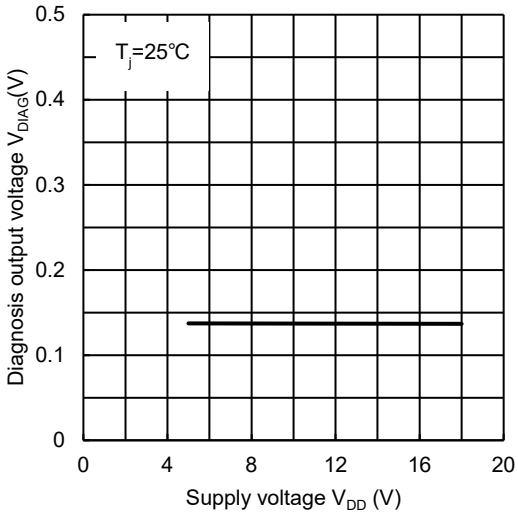
$R_{DS(ON)HS}$ - V_{DD}



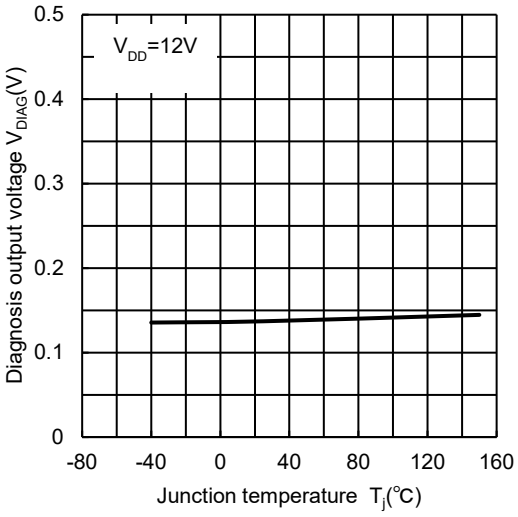
$R_{DS(ON)HS}$ - T_j



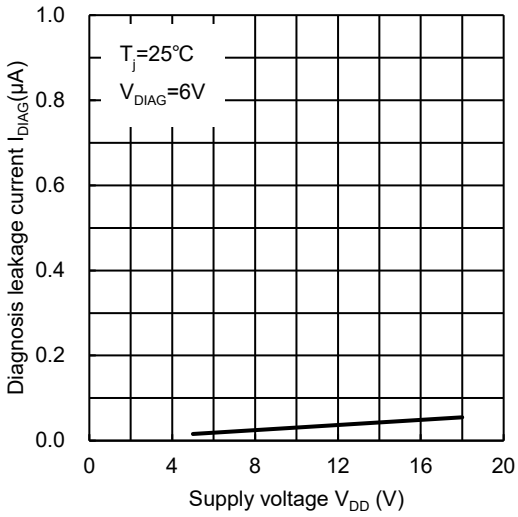
V_{DIAG} - V_{DD}



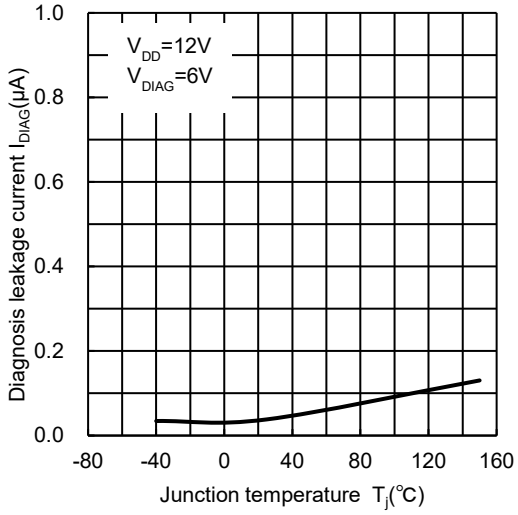
V_{DIAG} - T_j



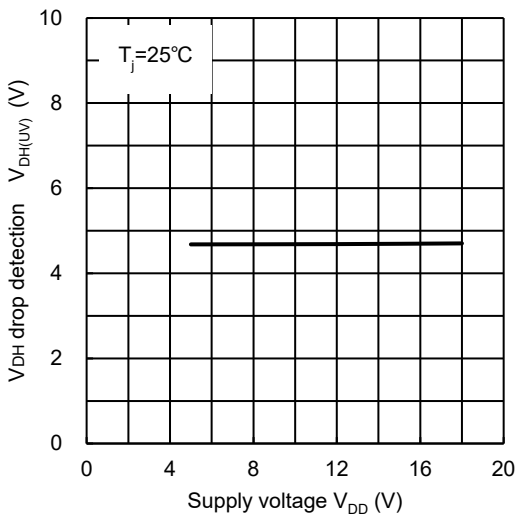
I_{DIAG}-V_{DD}



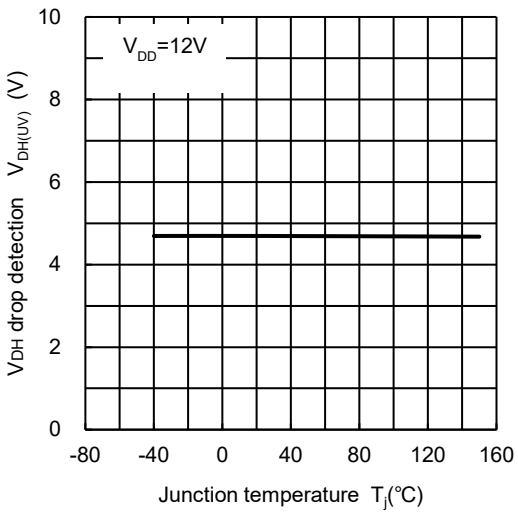
I_{DIAG}-T_j



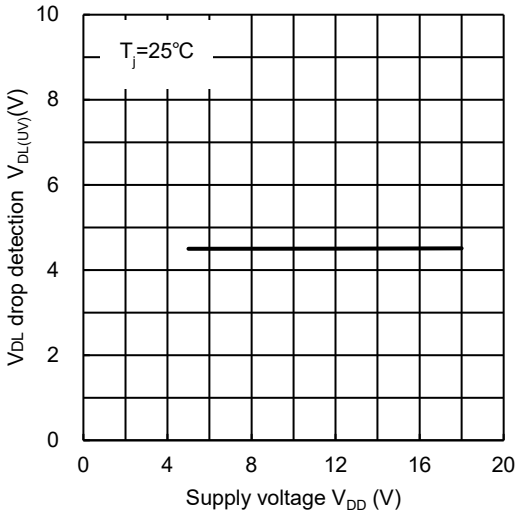
$V_{DH(UV)}$-V_{DD}



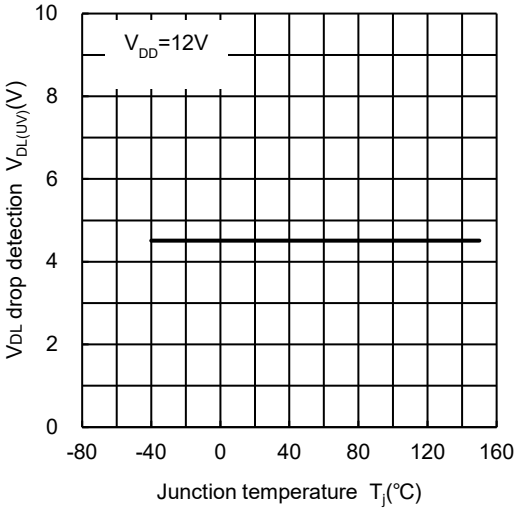
$V_{DH(UV)}$-T_j



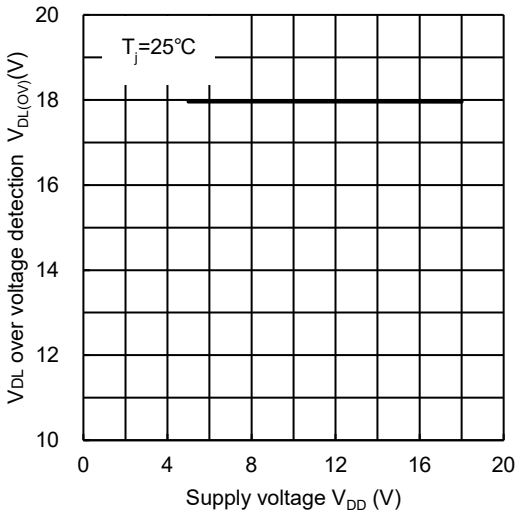
$V_{DL(UV)}$-V_{DD}



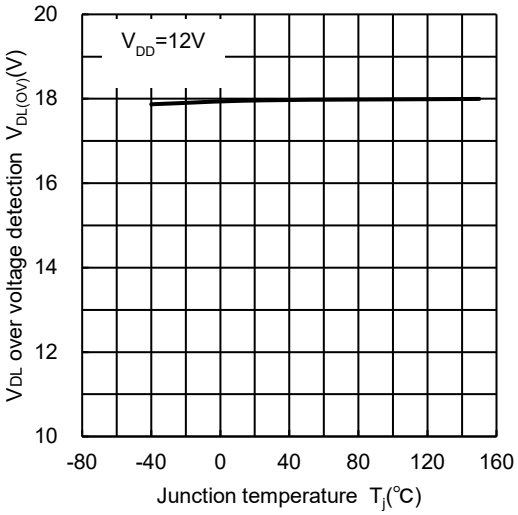
$V_{DL(UV)}$-T_j



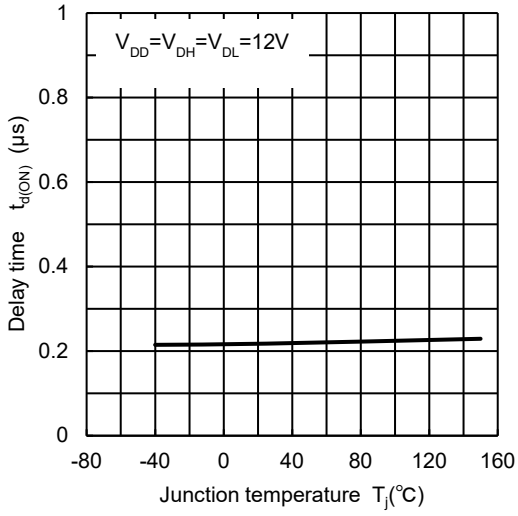
$V_{DL(OV)}$-V_{DD}



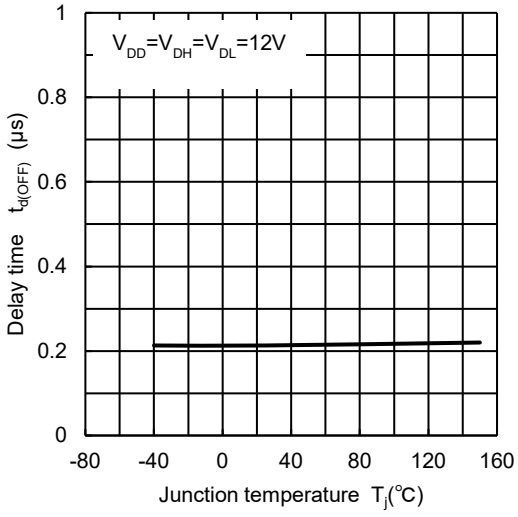
$V_{DL(OV)}$-T_j



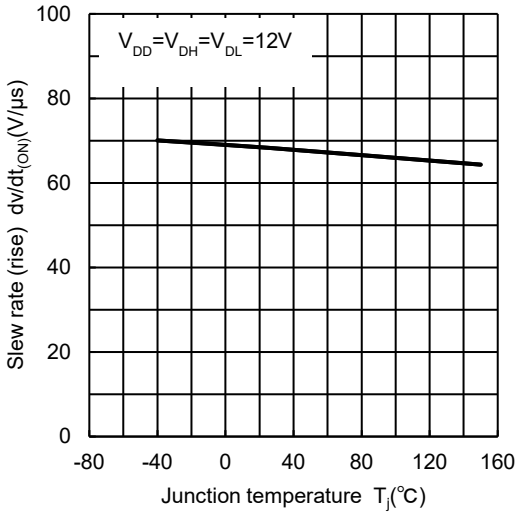
$t_{d(ON)}$-T_j



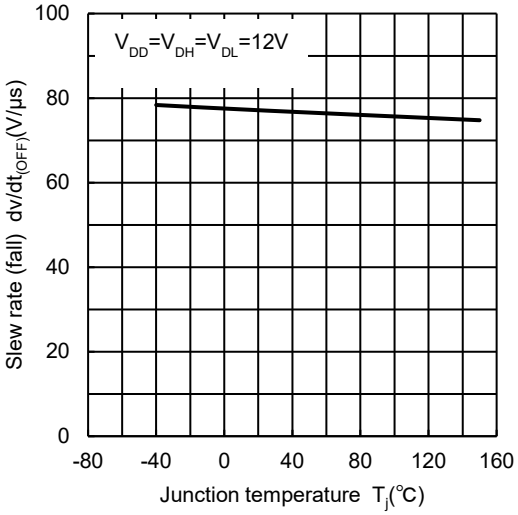
$t_{d(OFF)}$-T_j



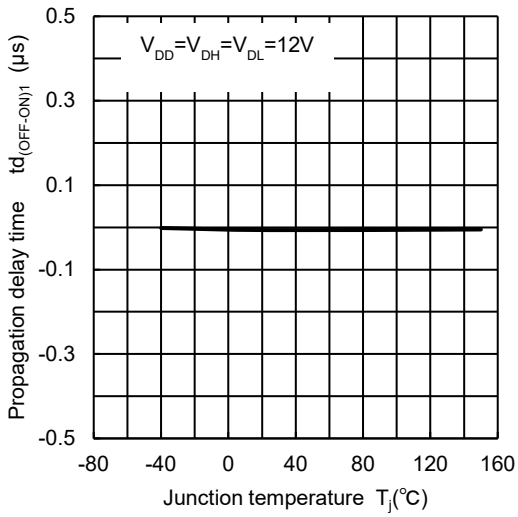
$dv/dt_{(ON)}$-T_j



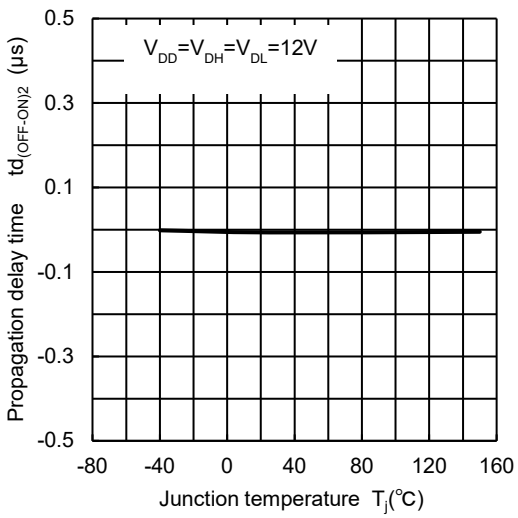
$dv/dt_{(OFF)}$-T_j



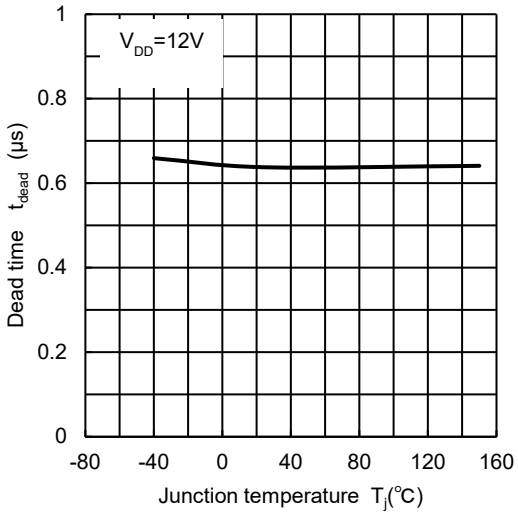
$\Delta t_{d(OFF-ON)1}$-T_j



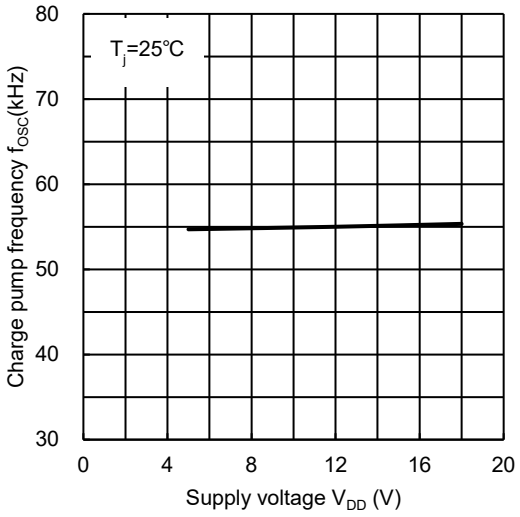
$\Delta t_{d(OFF-ON)2}$-T_j



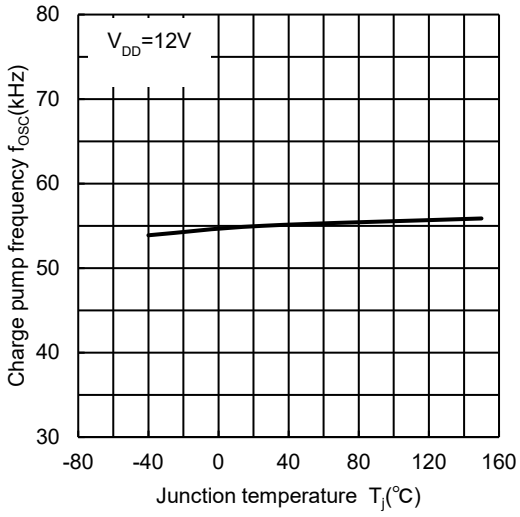
t_{dead} - T_j



f_{OSC}-V_{DD}



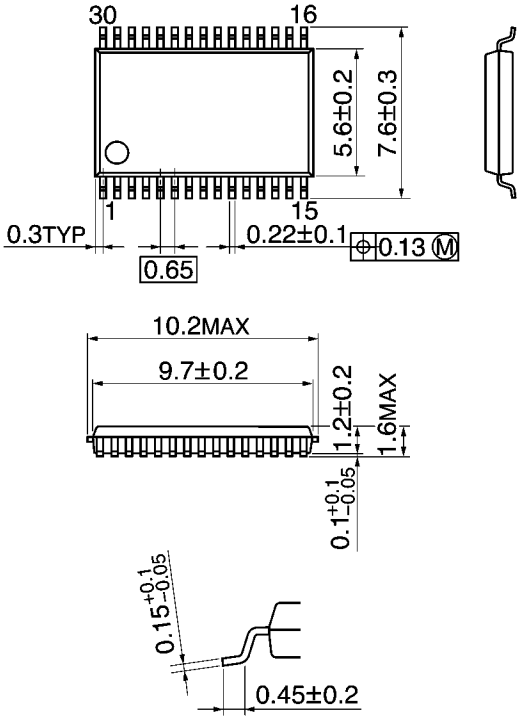
f_{OSC}-T_j



13. Package Information

13.1. Package Dimensions

Unit : mm



Weight: 0.176 g (typ.)

Figure 13.1 Package Dimensions

13.2. Marking

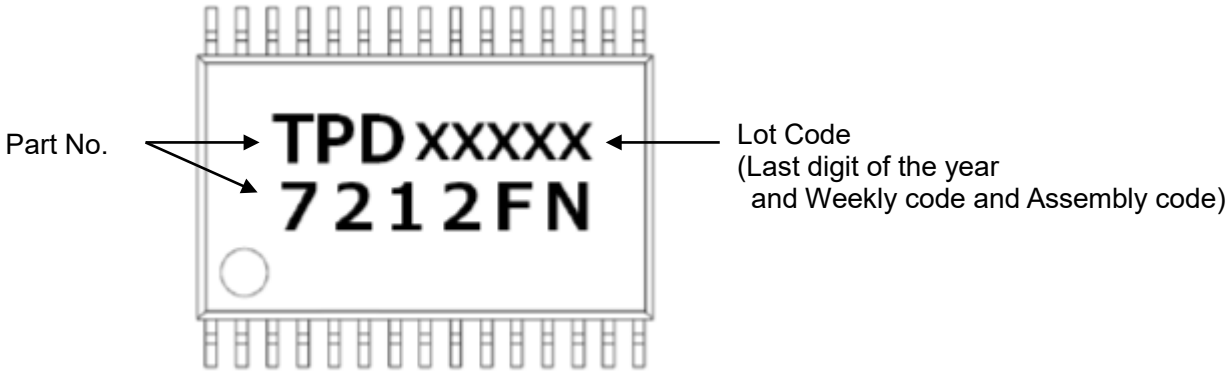


Figure 13.2 Marking

13.3. Land Pattern Dimensions for Reference only

SSOP30-P-300-0.65

"Unit: mm"

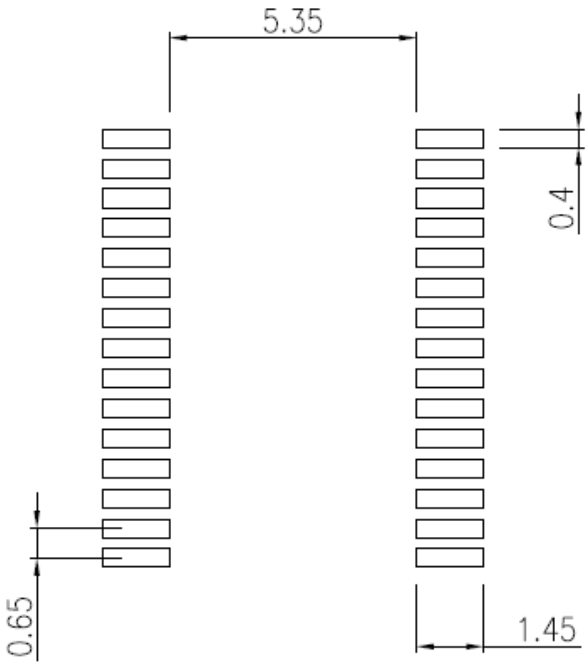


図 13.3 Land Pattern Dimensions for Reference only

14. IC Usage Considerations

14.1. Notes on Handling of ICs

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.

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