# NPS4001

## 5.5 V, 55 mΩ load switch with current limitation

Rev. 1 — 25 April 2024 Product data sheet

## 1. General description

The NPS4001 is a 5.5 V, 55 mΩ load switch suitable for applications up to 2 A.

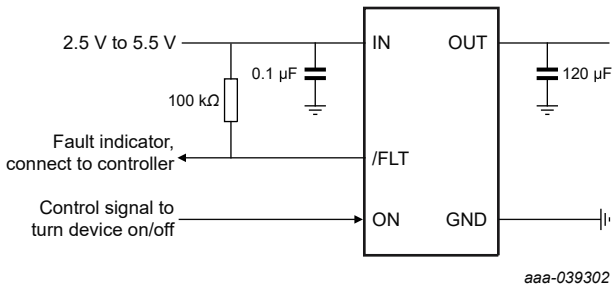
The NPS4001 switch limits the output current to a constant current by using a constant-current mode when the output load exceeds the current limit threshold or shorted. An internal voltage comparator disables the load switch when the output voltage is higher than the input to protect devices on the input side of the switch. The FLG pin is an active low output to indicate overcurrent, over temperature and reverse voltage conditions.

## 2. Features and benefits

- Input operating voltage range ($V_{IN}$): 2.5 V to 5.5 V
- Rated current ($I_{MAX}$): 2 A
- ON resistance ($R_{DS(on)}$):
  - $V_{IN}$ = 5.5 V: 55 mΩ (typical)
  - $V_{IN}$ = 3.6 V: 65 mΩ (typical)
  - $V_{IN}$ = 2.5 V: 80 mΩ (typical)
- Constant current during current limit
- No body diode when disabled (no current path from pin OUT to pin IN)
- Active reverse voltage protection
- Built in soft start
- UL 62368 recognition
- SOT753 (TSOP5) package
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C2a exceeds 500 V
  - IEC 61000-4-2 contact discharge 8000 V
  - IEC 61000-4-2 air-gap discharge 15000 V
- Specified from -40 °C to +125 °C

## 3. Applications

- USB ports/hubs, laptops, docking station and desktops
- Set top box
- HDTV
- Optical socket protection
- Current limiting circuits




**Note:** For USB port applications, connect a capacitor of at least 120 µF at the output. For other applications, choose output capacitor according to actual transit requirements.

**Fig. 1. Typical application circuit**

# 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| NPS4001GV | -40 °C to +125 °C | SC-74A | plastic surface-mounted package; 5 leads | SOT753 |

# 5. Marking

**Table 2. Marking**

| Type number | Marking code |
|---|---|
| NPS4001GV | s7 |

# 6. Functional diagram

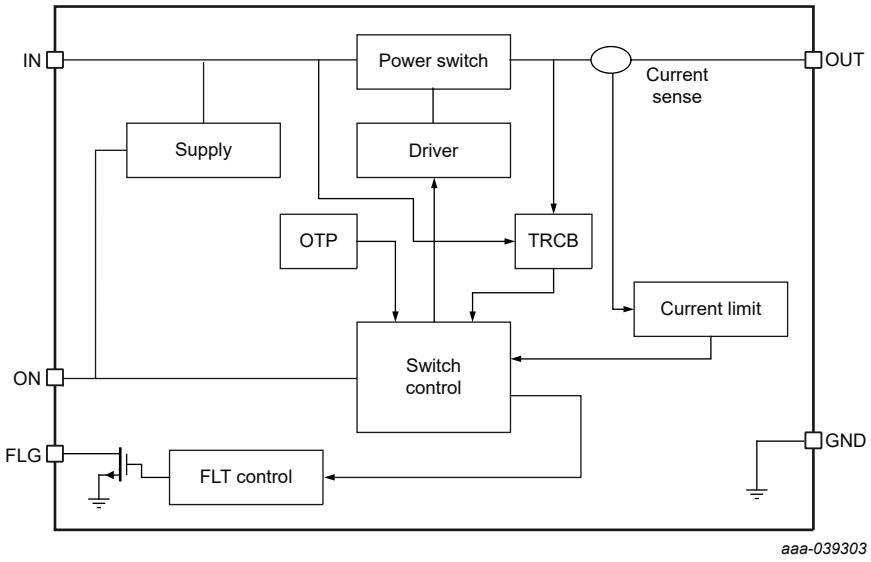
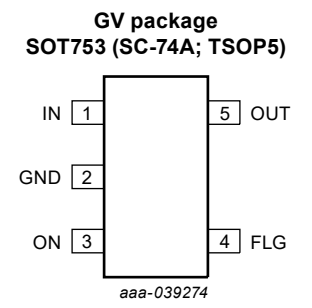



**Fig. 2. Functional block diagram**

# 7. Pinning information

## 7.1. Pinning



## 7.2. Pin description

**Table 3. Pin description**

| Symbol | Pin | I/O | Description |
|---|---|---|---|
| IN | 1 | Supply | Power-switch input pin. Connect a ceramic capacitor of minimal 0.1 µF from pin IN to GND, as close to the IC as possible. |
| GND | 2 | Supply | Ground connection; connect externally to PCB ground. |
| ON | 3 | I | ON/OFF (enable) input. LogicHIGH turns on power switch. |
| FLG | 4 | O | Active-low open-drain output, pulled up to VIN or other power rails via external resistor. Asserts low during overcurrent, overtemperature and reverse-voltage conditions. Can be shorted to GND or floating if not used. |
| OUT | 5 | O | Power-switch output pin. Connect at least 120 µF capacitor at output for USB port application. Choose output capacitor according to actual transient requirements for other applications other than USB. |

# 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V). [1]*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IN}$ | input voltage | pin IN | -0.3 | +6 | V |
| $V_{OUT}$ | output voltage | pin OUT | -0.3 | +6 | V |
| $V_{ON}$ | ON/OFF (enable) input voltage | pin ON | -0.3 | +6 | V |
| $V_{FLG}$ | FLG pin voltage | pin FLG | -0.3 | +6 | V |
| $V_{IN}$-$V_{OUT}$ | voltage range from pin IN to pin OUT | | -6 | +6 | V |
| $I_{FLG}$ | FLG pin sink current | pin FLG | 0 | 25 | mA |
| $T_j$ | junction temperature | | -40 | +150 | °C |
| $T_{stg}$ | storage temperature | | -65 | +150 | °C |
| **ESD** | | | | | |
| $V_{ESD}$ | electrostatic discharge voltage | HBM ANSI/ESDA/JEDEC JS-001 | -2 | +2 | kV |
| | | CDM ANSI/ESDA/JEDEC JS-002 | -0.5 | +0.5 | kV |
| | | IEC 61000-4-2 contact discharge | -8 | +8 | kV |
| | | IEC 61000-4-2 air-gap discharge | -15 | +15 | kV |

[1] Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

# 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IN}$ | input voltage | pin IN | 2.2 | 5.5 | V |
| $V_{ON}$ | ON/OFF (enable) input voltage | pin ON | 0 | 5.5 | V |
| $V_{IH}$ | HIGH-level input voltage | ON pin | 1.4 | - | V |
| $V_{IL}$ | LOW-level input voltage | ON pin | 0 | 0.35 | V |
| $I_{OUT}$ | continuous output current | | 0 | 2 | A |
| $I_{FLG}$ | continuous sink current pin FLG | | 0 | 10 | mA |
| $T_{amb}$ | ambient temperature | | -40 | +125 | °C |

# 10. Thermal Information

**Table 6. Thermal information**

*Thermal resistance according JEDEC51 -5 and -7*

| Symbol | Parameter | Measurement | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Junction to ambient thermal resistance | 160 | °C/W |
| $R_{\theta JC(top)}$ | Junction to case(top) thermal resistance | 132.1 | °C/W |
| $\Phi_{JT}$ | Junction to top char parameter | 21.1 | °C/W |
| $\Phi_{JB}$ | Junction to board char parameter | 37.1 | °C/W |

# 11. Static characteristics

**Table 7. Static characteristics**

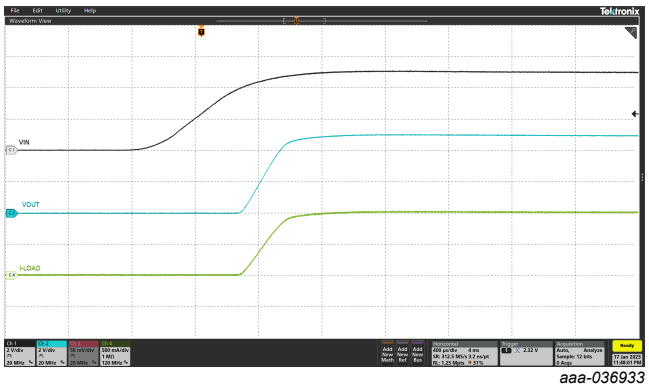
*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

*$V_{IN}$ = 5 V, $R_{FLG}$ = 100 kΩ, all typical values are measured at $T_{amb}$ = 25 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | $T_{amb}$ = -40 °C to +125 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **POWER SWITCH** | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{IN}$= 5.5 V | - | 55 | 88 | mΩ |
| | | $V_{IN}$= 3.6 V | - | 65 | 109 | mΩ |
| | | $V_{IN}$= 2.5 V | - | 80 | 140 | mΩ |
| $t_r$ | rise time output | $C_L$ = 1 µF; $R_L$ = 100 Ω | | | | |
| | | $V_{IN}$ = 5.5 V | - | 0.3 | 1 | ms |
| | | $V_{IN}$ = 2.5 V | - | 0.2 | 1 | ms |
| $t_f$ | fall time output | $C_L$ = 1 µF; $R_L$ = 100 Ω | | | | |
| | | $V_{IN}$ = 5.5 V | - | 0.2 | 0.3 | ms |
| | | $V_{IN}$ = 2.5 V | - | 0.2 | 0.3 | ms |
| **ON/OFF INPUT** | | | | | | |
| $I_{ON}$ | input current | $V_{ON}$ = 0 V or 5.5 V | -0.5 | - | 0.5 | uA |
| $t_{on}$ | turn-on time | $V_{IN}$= 2.5 V to 5.5 V; $C_L$ = 1 µF; $R_L$ = 100 Ω | - | - | 3 | ms |
| $t_{off}$ | turn-off time | $V_{IN}$=2.5 V to 5.5 V; $C_L$ = 1 µF; $R_L$ = 100 Ω | - | - | 3 | ms |
| $I_{LIMIT}$ | current-limit threshold | $V_{IN}$ - $V_{OUT}$ = 1.0 V | 1.58 | 2.37 | 3.17 | A |

| Symbol | Parameter | Conditions | $T_{amb}$ = -40 °C to +125 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **REVERSE VOLTAGE PROTECTION** | | | | | | |
| $V_{reverse}$ | reverse-voltage comparator trip point | | - | 75 | 110 | mV |
| $t_{reverse}$ | time from reverse-voltage condition to MOSFET turn off | $V_{IN}$ = 4 V; $V_{OUT}$ = 5 V | - | 0.5 | 5 | µs |
| **SUPPLY CURRENT** | | | | | | |
| $I_q$ | quiescent current | $V_{IN}$ = $V_{ON}$= 5.5 V; no load on pin OUT | - | - | 285 | µA |
| $I_{SD}$ | shut down current | $V_{IN}$ = 5.5 V; no load on pin OUT, $V_{ON}$ = 0 V | - | - | 1 | µA |
| $I_{REV}$ | reverse current leakage | $V_{IN}$ = 0 V; $V_{OUT}$ = 5.5 V | - | 150 | - | nA |
| **UNDERVOLTAGE LOCKOUT** | | | | | | |
| $V_{UVLO}$ | under voltage lockout low-level input voltage | $V_{IN}$ rising | - | 2.35 | 2.45 | V |
| $V_{hys(UVLO)}$ | undervoltage lockout hysteresis voltage | $T_j$ = 25 °C | - | 25 | - | mV |
| **FLG INDICATOR** | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{FLG}$ = 1 mA | - | - | 180 | mV |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{FLG}$ = 5.5 V | - | - | 1 | µA |
| $t_{degl}$ | deglitch time | FLG assertion or de-assertion due to overcurrent condition | - | 8.5 | 12 | ms |
| | | FLG assertion or de-assertion due to reverse-voltage condition | - | 0.2 | 1 | ms |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{th(sd)}$ | shutdown threshold temperature | | 155 | - | - | °C |
| $T_{sd(hys)}$ | shutdown temperature hysteresis | | - | 10 | - | °C |

## 11.1. Typical characteristics

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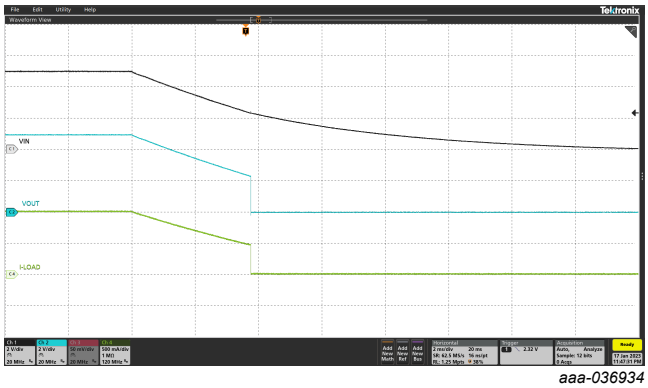
$V_{IN}$=5 V, $C_{OUT}$ = 1 µF, $I_{load}$ = 1 A

**Fig. 3. Turn ON**

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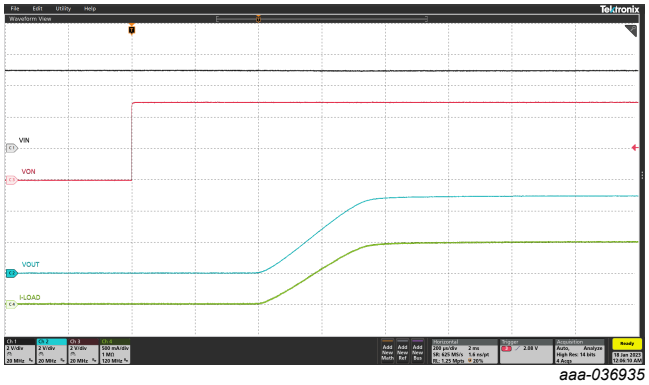
$V_{IN}$=5 V, $C_{OUT}$ = 1 µF, $I_{load}$ = 1 A

**Fig. 4. Turn OFF**

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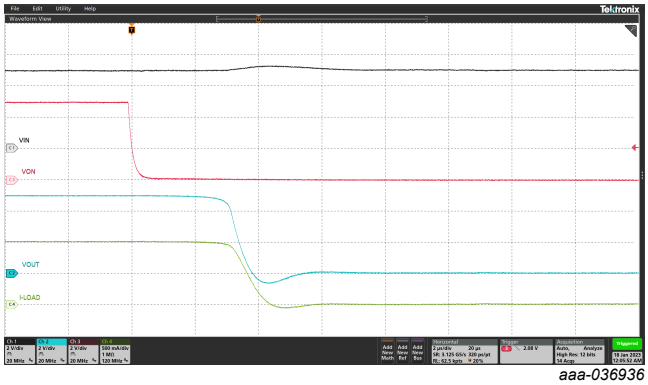
$V_{IN}$=5 V, $V_{ON}$=5 V, $C_{OUT}$ = 1 µF, $I_{load}$ = 1 A

**Fig. 5. Enable**

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$V_{IN}$=5 V, $V_{ON}$=5 V, $C_{OUT}$ = 1 µF, $I_{load}$ = 1 A

**Fig. 6. Disable**

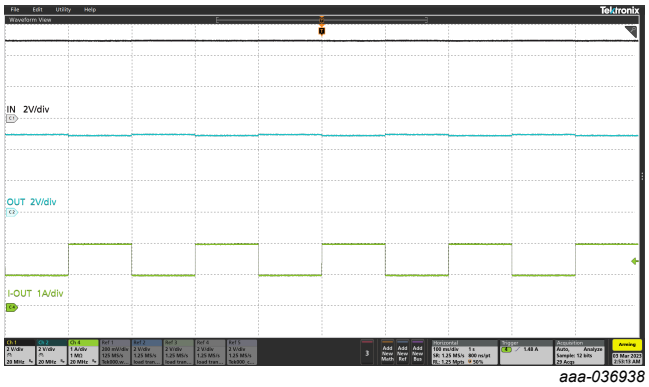


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**Fig. 7. $V_{IN}$ transient 1 A to 2 A**

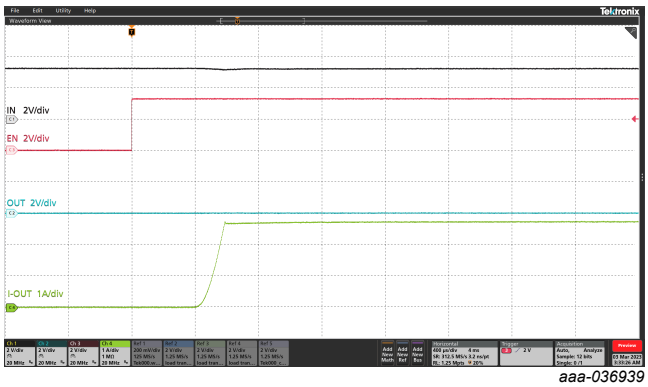


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**Fig. 8. Enable to short**

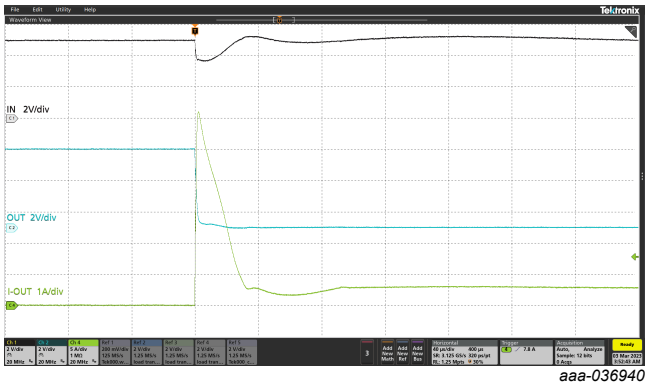



Fig. 9. Hard short

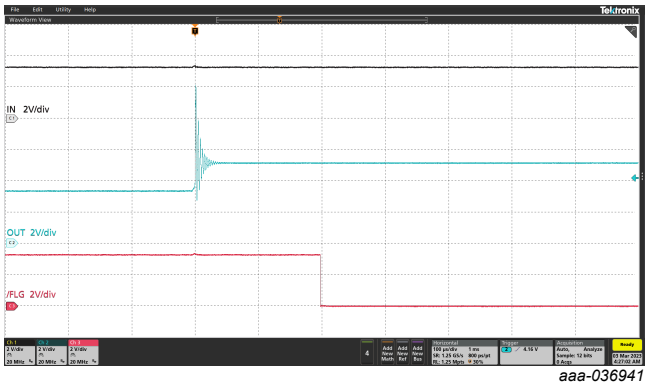



Fig. 10. Reverse voltage blocking

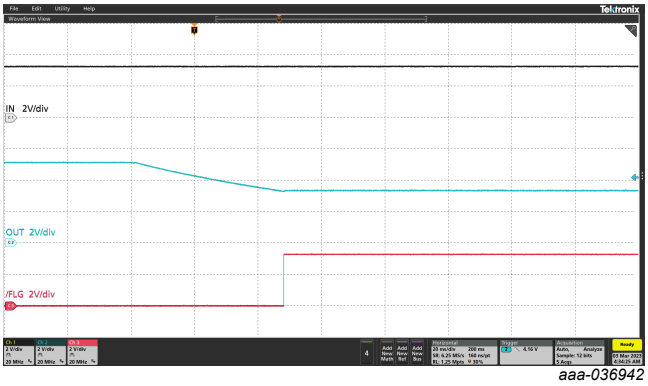
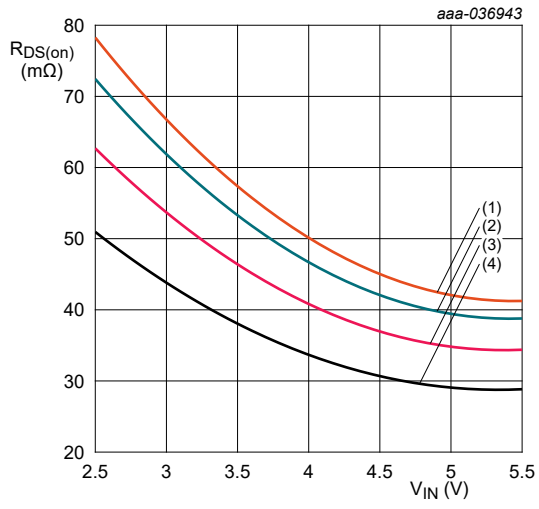
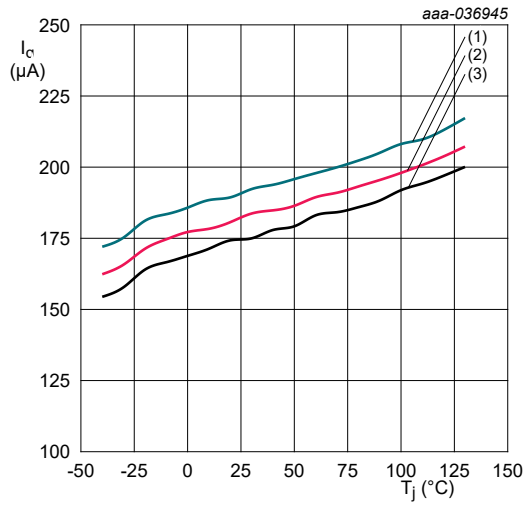



Fig. 11. Reverse voltage blocking



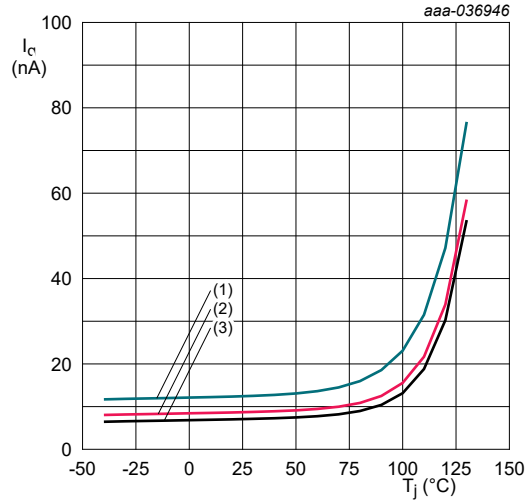

(1) $T_{amb}$ = 125 °C
(2) $T_{amb}$ = 85 °C
(3) $T_{amb}$ = 25 °C
(4) $T_{amb}$ = -40 °C

Fig. 12. $R_{DS(on)}$ vs $V_{IN}$




(1) $V_{IN}$ = 5.0 V
(2) $V_{IN}$ = 3.3 V
(3) $V_{IN}$ = 2.5 V

Fig. 13. Supply current (output enabled)




(1) $V_{IN}$ = 5.0 V
(2) $V_{IN}$ = 3.3 V
(3) $V_{IN}$ = 2.5 V

**Fig. 14. Supply current (output disabled)**

# 12. Functional description

## 12.1. Overview

The NPS4001 is a 5.5 V, 55 mΩ P-channel load switch with overcurrent, overtemperature and active reverse voltage protections. The NPS4001 offers fixed current-limit thresholds for applications that require 2 A loading.

The NPS4001 has built in soft-start functionality and controls the rising and falling times of the output voltage to limit large current and voltage surges. Additional features include overtemperature protection and active reverse-voltage protection.

NPS4001 enters constant-current limit when the load exceeds the current limit threshold.

### 12.1.1. Functional block diagram

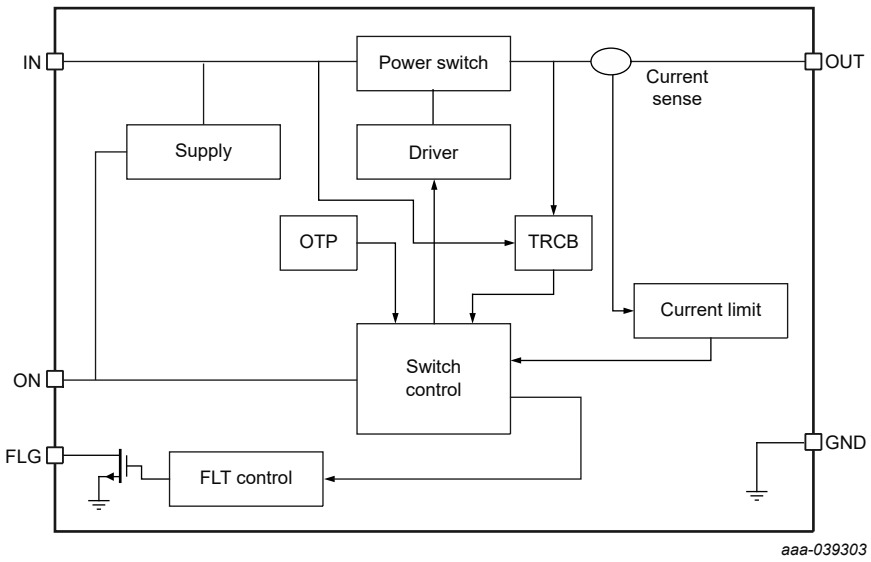



**Fig. 15. Functional block diagram**

## 12.2. Feature description

### 12.2.1. Overcurrent protection

When the load current exceeds the current limit threshold set by the external resistor, the NPS4001 enters constant current mode by limiting the output current to the current limit threshold until the overcurrent condition is removed. FLG pin asserts if the overcurrent condition persists for 8.5 ms.

### 12.2.2. Output short circuit protection ($I_{LIMIT}$)

When the switch is turned on while the output pin is shorted to ground, the NPS4001 enters constant current mode immediately and limits the output current to $I_{LIMIT}$ (see Fig. 16) until the short circuit condition is removed. When the output pin is shorted to ground while the switch is fully turned on, a large current will flow through the switch. The switch responds to short-circuit condition within the time $t_{SC}$ (see Fig. 17). As in previous cases, NPS4001 limits the output current to $I_{LIMIT}$ until the short circuit condition is removed.

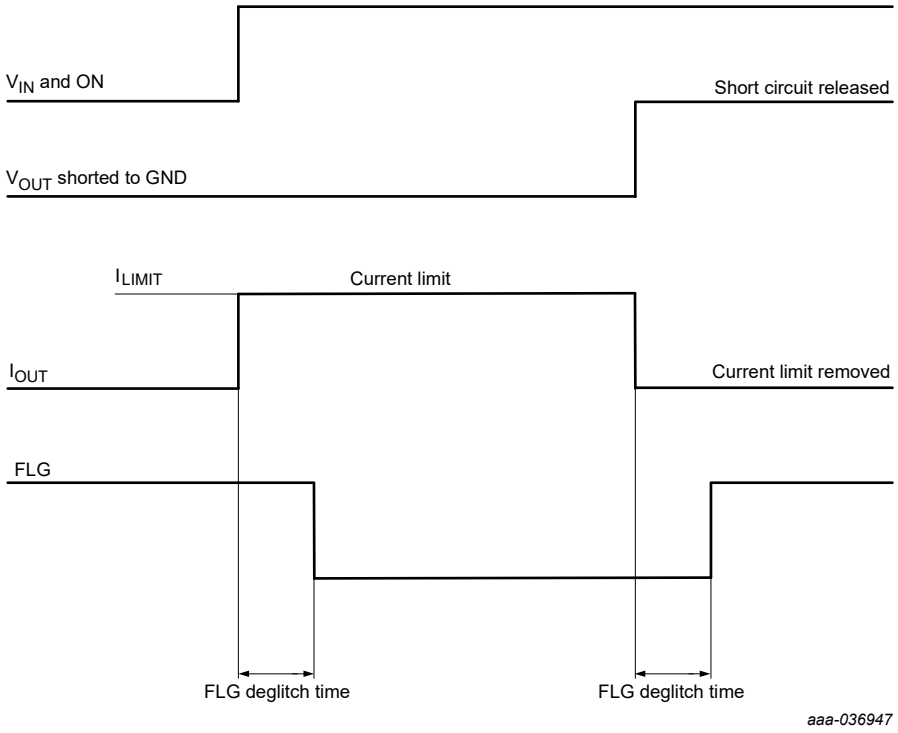



**Fig. 16. Power on to short circuit**

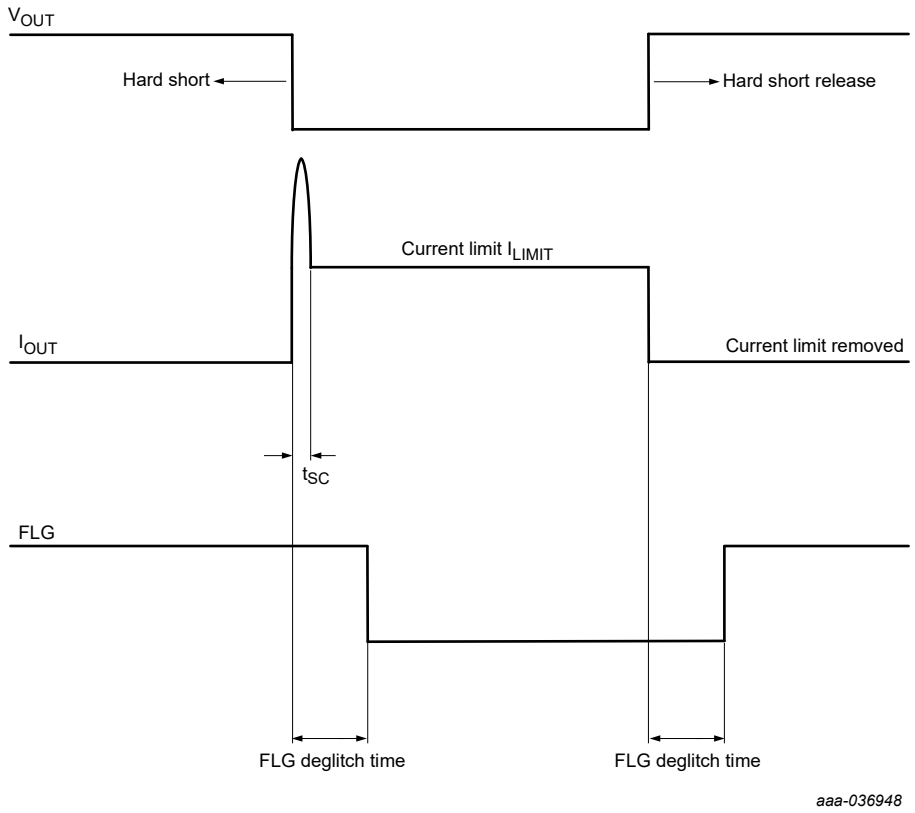



**Fig. 17. Hot short**

### 12.2.3. Output discharge

The NPS4001 integrates a 300 Ω pull-down resistor for quick output discharge when disabled.

### 12.2.4. Overtemperature protection

The NPS4001 thermal cycles if an over current condition is present long enough to activate thermal Limit in any of the above cases. The switch turns off when the junction temperature exceeds 155 °C (typical). The switch remains off until the junction temperature cools 10 °C (typical) and then restarts (see Fig. 18). FLG pin asserts immediately when the junction temperature exceeds 155 °C.

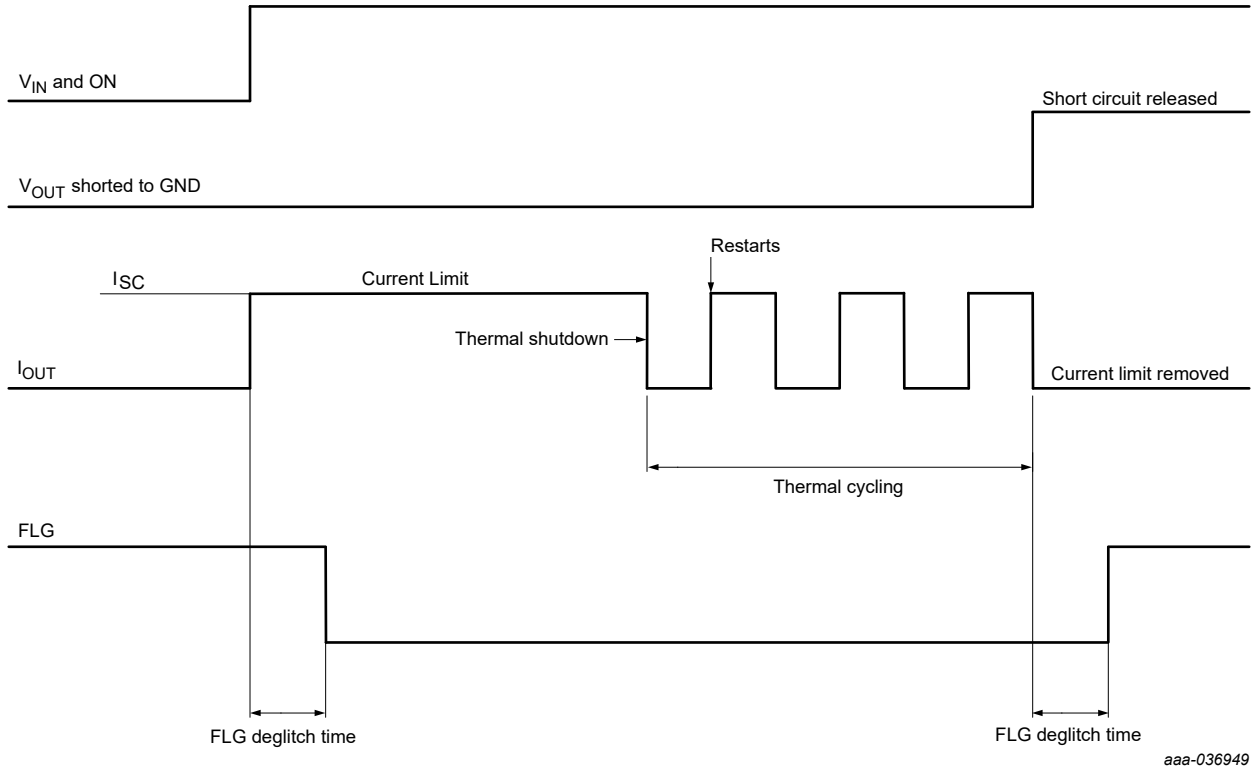



**Fig. 18. Power on to short circuit until thermal shutdown**

## 12.2.5. Reverse voltage protection

The NPS4001 integrates active reverse voltage protection. The switch turns off internal MOSFET whenever the output voltage exceeds the input voltage by 75 mV for 0.5 µs. The NPS4001 switch turns on once the reverse voltage condition is removed (see Fig. 19). FLG pin will assert low 0.2 ms after reverse voltage condition and de-assert after reverse voltage condition is removed.

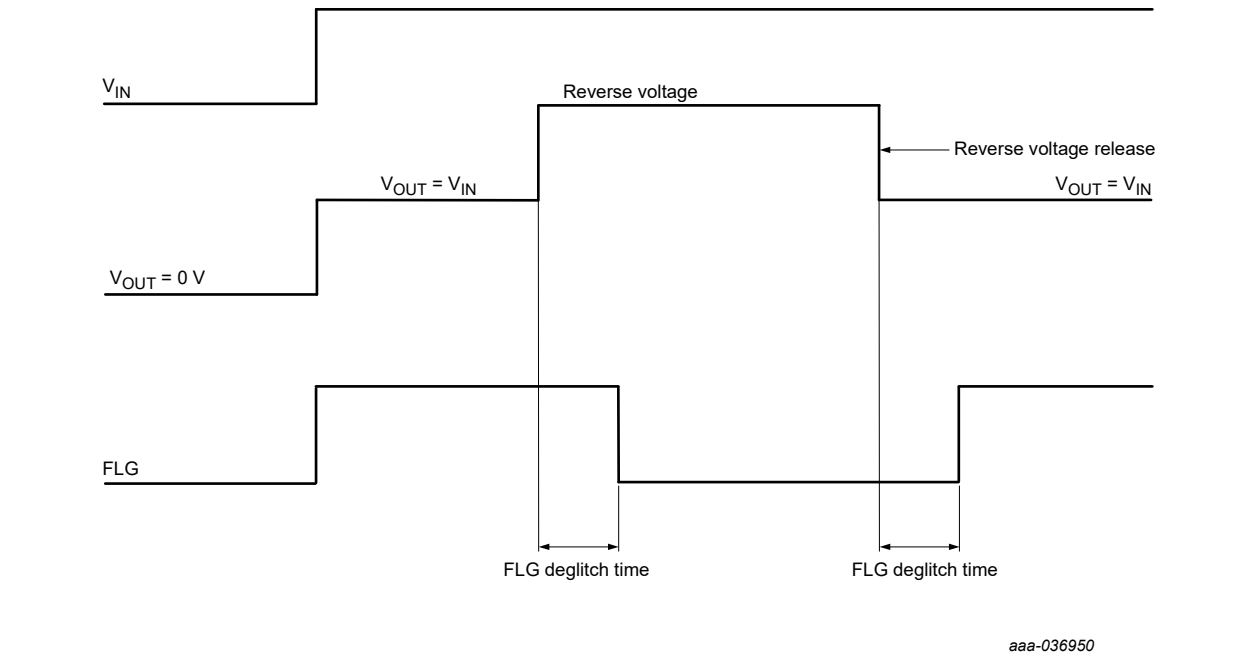



**Fig. 19. Reverse voltage protection**

### 12.2.6. FAULT flag response

Fault flag (pin FLG) output is an N-MOS open drain output. FLG pin is asserted low during overcurrent, overtemperature and reverse voltage conditions. An internal deglitch circuit is designed to eliminate false FLG reporting. Deglitch time for over current is 8.5 ms and that for reverse voltage is 0.2 ms. FLG pin voltage goes low 8.5 ms after over current and goes high 8.5 ms after over current condition is removed (see Fig. 16). FLG pin voltage goes low 0.2 ms after reverse voltage and goes high 0.2 ms after reverse voltage condition is removed (see Fig. 19). Overtemperature condition is not deglitched and asserts the FLG signal immediately when the junction temperature exceeds 155 °C. FLG pin can be shorted to ground or left floating when not used.

### 12.2.7. Undervoltage lockout (UVLO)

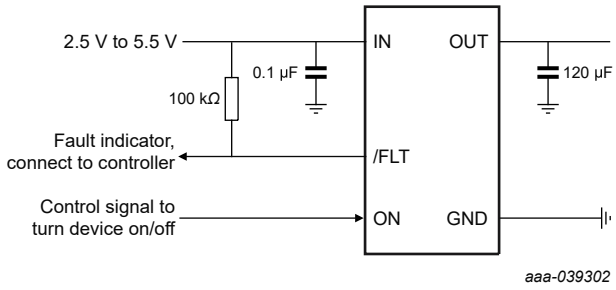
The undervoltage lockout (UVLO) circuit prevents the power switch from turning on until input voltage reaches the UVLO turn on threshold. Hysteresis is also built in to present unwanted on and off cycling due to input voltage drop from large current surges.

### 12.2.8. Enable (ON)

The logic enable (pin ON) circuit controls the power switch, a logic high enables the internal MOSFET. The enable input is compatible with both TTL and CMOS logic levels. The enable circuit also provides power to other circuits to reduce the supply current. The power supply current is reduced to less than 1 µA when a logic low is present on ON pin.

## 13. Application information

### 13.1.




$V_{IN}$ = 2.5 V to 5.5 V; $V_{OUT}$ = 2.5 V to 5.5 V

**Note:** For USB port applications, connect a capacitor of at least 120 µF at the output. For other applications, choose output capacitor according to actual transit requirements.

**Fig. 20. One-level current limit circuit**

## 14. Layout

### 14.1. Power supply recommendations

The NPS4001 is designed to operate with a $V_{IN}$ range of 2.5 V to 5.5 V. The $V_{IN}$ power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance ($C_{IN}$) of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

## 14.2. Layout guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for $V_{IN}$, $V_{OUT}$, and GND helps minimize the parasitic electrical effects.

## 14.3. Layout example

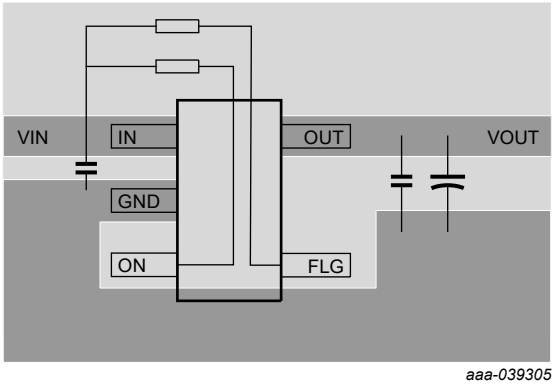



**Fig. 21. NPS4001 layout example (SOT753)**

# 15. Thermal considerations

The maximum IC junction temperature should be restricted to 125 °C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, the equation as shown below can be used:

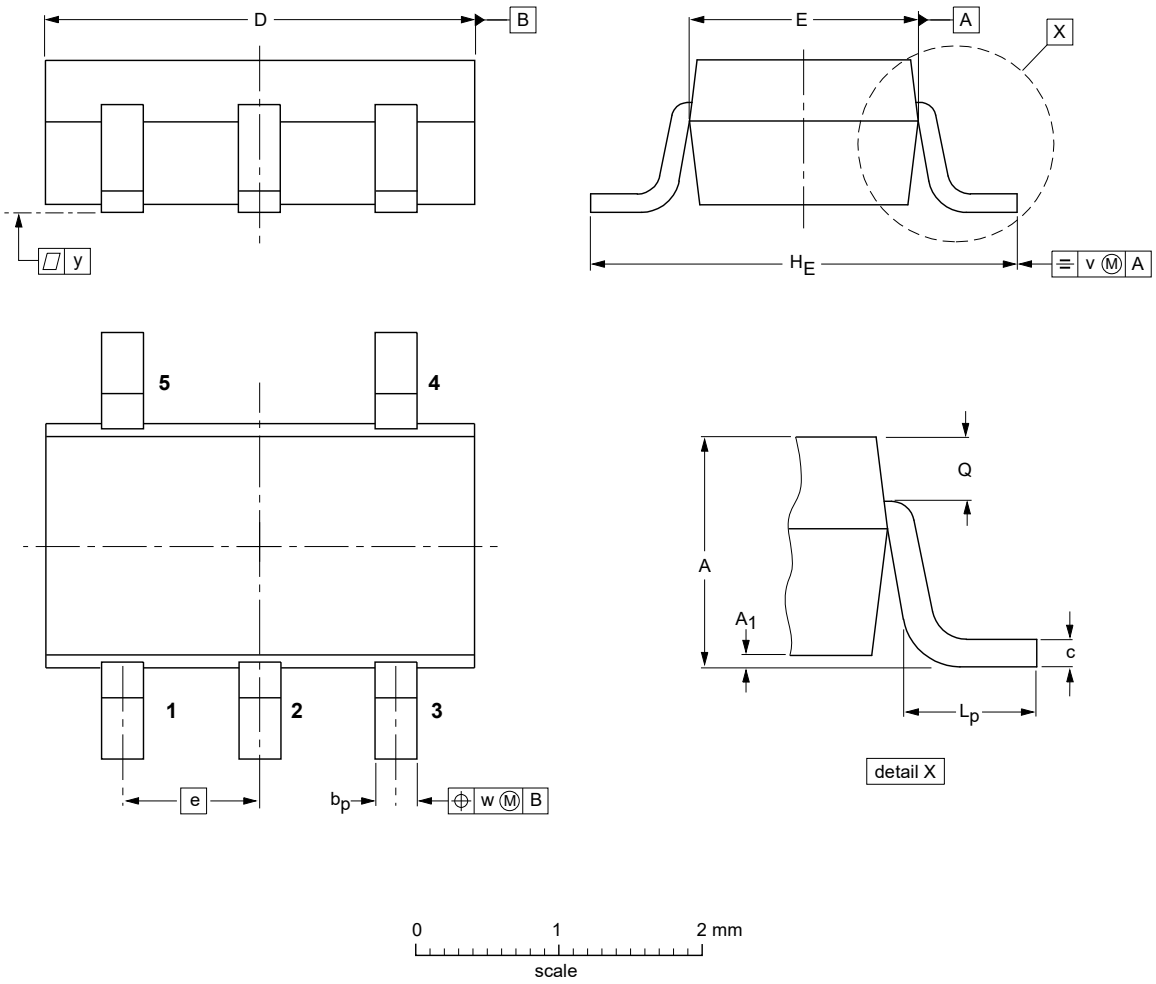
$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_{amb}}{\theta_{JA}}$$

Where:

$P_{D(MAX)}$ = maximum allowable power dissipation
$T_{J(MAX)}$ = maximum allowable junction temperature (125 °C for NPS4001)
$T_{amb}$ = ambient temperature of the device
$\theta_{JA}$ = junction to air thermal impedance. This parameter is highly dependent upon board layout.

# 16. Package outline

**Plastic surface-mounted package; 5 leads** **SOT753**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $b_p$ | c | D | E | e | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.9 | 0.100<br>0.013 | 0.40<br>0.25 | 0.26<br>0.10 | 3.1<br>2.7 | 1.7<br>1.3 | 0.95 | 3.0<br>2.5 | 0.6<br>0.2 | 0.33<br>0.23 | 0.2 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT753 | | | SC-74A | | | ~~02-04-16~~<br>06-03-16 |

**Fig. 22. Package outline SOT753 (SC-74A)**

# 17. Abbreviations

**Table 8. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

# 18. Revision history

**Table 9. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| NPS4001 v.1 | 20240425 | Product data sheet | - | - |

# 19. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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