



PMDPB30XNA

20 V, dual N-channel Trench MOSFET

12 February 2024

Product data sheet

1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a small and leadless ultra thin DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction
- AEC-Q101 qualified

3. Applications

- DC to DC conversion
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

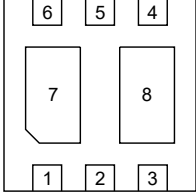
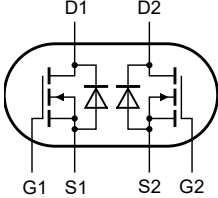
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	20	V
V_{GS}	gate-source voltage		-10	-	10	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	4.5	A
Static characteristics (per transistor)						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 4.5\text{ A}; T_j = 25\text{ °C}$	-	26	34	mΩ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>Transparent top view DFN2020-6 (SOT1118)</p>	 <p>017aaa254</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDPB30XNA	DFN2020-6	plastic, leadless thermal enhanced ultra thin small outline package; no leads; 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1118

7. Marking

Table 4. Marking codes

Type number	Marking code
PMDPB30XNA	8M

8. Limiting values

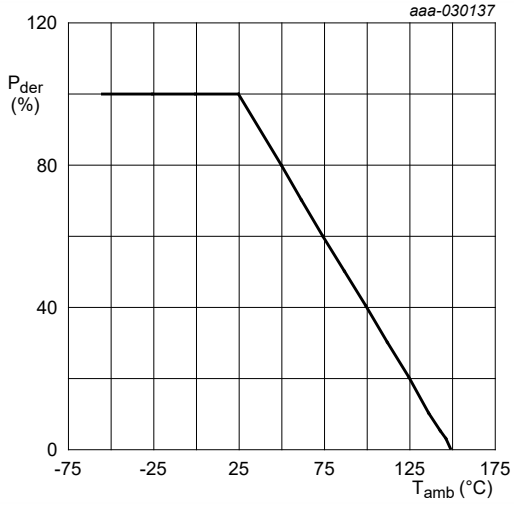
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	20	V
V_{GS}	gate-source voltage			-10	10	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	4.5	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	2.8	A
		$V_{GS} = 4.5\text{ V}; T_{sp} = 25\text{ °C}$		-	12	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	48	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	490	mW
			[1]	-	1.2	W
		$T_{sp} = 25\text{ °C}$		-	8.3	W
Per device						
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	640	mW
			[1]	-	1.6	W
		$T_{sp} = 25\text{ °C}$		-	11	W
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode (per transistor)						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	1.2	A
Avalanche ruggedness (per transistor)						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(init)} = 25\text{ °C}; I_D = 0.5\text{ A};$ DUT in avalanche (unclamped)		-	4.5	mJ

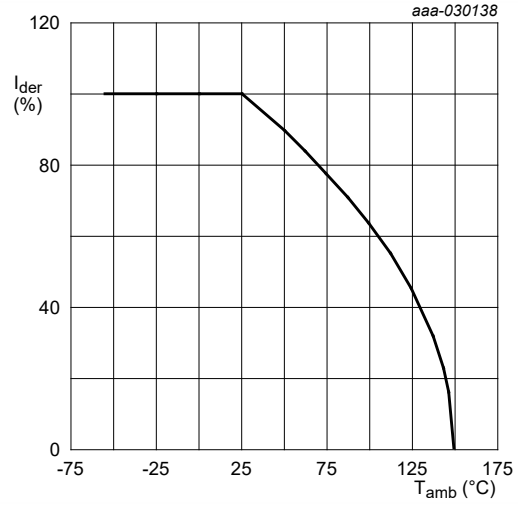
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm^2 .

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



$$P_{der} = \frac{P_{tot}}{P_{tot}(25^{\circ}\text{C})} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of ambient temperature



$$I_{der} = \frac{I_D}{I_D(25^{\circ}\text{C})} \times 100\%$$

Fig. 2. Normalized continuous drain current as a function of ambient temperature

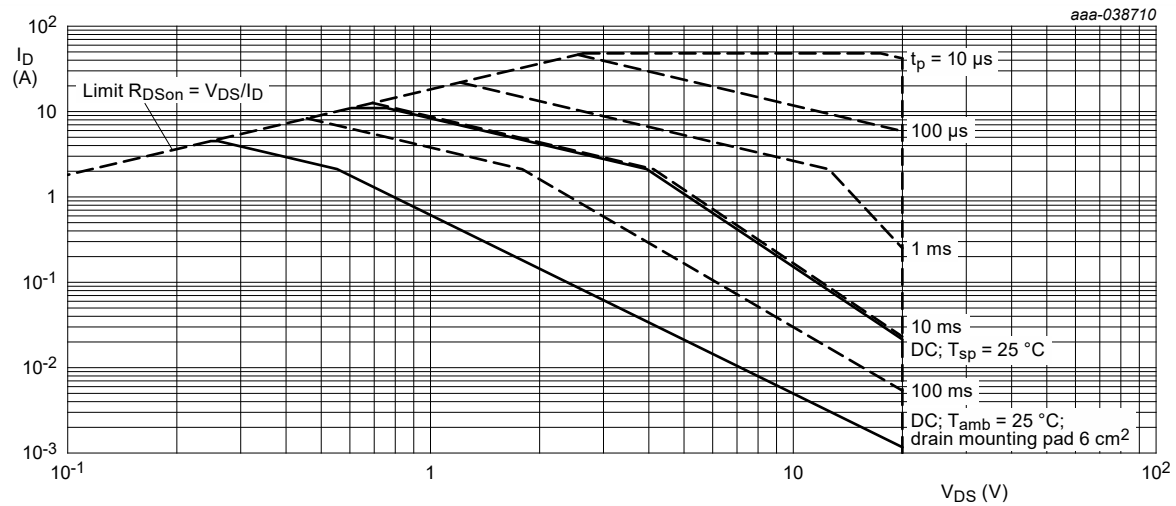


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

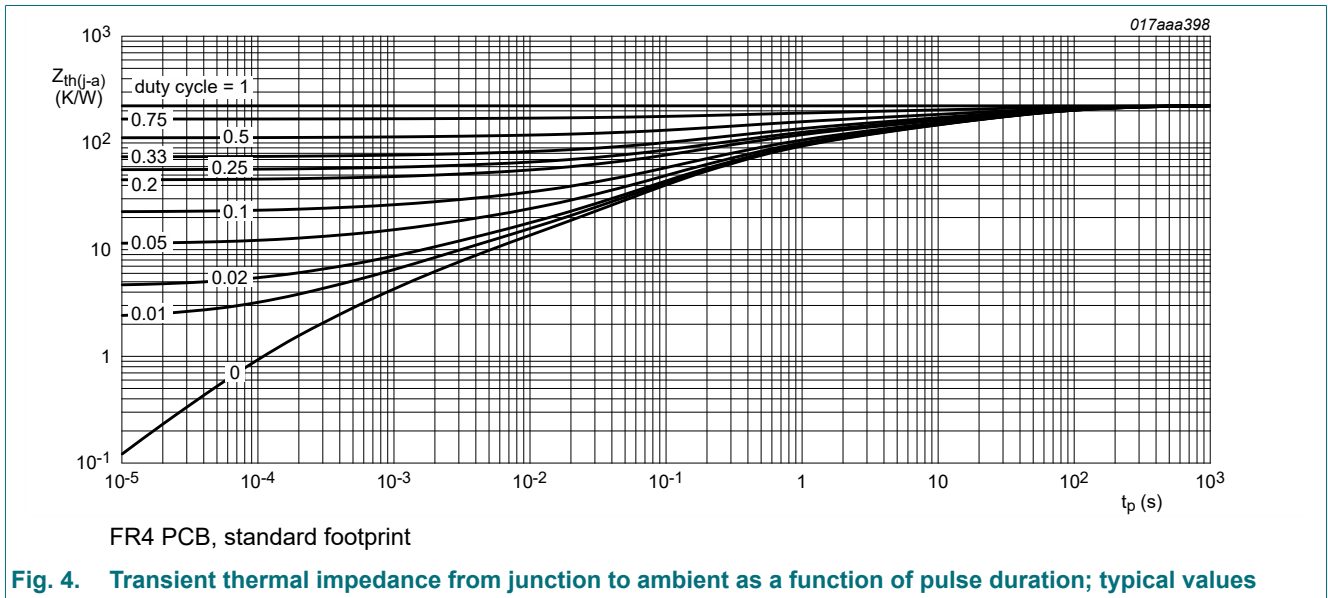
9. Thermal characteristics

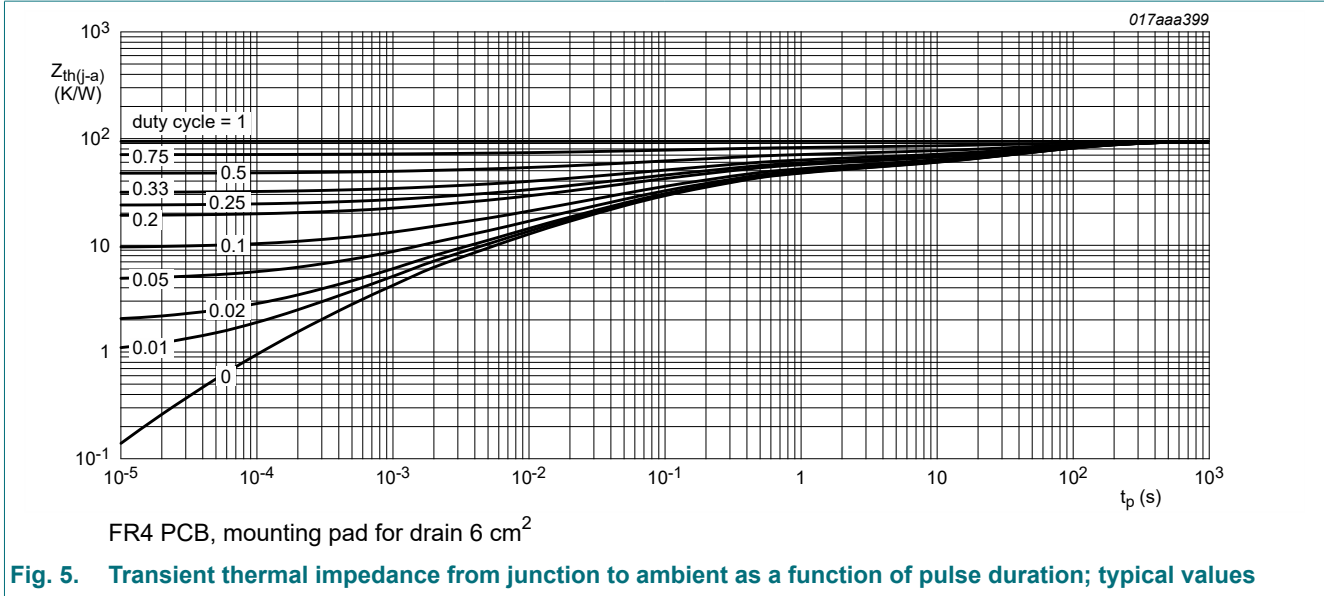
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	223	256	K/W
			[2]	-	93	107	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	10	15	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	190	K/W
			[2]	-	-	80	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	11	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².





10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics (per transistor)						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu\text{A}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ\text{C}$	0.4	0.65	0.9	V
I_{DSS}	drain leakage current	$V_{DS} = 20 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 10 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -10 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}$; $I_D = 4.5 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	26	34	m Ω
		$V_{GS} = 4.5 \text{ V}$; $I_D = 4.5 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$	-	42	55	m Ω
		$V_{GS} = 2.5 \text{ V}$; $I_D = 4 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	33	46	m Ω
		$V_{GS} = 1.8 \text{ V}$; $I_D = 0.5 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	50	80	m Ω
g_{fs}	forward transconductance	$V_{DS} = 10 \text{ V}$; $I_D = 4.3 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	8	-	S
R_G	gate resistance	$f = 1 \text{ MHz}$	-	8	-	Ω
Dynamic characteristics (per transistor)						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 10 \text{ V}$; $I_D = 4.3 \text{ A}$; $V_{GS} = 4.5 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	6.6	10	nC
Q_{GS}	gate-source charge		-	0.9	-	nC
Q_{GD}	gate-drain charge		-	1.5	-	nC
C_{iss}	input capacitance	$V_{DS} = 10 \text{ V}$; $f = 1 \text{ MHz}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	619	-	pF
C_{oss}	output capacitance		-	60	-	pF
C_{rss}	reverse transfer capacitance		-	53	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10 \text{ V}$; $I_D = 4.3 \text{ A}$; $V_{GS} = 4.5 \text{ V}$; $R_{G(ext)} = 6 \text{ } \Omega$; $T_j = 25 \text{ }^\circ\text{C}$	-	6.5	-	ns
t_r	rise time		-	2.3	-	ns
$t_{d(off)}$	turn-off delay time		-	10	-	ns
t_f	fall time		-	25	-	ns
Source-drain diode (per transistor)						
V_{SD}	source-drain voltage	$I_S = 1.2 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	0.7	1.2	V
t_{rr}	reverse recovery time	$I_S = 2 \text{ A}$; $di_S/dt = -75 \text{ A}/\mu\text{s}$; $V_{GS} = 4.5 \text{ V}$; $V_{DS} = 20 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	6.4	-	ns
Q_r	recovered charge		-	0.8	-	nC

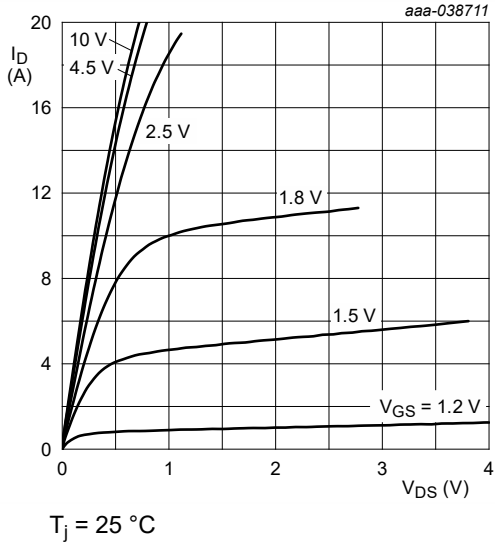


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

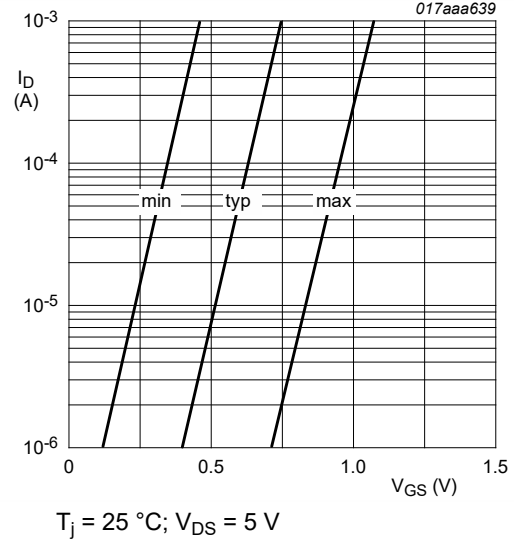


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

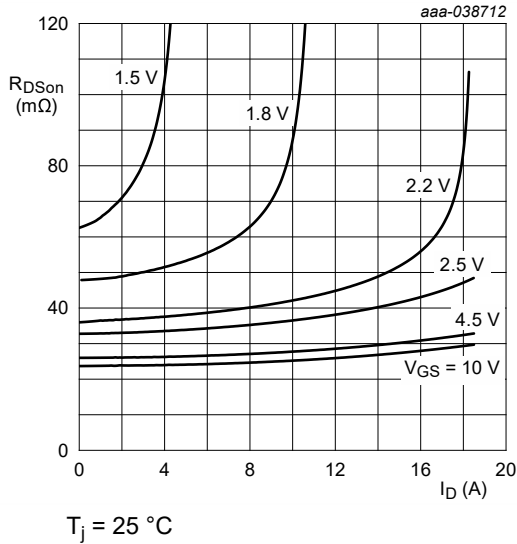


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

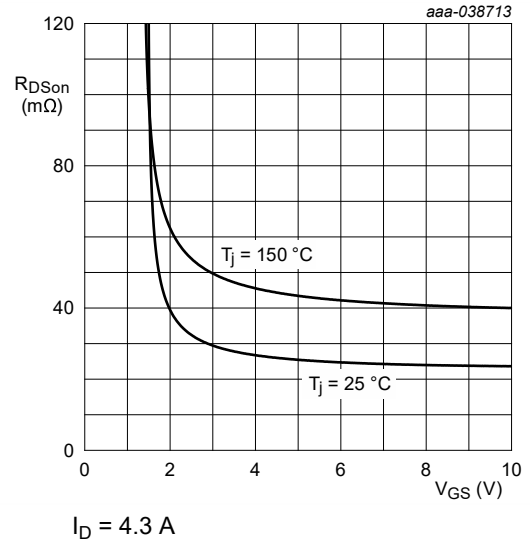


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

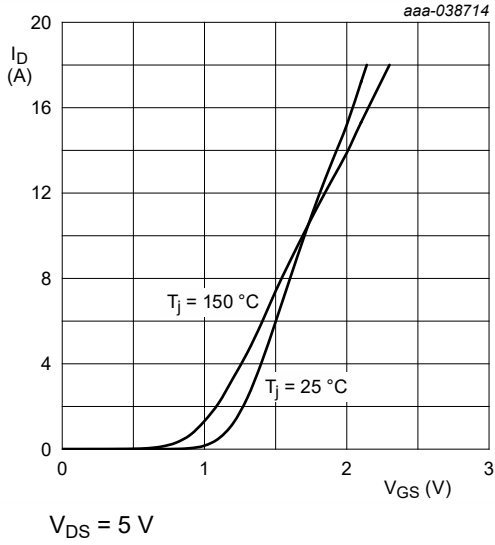


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

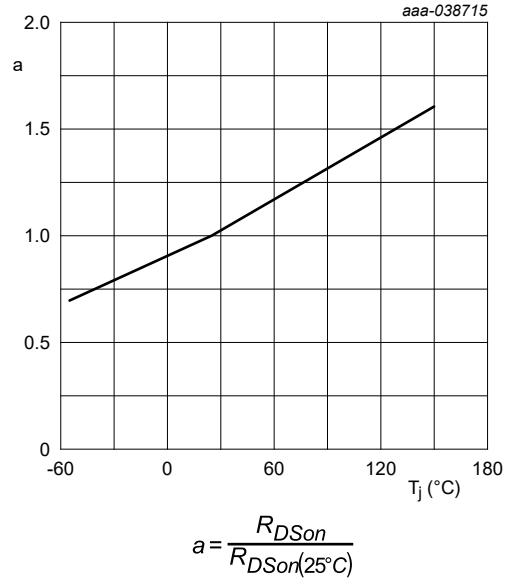


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

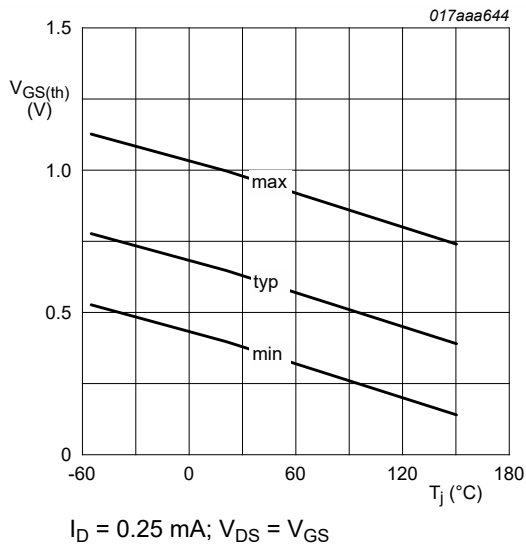


Fig. 12. Gate-source threshold voltage as a function of junction temperature

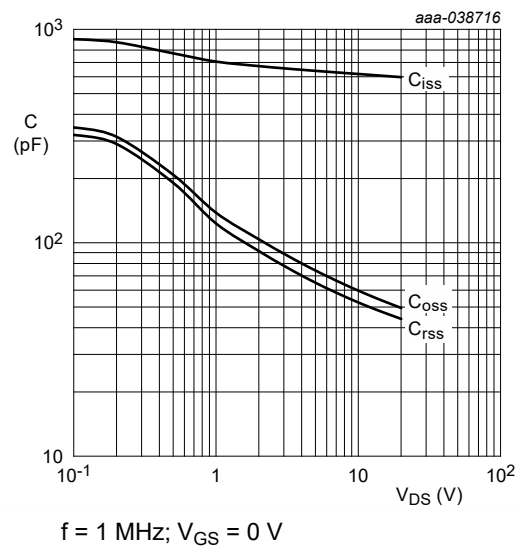
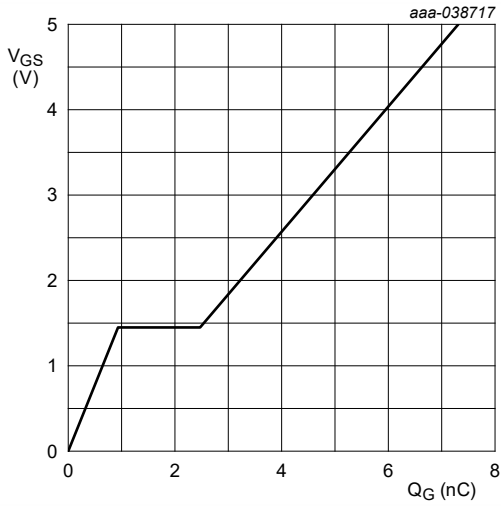


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 10\text{ V}; I_D = 4.3\text{ A}; T_j = 25\text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

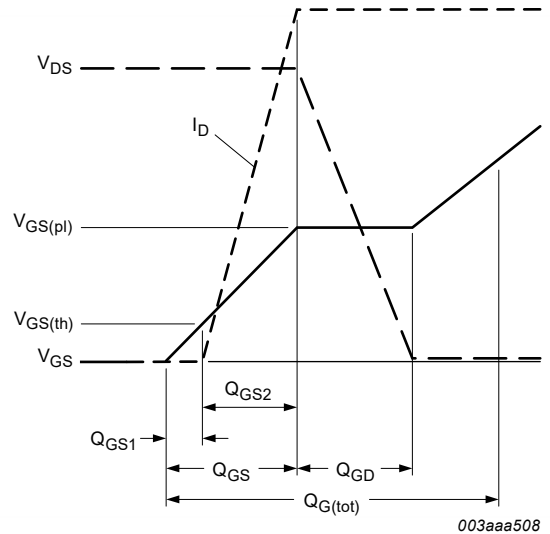
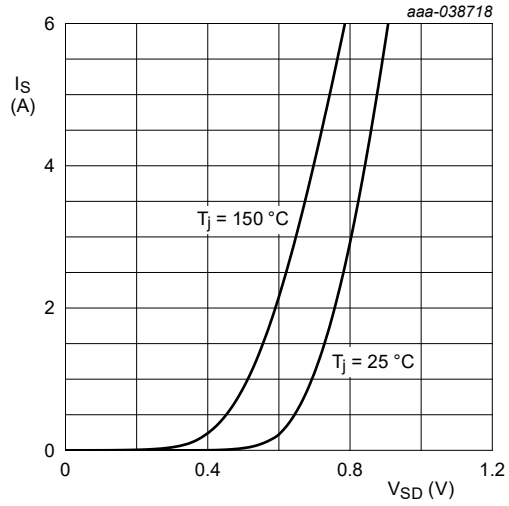


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

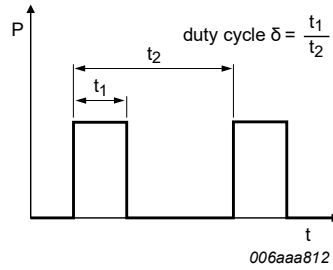


Fig. 17. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

HUSON6: plastic, thermal enhanced ultra thin small outline package; no leads;
6 terminals; body 2 x 2 x 0.65 mm

SOT1118

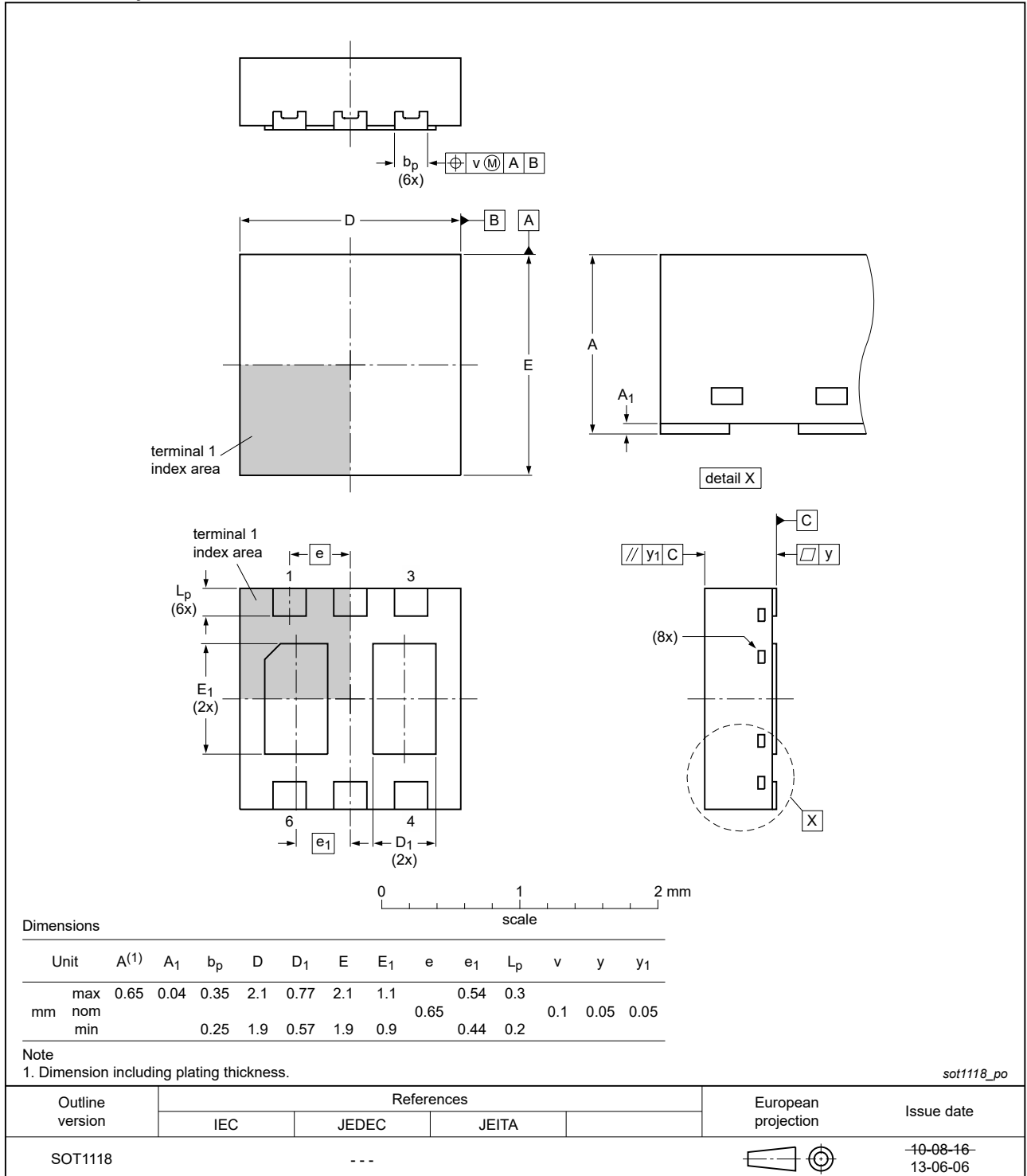


Fig. 18. Package outline DFN2020-6 (SOT1118)

13. Soldering

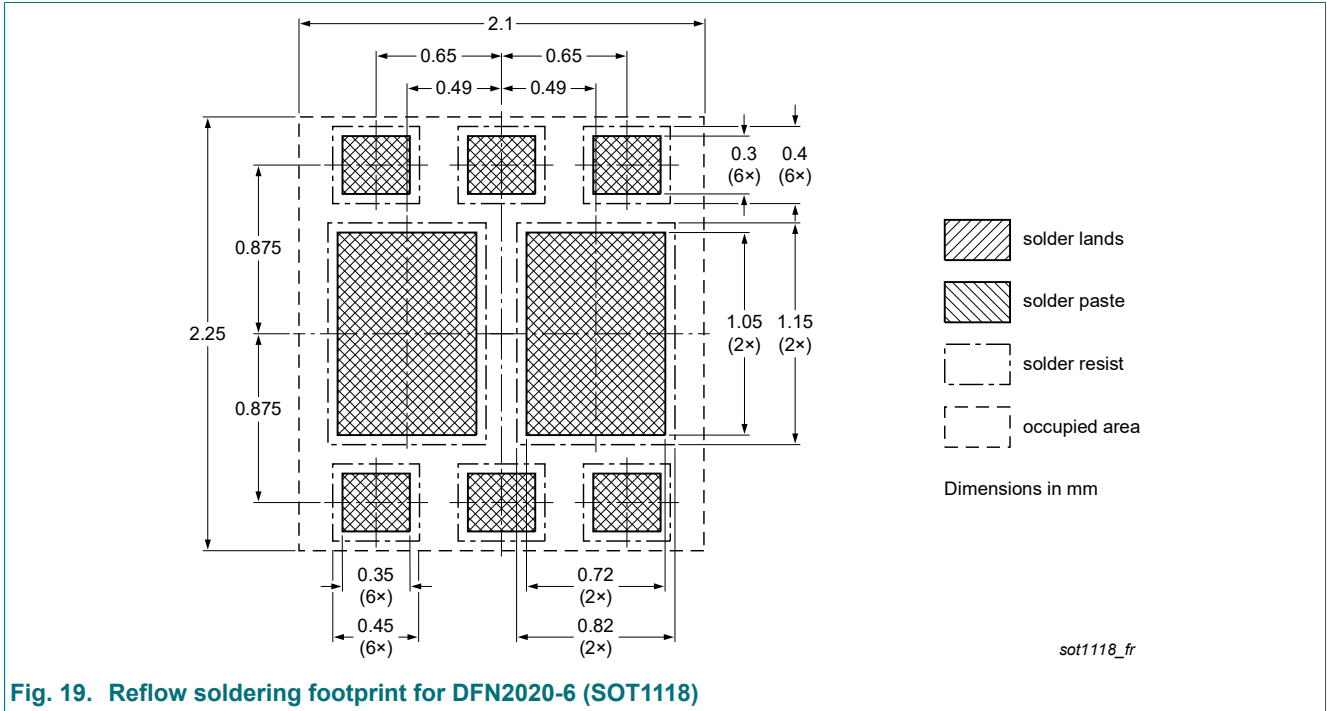


Fig. 19. Reflow soldering footprint for DFN2020-6 (SOT1118)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB30XNA v.2	20240212	Product data sheet	-	PMDPB30XNA v.1
Modifications:	• Chapter "Limiting values": Update of $E_{DS(AL)S}$			
PMDPB30XNA v.1	20240209	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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