MP5099

Dual-Channel Current Limit Switch with Current Monitor

DESCRIPTION

The MP5099 is a protection device that protects circuitry on the output from transients on the input. It also prevents undesired shorts at the input and transients from the output. The MP5099 is a small on resistance ($R_{DS(ON)}$), low quiescent current (I_Q), dual-channel current limit switch.

At start-up, the inrush current is limited by the slew rate at the output. The slew rate is controlled by a capacitor at the SS pin (C_{SS}). The maximum load at the output is current-limited. The current limit magnitude is internally fixed.

The output voltage (V_{OUT}) is limited by the over-voltage protection (OVP) function. The output current (I_{OUT}) of each rail can be monitored by a resistor connected to the IMON pins.

The MP5099 is available in a space-saving TQFN-10 (2mmx3mm) package.

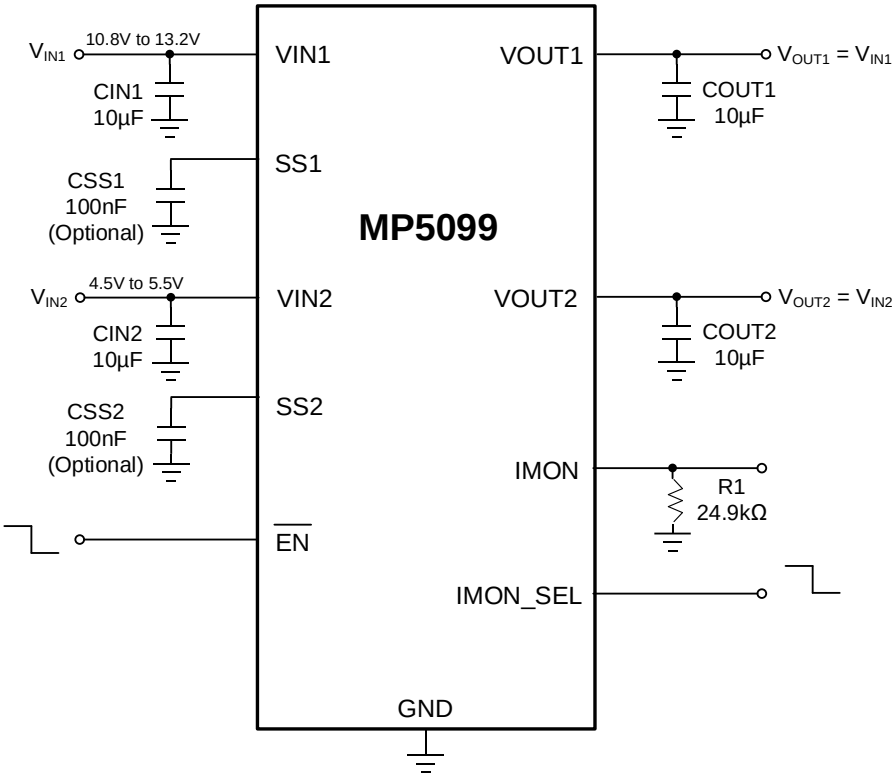
FEATURES

- Integrated 5V/12V Input Dual E-Fuse
- Up to 24V/100ms Maximum Input Voltage (V_{IN}) Surge Tolerance for 12V VIN Channel
- Up to 16V/100ms Maximum V_{IN} Surge Tolerance for 5V VIN Channel
- Integrated, Dual-Channel Current Limit Switch
- Low 40mΩ On Resistance ($R_{DS(ON)}$) for 12V V_{BUS} and 5V V_{BUS} Current Limit Switch
- 150μA Typical Low Quiescent Current (I_Q) for 12V VIN Channel and 130μA Low I_Q for 5V VIN Channel
- Configurable Soft-Start Time (t_{SS})
- Fixed 4A Trip and 2.95A Hold Current Limit for 12V VIN Channel
- Fixed 3A Trip and 2.2A Hold Current Limit for 5V VIN Channel
- Reverse Current Protection for 5V VIN Channel
- 5.7V Typical Over-Voltage Protection (OVP) Threshold for 5V VIN Channel
- 15V Typical OVP Threshold for 12V VIN Channel
- Over-Current Protection (OCP) in Hiccup Mode
- Latch-Off Thermal Shutdown
- Available in a TQFN-10 (2mmx3mm) Package

APPLICATIONS

- Hard Disk Drives (HHDs)
- Solid-State Drives (SSDs)
- Hot-Swap Applications

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5099GDT	TQFN-10 (2mmx3mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP5099GDT-Z).

TOP MARKING

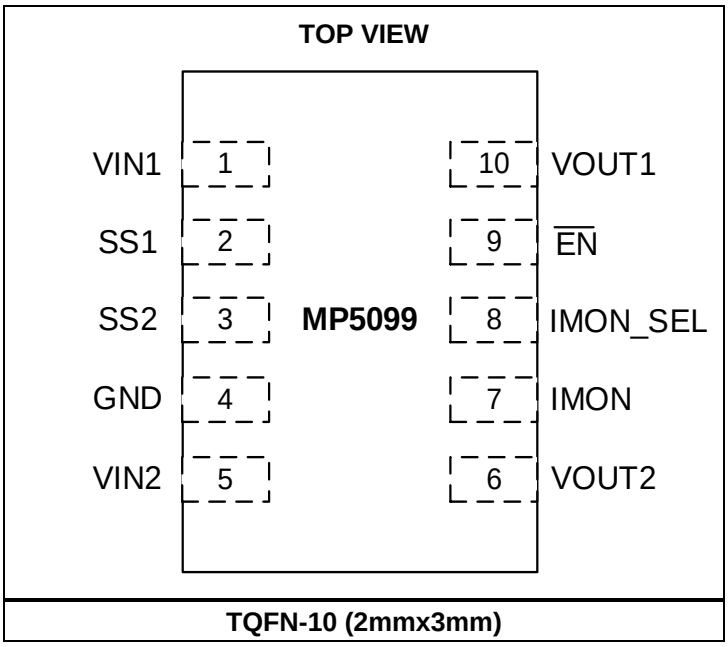
$\overline{\text{BNP}}$

YWW

LLLL

BNP: Product code of MP5099GDT
Y: Year code
WW: Week code
LLLL: Lot number

PACKAGE REFERENCE



TQFN-10 (2mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VIN1	**Channel 1 supply voltage.** The typical input voltage (V_{IN}) of channel 1 is 12V. A ceramic capacitor is required to decouple the input rail. Connect VIN1 using a wide PCB trace.
2	SS1	**Channel 1 soft start pin.** Connect a capacitor from SS1 to ground to set the soft-start time (t_{SS}).
3	SS2	**Channel 2 soft start pin.** Connect a capacitor from SS2 to ground to set t_{SS}.
4	GND	**System ground.**
5	VIN2	**Channel 2 supply voltage.** The typical V_{IN} of channel 2 is 5V. A ceramic capacitor is required to decouple the input rail. Connect VIN2 using a wide PCB trace.
6	VOUT2	**Channel 2 output terminal.**
7	IMON	**Current monitor pin.** Connect a resistor from IMON1 to ground to set the current monitor gain.
8	IMON_SEL	**Current monitor channel selection pin.** If IMON_SEL is pulled high, IMON detects the channel 1 output current (I_{OUT}). If IMON_SEL is floated or pulled low, IMON detects the channel 2 I_{OUT}.
9	$\overline{EN}$	**Enable pin for both channel 1 and channel 2.** $\overline{EN}$ is a digital input that turns the regulator on or off. Float $\overline{EN}$ or pull $\overline{EN}$ low to turn on the regulator; pull it high to turn off the regulator.
10	VOUT1	**Channel 1 output terminal.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN1}, V_{OUT1} .....-0.3V to +22V
Positive input transient (100ms CH1) 24V
V_{IN2}, V_{OUT2} .....-0.3V to +15V
Positive input transient (100ms CH2) 16V
EN .....-0.3V to +6.5V
All other pins .....-0.3V to +5V
Junction temperature ..... -40°C to +150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2) (4)
TQFN 3.1W

ESD Ratings

Human body model (HBM).....±2000V
Charged device model (CDM).....±2000V

Recommended Operating Conditions (3)

CH1 continuous voltage.....10.8V to 13.2V
CH2 continuous voltage.....4.5V to 5.5V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

TQFN-10 (2mmx3mm)		
EV5099-D-00A (4)	40	4 °C/W
JESD51-7 (5)	70	5 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EV5099-D-00A, a 2-layer PCB (54mmx46mm).
5) The θ_{JA} value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN1} = 12V, V_{IN2} = 5V, C_{OUT1} = C_{OUT2} = 10µF, T_J =-40°C to + 125°C (6), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent current	I_{Q_CH1}	$V_{\overline{EN}}$ = low		150		µA
	I_{Q_CH2}	$V_{\overline{EN}}$ = low		130		µA
Shutdown current	I_{SD_CH1}	$V_{\overline{EN}}$ = high		10		µA
	I_{SD_CH2}	$V_{\overline{EN}}$ = high		6.5		µA
Power FET						
On resistance	$R_{DS(ON)\_CH1}$	T_J = 25°C		40		mΩ
		T_J = 125°C			65	mΩ
	$R_{DS(ON)\_CH2}$	T_J = 25°C		40		mΩ
		T_J = 125°C			65	mΩ
Under-Voltage Protection (UVP) and Over-Voltage Protection (OVP)						
Under-voltage lockout (UVLO) rising threshold	V_{UVLO_CH1}		7.7	8.5	9.3	V
	V_{UVLO_CH2}		3.8	4.0	4.2	V
UVLO hysteresis	$V_{UVLO\_HYS\_CH1}$			800		mV
	$V_{UVLO\_HYS\_CH2}$			0.3		V
Output over-voltage (OV) clamp voltage	V_{OVLO_CH1}		13.8	15	16	V
	V_{OVLO_CH2}		5.5	5.7	6.2	V
Output OV response time (7)	$t_{OUT\_OV\_CH1}$	C_{OUT} = 10µF, add a 30Ω load resistor, V_{IN1} = 12V to 18V/10µs		2		µs
	$t_{OUT\_OV\_CH2}$	C_{OUT} = 10µF, add a 10Ω load resistor, V_{IN2} = 5V to 7V/10µs		2		µs
Current Limit						
Current limit at normal operation	$I_{LIMIT\_NO\_CH1\_TRIP}$		-10%	4	+10%	A
	$I_{LIMIT\_NO\_CH2\_TRIP}$		-10%	3	+10%	A
	$I_{LIMIT\_SC\_CH1\_HOLD}$			2.95		A
	$I_{LIMIT\_SC\_CH2\_HOLD}$			2.2		A
Current limit response time (7)	t_{CL_CH1}			15		µs
	t_{CL_CH2}			15		µs
Secondary current limit (7)	$I_{LIMIT\_H\_CH1}$			8		A
	$I_{LIMIT\_H\_CH2}$			8		A
Hiccup mode on time	t_{HICP_ON}			2		ms
Hiccup mode off time	t_{HICP_OFF}			200		ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, C_{OUT1} = C_{OUT2} = 10µF, T_J =-40°C to + 125°C (6), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Current Monitor						
Current monitor sense gain	G_{IMON_CH1}		26.1	28	30.6	µA/A
	G_{IMON_CH2}		26.5	29	33	µA/A
Current monitor sense offset	I_{OFFSET_CH1}		0.7	1.9	3.1	µA
	I_{OFFSET_CH2}		0.9	2	3.2	µA
Current monitor voltage range	V_{IMON1}	R_{IMON} = 24.9kΩ	0		2.4	V
	V_{IMON2}	R_{IMON} = 24.9kΩ	0		2.2	V
Enable (EN) Control						
$\overline{EN}$ falling threshold	$V_{\overline{EN}\_FALLING}$		0.92	1	1.08	V
$\overline{EN}$ hysteresis	$V_{\overline{EN}\_HYS}$			0.22		V
$\overline{EN}$ pull-down resistance	$R_{\overline{EN}\_PD}$			0.8		MΩ
Soft Start (SS)						
SS current	I_{SS_CH1}		3.7	4.8	7	µA
	I_{SS_CH2}		3.8	4.8	7	µA
SS time	t_{SS_FLOAT}			12		ms
Over-Temperature Protection (OTP)						
Thermal shutdown (7)	T_{SD}			150		°C

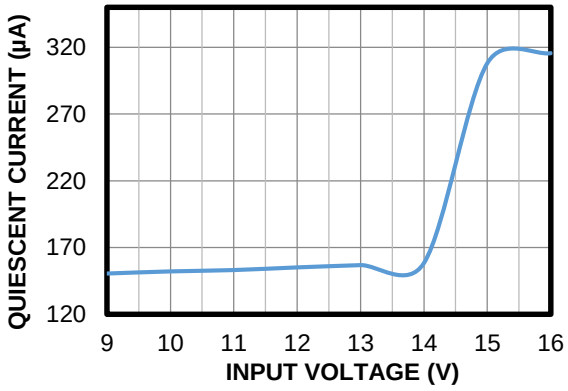
Notes:

6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by design and engineering sample characterization.

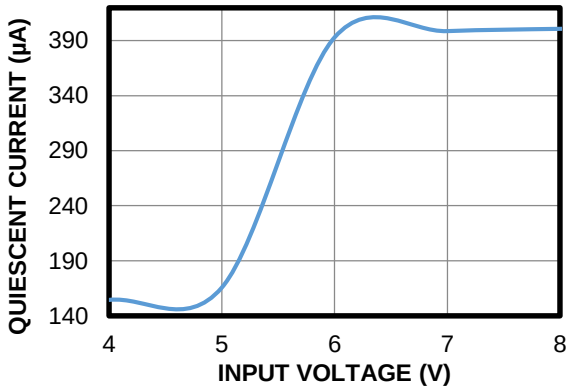
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

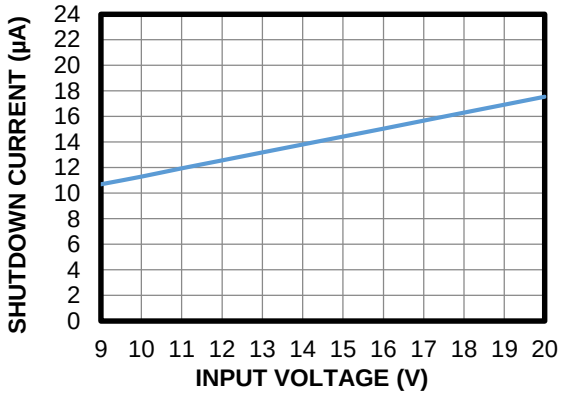
Quiescent Current vs. Input Voltage (12V E-Fuse)



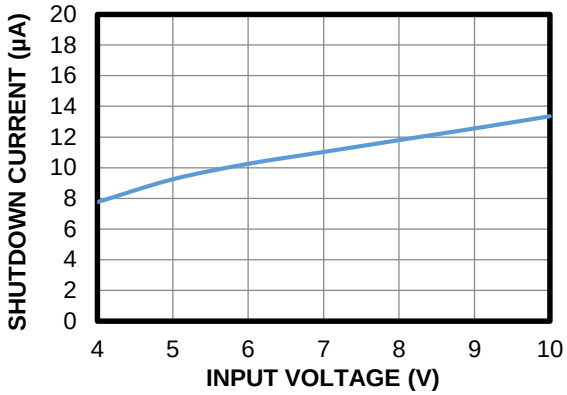
Quiescent Current vs. Input Voltage (5V E-Fuse)



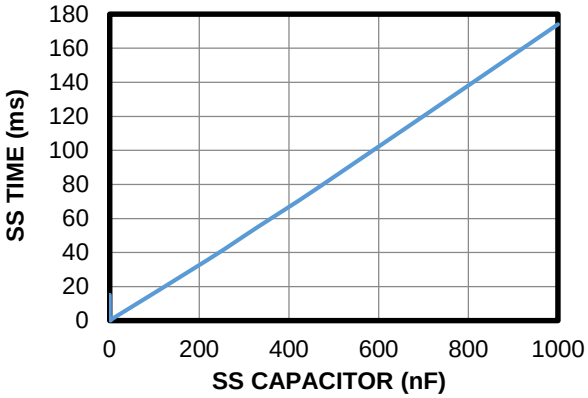
Shutdown Current vs. Input Voltage (12V E-Fuse)



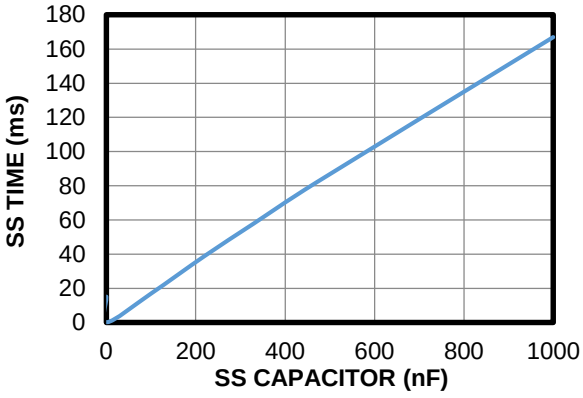
Shutdown Current vs. Input Voltage (5V E-Fuse)



SS Time vs. SS Capacitor (12V E-Fuse)



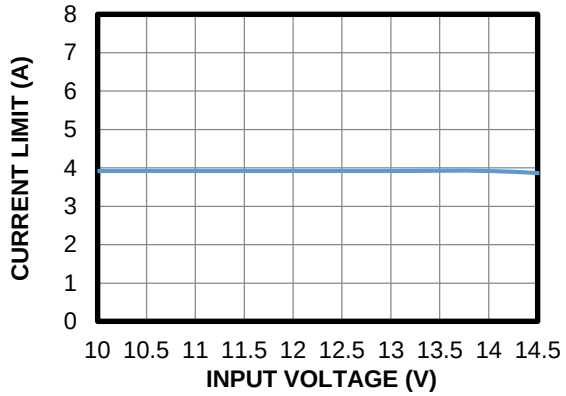
SS Time vs. SS Capacitor (5V E-Fuse)



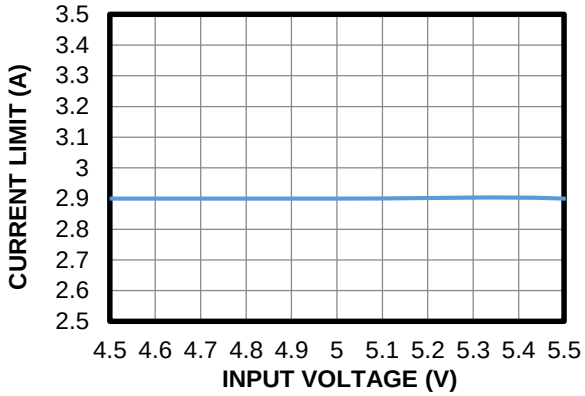
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

Current Limit vs. Input Voltage (12V E-Fuse)

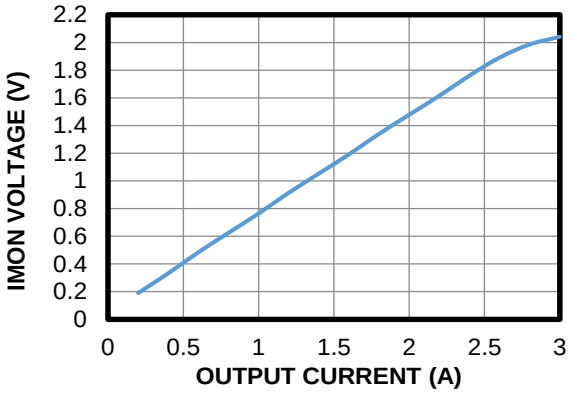


Current Limit vs. Input Voltage (5V E-Fuse)



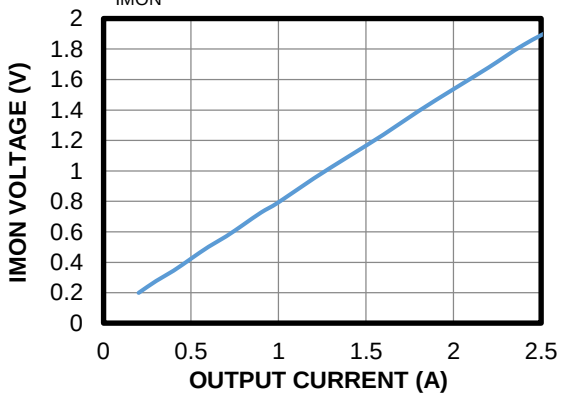
IMON Voltage vs. Output Current (12V E-Fuse)

R_{IMON} = 24.9kΩ



IMON Voltage vs. Output Current (5V E-Fuse)

R_{IMON} = 24.9kΩ

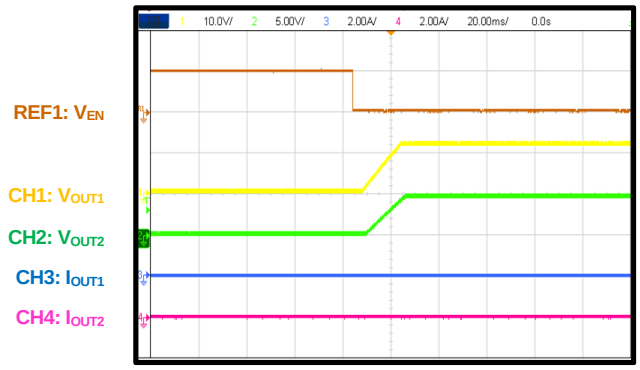


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

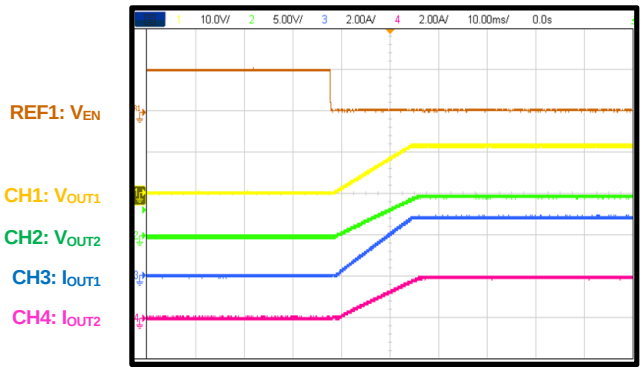
CH1/CH2 EN On Logic

I_{OUT1} = I_{OUT2} = 0A



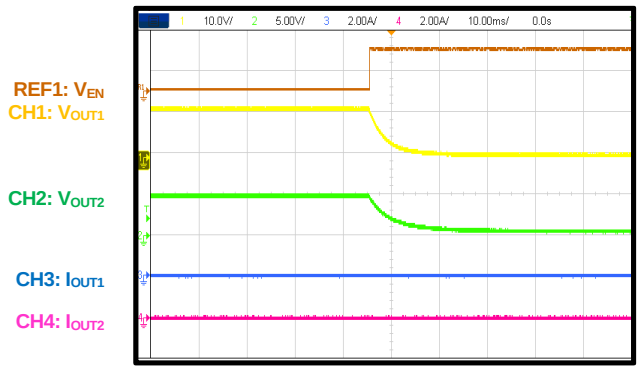
CH1/CH2 EN On Logic

I_{OUT1} = 3A, I_{OUT2} = 2A



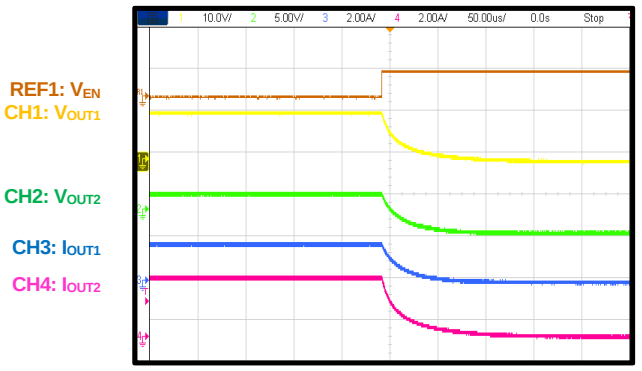
CH1/CH2 EN Off Logic

I_{OUT1} = I_{OUT2} = 0A



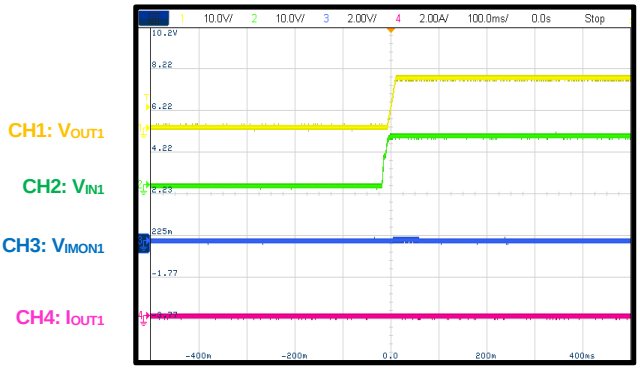
CH1/CH2 EN Off Logic

I_{OUT1} = 3A, I_{OUT2} = 2A



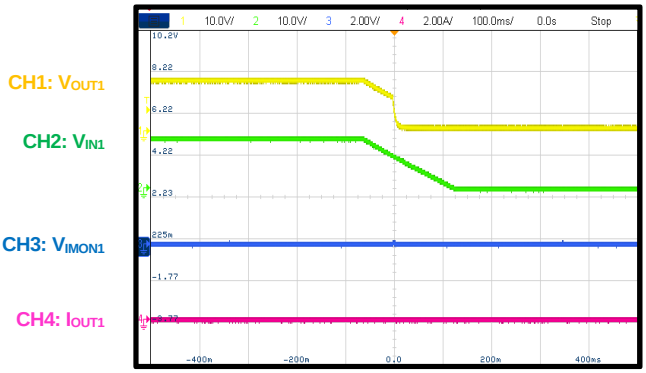
Start-Up through VIN1 without Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



Shutdown through VIN1 without Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A

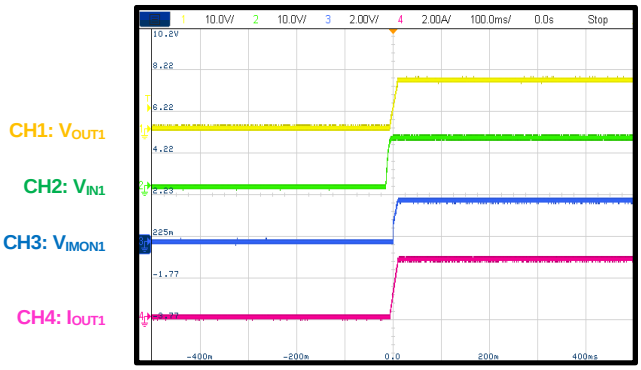


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

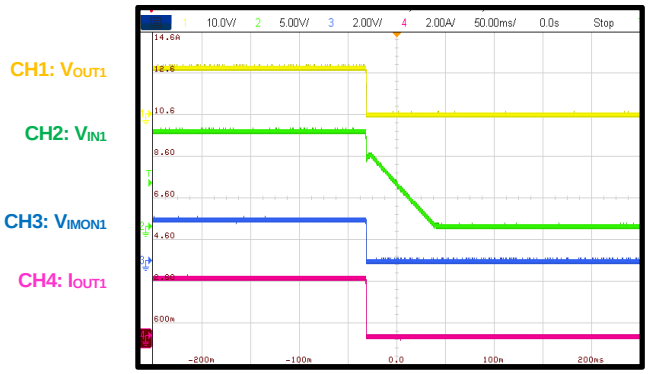
Start-Up through VIN1 with 3A Load (12V E-Fuse)

I_{OUT1} = 3A, V_{IN2} = 5V



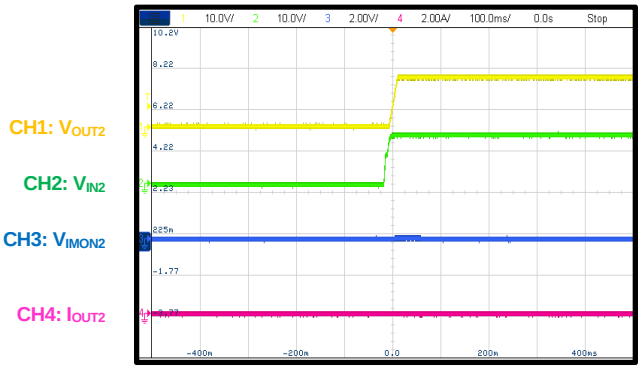
Shutdown through VIN1 with 3A Load (12V E-Fuse)

I_{OUT1} = 3A, V_{IN2} = 5V



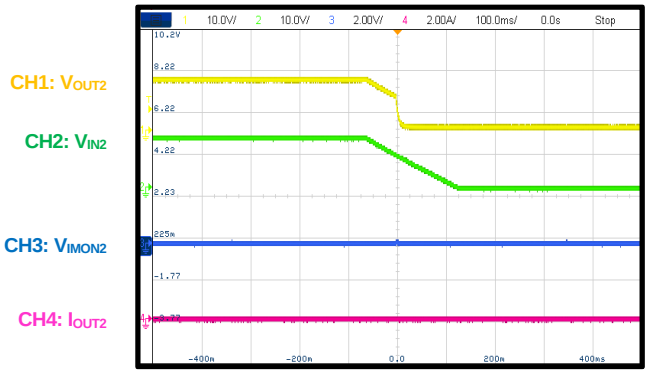
Start-Up through VIN2 without Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



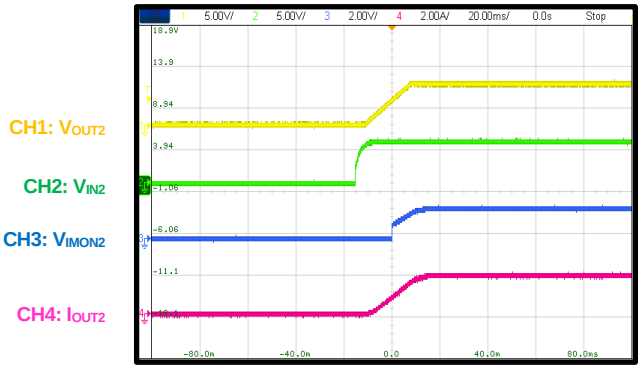
Shutdown through VIN2 without Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



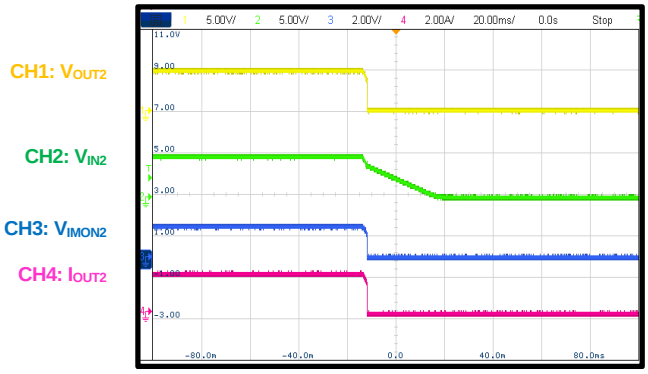
Start-Up through VIN2 with 2A Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A



Shutdown through VIN2 with 2A Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A

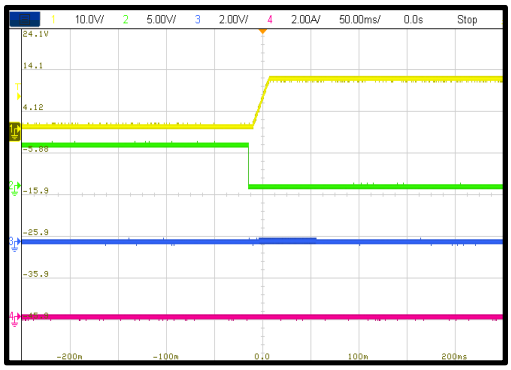


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

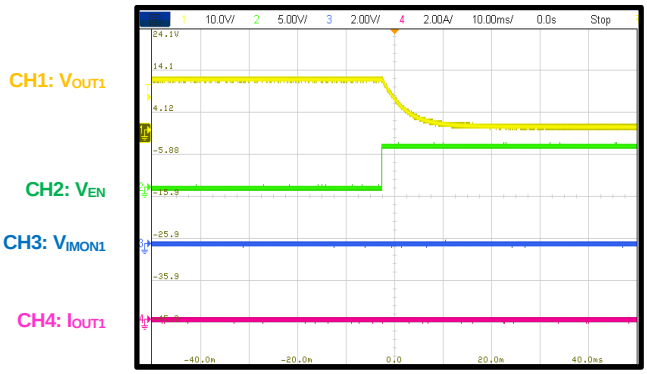
Start-Up through EN without Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



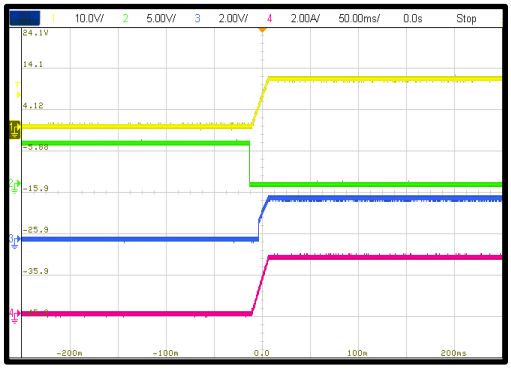
Shutdown through EN without Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



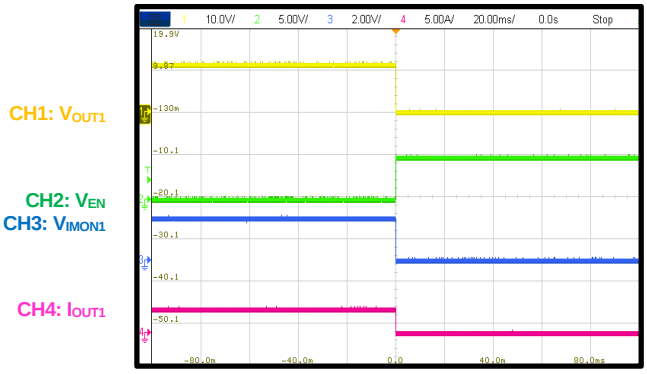
Start-Up through EN with 3A Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



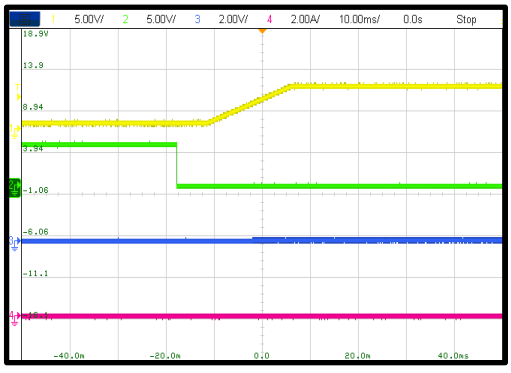
Shutdown through EN with 3A Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



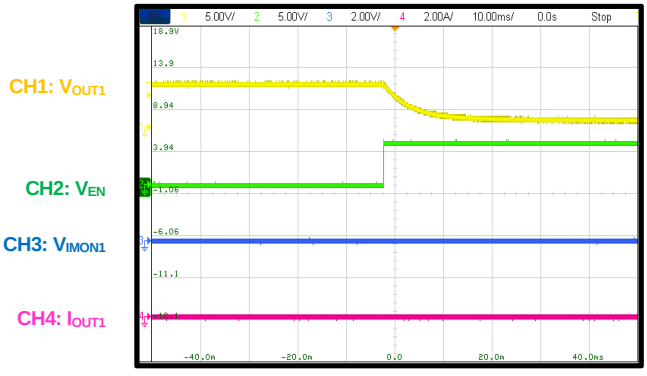
Start-Up through EN without Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



Shutdown through EN without Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A

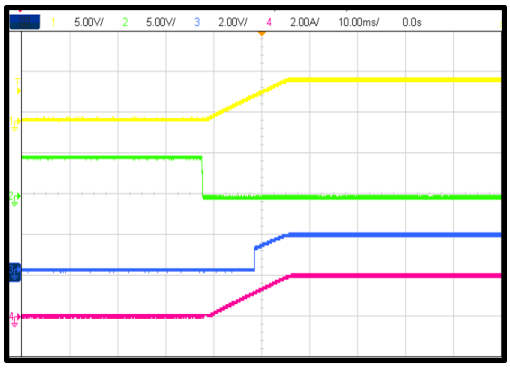


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

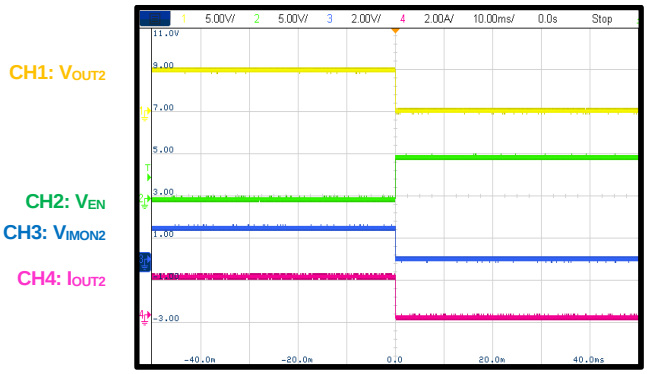
Start-Up through EN with 2A Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A

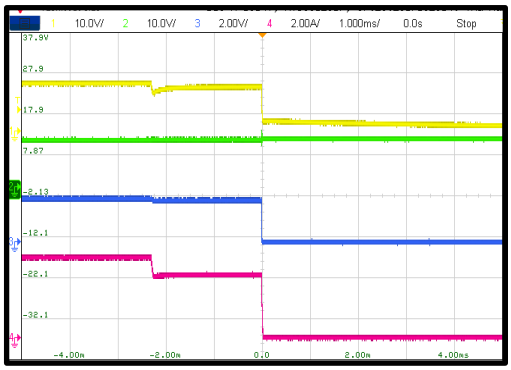


Shutdown through EN with 2A Load (5V E-Fuse)

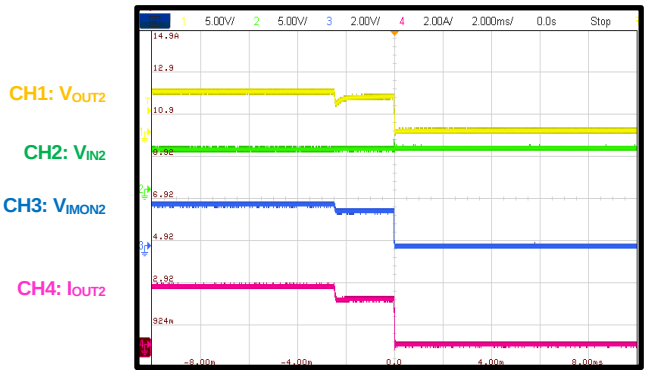
V_{IN1} = 12V, I_{OUT2} = 2A



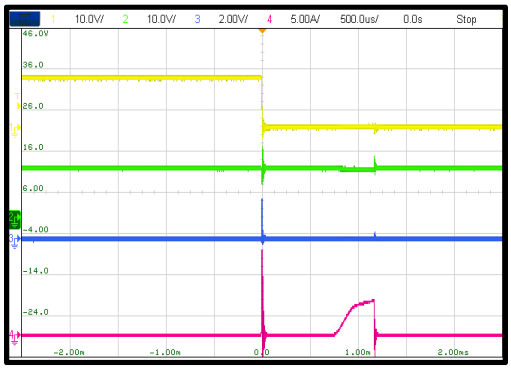
Current Limit (12V E-Fuse)



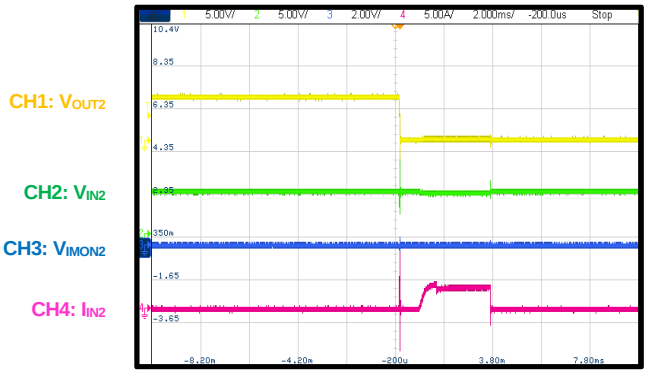
Current Limit (5V E-Fuse)



Short-Circuit Entry (12V E-Fuse)



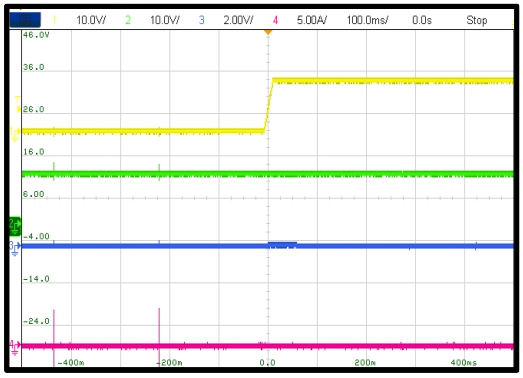
Short-Circuit Entry (5V E-Fuse)



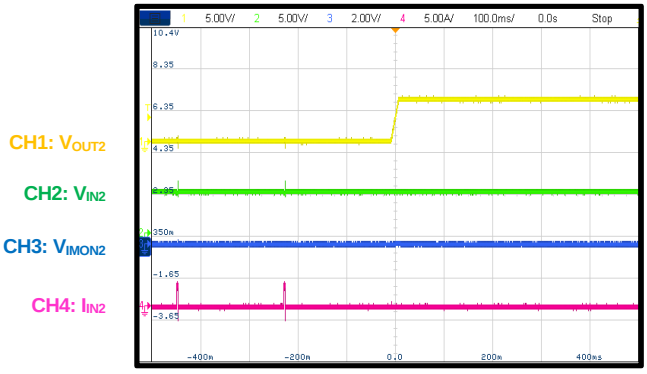
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

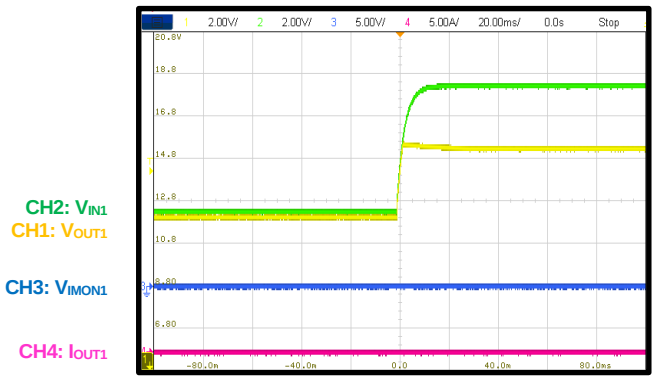
Short-Circuit Recovery (12V E-Fuse)



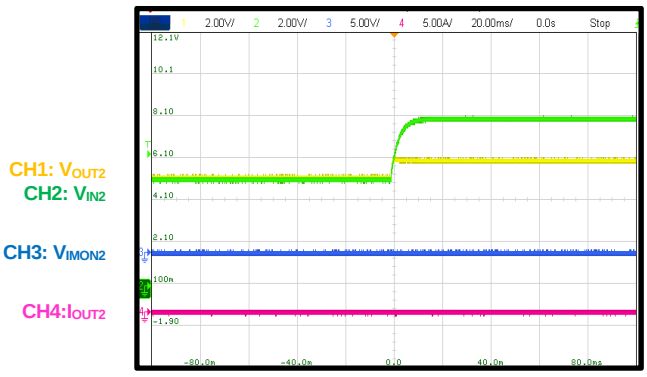
Short-Circuit Recovery (5V E-Fuse)



Output Over-Voltage Protection (12V E-Fuse)



Output Over-Voltage Protection (5V E-Fuse)



FUNCTIONAL BLOCK DIAGRAM

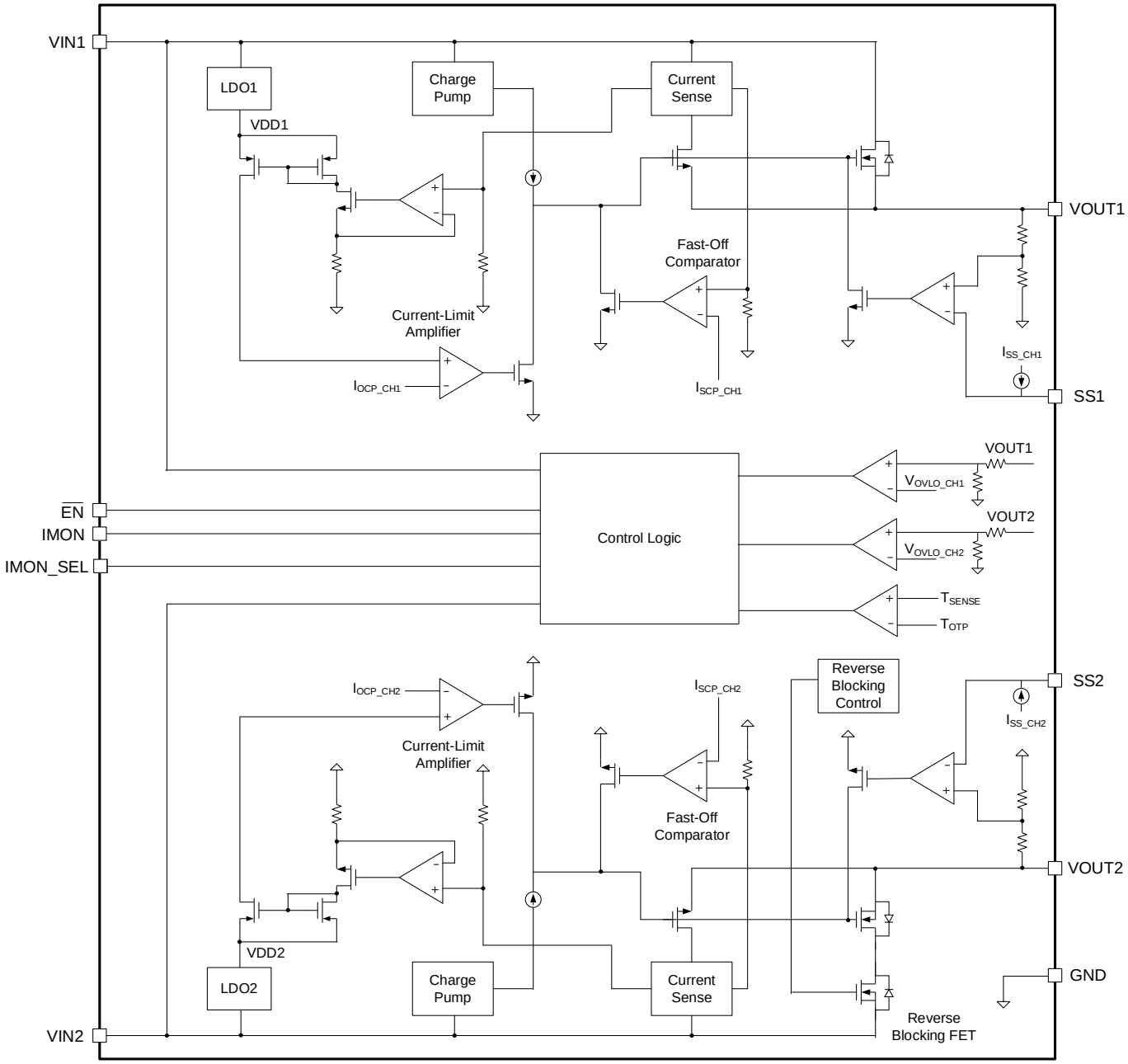


Figure 1: Functional Block Diagram

OPERATION

The MP5099 is a dual-channel current limit switch that limits the inrush current to the load when a circuit card inserts into a live backplane power source. This limits the backplane's voltage drop as well as the dv/dt of the voltage to the load. It offers an integrated solution to monitor the input voltage (V_{IN}), output voltage (V_{OUT}), output current (I_{OUT}), and die temperature, eliminating the requirement of an external current-sense power resistor, power MOSFET, and thermal sense device.

The MP5099 employs reverse current block function in the 5V channel. If the e-fuse 2 reverse current reaches the reverse protection current threshold, then only the 5V channel turns off.

Under-Voltage Lockout (UVLO)

The MP5099's channel 1 can be used in the 12V input supply system, and channel 2 can be used in the 5V input supply system. High energy transients occur during normal operation or during hot swap. These transients depend on the parasitic inductance and resistance of the wire, as well as a capacitor at the VCC node. If a power clamp (e.g. TVS or TransZorb) diode is not used, then the e-fuse must be able to withstand the transient voltage. The MP5099 integrates a high-voltage MOSFET and also uses a high-voltage circuit for the VCC node to guarantee safe operation.

If each channel's input supply falls below the under-voltage lockout (UVLO) threshold, then both channels' outputs shut down. Once both supplies exceed the UVLO threshold, the output of the two channels are enabled.

Soft Start (SS)

Connect a capacitor to the SS pin to set the soft-start time (t_{SS}). A constant current source charges the SS capacitor (C_{SS}) and results in a linear ramping voltage on the SS pin. V_{OUT} rises at a similar slew rate to the SS voltage (V_{SS}).

t_{SS} is a function of C_{SS}. The soft-start time from 0% to 100% V_{OUT} ($t_{DV/DT}$) can be calculated with Equation (1):

$$t_{DV/DT}(ms) = \frac{1V \times C_{SS}(nF)}{I_{SS}} \quad (1)$$

Where I_{SS} is the soft-start current, and 1V is the internal reference voltage (V_{REF}). Once the SS pin is charged up to 1V, soft start finishes.

When floating the SS pin, the default t_{SS} is 12ms typically.

Fast Output Over-Voltage Protection (OVP)

To protect downstream loading when a surge voltage occurs at the input, the MP5099 provides output over-voltage protection (OVP). An accurate and fast comparator monitors the output's over-voltage (OV) condition. If V_{OUT} exceeds the threshold, the internal MOSFETs' gate is quickly pulled down and regulated to a set value to maintain V_{OUT} clamped at the OVP threshold. The fast loop response speed (2µs typical) keeps the OV overshoot minimal.

Current Limit

When the MP5099 is active, if each load reaches the trip current threshold (the current triggers over-current protection) or a short is present, then both channels' outputs shut down and the part switches to constant-current (hold current) mode. If the over-current (OC) condition remains for longer than 2ms, the MP5099 enters hiccup protection mode. The IC automatically restarts after a 200ms off time and repeats this operation until the OC condition is released.

Channel 1's trip current is set to 4A internally, and its hold current is set to 2.95A. Channel 2's trip current is set to 3A internally, and its hold current is set to 2.2A.

Current Monitor

The MP5099 provides a current monitor function for channel 1 and channel 2. The MP5099 uses the IMON_SEL pin to select the I_{OUT} monitor channel. Pull IMON_SEL high to monitor channel 1's I_{OUT}. Float IMON_SEL or pull IMON_SEL low to monitor channel 2. The IMON pin generates a current proportional to channel 1 and channel 2's load current. Connect a resistor (R_{IMON}) to IMON to generate the current monitor voltage (V_{IMON}). The effective V_{IMON} range that guarantees sensing linearity depends on the R_{IMON} value, and V_{IMON} is clamped when I_{OUT} exceeds a set value.

Table 1 shows the recommended IMON resistances for common IMON clamp voltages. When R_{IMON} = 24.9kΩ, V_{IMON1} is 2.15V and V_{IMON2} is 1.88V, typically.

Table 1: IMON Resistor Selection for Common IMON Clamp Voltages

V_{IMON1} (V)	V_{IMON2} (V)	R_{IMON} (kΩ)
2.57	2.46	40.2(1%)
2.31	2.15	30(1%)
2.15	1.88	24.9(1%)
1.16	0.76	10(1%)

V_{IMON} can be calculated using Equation (2):

$$V_{IMONx}(mV) = G_{IMON\_CHX}(uA/A) \times I_{OUT}(A) \times R_{IMON}(k\Omega) + I_{OFFSET\_CHX}(uA) \times R_{IMON}(k\Omega) \quad (2)$$

Where G_{IMON_CHX} is the current monitor sense gain, R_{IMON} is the current monitor sense resistor, and I_{OFFSET_CHX} is the current monitor sense offset. x = 1 or 2, depending on the channel.

When the MP5099 works in sleep mode or I_{OUT} is below 150mA, the current monitor is disabled.

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short-circuit event, the current may exceed the current limit threshold before the control loop is able to respond. If the current reaches a secondary current limit level of 8A, a fast turn-off circuit activates to turn off the power FET (see Figure 1 on page 14). The fast turn-off circuit helps limit the peak current through the switch, which prevents V_{IN} from dropping drastically. The total short circuit response time is shorter than 1µs. After the FET switches off, the part restarts. During the restart process, if the short still exists, the MP5099 regulates the gate voltage to hold the current at a normal current limit level. The IC enters hiccup mode with a 200ms off time.

Enable ($\overline{EN}$) Control

$\overline{EN}$ is a digital control pin that turns the current limit switch on and off. Pull $\overline{EN}$ low or float $\overline{EN}$ to turn on the FETs; pull $\overline{EN}$ high to turn off the FETs. An internal 800kΩ resistor is connected from $\overline{EN}$ to GND.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If each channel triggers over-temperature protection (OTP), then both channels' outputs shut down. Once the silicon die temperature exceeds 150°C, the whole chip shuts down.

APPLICATION INFORMATION

Design Example

Table 2 shows a design example following the application guidelines for the specifications below.

Table 2: Design Example

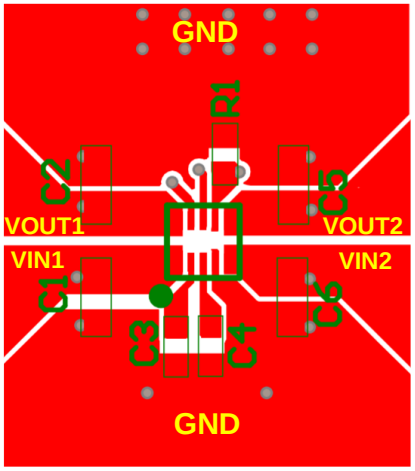
V_{IN1}	V_{OUT1}	V_{IN2}	V_{OUT2}
12V	12V	5V	5V

Figure 3 on page 18 shows the detailed application circuit. The typical performance and waveforms are shown in the Typical Performance Characteristics section on page 7. For more device applications, refer to the EV5099-D-00A datasheet.

PCB Layout Guidelines

Efficient PCB layout is critical for improved performance. For the best results, refer to Figure 2 and follow the guidelines below:

1. Place the high-current paths (VIN and VOUT) close to the device using short, direct, and wide traces.
2. Place the input capacitors close to the VIN and GND pins.
3. Connect the VIN and VOUT pads to large VIN and VOUT planes, respectively, to improve thermal performance.
4. Place C_{SS} close to the SS pin.



Top Layer

Figure 2: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

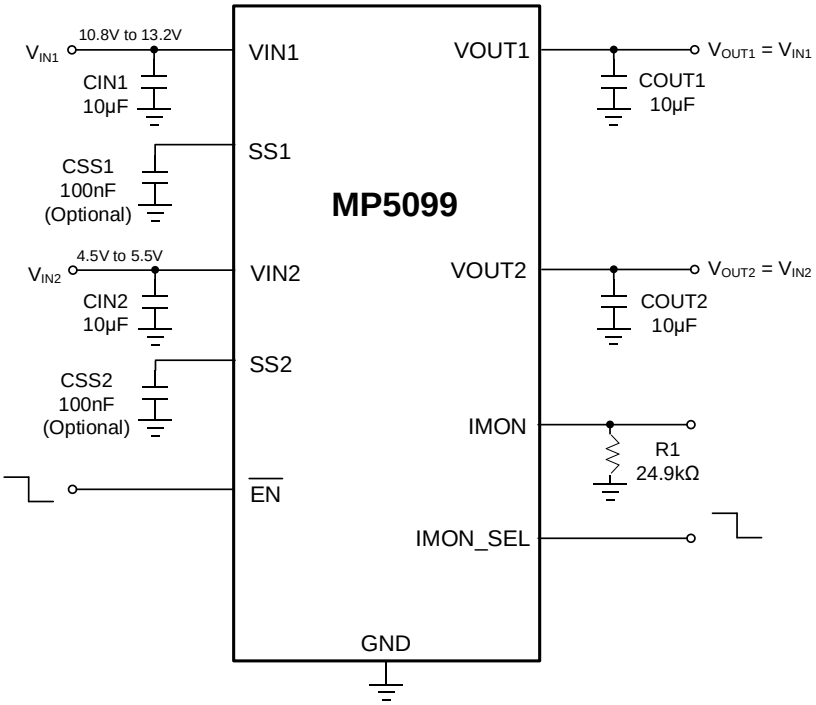
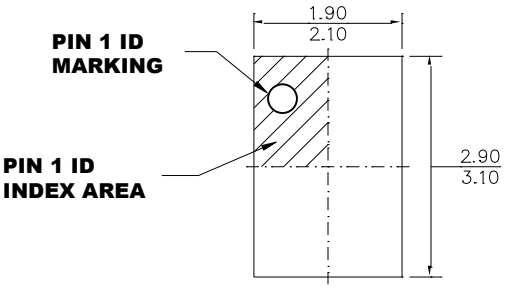


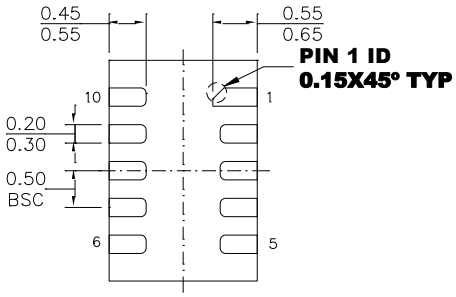
Figure 3: Typical Application Circuit

PACKAGE INFORMATION

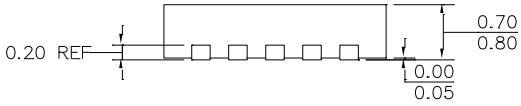
TQFN-10 (2mmx3mm)



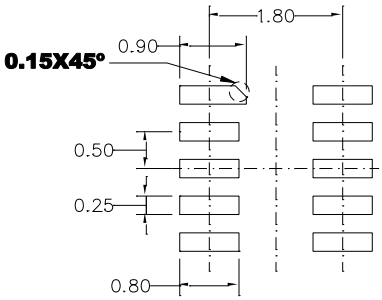
TOP VIEW



BOTTOM VIEW



SIDE VIEW

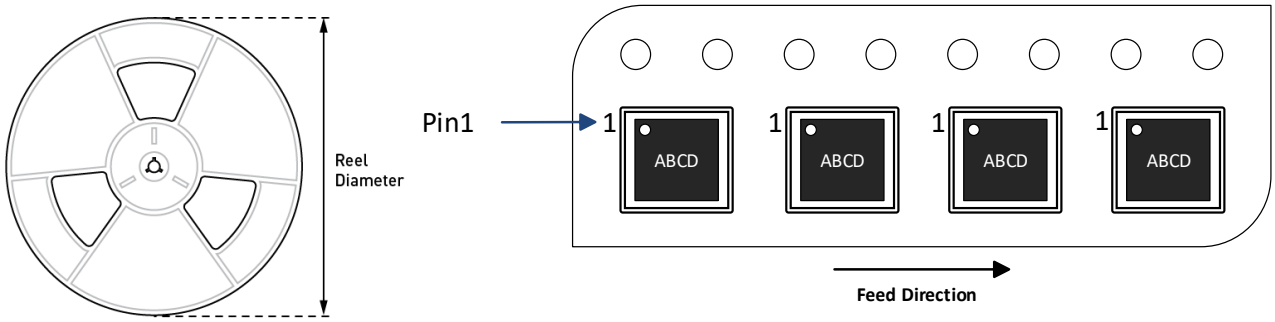


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5099GDT-Z	TQFN-10 (2mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/21/2022	Initial Release	-