EV5099-D-00A

12V/5V Dual-Channel Current-Limit Switch with Current Monitor Evaluation Board

DESCRIPTION

The EV5099-D-00A evaluation board is designed to demonstrate the capabilities of the MP5099, a protection device that protects circuitry on the output from transients on the input. The MP5099 also protects the input from undesired shorts and transients coming from the output. The MP5099 is a small on resistance ($R_{DS(ON)}$), low quiescent current (I_Q), dual-channel, current-limited switch.

During start-up, the inrush current is limited by limiting the slew rate at the output. The slew rate is controlled by a capacitor at the SS pin.

The maximum load at the output is current-limited. The magnitude of the current limit is fixed internally.

The output voltage (V_{OUT}) is limited by the output over-voltage protection (OVP) function. The output current (I_{OUT}) of each rail can be monitored via a resistor connected to the IMON pins.

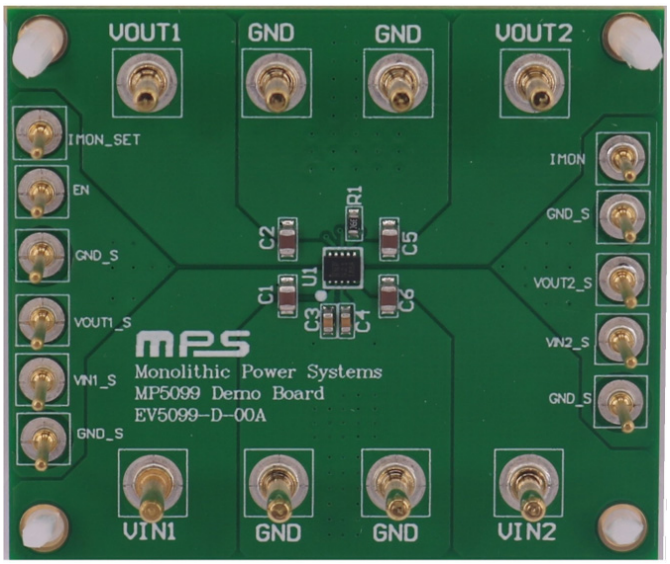
The MP5099 is available in a space-saving TQFN-10 (2mmx3mm) package.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
E-fuse 1 input voltage (V_{IN1}) range	$V_{IN2} > V_{UVLO\_CH2}$	10.8V to 13.2V
E-fuse 2 input voltage (V_{IN2}) range	$V_{IN1} > V_{UVLO\_CH1}$	4.5V to 5.5V
E-fuse 1 output current (I_{OUT1}) range	$V_{IN1} > V_{UVLO\_CH1}$ and $V_{IN2} > V_{UVLO\_CH2}$	0A to 4A
E-fuse 2 output current (I_{OUT2}) range	$V_{IN1} > V_{UVLO\_CH1}$ and $V_{IN2} > V_{UVLO\_CH2}$	0A to 3A

EV5099-D-00A EVALUATION BOARD



LxWxH (5.3cmx4.6cmx1.2cm)

Board Number	MPS IC Number
EV5099-D-00A	MP5099GDT

QUICK START GUIDE

The EV5099-D-00A evaluation board is easy to set up and use to evaluate the MP5099's performance. For proper measurement equipment set-up, refer to Figure 1 and follow the steps below:

1. Preset the e-fuse 1 power supply (V_{IN1}) to 12V and the e-fuse 2 power supply (V_{IN2}) to 5V, then turn off the power supplies.
2. Connect the power supply terminals to:
   a. Positive (+): V_{INX}
   b. Negative (-): GND
3. Connect the load terminals to:
   a. Positive (+): V_{OUTX}
   b. Negative (-): GND
4. After making the connections, turn on both power supplies. The board should automatically start up.
5. To use the enable function, float the EN pin or pull EN low to turn on the regulator; pull EN high to turn off the regulator.
6. To set the current monitor gain, connect a resistor from the IMON pin to ground.
7. Pull the IMON_SEL pin high to detect channel 1's output current (I_{OUT1}); float IMON_SEL or drive the pin low to detect channel 2's output current (I_{OUT2}).
8. To set the soft-start time (t_{SS}), connect a capacitor from the SS pin to ground.

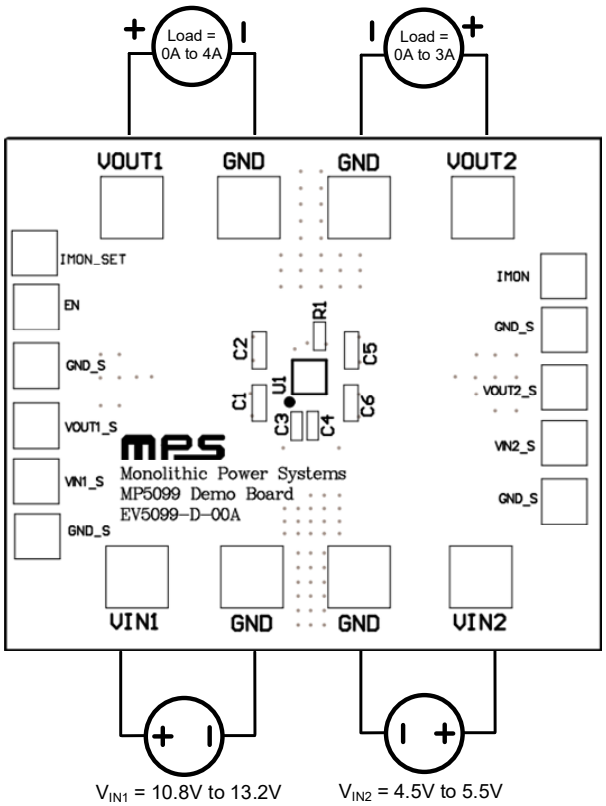


Figure 1: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

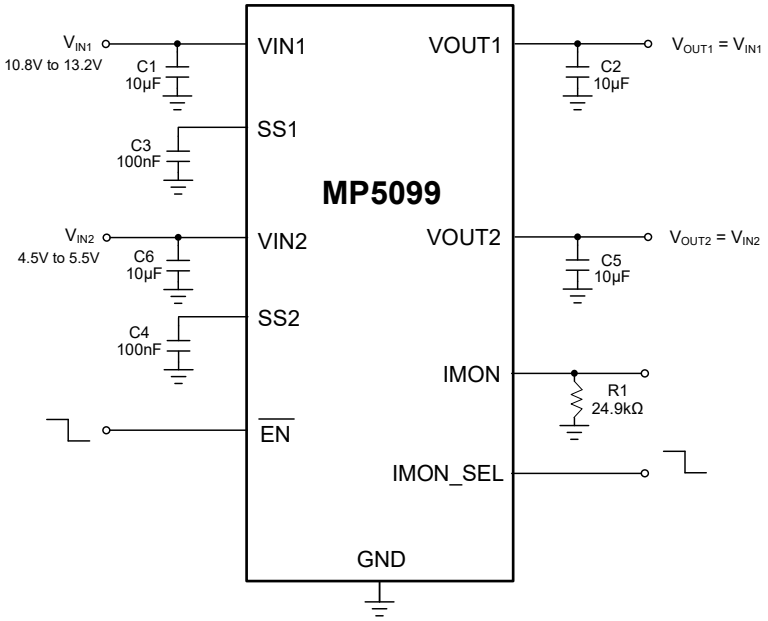


Figure 2: Evaluation Board Schematic

EV5099-D-00A BILL OF MATERIALS

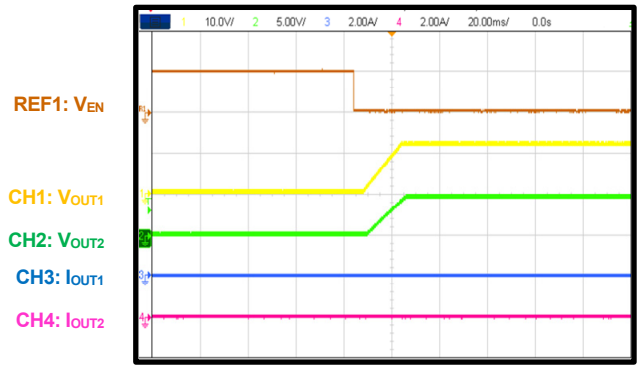
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	R1	24.9kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0720K9L
4	C1, C2, C6, C5	10μF	Ceramic capacitor, 50V, X5R	0805	Murata	GRM21BR61H106KE43L
2	C3, C4	100nF	Ceramic capacitor, 25V, X5R	0603	Murata	GRM216R61E104KA12D
1	U1	MP5099	12V/5V dual e-fuse with current monitor	TQFN-10 (2mmx 3mm)	MPS	MP5099GDT

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

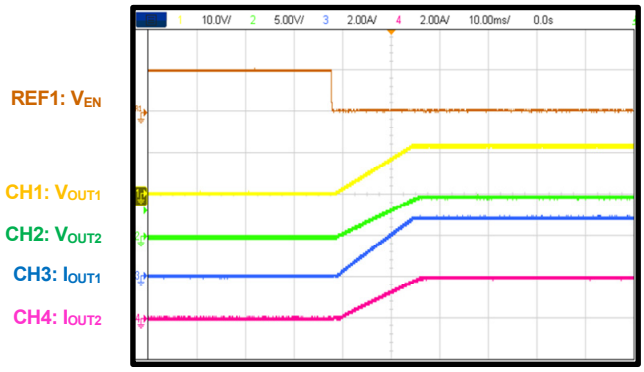
CH1 and CH2 EN On Logic

I_{OUT1} = I_{OUT2} = 0A



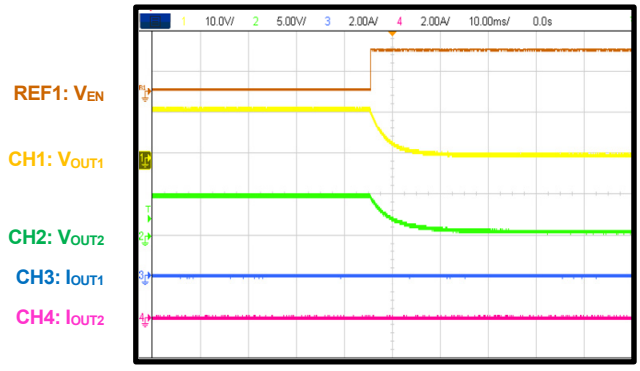
CH1 and CH2 EN On Logic

I_{OUT1} = 3A, I_{OUT2} = 2A



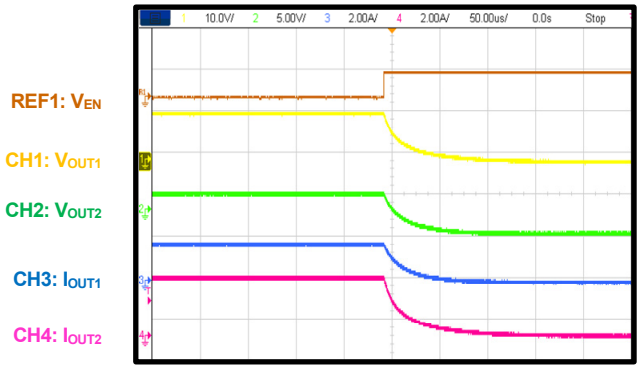
CH1 and CH2 EN Off Logic

I_{OUT1} = I_{OUT2} = 0A



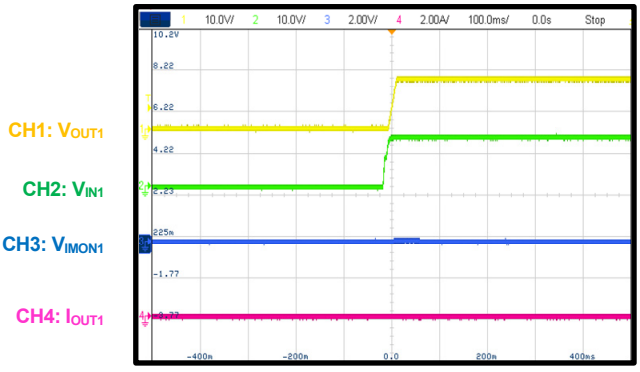
CH1 and CH2 EN Off Logic

I_{OUT1} = 3A, I_{OUT2} = 2A



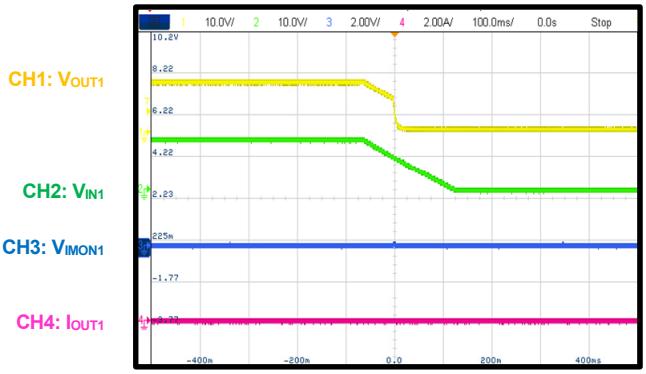
VIN1 Start-Up without Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



VIN1 Shutdown without Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A

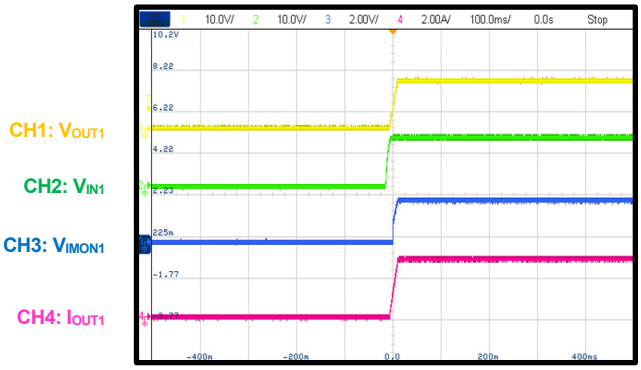


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

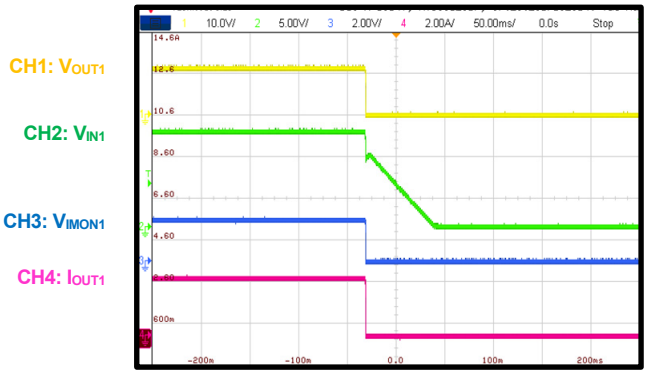
VIN1 Start-Up with 3A Load (12V E-Fuse)

I_{OUT1} = 3A, V_{IN2} = 5V



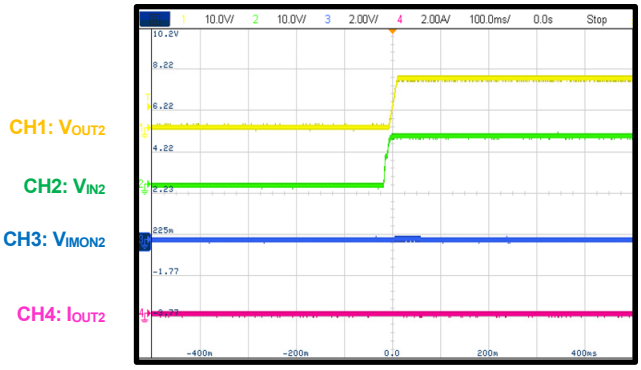
VIN1 Shutdown with 3A Load (12V E-Fuse)

I_{OUT1} = 3A, V_{IN2} = 5V



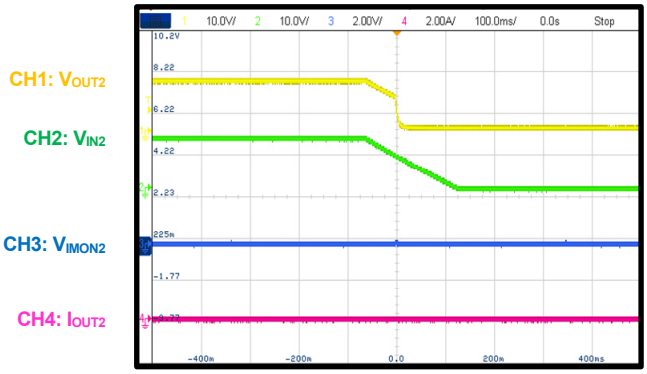
VIN2 Start-Up without Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



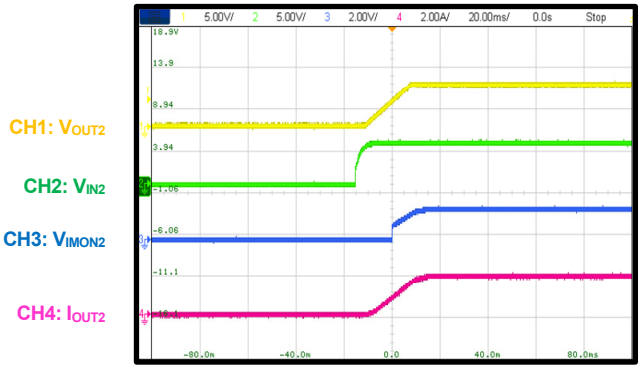
VIN2 Shutdown without Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



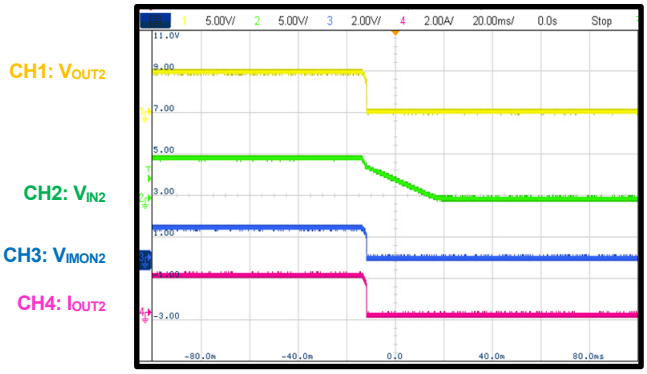
VIN2 Start-Up with 2A Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A



VIN2 Shutdown with 2A Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A

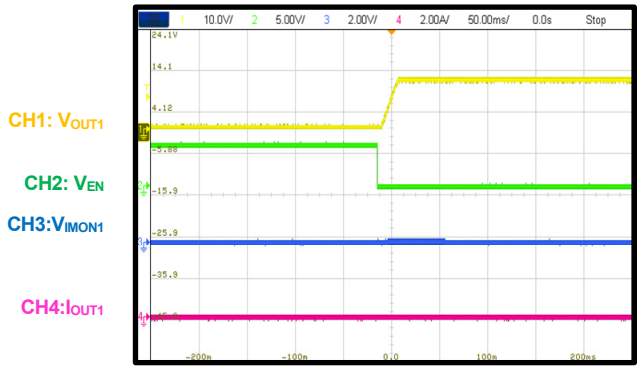


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

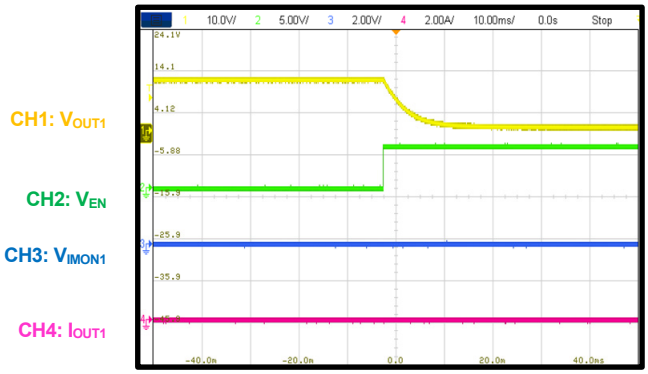
EN Start-Up without Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



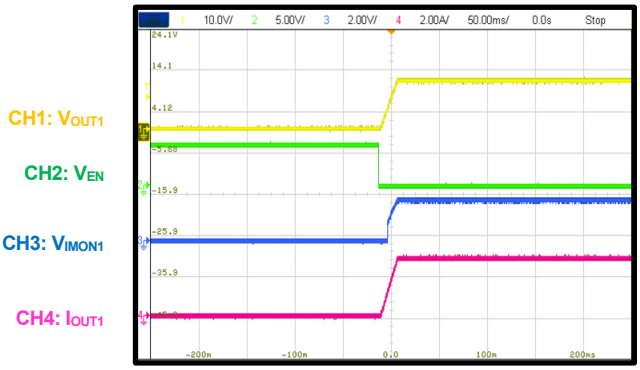
EN Shutdown without Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



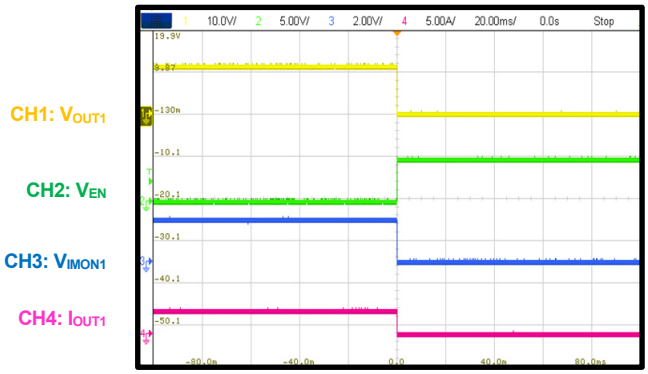
EN Start-Up with 3A Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



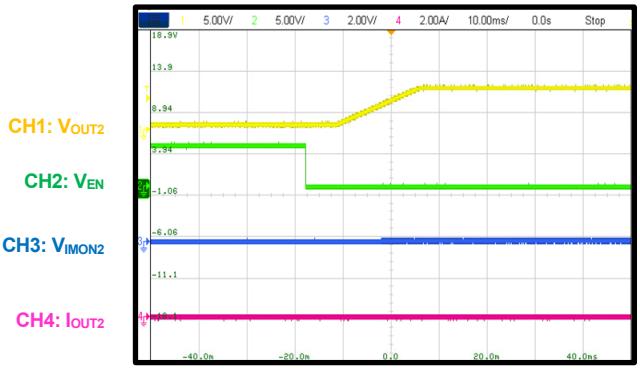
EN Shutdown with 3A Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



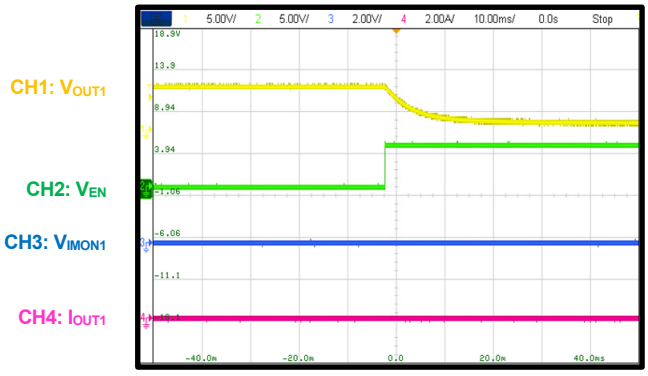
EN Start-Up without Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



EN Shutdown without Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A

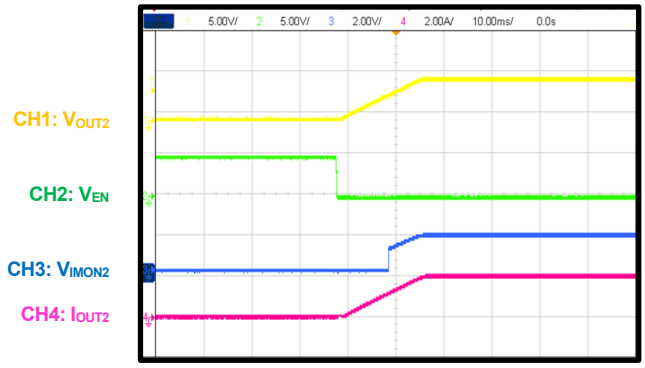


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

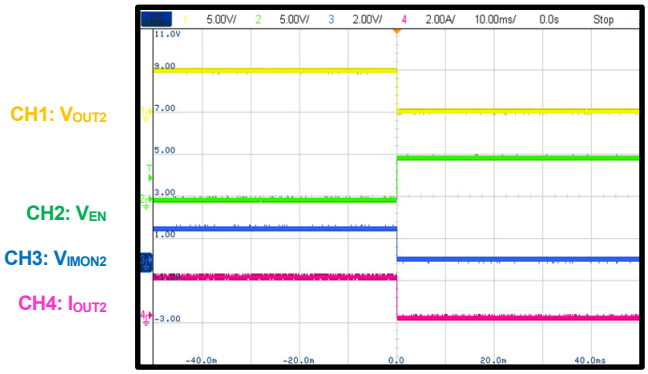
EN Start-Up with 2A Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A

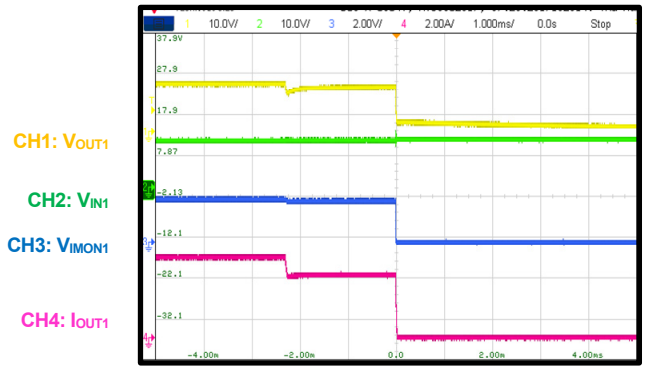


EN Shutdown with 2A Load (5V E-Fuse)

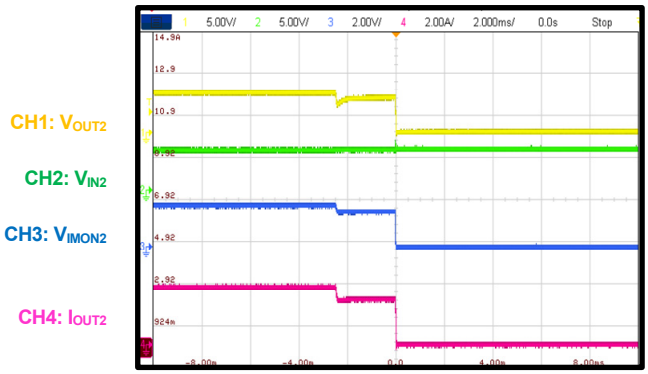
V_{IN1} = 12V, I_{OUT2} = 2A



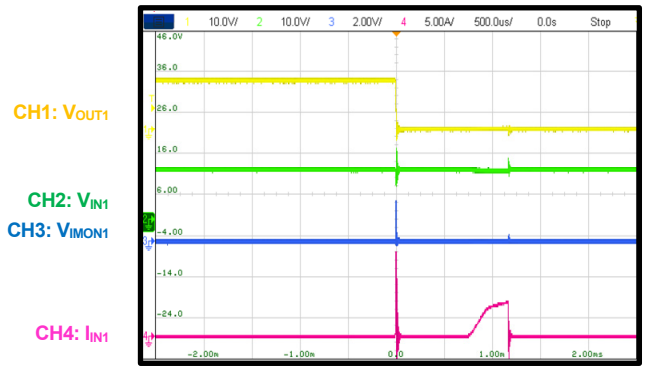
Current Limit (12V E-Fuse)



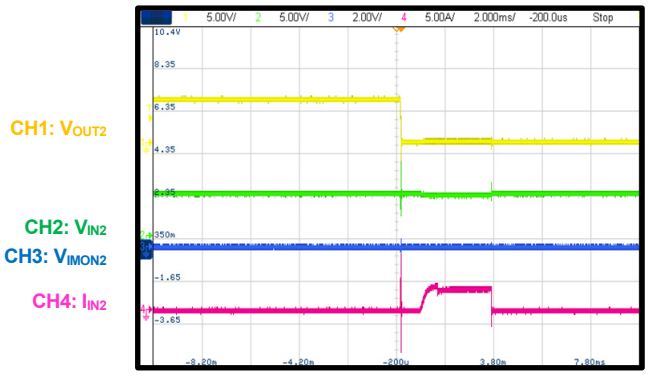
Current Limit (5V E-Fuse)



Short-Circuit Entry (12V E-Fuse)



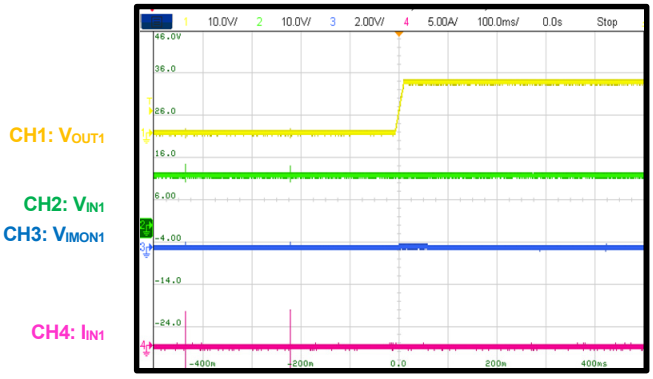
Short-Circuit Entry (5V E-Fuse)



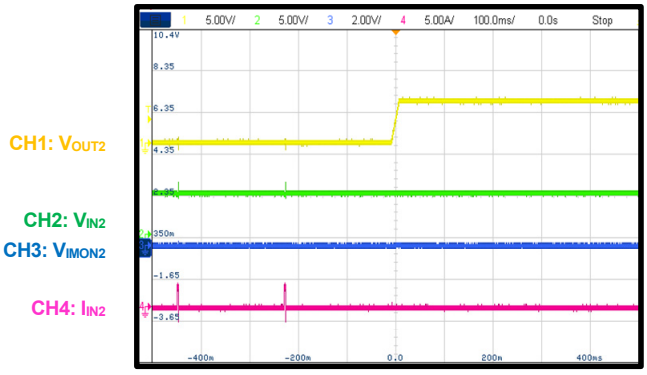
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN1} =12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

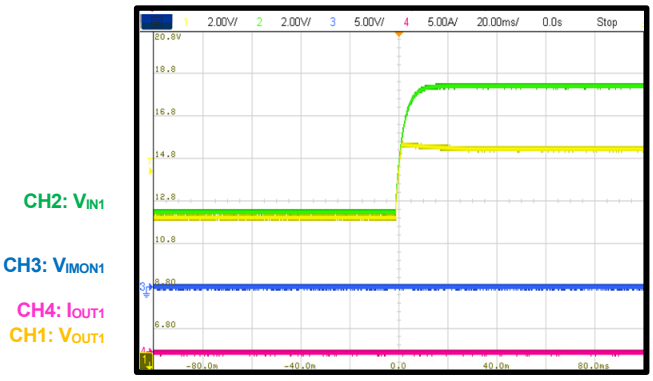
Short-Circuit Recovery (12V E-Fuse)



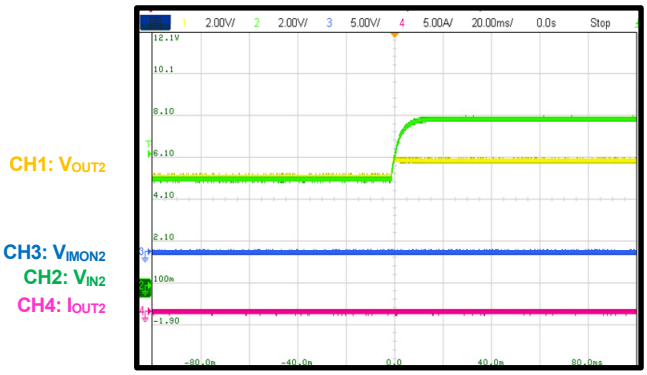
Short-Circuit Recovery (5V E-Fuse)



Output Over-Voltage Protection (12V E-Fuse)



Output Over-Voltage Protection (5V E-Fuse)



PCB LAYOUT

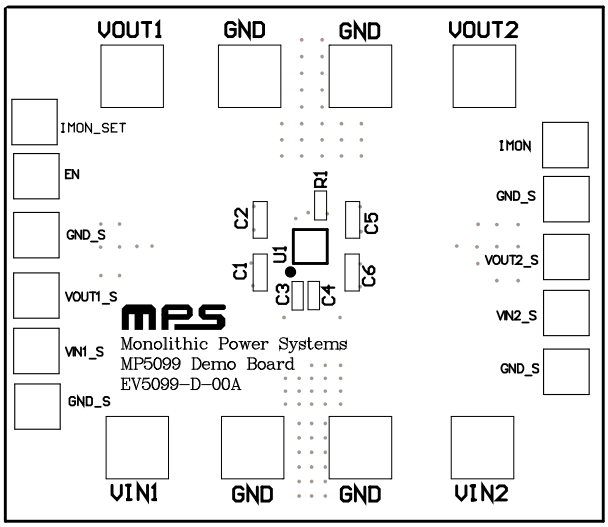


Figure 3: Top Silk

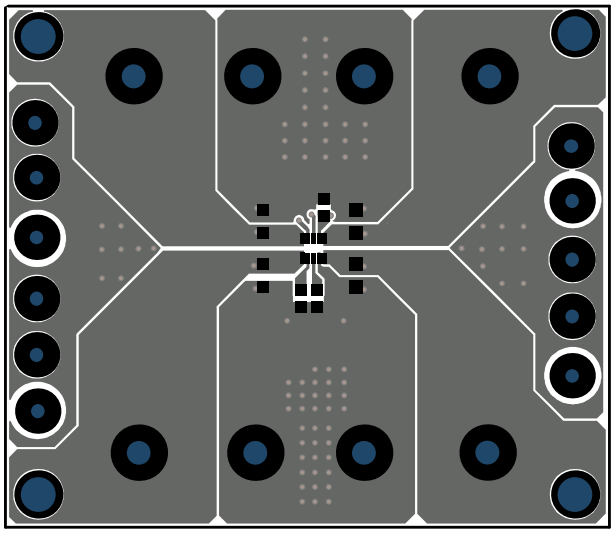


Figure 4: Top Layer

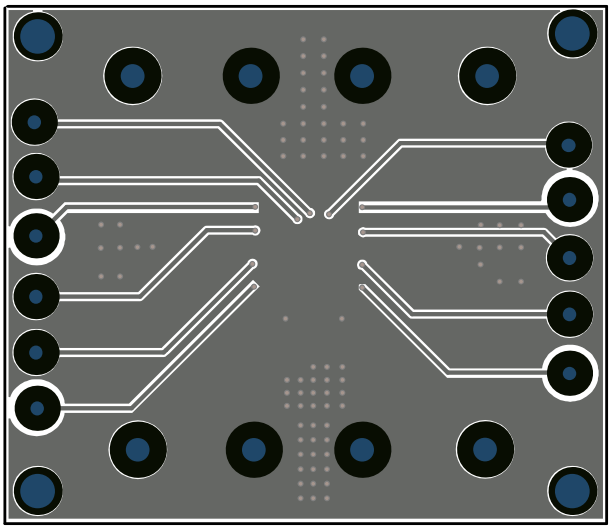


Figure 5: Bottom Layer

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/25/2022	Initial Release	-