



# MPQ4242

## 5A, 36V, Fully Integrated USB PD Solution with Integrated Buck-Boost Converter, AEC-Q100 Qualified

### DESCRIPTION

The MPQ4242 is a fully integrated power delivery (PD) solution for USB Type-C sourcing ports. It integrates a buck-boost converter with four power switches and a USB PD controller. The device supports up to 5A of continuous output current ( $I_{OUT}$ ) under a certain input supply range.

The MPQ4242's USB Type-C port supports USB PD revision 3.0 with PPS. It is backward compatible with DCP schemes for battery charging specification (BC1.2), 3A divider mode, and 1.2V/1.2V mode. The MPQ4242 also supports QC 2.0/3.0 and Huawei FCP mode.

The MPQ4242 provides a configurable PD power management state machine when the battery voltage ( $V_{BATT}$ ) is low, or if an over-temperature condition occurs. When two MPQ4242s are used as dual PD ports, the internal power sharing logic can effectively distribute the total power.

Fault condition protections include I/O pin short for the BUS and VIN pins, CC over-current protection (OCP), current limiting with hiccup mode, output over-voltage protection (OVP), and thermal shutdown.

The MPQ4242 requires a minimal number of readily available, standard external components. It is available in a QFN-22 (4mmx5mm) package.

### FEATURES

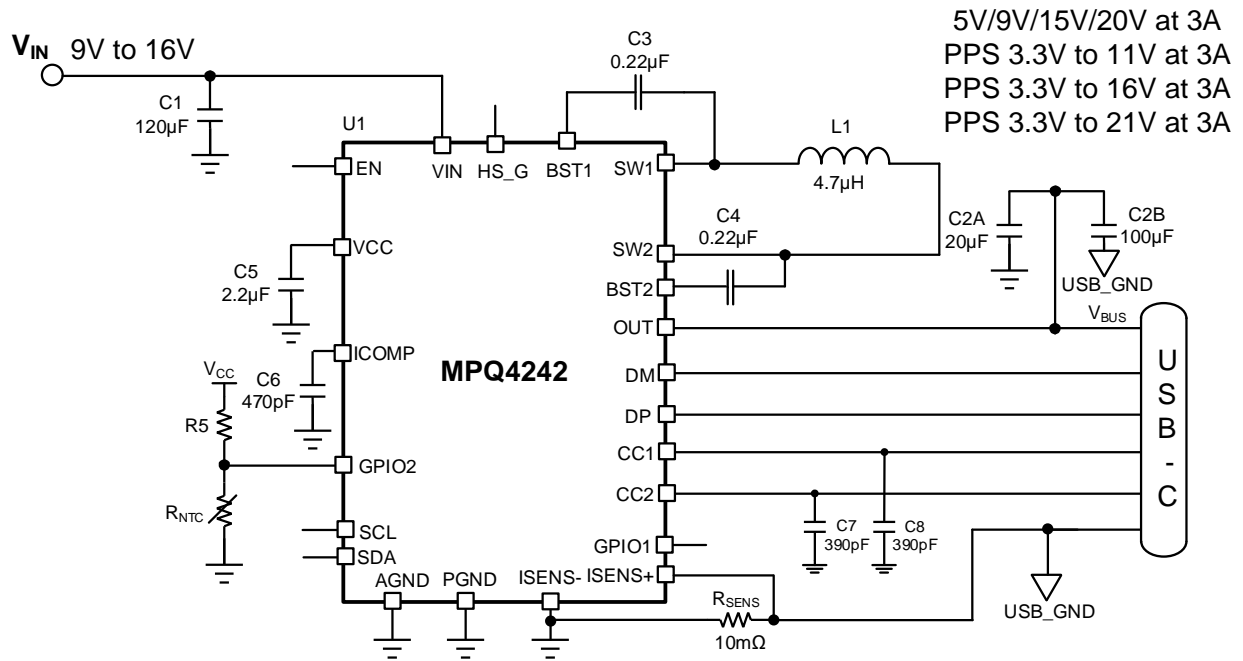
- All-In-One USB PD Solution for Automotive Sourcing Ports
- Integrated 4-Switch Buck-Boost Converter
- Integrated PD 3.0 Controller
- Wide 4.8V to 36V Operating Input Voltage ( $V_{IN}$ ) Range
- 3.3V to 22.5V Output Voltage ( $V_{OUT}$ ) Range
- Accurate Output CC Current Limit:  $\pm 5\%$
- External High-Side MOSFET (HS-FET) can be Paralleled
- Low  $I_Q$  when USB Type-C is Disconnected
- 250kHz / 420kHz Configurable Frequency with Spread Spectrum
- Supports USB Type-C V2.0
- Supports USB PD R3.0, V2.0, and PPS with 7 PDO List
- Supports QC 3.0 Specification, Huawei FCP
- Supports DCP Schemes for BC1.2, 3A Divider Mode, and 1.2V/1.2V Mode
- CCx, DP, and DM Short to  $V_{BUS}$  /  $V_{BATT}$  Protection
- Battery Short to Ground Protection Driver
- I<sup>2</sup>C Slave Interface
- Output Line Drop Compensation
- Configurable PD Power Management during Low Battery Voltages or High Temperatures
- Supports Dual-Port PD Power Sharing
- PWM Duty Cycle Configurable LED Driver
- Up to 120 Minutes for EN Off Delay
- Available in a QFN-22 (4mmx5mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

### APPLICATIONS

- USB Power Delivery Charging Ports
- USB Power Supplies

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### TYPICAL APPLICATION



## ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL
MPQ4242GVE-0000-AEC1	QFN-22 (4mmx5mm)	<i>See Below</i>	1
MPQ4242GVE-0001-AEC1			
MPQ4242GVE-0015-AEC1			
MPQ4242GVE-xxxx-AEC1**			
EVKT-MPQ4242	-	-	-

\* For Tape & Reel, add suffix -Z (e.g. MPQ4242GVE-xxxx-AEC1-Z).

\*\* “-xxxx” is the configuration code identifier for the register setting stored in the OTP. Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number.

\*\*\* The MPQ4242GVE-0000-AEC1 is the default 60W PD version, which can be configured once by the one-time programmable (OTP) memory. The MPQ4242GVE-0001-AEC1 is the standard version for a 45W PD application, and it cannot be written with the OTP again.

## TOP MARKING

MPSYWW  
**MP4242**  
LLLLLL  
**E**

MPS: MPS prefix  
 Y: Year code  
 WW: Week code  
 MP4242: Part number  
 LLLLLL: Lot number  
 E: Wettable flank

## EVALUATION KIT EVKT-MPQ4242

EVKT-MPQ4242 kit contents (items below can be ordered separately):

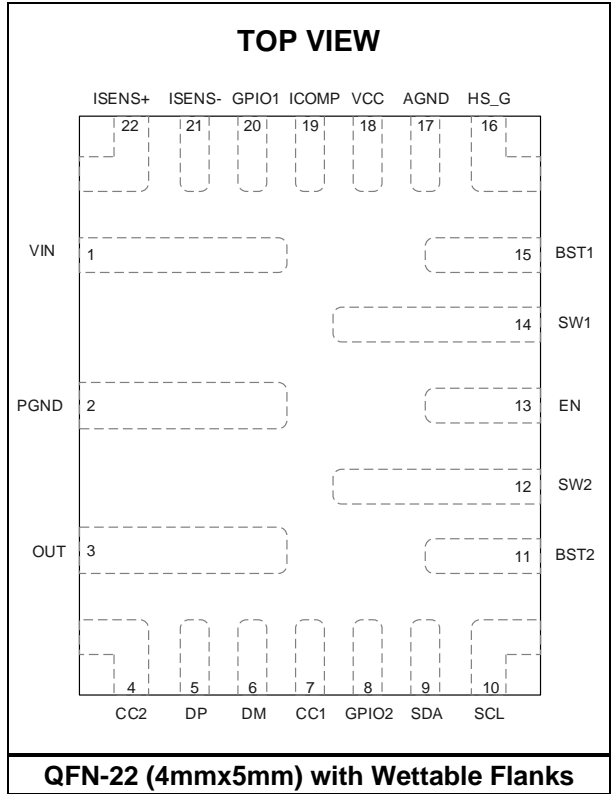
#	Part Number	Item	Quantity
1	EVQ4242-VE-00B	The MPQ4242 evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I <sup>2</sup> C communication interface device, one USB cable, and one ribbon cable	1
3	MPQ4242GVE-0000-AEC1	The MPQ4242 IC, which can be used for OTP configurations	2

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**Figure 1: EVKT-MPQ4242 Evaluation Kit Set-Up**

### PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	Description	
1	VIN	<b>Supply voltage.</b> The MPQ4242 operates from a 4.8V to 36V unregulated input. An input capacitor ( $C_{IN}$ ) is required to prevent large voltage spikes at the input. Place $C_{IN}$ as close to the IC as possible. The VIN pin is the drain of the internal power device, and it is the power supply for the whole chip.	
2	PGND	<b>Power ground.</b> Place the PGND pin outside of the $C_{IN}$ and output capacitor ( $C_{OUT}$ ) ground path to prevent switching current spikes. PGND requires extra consideration during the PCB layout. Make the PGND connection with copper traces and vias.	
3	OUT	<b>Buck-boost output pin.</b> $C_{OUT}$ is required to prevent large voltage spikes from appearing at the output in buck-boost and boost mode. Place $C_{OUT}$ as close to the IC as possible.	
4	CC2	<b>Configuration channel (CC).</b> The CC2 pin discovers, configures, and manages connections across a USB Type-C cable.	
5	DP	<b>D+ data line to USB connector.</b> The DP pin is the input/output used for handshaking with portable devices.	
6	DM	<b>D- data line to USB connector.</b> The DM pin is the input/output used for handshaking with portable devices.	
7	CC1	<b>Configuration Channel (CC).</b> The CC1 pin discovers, configures, and manages connections across a USB Type-C cable.	
8	GPIO2	POL	<b>USB Type-C polarity indication.</b> The POL pin is an open drain. When CC1 is selected as the CC line, POL is pulled low; when CC2 is selected as the CC line, POL is an open drain.
		NTC	<b>NTC thermal-sense input.</b>
		VCONN_IN	<b>1W VCONN power supply input.</b>
		LED_PWM	<b>Output for the PWM driver to the LED.</b>
		ATTACH	<b>Output to indicate if the device is attached.</b> The ATTACH pin is active low.
		POWER_SHARE2	<b>Power sharing 2 input.</b> The POWER_SHARE2 pin is active high. When this pin's voltage exceeds 1.87V, the PD power drops to the PS_PDP_THD setting.
9	SDA	<b>I<sup>2</sup>C data line.</b>	
10	SCL	<b>I<sup>2</sup>C clock signal input.</b>	
11	BST2	<b>Bootstrap 2.</b> Connect a 0.22 $\mu$ F capacitor between the SW2 and BST2 pins to form a floating supply across the high-side switch driver.	
12	SW2	<b>Switch 2 output.</b> Use a wide PCB trace to make the SW2 connection.	
13	EN	<b>Enable control pin.</b> Apply a logic high voltage on the EN pin to enable the IC. Pull EN to logic low to disable the IC. The EN pin has an internal 6 $\mu$ A pull-up.	
14	SW1	<b>Switch 1 output.</b> Use a wide PCB trace to make the SW1 connection.	
15	BST1	<b>Bootstrap 1.</b> Place a 0.22 $\mu$ F capacitor between the SW1 and BST1 pins to form a floating supply across the high-side switch driver.	
16	HS_G	<b>High-side gate driver signal for an external N-channel MOSFET.</b>	
17	AGND	<b>Analog ground.</b> Connect the AGND pin to PGND.	
18	VCC	<b>Internal 5V LDO regulator output.</b> Decouple the VCC pin with a 2.2 $\mu$ F capacitor.	
19	ICOMP	<b>Compensation pin for the CC current limit loop.</b> Decouple the ICOMP pin with a 470pF capacitor.	

**PIN FUNCTIONS (continued)**

Pin #	Name	Description													
20	GPIO1	<b>GATE</b> Gate drive for the external low-side N-channel power MOSFET. The GATE pin is an open-drain structure. GATE pulls low to turn off the power MOSFET when the secondary current limit is triggered. If GATE is not selected, the GND short to V <sub>BATT</sub> detection function is disabled.													
		<b>POWER_SHARE1</b> Power sharing 1 input. The POWER_SHARE1 pin is active low. When this pin's voltage is low, the PD power drops to the value set by PS_PDP_THD.													
		<b>FAULT</b> Fault indication. Open-drain output. If a fault occurs, the FAULT pin pulls low.													
		<b>NTC2</b> Second NTC detection input. If the NTC2 pin is triggered, PDP reduces its power to the set power share value.													
		<b>ATTACH_FLT_ALT</b> Attach and fault indicator. The ATTACH_FLT_ALT pin is an open-drain output. If no fault event has occurred, this pin pulls low for 12μs when a sink plug-in is detected. If a fault occurs, it pulls low. See the truth table below for more details. <table border="1" data-bbox="695 806 1443 932" style="margin-left: auto; margin-right: auto;"> <tbody> <tr> <td><b>Device Plug In</b></td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td><b>Fault Event</b></td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td><b>ATTACH_FLT_ALT</b></td> <td>Open drain</td> <td>12μs pull-down pulse</td> <td>Low</td> <td>Low</td> </tr> </tbody> </table>	<b>Device Plug In</b>	0	1	1	0	<b>Fault Event</b>	0	0	1	1	<b>ATTACH_FLT_ALT</b>	Open drain	12μs pull-down pulse
<b>Device Plug In</b>	0	1	1	0											
<b>Fault Event</b>	0	0	1	1											
<b>ATTACH_FLT_ALT</b>	Open drain	12μs pull-down pulse	Low	Low											
<b>IMON</b> Current monitor output. The IMON pin represents the signal between the ISENS+ and ISENS- pins.															
21	ISENS-	<b>Negative node of current-sense signal input.</b> Place a current-sense resistor between the PGND pin and the USB port's GND. Connect the ISENS- pin to the PGND side.													
22	ISENS+	<b>Positive node of current-sense signal input.</b> Place a current-sense resistor between the PGND pin and the USB port's GND. Connect the ISENS+ pin to the USB port's GND side.													

**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

Supply voltage ( $V_{IN}$ )	-0.3V to +40V
$V_{HS\_G}$	-0.3V to $V_{IN} + 12V$
$V_{EN}$	-0.3V to +40V
$V_{OUT}, V_{CC1}, V_{CC2}, V_{DP}, V_{DM}$	-0.3V to +26V
$V_{SW1}$	-0.3V (-5V for <10ns)
to $V_{IN} + 0.3V$ (+43V for <10ns)	
$V_{SW2}$	-0.3V (-5V for <10ns)
to $V_{OUT} + 0.3V$ (29V for <10ns)	
$V_{BST1}$	$V_{SW1} + 6.5V$
$V_{BST2}$	$V_{SW2} + 6.5V$
All other pins	-0.3V to +5.5V
Continuous power dissipation ( $T_A = 25^\circ C$ ) <sup>(2)</sup>	
QFN-22 (4mmx5mm)	4.55W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

**ESD Ratings** <sup>(3)</sup>

CC1/CC2/DP/DM (HBM) <sup>(4)</sup>	±8kV
Human body model (HBM)	±2kV
Charged device model (CDM)	±750V

**Recommended Operating Conditions** <sup>(5)</sup>

Supply voltage ( $V_{IN}$ )	4.8V to 36V
Output voltage ( $V_{OUT}$ )	3.3V to 22.5V
Output current	5A or 100W peak
Operating junction temp ( $T_J$ )	-40°C to +150°C

Thermal Resistance	$\theta_{JA}$	$\theta_{JC}$
EVQ4242-VE-00B <sup>(6)</sup>	27.5	5.2
QFN-22 (4mmx5mm) <sup>(7)</sup>	44	9

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_J$  (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AECQ100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
- 4) HBM with regard to GND.
- 5) The device is not guaranteed to function outside of its operating conditions.
- 6) Measured on MPQ4242 test board, 43mmx5mm, 4-layer PCB.
- 7) Measured on JESD51-7, 4-layer PCB. The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{EN} = \text{floating}$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	$I_{IN}$	$EN = 0V$ , $T_J = 25^{\circ}C$		12	20	$\mu A$
		$EN = 0V$ , $T_J = -40^{\circ}C \sim 125^{\circ}C$		12	80	$\mu A$
Supply current (standby)	$I_{Q\_STB}$	No device attached, set EN to 1b via the I <sup>2</sup> C, $T_J = 25^{\circ}C$		150	200	$\mu A$
Supply current (quiescent)	$I_{Q\_BB}$	Buck-boost non-switching, CC attached		4		mA
EN rising threshold	$V_{EN\_RISING}$		-4%	1.3	+4%	V
EN hysteresis	$V_{EN\_HYS}$			100		mV
EN pull-up current	$I_{EN}$	$V_{EN} = 2V$	3	6	9	$\mu A$
Thermal shutdown <sup>(8)</sup>	$T_{TSD}$			175		$^{\circ}C$
Thermal hysteresis <sup>(8)</sup>	$T_{TSD\_HYS}$			20		$^{\circ}C$
$V_{IN}$ under-voltage lockout threshold rising	$V_{IN\_UVLO\_RISING}$		-4%	4.3	+4%	V
$V_{IN}$ under-voltage lockout threshold hysteresis	$V_{IN\_UVLO\_HYS}$			400		mV
VCC regulator	$V_{CC}$		4.75	5	5.25	V
VCC load regulation	$V_{CC\_REG}$	$I_{CC} = 70mA$		3		%
VBUS_UV falling threshold 1	$V_{BUS\_UV1}$		2.9	3	3.1	V
VBUS_UV falling threshold 2	$V_{BUS\_UV2}$		-3%	4.5	+3%	V
<b>Buck-boost Converter</b>						
Switch A on resistance	$R_{DS\_ON\_A}$			16.3		m $\Omega$
Switch B on resistance	$R_{DS\_ON\_B}$			41.5		m $\Omega$
Switch C on resistance	$R_{DS\_ON\_C}$			15		m $\Omega$
Switch D on resistance	$R_{DS\_ON\_D}$			15.3		m $\Omega$
VHS_G voltage	$V_{HSG}$			$V_{IN} + 10$		V
VHS_G source current <sup>(8)</sup>	$I_{HSG}$			100		$\mu A$
VHS_G pull-down	$R_{HS\_DN}$			3	6.5	$\Omega$
Output voltage	$V_{OUT0}$		-3%	3.3	+3%	V
	$V_{OUT1}$		-2%	5	+2%	V
	$V_{OUT2}$		-1.5%	9	+1.5%	V
	$V_{OUT3}$		-1.5%	20	+1.5%	V
Output over-voltage protection (OVP)	$V_{OVP}$		112	117	122	%
Output absolute OVP	$V_{OVP\_ABS}$		24	25	26	V
OVP recovery hysteresis	$V_{OVP\_HYS}$			10		%
Input over-voltage protection	$V_{IN\_OVP}$	OTP trim option	21.4	22.4	23.4	V
Input OVP recovery hysteresis	$V_{OVP\_HYS}$	OTP trim option		2		V



**ELECTRICAL CHARACTERISTICS (continued)**

$V_{IN} = 12V$ ,  $V_{EN} = \text{floating}$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switch leakage	SWLKG	$V_{EN} = 0V$ , $V_{SW} = 36V$ , $T_J = 25^{\circ}C$			1000	nA
		$V_{EN} = 0V$ , $V_{SW} = 36V$ , $T_J = -40^{\circ}C \sim 125^{\circ}C$			80	$\mu A$
Line drop compensation	VLDC	Set LINE_DROP_COMP to 01b via the I <sup>2</sup> C, $V_{OUT} = 5V$ , $I_{OUT} = 3A$ (only enabled when $V_{OUT} > 4.9V$ )		150		mV
ISENS OC Threshold	I <sub>OC1</sub>	OC threshold = 1A, $R_{SENS} = 10m\Omega$	9	10	11	mV
	I <sub>OC2</sub>	OC threshold = 3A, $R_{SENS} = 10m\Omega$	28.5	30	31.5	mV
Switch A current limit	I <sub>LIMIT1</sub>	Switch A, boost mode		20		A
Switch B valley limit	I <sub>LIMIT2</sub>	Switch B, buck mode		6.7		A
Oscillator frequency	f <sub>SW1</sub>	Set FREQ to 00b via the I <sup>2</sup> C	200	250	300	kHz
	f <sub>SW2</sub>	Set FREQ to 01b via the I <sup>2</sup> C	350	420	490	kHz
Frequency dithering span	f <sub>DITH_SPAN</sub>	Set FREQ to 01b via the I <sup>2</sup> C		$\pm 11$		%
Minimum on time <sup>(8)</sup>	t <sub>ON_MIN</sub>	Buck SWC		80		ns
Minimum off time <sup>(8)</sup>	t <sub>OFF_MIN</sub>	Buck SWB		60		ns
Soft-start time	t <sub>SS</sub>	5V output from 10% to 90%, Constant slew rate for other $V_{OUT}$	0.5	1.1	1.7	ms
Output discharge resistance	R <sub>DIS_OUT</sub>			320		$\Omega$
<b>Ground NMOSFET Gate Driver</b>						
GND short to battery threshold	V <sub>RGND</sub>	$R_{SENS} = 10m\Omega$		135		mV
Short to battery retry delay <sup>(8)</sup>	t <sub>SBP</sub>			1		s
Gate pull-down resistance	R <sub>PD</sub>			20	45	$\Omega$
<b>NTC, NTC2</b>						
External thermal sense triggering voltage	V <sub>NTC_ETY</sub>	$R_P = 43.2k\Omega$ , $R_{NTC} = 4.79k\Omega$ (100 <sup>o</sup> C)	8%	10%	12%	V <sub>CC</sub>
External thermal sense recovery voltage 1	V <sub>NTC_RCY1</sub>	Set NTC_HYSTERESIS to 0b via the I <sup>2</sup> C		20%		V <sub>CC</sub>
External thermal sense recovery voltage 2	V <sub>NTC_RCY2</sub>	Set NTC_HYSTERESIS to 1b via the I <sup>2</sup> C		30%		V <sub>CC</sub>
<b>GPIO1</b>						
Power share input high	V <sub>IH_PS</sub>		2			V
Power share input low	V <sub>IL_PS</sub>				0.8	V
Power share pull-up resistance	I <sub>LKG_PS</sub>	5V pull-up		1		M $\Omega$
Fault pull-down resistance	R <sub>PD_FAULT</sub>			20	45	$\Omega$
Fault leakage	I <sub>LKG_FAULT</sub>				3	$\mu A$
<b>GPIO2</b>						
POL pull-down resistance	R <sub>PD_POL</sub>	Connect CC1 to GND with a 5.1k $\Omega$ resistor			45	$\Omega$
POL leakage	I <sub>LKG_POL</sub>	Connect CC2 to GND with a 5.1k $\Omega$ resistor			3	$\mu A$

**ELECTRICAL CHARACTERISTICS (continued)**

$V_{IN} = 12V$ ,  $V_{EN} = \text{floating}$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LED PWM output FREQ	f <sub>LED</sub>		21	24	27	kHz
LED_PWM output duty	D <sub>LED</sub>			50		%
Connected output	V <sub>ATTO</sub>	USB Type-C connected, force 50μA			0.4	V
Power share input threshold	V <sub>TH_PS</sub>		1.52	1.87	2.22	V
<b>USB Charging Mode Identification</b>						
<b>BC1.2 DCP Mode</b>						
DP and DM short resistance	R <sub>DP_DM_SHORT</sub>	V <sub>DP</sub> = 0.8V, I <sub>DM</sub> = 1mA		30	70	Ω
<b>Divider Mode</b>						
DP output voltage	V <sub>DIVIDER_DP</sub>	V <sub>OUT</sub> = 5V	2.5	2.7	2.9	V
DM output voltage	V <sub>DIVIDER_DM</sub>	V <sub>OUT</sub> = 5V	3.05	3.3	3.55	V
DP output impedance	R <sub>DIVIDER_DP</sub>			23		kΩ
DM output impedance	R <sub>DIVIDER_DM</sub>			17		kΩ
<b>1.2V/1.2V Mode</b>						
DP/DM output voltage	V <sub>DP_DM_1.2V</sub>	V <sub>OUT</sub> = 5V	1.15	1.25	1.35	V
DP/DM output impedance	R <sub>DP_DM_1.2V</sub>			75		kΩ
<b>Quick Charge 3.0 Mode</b>						
DP/DM low voltage	V <sub>QC_LOW</sub>		0.2	0.3	0.4	V
DP/DM high voltage	V <sub>QC_HIGH</sub>		1.8	2	2.2	V
QC mode entry voltage glitch time (QC identify) <sup>(8)</sup>	t <sub>QC_GLITCH</sub>			1000		ms
DP output impedance	R <sub>DP_QC</sub>			350		kΩ
DM output impedance	R <sub>DM_QC</sub>			20		kΩ
Request voltage time <sup>(8)</sup>	t <sub>V_NEW_REQUEST</sub>		200			ms
Output voltage change glitch time <sup>(8)</sup>	t <sub>GLITCH_V_CHANGE</sub>		20		60	ms
Unplug V <sub>BUS</sub> discharge time <sup>(8)</sup>	t <sub>VBUS_DISC_QC</sub>				500	ms
<b>CDP Mode</b>						
DM CDP output voltage	V <sub>DM_SRC</sub>	V <sub>DP</sub> = 0.6V, DM sink = 250μA	0.5	0.6	0.7	V
DP rising lower window threshold for V <sub>DM_SRC</sub> EN	V <sub>DAT_REF</sub>		0.25	0.35	0.45	V
DP rising lower window threshold hysteresis	V <sub>DAT_REF_HYS</sub>			30		mV
DP rising upper window threshold for V <sub>DM_SRC</sub>	V <sub>LGCC_SRC</sub>		0.8	0.9	1	V
DP rising upper window threshold hysteresis	V <sub>LGCC_SRC_HYS</sub>			50		mV
<b>FCP Mode</b>						
DM Tx high voltage <sup>(8)</sup>	V <sub>FCPT_H</sub>	R <sub>LOAD</sub> = 15kΩ	2.55		5	V
DM Tx low voltage <sup>(8)</sup>	V <sub>FCPT_L</sub>	R <sub>LOAD</sub> = 15kΩ			0.4	V
DM Rx high voltage	V <sub>FCPR_H</sub>		1.5		5	V

**ELECTRICAL CHARACTERISTICS (continued)**

$V_{IN} = 12V$ ,  $V_{EN} = \text{floating}$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
DM Rx low voltage	$V_{FCPR\_L}$				1	V
DM pull-low resistance	$R_{LD\_D-}$			15		k $\Omega$
Unit interval of PHY <sup>(8)</sup>	UI		144	160	176	$\mu$ s
<b>USB Type-C - CC1 and CC2 pins</b>						
CC pull-up current 1	$I_{RP1}$	$V_{BUS} = 5V @ 3A, T_J = 0^{\circ}C$ to $85^{\circ}C$	-8%	330	+8%	$\mu$ A
CC pull-up current 2	$I_{RP2}$	$V_{BUS} = 5V @ 1.5A, T_J = 0^{\circ}C$ to $85^{\circ}C$	-8%	180	+8%	$\mu$ A
CC voltage to enable VCONN for 3A USB Type-C mode	$V_{RA1}$				0.75	V
CC voltage to enable VBUS for 3A USB Type-C mode	$V_{RD1}$		0.85		2.45	V
CC disconnect threshold for 3A USB Type-C mode	$V_{OPEN1}$		2.75			V
CC voltage to enable VCONN for 1.5A USB Type-C mode	$V_{RA2}$				0.35	V
CC voltage to enable VBUS for 1.5A USB Type-C mode	$V_{RD2}$		0.45		1.5	V
CC disconnect threshold for 1.5A USB Type-C mode	$V_{OPEN2}$		1.7			V
CC voltage falling de-bounce timer	$t_{CC\_DEBOUNCE}$	VBUS enable deglitch	100	150	200	ms
CC voltage rising de-bounce timer	$t_{PD\_DEBOUNCE}$	VBUS disable deglitch	5	10	15	ms
100mW VCONN output power	$P_{VCONN\_100mW}$	Default	100			mW
1W VCONN output power	$P_{VCONN\_1W}$	Set GPIO2 to 011b via the I <sup>2</sup> C	1			W
<b>USB PD</b>						
Unit interval time <sup>(8)</sup>	$t_{UI}$		3.03		3.7	$\mu$ s
<b>Transmitter</b>						
End drive BMC time <sup>(8)</sup>	$t_{EDBMC}$				23	$\mu$ s
Falling time <sup>(8)</sup>	$t_{FALL}$		300	400		ns
Rising time <sup>(8)</sup>	$t_{RISE}$		300	400		ns
Hold low BMC time <sup>(8)</sup>	$t_{HLBMC}$		1			$\mu$ s
Logic high voltage	$V_{LH}$		1.05		1.2	V
Logic low voltage	$V_{LL}$				70	mV
Output impedance	$Z_{TX}$			45		$\Omega$
<b>Receiver <sup>(8)</sup></b>						
CC receiver capacitance	$C_{RECEIVER}$				600	pF
Transitions for signal detection	$N_{TRANSITION}$		3			Edges
Rx bandwidth limiting filter	$t_{RX\_FILTER}$		100			ns
Time window for detecting non-idle	$t_{TRANSITION\_WINDOW}$		12		20	$\mu$ s

## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{EN} = \text{floating}$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

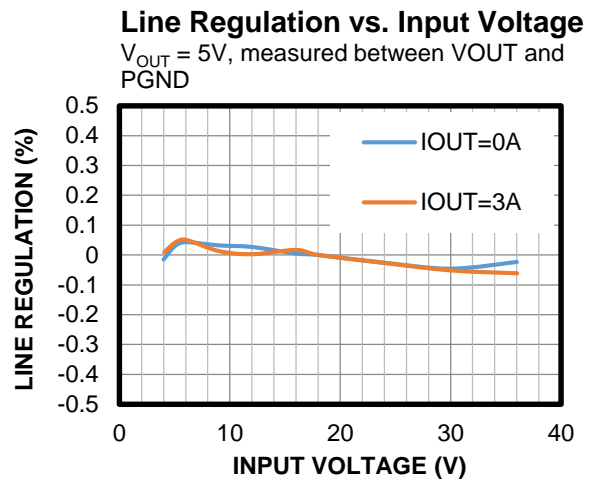
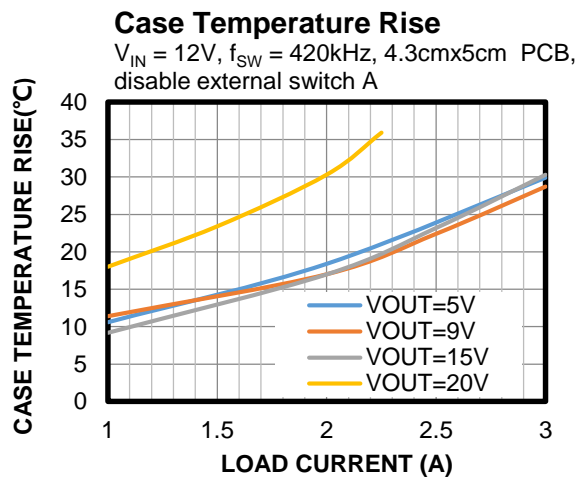
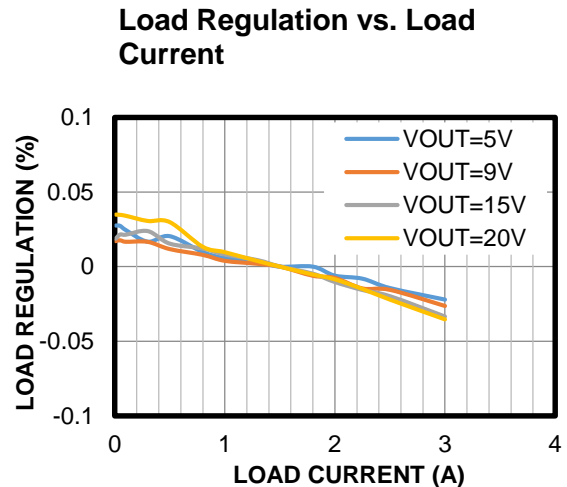
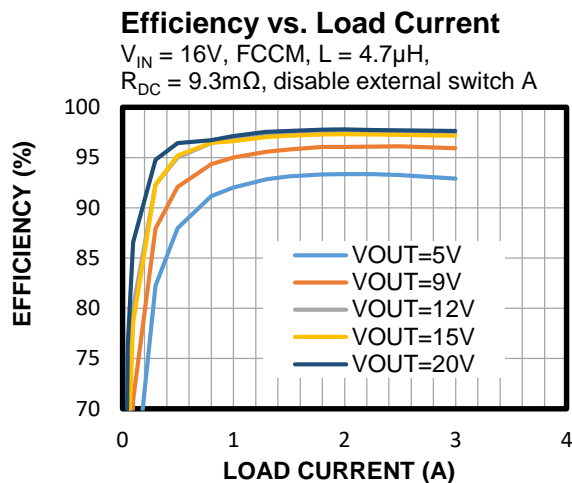
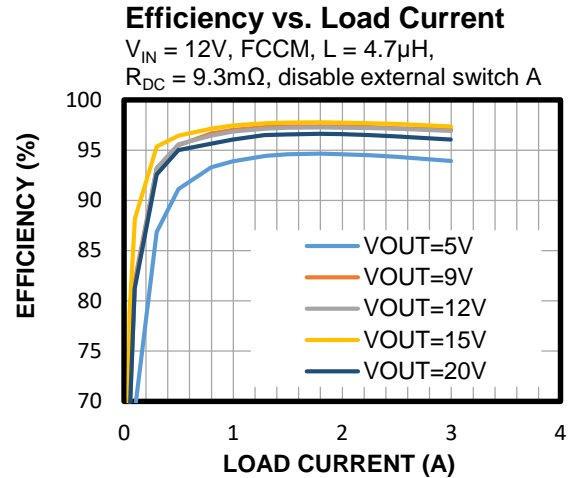
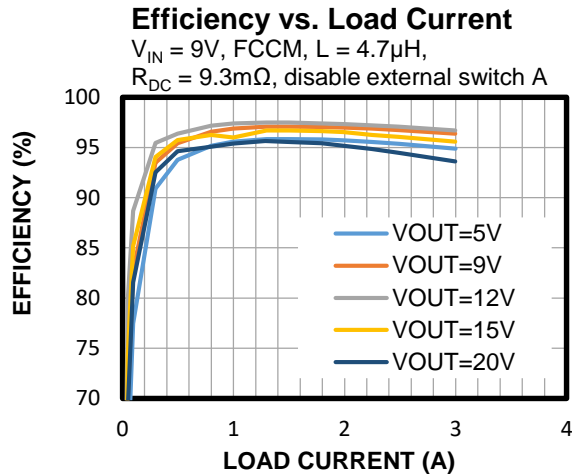
Parameter	Symbol	Condition	Min	Typ	Max	Units
Receiver input impedance	$Z_{BMC\_RX}$		1			M $\Omega$
<b>I<sup>2</sup>C Interface Specifications <sup>(8)</sup></b>						
Input logic high	$V_{IH}$	I <sup>2</sup> C pull-up VDD can be to 1.8V to 5V	1.26			V
Input logic low	$V_{IL}$				0.54	V
Output voltage logic low	$V_{OUT\_L}$				0.45	V
SCL clock frequency	$f_{SCL}$			400		kHz
SCL high time	$t_{HIGH}$		60			ns
SCL low time	$t_{LOW}$		160			ns
Data set-up time	$t_{SU\_DAT}$		10			ns
Data hold time	$t_{HD\_DAT}$			70		ns
Set-up time for repeated start condition	$t_{SU\_STA}$		160			ns
Hold time for repeated start condition	$t_{HD\_STA}$		160			ns
Bus free time between a start and a stop condition	$t_{BUF}$		160			ns
Set-up time for stop condition	$t_{SU\_STO}$		160			ns
Rising time of SCL and SDA	$t_R$		10		300	ns
Falling time of SCL and SDA	$t_F$		10		300	ns
Pulse width of suppressed spike	$t_{SP}$		0		50	ns
Capacitance bus for each bus line	$C_B$				400	pF
SCL low time	$t_{LOW}$		160			ns

**Note:**

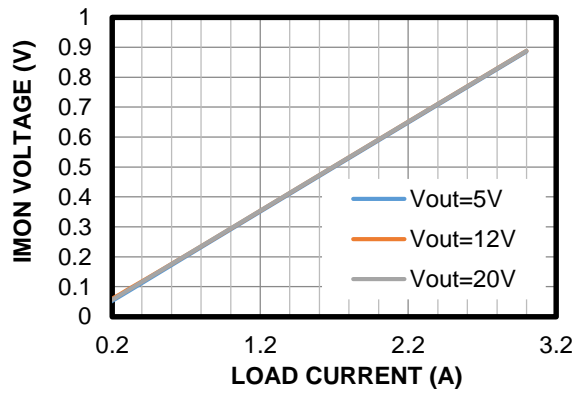
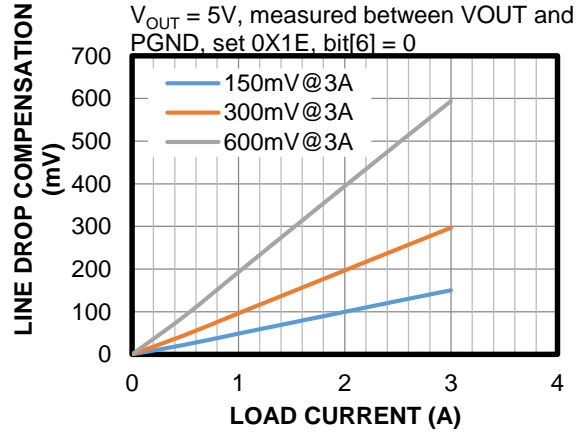
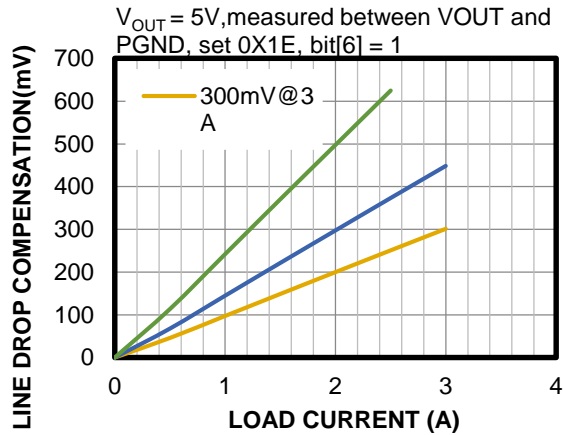
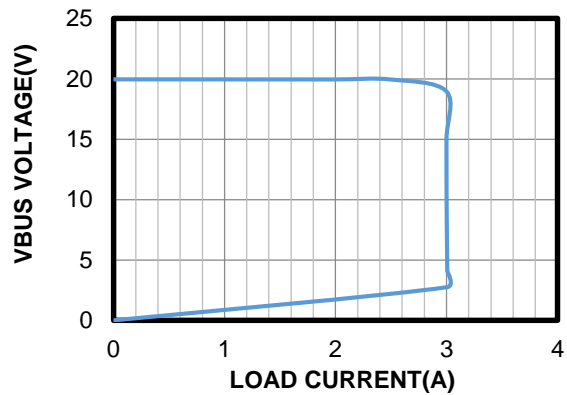
8) Guaranteed by characterization sample test.

## TYPICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



**TYPICAL CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

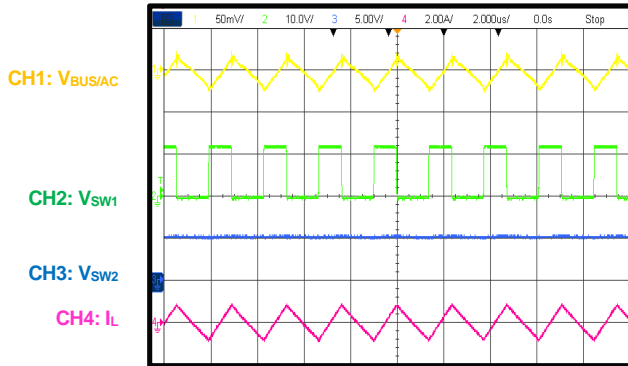
**IMON Voltage vs. Load Current**

**Line Drop Compensation vs. Load Current**

**Line Drop Compensation vs. Load Current**

**VBUS Voltage vs. Load Current**


## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

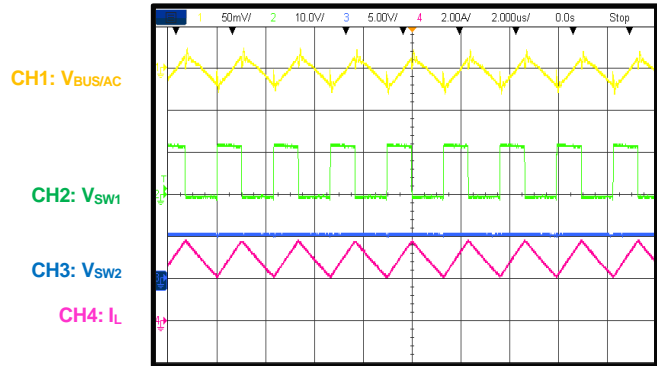
### Output Voltage Ripple

$V_{BUS} = 5V$ , load = 0A



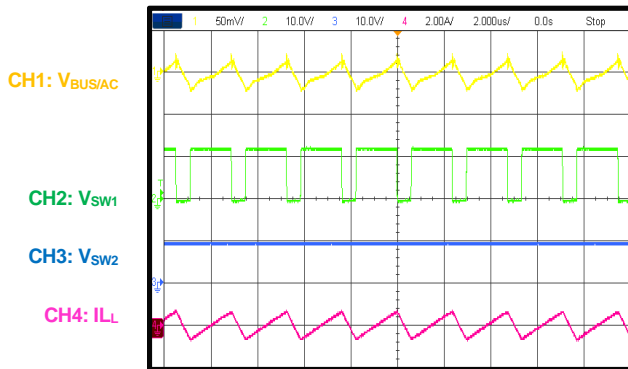
### Output Voltage Ripple

$V_{BUS} = 5V$ , load = 3A



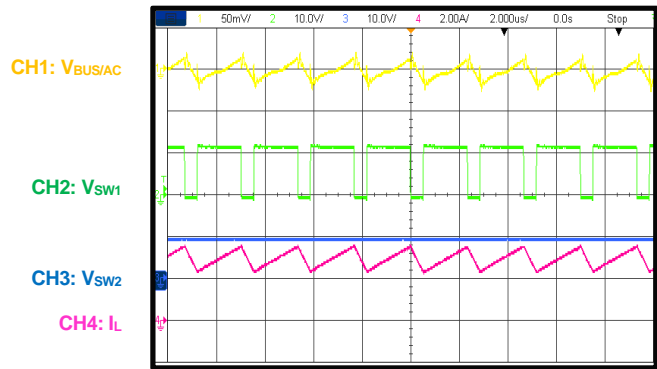
### Output Voltage Ripple

$V_{BUS} = 9V$ , load = 0A,



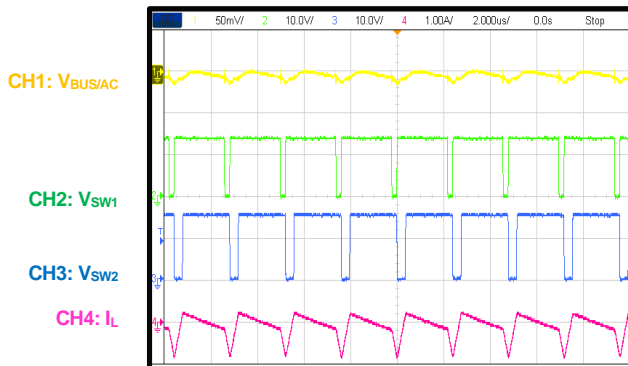
### Output Voltage Ripple

$V_{BUS} = 9V$ , load = 3A,



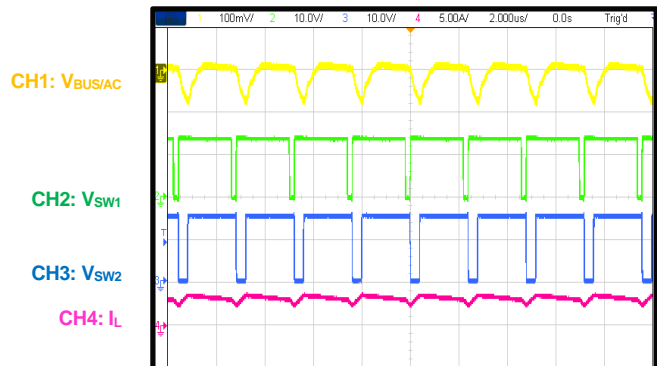
### Output Voltage Ripple

$V_{IN} = 14V$ ,  $V_{BUS} = 15V$ , load = 0A



### Output Voltage Ripple

$V_{IN} = 14V$ ,  $V_{BUS} = 15V$ , load = 3A

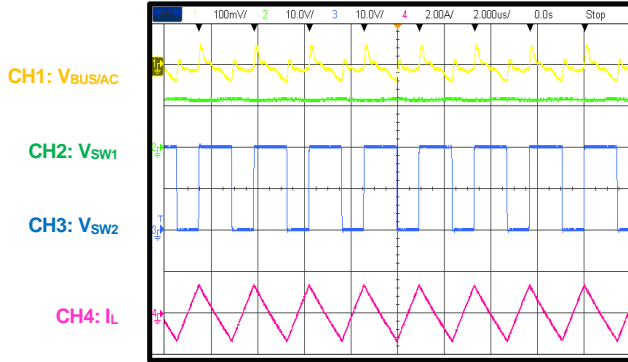


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

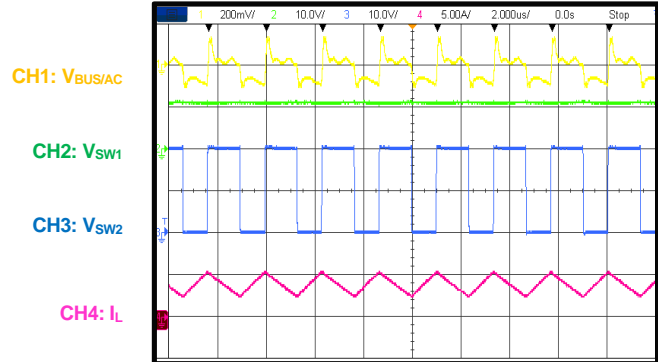
### Output Voltage Ripple

$V_{BUS} = 20V$ , load = 0A



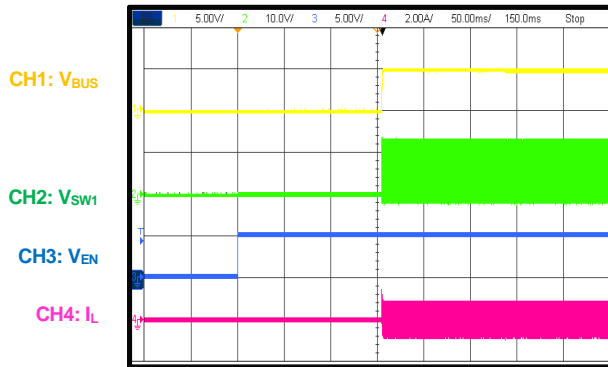
### Output Voltage Ripple

$V_{BUS} = 20V$ , load = 2.25A



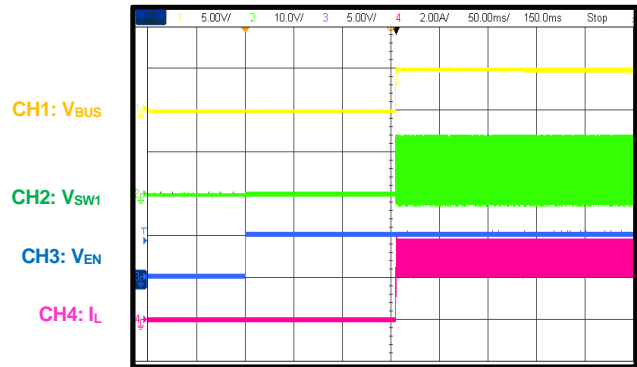
### EN Pin Enabled

CC1 connected to a 5.1kΩ  $R_d$  resistor, load = 0A



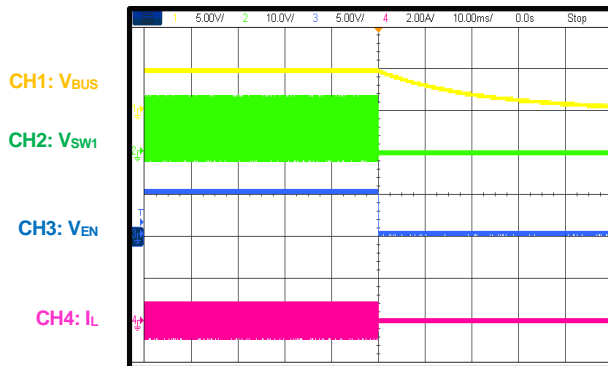
### EN Pin Enabled

CC1 connected to a 5.1kΩ  $R_d$  resistor, load = 3A



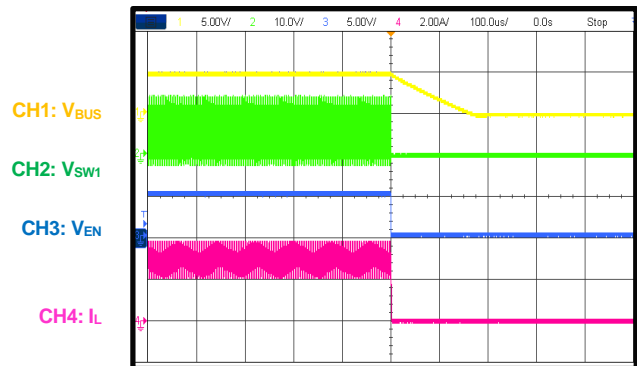
### EN Pin Disabled

CC1 connected to a 5.1kΩ  $R_d$  resistor, load = 0A



### EN Pin Disabled

CC1 connected to a 5.1kΩ  $R_d$  resistor, load = 3A



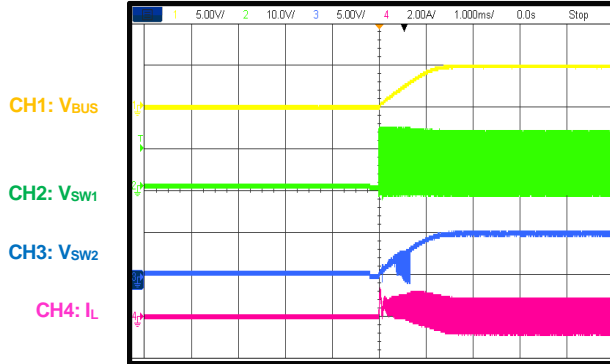


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

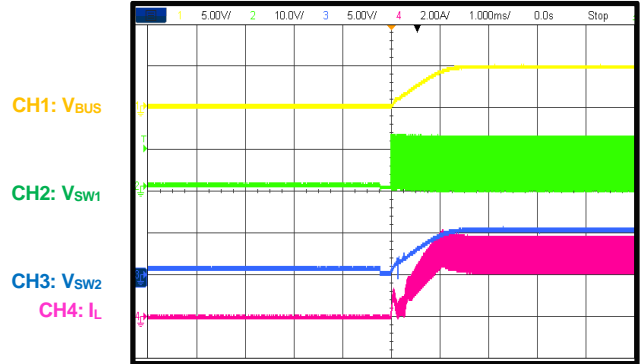
**Input Start-Up**

Load = 0A, CC1 connected to a 5.1kΩ  $R_d$  resistor



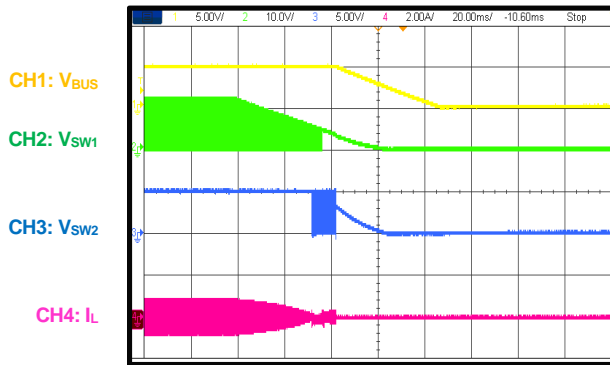
**Input Start-Up**

Load = 3A, CC1 connected to a 5.1kΩ  $R_d$  resistor



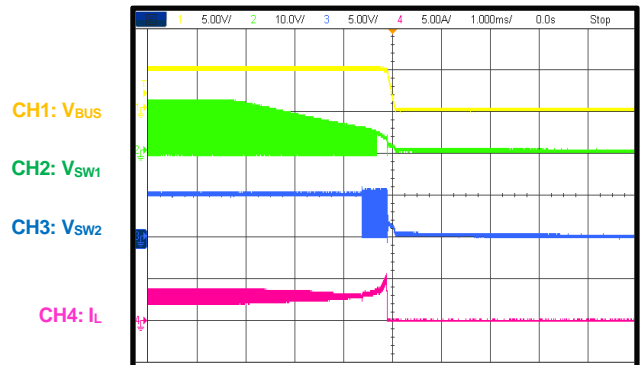
**Input Shutdown**

Load = 10mA

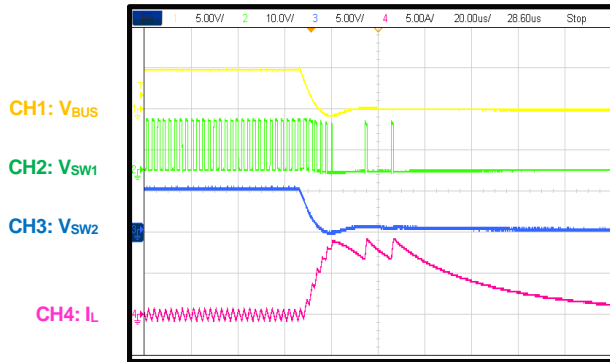


**Input Shutdown**

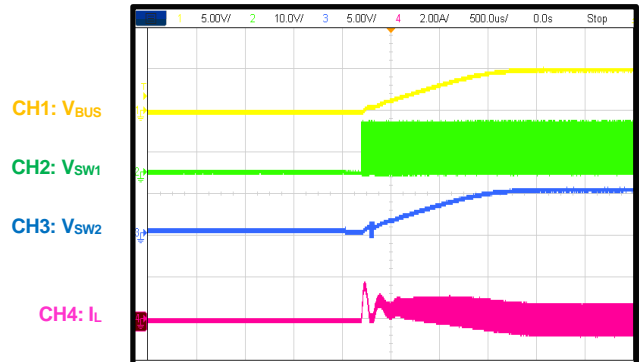
Load = 3A



**SCP Entry**



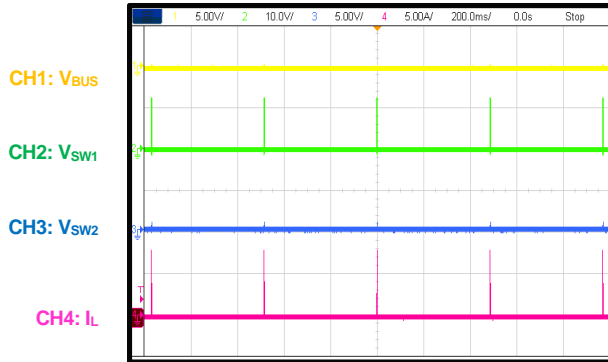
**SCP Recovery**



## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

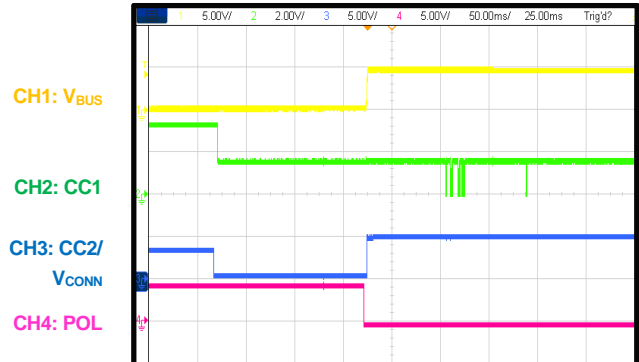
$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**SCP Steady State**



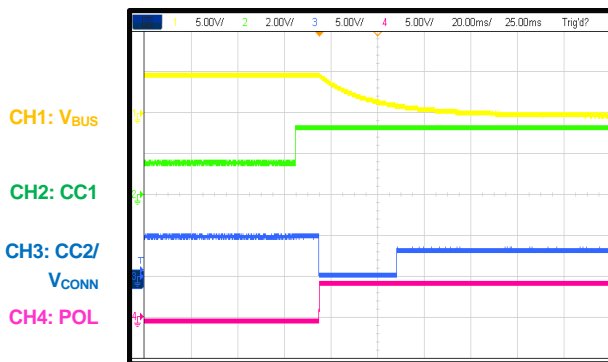
**CC1 Connected to  $R_d$  to Enable  $V_{BUS}$**

$I_{OUT} = 0A$ , CC2 connected to a  $1k\Omega R_a$  resistor



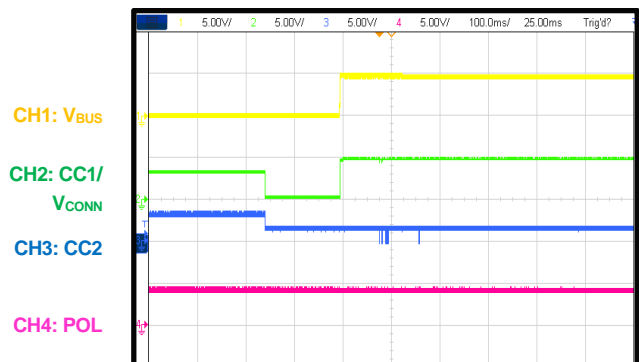
**CC1 Disconnected from  $R_d$  to Disable  $V_{BUS}$**

$I_{OUT} = 0A$ , CC2 connected to a  $1k\Omega R_a$  resistor



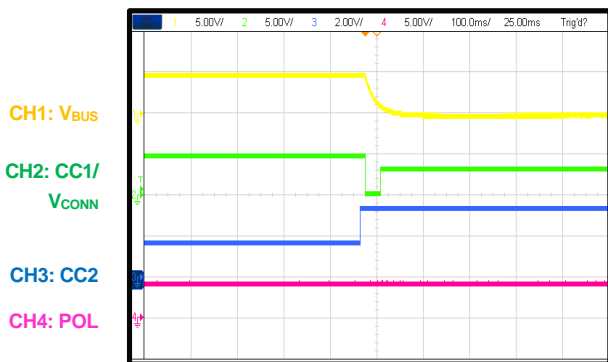
**CC2 Connected to  $R_d$  to Enable  $V_{BUS}$**

$I_{OUT} = 0A$ , CC1 connected to a  $1k\Omega R_a$  resistor

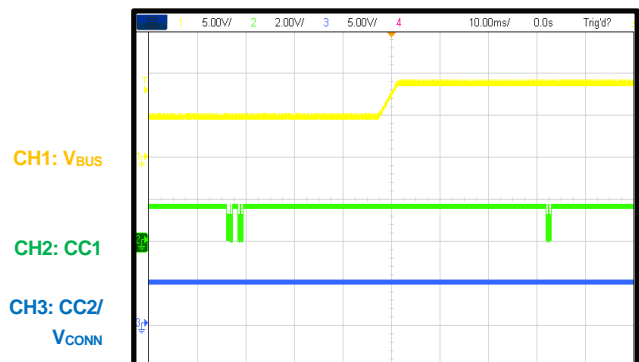


**CC2 Disconnected from  $R_d$  to Disable  $V_{BUS}$**

$I_{OUT} = 0A$ , CC1 connected to  $1k\Omega R_a$  resistor



**PDO Transition  
5V PDO to 9V PDO**



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

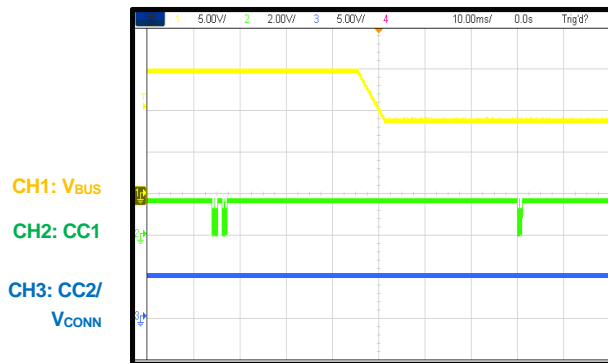
**PDO Transition**  
9V PDO to 5V PDO



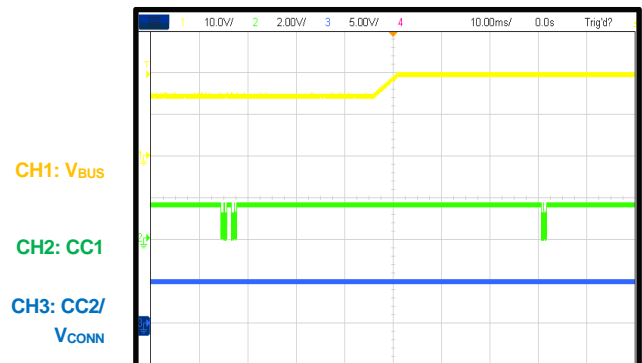
**PDO Transition**  
9V PDO to 15V PDO



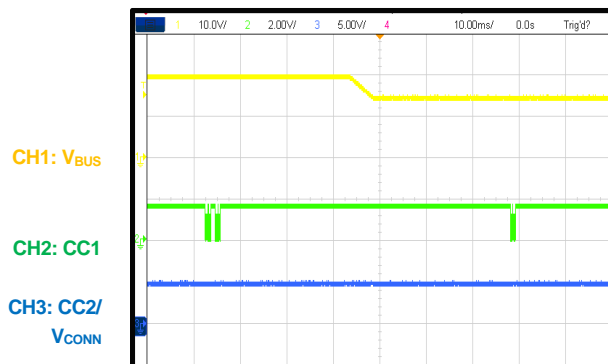
**PDO Transition**  
15V PDO to 9V PDO



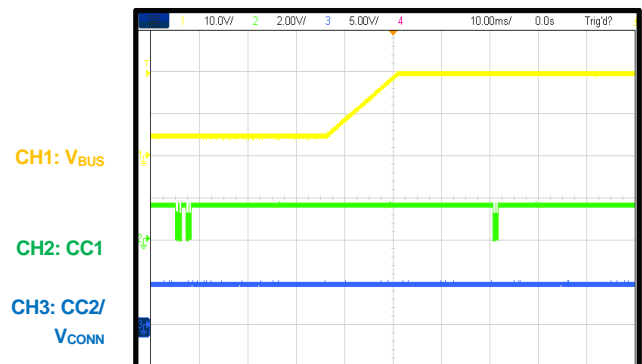
**PDO Transition**  
15V PDO to 20V PDO



**PDO Transition**  
20V PDO to 15V PDO



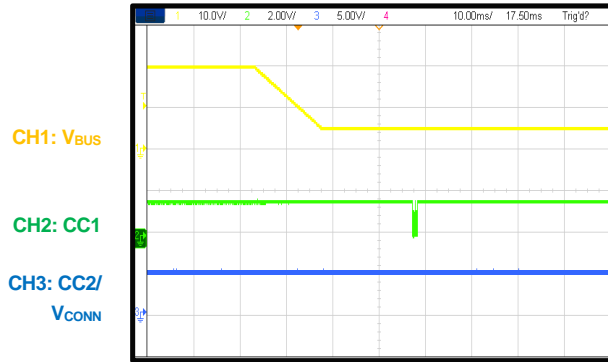
**PDO Transition**  
5V PDO to 20V PDO



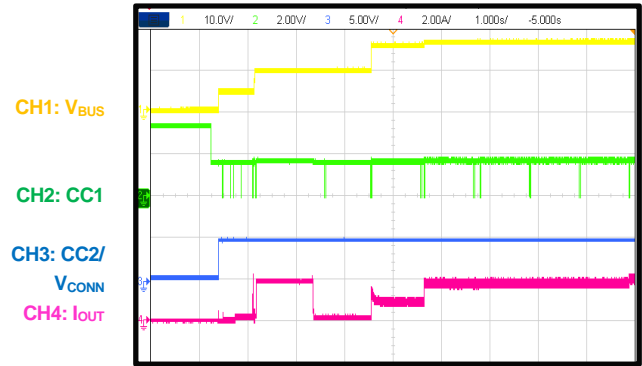
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

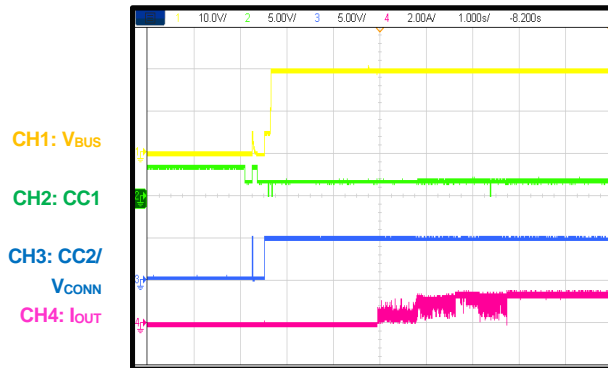
**PDO Transition**  
20V PDO to 5V PDO



**Mobile Phone Charging Test**  
Phone requests 3.3V to 21V APDO

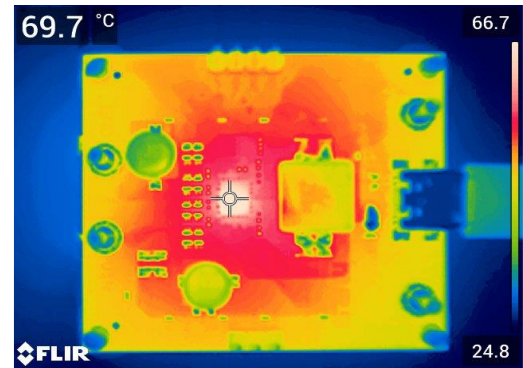


**Laptop Charging Test**  
Laptop requests 20V PDO



**Thermal Image**

$V_{IN} = 13.5V$ ,  $V_{OUT} = 20V$ ,  $I_{OUT} = 3A$ ,  
 $f_{SW} = 420kHz$ , 4.3cmx5cm PCB,  
top/bottom layer: 2oz; mid-layer 1 and 2: 1oz,  
enable external switch A



## FUNCTIONAL BLOCK DIAGRAM

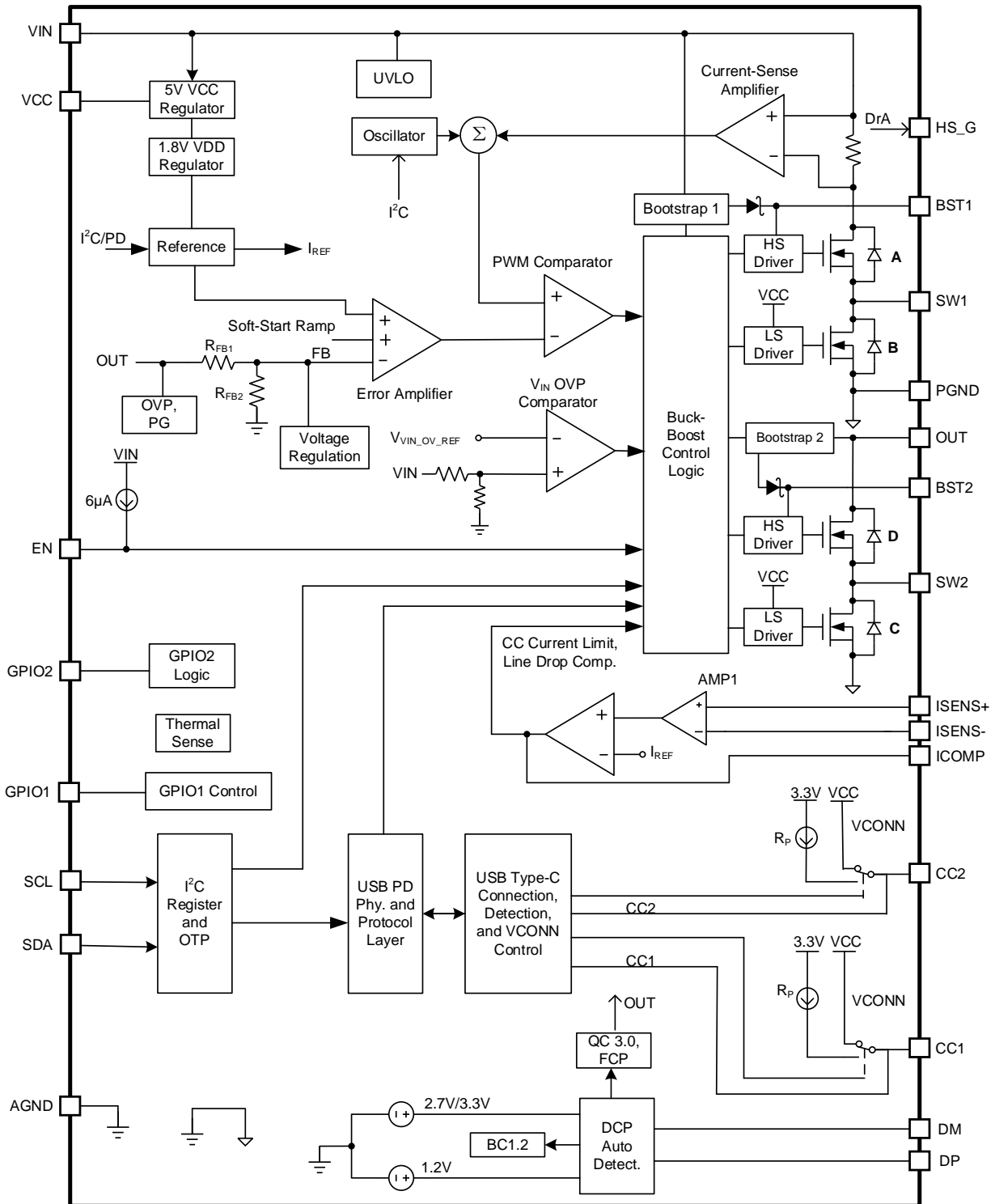


Figure 2: Functional Block Diagram

## OPERATION

The MPQ4242 is a buck-boost converter with four integrated switches and USB charging protocols. The buck-boost converter works in current mode, which provides a fast transient response for buck, boost, and buck-boost modes. One special buck-boost control strategy provides high efficiency across the full input range and smooths transitions between different modes. Figure 2 on page 21 shows the internal block diagram.

### Pulse-Width Modulation (PWM) Operation

The MPQ4242 operates in a fixed-frequency peak current mode control to regulate the output voltage ( $V_{OUT}$ ). The internal clock initiates the PWM cycle and turns on the related power switch. The switch remains on until its current reaches the value set by the COMP voltage ( $V_{COMP}$ ). When the power switch is off, it remains off until the next clock cycle starts. The switching frequency ( $f_{SW}$ ) can be configured to 250kHz or 420kHz via the I<sup>2</sup>C.

### Buck-Boost Operation

The MPQ4242 can regulate  $V_{OUT}$  to be above, below, or equal to the input voltage ( $V_{IN}$ ). Figure 3 shows a buck-boost power structure with one inductor and four switches (SWA, SWB, SWC, and SWD).

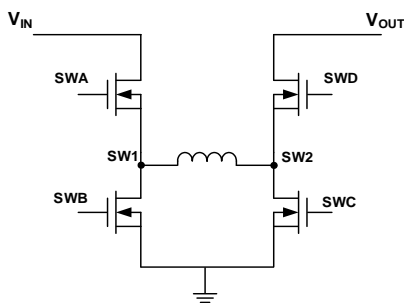


Figure 3: Buck-Boost Topology

Buck mode, boost mode, and buck-boost mode can have different  $V_{IN}$  inputs (see Figure 4).

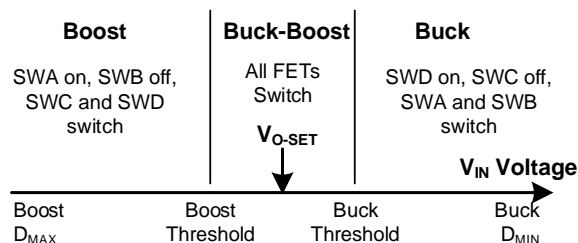


Figure 4: Buck-Boost Operation Range

### Buck Mode ( $V_{IN} > V_{OUT}$ )

When  $V_{IN}$  exceeds  $V_{OUT}$ , the MPQ4242 works in buck mode. In buck mode, switch A (SWA) and switch B (SWB) switch for buck regulation. Meanwhile, switch C (SWC) is off, and switch D (SWD) stays on to conduct the inductor current ( $I_L$ ).

SWA works with a peak current mode control logic, and SWB turns on until the  $t_{CLK}$  times out. In each buck mode cycle, SWA turns on to charge  $I_L$ . When  $I_L$  reaches the value set by  $V_{COMP}$ , SWA turns off and SWB turns on. SWB stays on until the next clock begins. Then SWA turns on and the cycle repeats. The COMP signal is the error amplifier (EA) output from the  $V_{OUT}$  feedback and the internal FB reference voltage. Figure 5 shows the buck mode waveform.

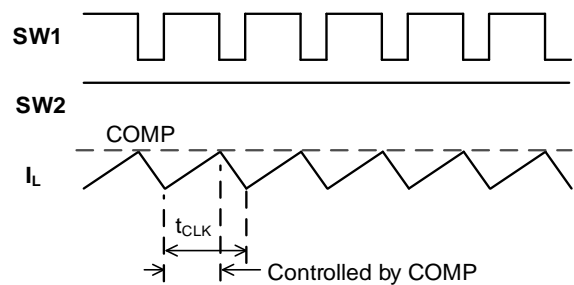


Figure 5: Buck Mode Waveform

### Boost Mode ( $V_{IN} < V_{OUT}$ )

When  $V_{IN}$  is below  $V_{OUT}$ , the MPQ4242 works in boost mode. In boost mode, SWC and SWD switch for boost regulation. Meanwhile, SWB is off and SWA stays on to conduct  $I_L$ .

SWC turns on at the beginning of each clock cycle. SWC turns off when  $I_L$  reaches the value set by  $V_{COMP}$ . SWD turns on until  $t_{CLK}$  times out to boost  $I_L$  to the output. Figure 6 shows the boost work waveform.

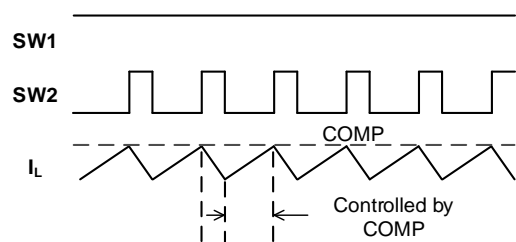
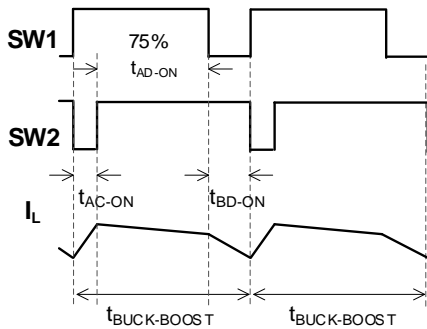


Figure 6: Boost Waveform

### Buck-Boost Mode ( $V_{IN} \approx V_{OUT}$ )

When  $V_{IN}$  is almost equal to  $V_{OUT}$ , the converter cannot provide enough energy to the load in buck mode due to SWA's minimum off time. In boost mode, the converter supplies too much power to the load due to SWC's minimum on time. Under these conditions, the MPQ4242 adopts buck-boost control to regulate the output (see Figure 7).



**Figure 7: Buck-Boost Waveform**

If  $V_{IN}$  is almost equal to  $V_{OUT}$ , buck-boost mode activates. The MOSFET turn-on sequence is as follows:

1. SWA and SWC
2. SWA and SWD
3. SWB and SWD

Throughout this process,  $I_L$  can reach the  $V_{COMP}$  requirement, and supply enough current to the output.

The SWA and SWD turn-on time is fixed to 75% of the buck-boost operation frequency.

If the buck mode minimum off time is almost reached, the IC enters buck-boost mode. If  $V_{IN}$  is about 10% above  $V_{OUT}$  in buck-boost mode, the IC changes to buck mode. If  $V_{IN}$  is about 10% below  $V_{OUT}$ , the IC enters boost mode. If the boost mode minimum on time is almost reached, the IC enters buck-boost mode.

### External High-Side MOSFET Gate Driver

An external N-channel MOSFET can be added to improve system efficiency, especially for PD applications exceeding 45W. For applications below 45W, an external MOSFET is not required, and EXT\_HS\_FET\_RON should be set to 000b.

The external MOSFET is paralleled with the internal SWA. To accurately sense the input current, a  $5m\Omega$  to  $12m\Omega$   $R_{DS(ON)}$  MOSFET is

recommended. The EXT\_HS\_FET\_RON configuration value should match (or be close to) the MOSFET's real  $R_{DS(ON)}$  under a  $10V_{GS}$  condition. The external MOSFET only turns on in boost mode when  $V_{IN}$  is significantly below  $V_{OUT}$ .

### 5V Internal VCC Regulator

The 5V internal regulator powers the CC pin's pull-up, VCONN, and most of the internal logic circuitries. The regulator takes the  $V_{IN}$  input and operates across the full  $V_{IN}$  range. When  $V_{IN}$  exceeds 5V, the regulator's output is in full regulation. If  $V_{IN}$  is below 5V, the output decreases with  $V_{IN}$ .

The VCC pin can support 0.1W of output power ( $P_{OUT}$ ). The VCC pin requires a  $2.2\mu F$  ceramic decoupling capacitor.

### Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPQ4242's UVLO comparator monitors  $V_{IN}$ .

### Internal Soft-Start

Soft start prevents the converter's  $V_{OUT}$  from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage ( $V_{SS}$ ) that ramps up from 0V to 5V. When SS is below the reference voltage ( $V_{REF}$ ), the error amplifier uses  $V_{SS}$  as the reference. When  $V_{SS}$  exceeds  $V_{REF}$ , the error amplifier uses  $V_{REF}$  as the reference. The SS time is internally set to 1ms for a 5V  $V_{OUT}$ .

If the output of the MPQ4242 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the internal feedback voltage.

### Constant Current (CC) Mode Over-Current-Protection (OCP)

The MPQ4242 senses the ground current via an external current-sense resistor. The device uses this information to limit the output current ( $I_{OUT}$ ). This is a highly accurate current limit. If  $I_{OUT}$  exceeds the current-limit threshold, the MPQ4242 enters constant current (CC) limit mode, and the current amplitude is limited.

If the MPQ4242 works in fixed PDO mode, it sends a hard reset message once  $I_{OUT}$  exceeds the constant current limit. If the MPQ4242 works



in APDO mode and continues to reduce the load resistance,  $V_{OUT}$  drops until reaches its under-voltage (UV) threshold (about 3V). If a UV condition is triggered, the MPQ4242 sends a hard reset message. If  $I_{OUT}$  still exceeds the over-current protection (OCP) threshold, the MPQ4242 enters hiccup mode to periodically restart the part.

This protection is especially useful when the output is dead-short to ground. This operation greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MPQ4242 exits hiccup mode once the OC condition is removed.

The current limit threshold can be set from 1A to 6.35A (with a 50mA resolution) via the I<sup>2</sup>C.

### Peak and Valley Current Limit.

In addition to the output CC limit, the MPQ4242 also has SWA peak current and SWB valley current limits.

In buck mode and buck-boost mode, both the SWA peak current limit and the SWB valley current limit work as thresholds. The SWB's valley current limit has a 6.7A falling threshold. In boost mode, only the SWA peak current limit threshold operates. The peak current limit can be configured via the I<sup>2</sup>C or one-time-programmable (OTP) memory.

### Output Over-Voltage Protection (OVP)

The MPQ4242 has output over-voltage protection (OVP). If  $V_{OUT}$  exceeds 117% of  $V_{REF}$ , SWA, SWB, SWC, and SWD turn off. The resistor discharge path from the OUT pin to ground turns on. When  $V_{OUT}$  drops to 107% of  $V_{REF}$ , the chip returns to normal operation.

The absolute output OVP threshold is about 25V. The discharge resistor turns on when absolute OVP is triggered.

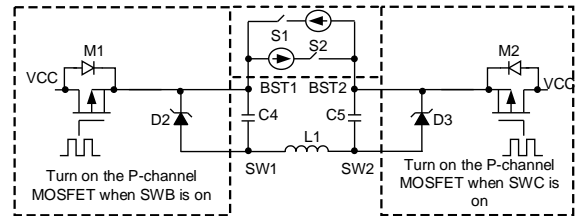
### Input Over-Voltage Protection ( $V_{IN}$ OVP)

The MPQ4242 has input OVP. If  $V_{IN}$  exceeds its OVP rising threshold (about 22V), SWA, SWB, SWC, and SWD turn off. The chip returns to normal operation when  $V_{IN}$  drops to its OVP falling threshold (about 20V).

$V_{IN}$  OVP is disabled by default, and it is controlled by OTP trimming. The MPQ4242-0000 does not have  $V_{IN}$  OVP. The MPQ4242-0001 provides  $V_{IN}$  OVP.

### Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. Its UVLO rising threshold is 2.2V, with a hysteresis of 150mV. The BST1 capacitor's voltage is regulated internally by VCC through D2, M1, and C4. The BST2 capacitor's voltage is regulated internally by VCC through D3, M2, and C5 (see Figure 8).



**Figure 8: Internal Bootstrap Charging Circuit**

In buck mode, S2 is always on, and BST2 is charged by BST1. In boost mode, S1 is always on, and BST1 is charged by BST2.

### Output Line Drop Compensation

The MPQ4242 is capable of compensating for a  $V_{OUT}$  drop.

If  $I_{OUT}$  is 0A, there is no compensation. If  $I_{OUT}$  is 3A, the line drop compensation voltage is 150mV. For example, if the USB output current exceeds 3A, the line drop compensation voltage stays at 150mV and does not rise. The line drop compensation value can be set to 150mV, 300mV, or 600mV via 0x18, bits[2:1]. Set 0x1E, bit[6] = 1 to enable an additional compensation voltage. Then the line drop compensation value can be set to 300mV, 450mV, or 750mV when the load is 3A.

Line drop compensation can be configured via the I<sup>2</sup>C or OTP. The compensated voltage is the same for all voltages.

For the default IC, line drop compensation is disabled in PPS mode. Line drop compensation can be enabled in PPS mode through factory OTP trimming.

### Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures.

If the silicon die temperature exceeds 175°C, the whole chip shuts down. When the temperature



falls below its lower threshold (about 155°C), the chip is enabled again.

## CHARGING MODE AUTO-DETECTION

### Legacy USB 2.0 Mode

The MPQ4242 integrates a USB-dedicated charging port automatic detection function that recognizes most mainstream portable devices. The device supports the following charging schemes:

- USB battery charging specification (BC1.2) / Chinese Telecommunications Industry Standard YD/T 1591-2009
- Apple 3A Divider Mode
- 1.2V/1.2V Mode
- QC 3.0
- Huawei FCP Class A

The automatic detection function is a state machine that supports all of the above DCP charging schemes. This function starts in 3A divider mode. If a device compliant to divider mode is connected, the MPQ4242 stays in divider mode. Meanwhile, 3.3V is applied to the DM pin, while 2.7V is applied to the DP pin.

If a BC1.2 or YD/T 1591-2009 compliant device is connected, the MPQ4242 operates in 1.2V/1.2V and BC1.2 DCP mode. In this scenario, DM and DP are shorted together with a resistance. The device then stays in this mode until the data line is released. If this occurs, the MPQ4242 returns to 3A divider mode.

When a QC 3.0 or FCP device (without PD protocol) is connected, the MPQ4242 can automatically enter high-voltage, quick charge mode.

The MPQ4242 supports BC1.2 charging downstream port (CDP) handshaking as well. This can be enabled by setting CDP\_EN to 1b via the I<sup>2</sup>C.

If a USB PD contract is established after the sink is connected, the QC 3.0 and FCP functions are disabled.

### USB Type-C Port

The USB Type-C receptacle, plug, and cable solution incorporates a configuration process to detect a downstream facing port (DFP) to upstream facing port (UFP) connection. This

detection function is used for V<sub>BUS</sub> management and can determine the host-to-device connection.

Initially, a DFP-to-UFP connection is detected by a host (DFP) when one of the CC pins at its USB Type-C receptacle senses a specified resistance at GND. Subsequently, DFP-to-UFP disconnect is detected when the CC pin that was terminated at its USB Type-C receptacle is no longer connected to GND via a specified resistance.

Power is not applied to the USB Type-C host or hub receptacle (VBUS or VCONN) until the DFP detects the presence of a connected device (UFP) port. When a DFP-to-UFP connection is detected, the DFP is expected to enable power to the receptacle and proceed to normal USB operation with the connected device. When a DFP-to-UFP disconnect is detected, the port sourcing V<sub>BUS</sub> removes power.

The MPQ4242's power supply capability is rated for 5V @ 3A by default. V<sub>CONN</sub> is provided by the DFP to power cables with electronics that are plugged in. V<sub>CONN</sub> is provided power over the CC pin that is not connected to the cable's CC wire. The maximum output power of V<sub>CONN</sub> is 1W.

VCONN is disabled until R<sub>A</sub> is detected. R<sub>A</sub> is a pull-down resistor connected from the CC pin to GND. Its resistance must be below 1.2kΩ.

### USB Power Delivery (PD) 3.0

In USB power delivery (PD), pairs of directly connected ports negotiate the voltage, current, and/or the direction of power flow over the USB cable, using VBUS or the CC wire as the communication channel. The mechanisms used operate independently of other USB methods that negotiate power. USB Type-C connectors can support the CC wire as the communication channel.

The USB PD engine can disable the clock and enter sleep mode if no PD command is detected. The input current is typically 150μA in sleep mode. Figure 9 on page 26 shows the USB PD communication stack.

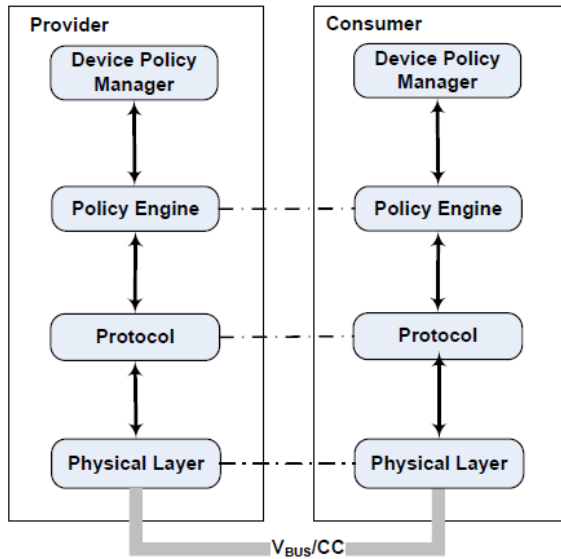


Figure 9: USB PD Communication Stack

Table 1 shows the functions and DFP commands supported by the MPQ4242.

Table 1: Control Message

Transmitted Message	Received Message
ACCEPT	GET_PPS_STATUS
GET_STATUS	GET_STATUS
GOODCRC	GOODCRC
NOT_SUPPORTED	NOT_SUPPORTED
PS_RDY	REJECT
REJECT	SOFT_RESET
SOFT_RESET	HARD_RESET
HARD_RESET	VCONN_SWAP
-	GET_SOURCE_CAP
-	GET_SOURCE_CAP_EXTENDED

Table 2 shows the data messages.

Table 2: Data Message

Transmitted Message	Received Message
SOURCE_CAPABILITIES	SINK_CAPABILITIES
BIST	REQUEST
ALERT	BIST
-	ALERT

Table 3 shows the extended messages.

Table 3: Extended Message

Transmitted Message	Received Message
STATUS	-
PPS_STATUS	-
SOURCE_CAPABILITIES_EXTENDED	-

Figure 10 shows the MPQ4242’s device policy manager function block.

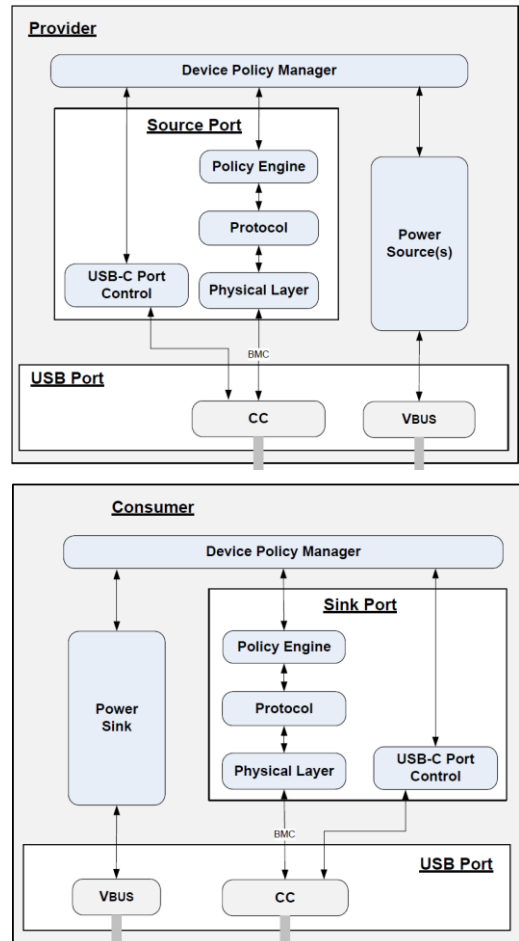


Figure 10: Device Policy Manager

Figure 11 shows a PD contract handshake sequence for the MPQ4242.

#	CH	OS	Power	Data	Cable Plug	Type
0	CC2	SOP'			UFP or DFP	Vendor_Defined
1	CC2	SOP'			Cable Plug	GoodCRC
2	CC2	SOP'			Cable Plug	Vendor_Defined
3	CC2	SOP'			UFP or DFP	GoodCRC
4	CC2	SOP	Source	DFP		Source_Capabilities
5	CC2	SOP	Sink	UFP		GoodCRC
6	CC2	SOP	Sink	UFP		Request
7	CC2	SOP	Source	DFP		GoodCRC
8	CC2	SOP	Source	DFP		Accept
9	CC2	SOP	Sink	UFP		GoodCRC
10	CC2	SOP	Source	DFP		PS_RDY
11	CC2	SOP	Sink	UFP		GoodCRC

Figure 11: PD Contract Handshake

### VCONN Power Supply

The integrated VCONN power supply has a maximum of 100mW. The power switch connected from VCC to VCONN has a current limit. During a VCONN short to ground event, the MPQ4242 turns off VCONN.

For a 1W VCONN application, an external VCONN supply should be applied to GPIO2.

### LED PWM Driver

The GPIO2 pin can be configured as a PWM output to drive an LED. By default, it is 25kHz, with a 50% duty cycle PWM and a maximum 15mA capability.

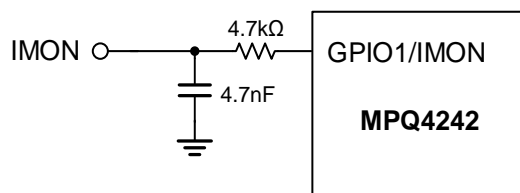
The PWM duty cycle can be set between 5% and 100% (with a 1% resolution) via the I<sup>2</sup>C.

### EN Off Time

The MPQ4242 has a configurable EN off time. When the EN pin is pulled low, the device operates at full functionality until the timer elapses. The maximum EN off delay is 120 minutes. If the EN pin is pull high within this time, the counter is reset.

### Current Monitor Output

When the GPIO1 pin is set as IMON, the MPQ4242 senses the average load current through a current-sense resistor. The IMON amplifier outputs a voltage signal on the GPIO1 pin. This signal is amplified from the voltage difference between the ISEN+ and ISEN- pins. It is recommended to place a 4.7nF + 4.7kΩ filter on the GPIO1 pin (see Figure 12). The minimum load that IMON can recognize is 0.2A.



**Figure 12: IMON Connection**

The relationship between the IMON voltage and the load current can be calculated with Equation (1):

$$V_{\text{IMON}} = \text{Gain} \times I_{\text{OUT}} \times R_{\text{SENS}} \quad (1)$$

Where Gain is 27.5V/V, and R<sub>SENS</sub> = 10mΩ.

When automatic PFM/PWM mode is set up, the IMON function can only work normally when the part enters continuous conduction mode (CCM).

### NTC Function

When the GPIO2 pin is set to the NTC function, the device compares the NTC voltage to V<sub>REF</sub>. If the NTC voltage is below the threshold, the MPQ4242 initiates thermal shutdown protection. In this scenario, the device will either shut down or reduce the PD power. The response can be selected via NTC\_MODE.

If NTC\_MODE is set to 1, OTW2\_NTC\_PDP determines the value to which PD power should be reduced. OTW2\_NTC\_PDO\_SELECT sets which PDO voltage is enabled after entering NTC mode. See Table 4 on page 29 for more details.

If the NTC voltage rises above the recovery threshold, the device recovers to a normal state. The I<sup>2</sup>C can set one of two NTC recovery hysteresis values. There is no 16s recover delay.

### NTC2 Function

When the GPIO1 pin is set to the NTC2 function, the device compares the NTC2 voltage to V<sub>REF</sub>. If the NTC2 voltage drops below this threshold, the MPQ4242 triggers power sharing. When the power share function is triggered, PD power rating drops to the value set by PS\_PDP\_THD. Table 4 on page 29 shows the PDO / APDO voltage and current.

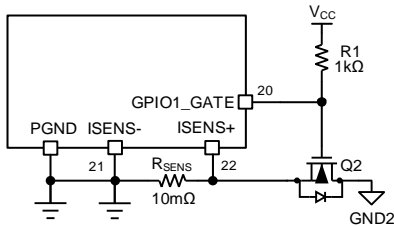
If the NTC2 voltage rises above the recovery threshold, the MPQ4242 exits power sharing. NTC\_HYSTERESIS sets the hysteresis, which is also sets the hysteresis for the GPIO1 pin's NTC function.

The NTC\_MODE, OTW2\_NTC\_PDO\_SELECT, and OTW2\_NTC\_PDP bits do not control the NTC2 pin's behavior.

If GPIO2 is set to the power share function while GPIO1 is set for the NTC2 function, the MPQ4242 enters power sharing when either NTC2 or GPIO2\_POWER\_SHARE is triggered.

### Battery to Ground Short Protection Driver

The GPIO1 pin can be set to the GATE function for GND to battery short protection. If a battery to output ground (GND2) short occurs, the GATE pin pulls low and Q2 turns off. Figure 13 on page 28 shows the battery to ground short driver.



**Figure 13: Battery Short-to-Ground Driver**

### Over Temperature Warning (OTW) Function

The MPQ4242 senses its die temperature internally. If the chip’s temperature exceeds the OTW1 threshold, the MPQ4242 reduces the PD power state to the value set by OTW1\_PDP. OTW1\_PDO\_SELECT sets which PDO voltage is enabled after entering OTW1 mode. Table 4 on page 29 shows the OTW\_PDO\_SELECT function.

If the die temperature continues increasing and triggers the second threshold set by OTW2, the MPQ4242 reduces the PD power to the level set by OTW2\_NTC\_PDP.

OTW2\_NTC\_PDO\_SELECT sets which PDO voltage is enabled. The MPQ4242 waits 16 seconds after the OTW condition is removed before recovering to a normal PD rating.

### Low-Battery Operation

During the first  $V_{IN}$  start-up, the MPQ4242 is delayed for 1s before detecting  $V_{IN}$ .

If the MPQ4242 detects that the battery voltage (its  $V_{IN}$  voltage) is lower than the VBATT\_LOW\_THLDD1 falling threshold for the VBATT\_LOW\_BLK deglitch time, it reduces the PD power rating according to the set value. Meanwhile, VBATT\_LOW1\_FLAG is set. If there is a PD contract, the PD engine resends the updated PDO with a reduced PDP. The PDO list is determined by VBATT\_L1\_PDO\_SELECT.

If the MPQ4242 detects that the battery voltage (its  $V_{IN}$  voltage) is below the VBATT\_LOW\_THLDD2 falling threshold for the VBATT\_LOW\_BLK deglitch time, it reduces the PD power rating according to the set value. Meanwhile, VBATT\_LOW2\_FLAG is set. If there is a PD contract, the PD engine resends the

updated PDO with a reduced PDP. The PDO list is determined by VBATT\_L2\_PDO\_SELECT.

If the MPQ4242 detects that the battery voltage (its  $V_{IN}$  voltage) is below the VBATT\_LOW\_THLDD3 falling threshold for the VBATT\_LOW\_BLK deglitch time, it shuts down.

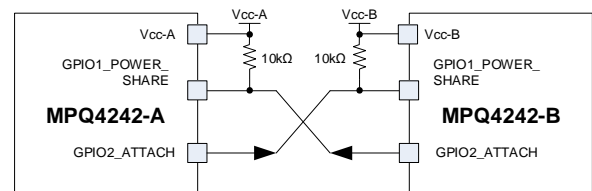
When the battery voltage recovers and exceeds the VBATT\_LOW\_THLDD rising threshold with a 1s digital deglitch time, the PDO recovers to normal PDP.

There are three battery voltage ( $V_{BATT}$ ) low thresholds: VBATT\_LOW\_THLDD1, VBATT\_LOW\_THLDD2, and VBATT\_LOW\_THLDD3. Accordingly, VBATT\_LOW1\_PDP and VBATT\_LOW2\_PDP define the MPQ4242’s reduced PDP level. During the MPQ4242’s first start-up, the internal VBATT\_LOW\_FLAG default state is 0. The VBATT\_LOW detection circuitry starts to work when a USB Type-C receptacle is attached; it is reset by UVLO or an EN shutdown.

### POWER SHARE FUNCTION

#### GPIO1\_POWER\_SHARE

The GPIO1\_POWER\_SHARE pin can accept an external input voltage. If the second MPQ4242 (MPQ4242-B) detects that a valid sink is attached in, the first MPQ4242’s (MPQ4242-A) GPIO1\_POWER\_SHARE pin is pulled down by the MPQ4242-B’s GPIO2\_ATTACH pin (see Figure 14).



**Figure 14: Power Share Connection Between Two MPQ4242s (e.g. Cut Total Power to 50% / 50%)**

When the power share function is triggered, the PDO list and current are determined by PS\_PDP\_THD and PS\_PDP\_THD\_PDO\_SELECT (see Table 4 on page 29). For example, a 3.3V to 21V APDO current rating is can be calculated as  $45W / 21V = 2.1A$ .

**Table 4: PDO Voltage and Current Set Table based on the PS\_PDP\_THD and PS\_PDP\_THD\_PDO\_SEL**

PDO List	5V (Fixed)	9V (Fixed)	12V (Fixed)	15V (Fixed)	20V (Fixed)	5V (Prog.)	9V (Prog.)	15V (Prog.)	20V (Prog.)
Output Current	PDP / 5 <sub>(9)</sub>	PDP / 9	PDP / 12	PDP / 15	PDP / 20 <sub>(10)</sub>	PDP / 5.9	PDP / 11	PDP / 16	PDP / 21 <sub>(10)</sub>
PS_PDP_THD_PDO_SEL Register Selection Bit <sup>(13)</sup>	x	1	0	1	1	1	1	0	0
PS_PDP_THD = 22.5W	5V, 3A <sub>(11)</sub>	9V, 2.5A	-	15V, 1.5A	20V, 1.13A	3.3V to 5.9V, 3A <sub>(12)</sub>	3.3V to 11V, 2A	-	-

**Notes:**

- 9) A fixed 5V PDO is always enabled after enter power sharing.
- 10) The fixed PDO current is equal to PDP / Voltage. The maximum current is 3A for <20V fixed PDOs. The maximum current can be 5A for 20V PDO and all APDOs.
- 11) The minimum PDP is 5V x 1.5A = 7.5W. R<sub>p</sub> changes to 5V / 1.5A when PDP <15W.
- 12) The PPS current is calculated with PDP / 5.9V for 5V PPS; PDP / 11V for 9V PPS; PDP / 16V for 15V PPS; PDP / 21V for 20V PPS.
- 13) The registers PS\_PDP\_THD, PS\_PDO\_SELECT, VBATT\_L1\_PDO\_SELECT, VBATT\_L2\_PDO\_SELECT, OTW1\_PDO\_SELECT, and OTW2\_NTC\_PDO\_SELECT share the same format. The gray cells are set by 8-bit register values.

**GPIO2\_POWER\_SHARE**

The GPIO2\_POWER\_SHARE threshold is V<sub>TH\_PS</sub> (typically 1.87V). When the GPIO2 pin is set for the power share function, and the

MPQ4242-A detects that its GPIO2 voltage exceeds V<sub>TH\_PS</sub>, the power share function is triggered. In this scenario, the PDO list and current is determined by PS\_PDP\_THD and PS\_PDP\_THD\_PDO\_SELECT (see Table 5).

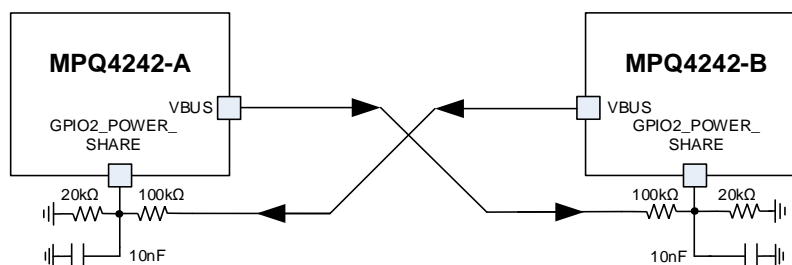
**Table 5: PDO Voltage and Current Set Table based on PS\_PDP\_THD and PS\_PDP\_THD\_PDO\_SEL**

PDO List	5V Fixed	9V Fixed	12V Fixed	15V Fixed	20V Fixed	5V Prog.	9V Prog.	15V Prog.	20V Prog.
Output Current	PDP / 5 <sub>(9)</sub>	PDP / 9	PDP / 12	PDP / 15	PDP / 20 <sub>(10)</sub>	PDP / 5.9	PDP / 11	PDP / 16	PDP / 21 <sub>(10)</sub>
PS_PDP_THD_PDO_SEL Register Selection Bit <sup>(13)</sup>	x	1	0	0	0	1	1	0	0
PS_PDP_THD = 15W	5V, 3A <sub>(11)</sub>	9V, 1.6A	-	-	x	3.3V to 5.9V, 3A <sub>(12)</sub>	3.3V to 11V, 1.35A	-	-

The MPQ4242 exits the power sharing status after the GPIO2 voltage drops below V<sub>TH\_PS</sub>. Figure 15 shows the GPIO2\_POWER\_SHARE connection block.

When V<sub>BUS</sub> exceeds 11.2V, the power share function is triggered.

Table 6 on page 30 shows the PDP of the MPQ4242-A and MPQ4242-B in the GPIO2\_POWER\_SHARE function.


**Figure 15: GPIO2 Power Share Connection Between Two MPQ4242s**



**Table 6: GPIO2 Power Share PDP Management In Dual-Channel Application <sup>(14)</sup>**

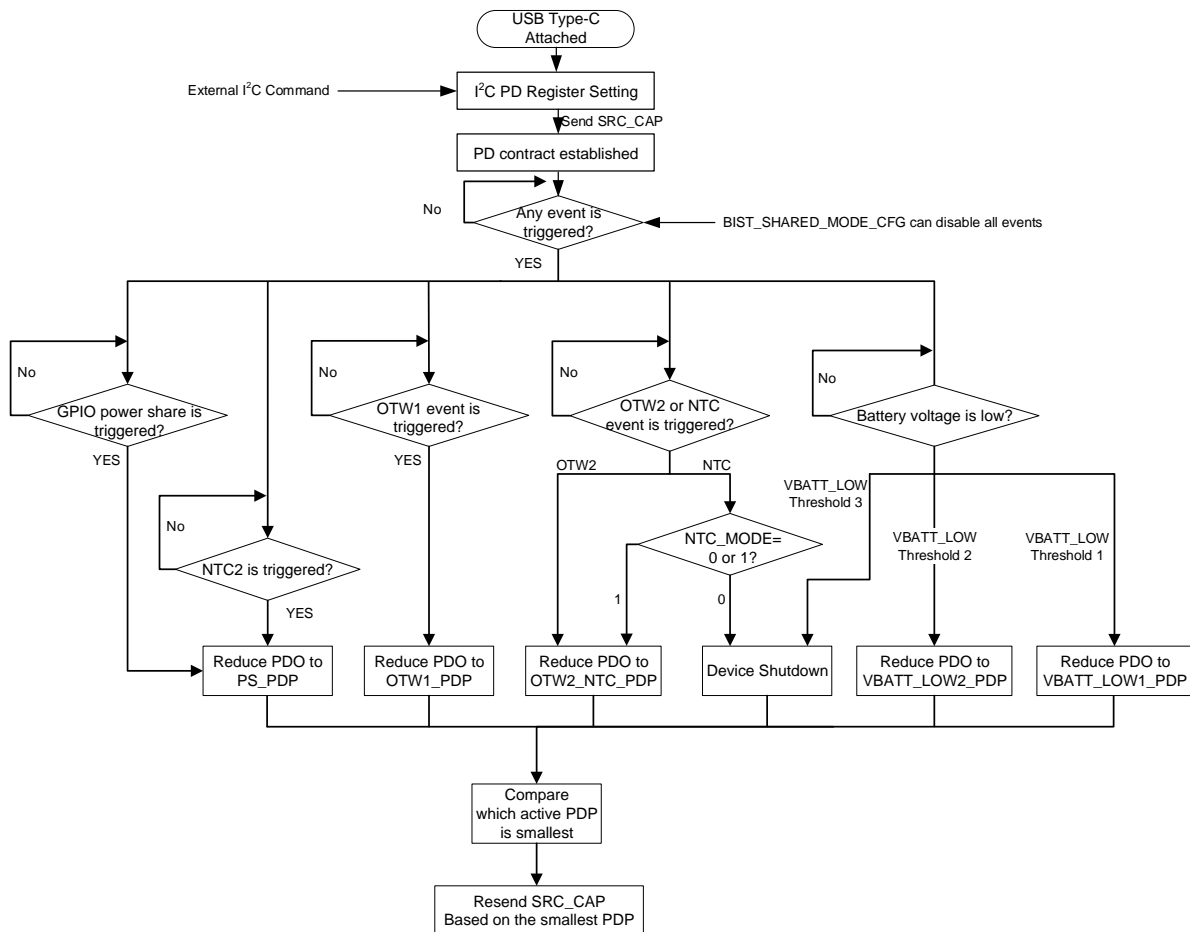
Column Format = <PD Contract W> (<Advertised Power W>)  
 Total Shared Power = 60W  
 Each Port PDP = 45W

Condition	USB Type-C Port 1	USB Type-C Port 2	Total Power
1	-- (45W) <sup>(15)</sup>	-- (45W) <sup>(15)</sup>	-
2	15W (45W)	-- (45W) <sup>(15)</sup>	15W
3	27W (45W)	-- (45W) <sup>(15)</sup>	27W
4	45W (45W)	15W (15W)	60W
5	27W (45W)	15W (45W)	42W
6	27W (45W)	27W (45W)	54W
7	15W (15W)	45W (45W)	60W
8	-- (15W) <sup>(16)</sup>	45W (45W)	45W
9	-- (45W) <sup>(15)</sup>	27W (45W)	27W

**Notes:**

- 14) The PDP table is based on the GPIO2\_POWER\_SHARE set-up in Figure 15 on page 29. The MPQ4242-A triggers power sharing when the MPQ4242-B's  $V_{BUS} > 11.2V$ .
- 15) The port is not connected and there is no valid PD contract, but the maximum PDP (45W) is still advertised.
- 16) Power sharing has been triggered because another port has made a PD contract with a high PDP. To limit the total shared power to 60W or less, the advertised power drops to 15W.

Figure 16 shows the PDP state machine. Figure 17 on page 31 shows the PDP foldback scheme.


**Figure 16: PDP State Machine (I<sup>2</sup>C Still Operates during NTC Shutdown)**

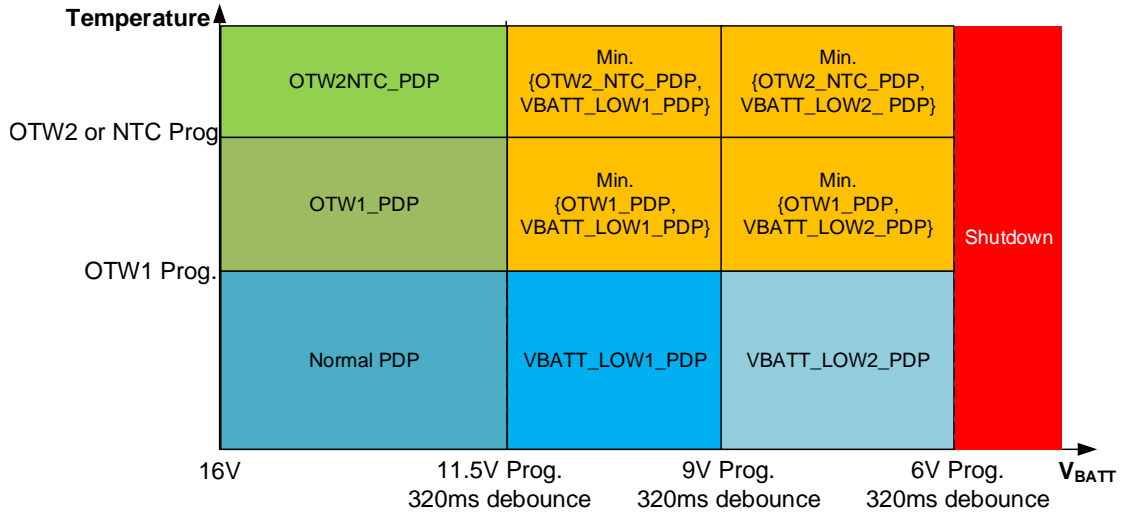


Figure 17: PDP Foldback Scheme

## I<sup>2</sup>C INTERFACE

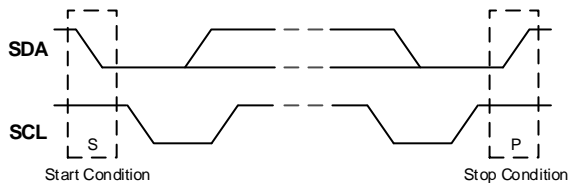
### I<sup>2</sup>C Serial Interface Description

The I<sup>2</sup>C is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence.

The MPQ4242 interface is an I<sup>2</sup>C slave that supports fast mode (400kHz). The I<sup>2</sup>C interface adds flexibility to the power supply solution. The output voltage ( $V_{OUT}$ ), transition slew rate, and additional parameters can be instantaneously controlled by the I<sup>2</sup>C interface. When the master sends the address as an 8-bit value, the 7-bit address should be followed by 0 or 1 to indicate a write or read operation, respectively.

### Start and Stop Conditions

The start (S) condition and stop (P) condition are signaled by the master device, which signifies the beginning and the end of the I<sup>2</sup>C transfer. The start condition is defined as the SDA signal transitioning from high to low while SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 18).



**Figure 18: Start and Stop Conditions**



<input type="checkbox"/>	Master to Slave	A = Acknowledge (SDA = low)	S = Start Condition	Write (Wr) = 0
<input checked="" type="checkbox"/>	Slave to Master	NA = Not Acknowledge (SDA = high)	P = Stop Condition	Read (Rd) = 1

**Figure 19: I<sup>2</sup>C Write Example (Write Single Register)**

The master then generates the SCL clocks, and transmits the device address and the read/write (R/W) direction bit on the SDA line.

### Transfer Data

Data is transferred in 8-bit bytes by the SDA line. Each byte of data should be followed by an acknowledge bit.

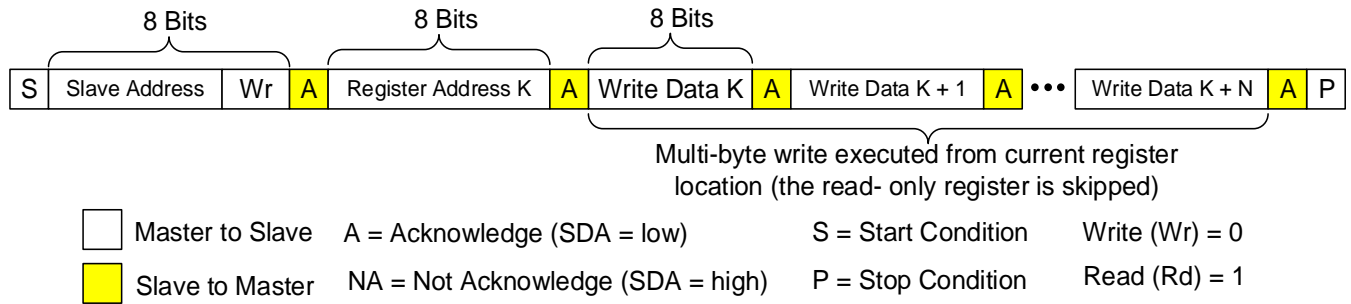
### I<sup>2</sup>C Start-Up Timing

The I<sup>2</sup>C function is enabled once  $V_{IN}$  exceeds its UVLO threshold and EN is active.

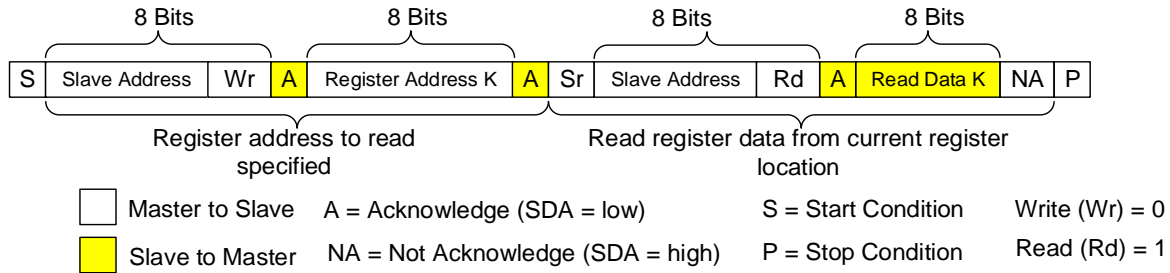
### I<sup>2</sup>C Update Sequence

The MPQ4242 requires a start condition, a valid I<sup>2</sup>C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPQ4242 acknowledges by pulling SDA low during the high period of a single clock pulse. A valid I<sup>2</sup>C address selects the MPQ4242. The MPQ4242 performs an update on the falling edge of the LSB. Figure 19 shows an I<sup>2</sup>C write example for a single register. Figure 20 on page 33 shows an I<sup>2</sup>C write example for multiple registers. Figure 21 on page 33 shows an I<sup>2</sup>C read example for a single register.





**Figure 20: I²C Write Example (Write Multiple Registers)**



**Figure 21: I²C Read Example (Read Single Register)**

**I<sup>2</sup>C REGISTER MAP**

Addr. (Hex)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
00	PDO_SET1	R/W	-	-	PDO7_EN <sup>(17)</sup>	PDO6_EN <sup>(17)</sup>	PDO5_EN <sup>(17)</sup>	PDO4_EN <sup>(17)</sup>	PDO3_EN <sup>(17)</sup>	PDO2_EN <sup>(17)</sup>	
01	PDO_SET2	R/W	-	-	PDO7_TYPE <sup>(17)</sup>	PDO6_TYPE <sup>(17)</sup>	PDO5_TYPE <sup>(17)</sup>	PDO4_TYPE <sup>(17)</sup>	PDO3_TYPE <sup>(17)</sup>	PDO2_TYPE <sup>(17)</sup>	
02	HOST_SET	R/W	COMMUNICA_CAPA B_HOST <sup>(17)</sup>	PRODUCT_TYPE_DFP <sup>(17)</sup>	HOST_CAPABILITY(000B) <sup>(17)</sup>			PORT_NUMBER <sup>(17)</sup>			
03	PDO_I1	R/W	PDO1_CURRENT_SETTING <sup>(17)</sup> (3A default)								
04	PDO_V2_L	R/W	PDO2_VOLTAGE_SETTING (low byte) <sup>(17)</sup> (9V default)								
05	PDO_V2_H	R/W	PDO2_VOLTAGE_SETTING (high byte) <sup>(17)</sup> (0x00)								
06	PDO_I2	R/W	PDO2_CURRENT_SETTING <sup>(17)</sup> (3A default)								
07	PDO_V3_L	R/W	PDO3_VOLTAGE_SETTING (low byte) <sup>(17)</sup> (15V default)								
08	PDO_V3_H	R/W	PDO3_VOLTAGE_SETTING (high byte) <sup>(17)</sup> (0x00)								
09	PDO_I3	R/W	PDO3_CURRENT_SETTING <sup>(17)</sup> (3A)								
0A	PDO_V4_L	R/W	PDO4_VOLTAGE_SETTING (low byte) <sup>(17)</sup> (20V default)								
0B	PDO_V4_H	R/W	PDO4_VOLTAGE_SETTING (high byte) <sup>(17)</sup> (0x00)								
0C	PDO_I4	R/W	PDO4_CURRENT_SETTING <sup>(17)</sup> (3A)								
0D	PDO_V5_L	R/W	PDO5_VOLTAGE_SETTING (low byte) <sup>(17)</sup> (3.3V)								
0E	PDO_V5_H	R/W	PDO5_VOLTAGE_SETTING (high byte) <sup>(17)</sup> (11V)								
0F	PDO_I5	R/W	PDO5_CURRENT_SETTING <sup>(17)</sup> (3A)								
10	PDO_V6_L	R/W	PDO6_VOLTAGE_SETTING (low byte) <sup>(17)</sup> (3.3V)								
11	PDO_V6_H	R/W	PDO6_VOLTAGE_SETTING (high byte) <sup>(17)</sup> (16V)								
12	PDO_I6	R/W	PDO6_CURRENT_SETTING <sup>(17)</sup> (3A)								
13	PDO_V7_L	R/W	PDO7_VOLTAGE_SETTING (low byte) <sup>(17)</sup> (3.3V)								
14	PDO_V7_H	R/W	PDO7_VOLTAGE_SETTING (high byte) <sup>(17)</sup> (21V)								
15	PDO_I7	R/W	PDO7_CURRENT_SETTING <sup>(17)</sup> (3A)								
16	PD_CTL1	R/W	CDP_EN <sup>(17)</sup>	LEGACY_CHARGING_MODE_SEL <sup>(17)</sup>	USBCOMMUNICATE <sup>(17)</sup>	NTC_CTL_RP <sup>(17)</sup>	TOUCH_TEMP <sup>(17)</sup>		TYPE-C_MODE <sup>(17)</sup>		
17	PD_CTL2	R/W	HDRST	USBSUSPEND <sup>(17)</sup>	TOUCH CURRENT <sup>(17)</sup>			COMPLIANCE <sup>(17)</sup>			
18	PWR_CLT1	R/W	EN <sup>(17)</sup>	MODE <sup>(17)</sup>	FREQ <sup>(17)</sup>		DITHER <sup>(17)</sup>	LINE_DROP_COMP <sup>(17)</sup>		SLEW_RATE <sup>(17)</sup>	
19	PWR_CLT2	R/W	EN_VBUS <sup>(17)</sup>	PPS_MIN_SEL <sup>(17)</sup>	OTW1_THRESHOLD <sup>(17)</sup>			OTP_THRESHOLD <sup>(17)</sup>			
1A	VOUT_L	R/W	RESERVED_ALL: 0					VOUT_DATA_BIT_LOW[2:0] <sup>(17)</sup>			
1B	VOUT_H	R/W	VOUT_DATA_BIT_HIGH[10:3] <sup>(17)</sup> (use this as default DAC V <sub>REF</sub> )								
1C	IOUT_LIM	R/W	-	OUTPUT_CURRENT_LIMIT_THRESHOLD <sup>(17)</sup> (1A to 6.35A/50mA step)							
1D	CTL_SYS0	R/W	-	-	-	-	-	-	-	GO_BIT	
1E	CTL_SYS1	R/W	SEND_SRC_CAP	ADDITIONAL_LINE_DROP_COMPENSATION <sup>(17)</sup>	EN_OFF_TIMER <sup>(17)</sup>		I2C_SLAVE_ADDRESS (A4~A1) <sup>(17)</sup>				
1F	CTL_SYS2	R/W	GPIO1 <sup>(17)</sup>			GPIO2 <sup>(17)</sup>			I2C_CTL_VOUT_EN <sup>(17)</sup>		
20	CTL_SYS3	R/W	PS_PDP_THD <sup>(17)</sup> (PDP is reduced to this value after power sharing)								
21	CTL_SYS4	R/W	PS_PDP_THD_PDO_SELECT <sup>(17)</sup>								
22	CTL_SYS5	R/W	-	PPS_3A_5A <sup>(17)</sup>	CC_BLANK_TIMER <sup>(17)</sup>		-	PD_CAP_PEAK_CURRENT <sup>(17)</sup>			

**I<sup>2</sup>C REGISTER MAP (continued)**

Addr. (Hex)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
23	CTL_SYS6	R/W	VBATT_LOW1_PDP <sup>(17)</sup>								
24	CTL_SYS7	R/W	VBATT_L1_PDO_SELECT <sup>(17)</sup>								
25	CTL_SYS8	R/W	VBATT_LOW2_PDP <sup>(17)</sup>								
26	CTL_SYS9	R/W	VBATT_L2_PDO_SELECT <sup>(17)</sup>								
27	CTL_SYS10	R/W	OTW1_PDP <sup>(17)</sup>								
28	CTL_SYS11	R/W	OTW1_PDO_SELECT <sup>(17)</sup>								
29	CTL_SYS12	R/W	OTW2_NTC_PDP <sup>(17)</sup>								
2A	CTL_SYS13	R/W	OTW2_NTC_PDO_SELECT <sup>(17)</sup>								
2B	CTL_SYS14	R/W	VBATT_LOW_THLD1 <sup>(17)</sup>				VBATT_LOW_THLD2 <sup>(17)</sup>				
2C	CTL_SYS15	R/W	VBATT_LOW_THLD3 <sup>(17)</sup>				VBATT_LOW_BLK <sup>(17)</sup>		-	-	
2D	CTL_SYS16	R/W	-	EXT_HS_FET RON <sup>(17)</sup>			OTW2_THRESHOLD <sup>(17)</sup>			-	
2E	CTL_SYS17	R/W	PEAK_CL <sup>(17)</sup>		-	NTC_HYST ERESIS <sup>(17)</sup>	NTC_MODE <sup>(17)</sup>	-	VBUS_VOLTAGE <sup>(17)</sup>		
2F	CTL_SYS18	R/W	OTP_PROGRAM	LED_PWM_DUTY <sup>(17)</sup>							
30	STATUS1	R	ATTACHED	NTC2_ENTER	POL	SHORT_VBATT	FAULT	OTP_PAGE	CC_CV	NTC_ENTER	
31	STATUS2	R	VBATT_LOW1_FLAG	VBATT_LOW2_FLAG	OTW1	OTW2	SELECTED_PDO_INDEX			PDO_TYPE	
32	STATUS3	R	CONTRACT_POWER (CP)								
33	ID1	R	OTP_SUFFIX_CODE <sup>(17)</sup>								
34	ID2	R	OTP_SOFTWARE_REVISION_NO <sup>(17)</sup>								
35	FW_REV	R	MISMATCH	GIVEBACK_FLAG	CABLE_CAP	FIRMWARE_REVISION					
36	MAX_REQ_CUR	R	Max requested operation current (MISMATCH = 1) in a 20mA unit; only valid when GIVEBACK_FLAG = 0; fixed PDO								
37	MFR_ID	R	MANUFACTURER_ID <sup>(17)</sup> : 0000 1001b								
38	DEV_ID	R	DEVICE_ID <sup>(17)</sup> : 0101 1000b								
39	CLK_ON	W	Write 1b to enable clock								

**Note:**

<sup>17)</sup> This register can be configured via the one-time programmable (OTP) memory.

## REGISTER MAP

The default register value is based on MPQ4242-0000.

### PDO\_SET1

Address: 0x00

Type: Read/Write

Bits	Name	Description
D[7:6]	RESERVED	Reserved.
D[5]	PDO7_EN	Enables the PDO7's power object setting. The default is 1b. 0b: Disabled 1b: Enabled
D[4]	PDO6_EN	Enables the PDO6's power object setting. The default is 1b. 0b: Disabled 1b: Enabled
D[3]	PDO5_EN	Enables the PDO5's power object setting. The default is 1b. 0b: Disabled 1b: Enabled
D[2]	PDO4_EN	Enables the PDO4's power object setting. The default is 1b. 0b: Disabled 1b: Enabled
D[1]	PDO3_EN	Enables the PDO3's power object setting. The default is 1b. 0b: Disabled 1b: Enabled
D[0]	PDO2_EN	Enables the PDO2's power object setting. The default is 1b. 0b: Disabled 1b: Enabled

PDO1 is fixed as a 5V power data object, and it is always enabled. Its voltage can be changed by VBUS\_VOLTAGE.

### PDO\_SET2

Address: 0x01

Type: Read/Write

Bits	Name	Description
D[7:6]	RESERVED	Reserved.
D[5]	PDO7_TYPE	Sets the PDO7's power object. The default is 1b. 0b: Fixed PDO 1b: APDO
D[4]	PDO6_TYPE	Sets the PDO6's power object. The default is 1b. 0b: Fixed PDO 1b: APDO
D[3]	PDO5_TYPE	Sets the PDO5's power object. The default is 1b. 0b: Fixed PDO 1b: APDO

D[2]	PDO4_TYPE	Sets the PDO4's power object. The default is 0b. 0b: Fixed PDO 1b: APDO
D[1]	PDO3_TYPE	Sets the PDO3's power object. The default is 0b. 0b: Fixed PDO 1b: APDO
D[0]	PDO2_TYPE	Sets the PDO2's power object. The default is 0b. 0b: Fixed PDO 1b: APDO

### HOST\_SET

Address: 0x02

Type: Read/Write

Bits	Name	Description
D[7]	COMMUNICA_CAPAB_HOST	Sets the USB communication capabilities for the USB host. The default is 0b. 0b: Other 1b: The product can enumerate USB devices
D[6:5]	PRODUCT_TYPE_DFP	Sets the product type (DFP). The default is 11b. 00b: Undefined 01b: PDUSB hub 10b: PDUSB host 11b: Power Brick
D[4:2]	HOST_CAPABILITY	Sets the DFP VDO message's B26...24 bits. The default is 000b.
D[1:0]	PORT_NUMBER	Sets the unique port number to identify a specific port on a multi-port device.

### PDO\_I1

Address: 0x03

Type: Read/Write

Bits	Name	Description
D[7:0]	PDO1_CURRENT_SETTING	Sets PDO1's maximum output current setting in 20mA units. The default is 0x96 (3A). When this bit is set to exceed 3A, the MPQ4242 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

### PDO\_V2\_L and PDO\_V2\_H

Address: 0x04, 0x05

Type: Read/Write

If PDO2\_TYPE is set to 0b (fixed PDO).

Register	Name	Description
PDO_V2_L, Bits D[7:0]	PDO2_VOLTAGE_SETTING	Sets the PDO2's output voltage in 100mV units. The default is 0x5A (9V). The maximum voltage that can be set is 22.97V.

If PDO2\_TYPE is set to 1b (APDO).

Register	Name	Description
PDO_V2_H, Bits D[7:0]	PDO2_MAXIMUM_VOLTAGE	Sets the maximum PDO2 voltage in 100mV increments.
PDO_V2_L, Bits D[7:0]	PDO2_MINIMUM_VOLTAGE	Sets the minimum PDO2 voltage in 100mV increments.

**PDO\_I2**

Address: 0x06

Type: Read/Write

Bits	Name	Description
D[7:0]	PDO2_CURRENT_SETTING	Sets PDO2's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 0x96 (3A and fixed PDO). When this bit is set to exceed 3A, the MPQ4242 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

**PDO\_V3\_L and PDO\_V3\_H**

Address: 0x07, 0x08

Type: Read/Write

If PDO3\_TYPE is set to 0b (fixed PDO).

Register	Name	Description
PDO_V3_L, Bits D[7:0]	PDO3_VOLTAGE_SETTING	Sets the PDO3's output voltage in 100mV units. The default is 0x96 (15V). The maximum voltage that can be set is 22.97V.

If PDO3\_TYPE is set to 1b (APDO).

Register	Name	Description
PDO_V3_H, Bits D[7:0]	PDO3_MAXIMUM_VOLTAGE	Sets the maximum PDO3 voltage in 100mV increments.
PDO_V3_L, Bits D[7:0]	PDO3_MINIMUM_VOLTAGE	Sets the minimum PDO3 voltage in 100mV increments.

**PDO\_I3**

Address: 0x09

Type: Read/Write

Bits	Name	Description
D[7:0]	PDO3_CURRENT_SETTING	Sets PDO3's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 0x96 (3A). When this bit is set to exceed 3A, the MPQ4242 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

**PDO\_V4\_L and PDO\_V4\_H**

Address: 0x0A, 0x0B

Type: Read/Write

If PDO4\_TYPE is set to 0b (fixed PDO).

Register	Name	Description
PDO_V4_L, Bits D[7:0]	PDO4_VOLTAGE_SETTING	Sets the PDO4's output voltage in 100mV units. The default is 0xC8 (20V). The maximum voltage that can be set is 22.97V.

If PDO4\_TYPE is set to 1b (APDO).

Register	Name	Description
PDO_V4_H, Bits D[7:0]	PDO4_MAXIMUM_VOLTAGE	Sets the maximum PDO4 voltage in 100mV increments.
PDO_V4_L, Bits D[7:0]	PDO4_MINIMUM_VOLTAGE	Sets the minimum PDO4 voltage in 100mV increments.

**PDO\_I4**

Address: 0x0C

Type: Read/Write

Bits	Name	Description
D[7:0]	PDO4_CURRENT_SETTING	Sets PDO4's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 0x96 (3A and fixed PDO). When this bit is set to exceed 3A, the MPQ4242 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

**PDO\_V5\_L and PDO\_V5\_H**

Address: 0x0D, 0x0E

Type: Read/Write

If PDO5\_TYPE is set to 0b (fixed PDO).

Register	Name	Description
PDO_V5_L, Bits D[7:0]	PDO5_VOLTAGE_SETTING	Sets the PDO5's output voltage in 100mV units.

If PDO5\_TYPE is set to 1b (APDO).

Register	Name	Description
PDO_V5_H, Bits D[7:0]	PDO5_MAXIMUM_VOLTAGE	Sets the maximum PDO5 voltage in 100mV increments. The default is 0x6E (11V).
PDO_V5_L, Bits D[7:0]	PDO5_MINIMUM_VOLTAGE	Sets the minimum PDO5 voltage in 100mV increments. The default is 0x21 (3.3V).

**PDO\_I5**

Address: 0x0F

Type: Read/Write

Bits	Name	Description
D[7:0]	PDO5_CURRENT_SETTING	Sets PDO5's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 0x3C (3A). When this bit is set to exceed 3A, the MPQ4242 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

**PDO\_V6\_L and PDO\_V6\_H**

Address: 0x10, 0x11

Type: Read/Write

If PDO6\_TYPE is set to 0b (fixed PDO).

Register	Name	Description
PDO_V6_L, Bits D[7:0]	PDO6_VOLTAGE_SETTING	Sets the PDO6's output voltage in 100mV units.

If PDO6\_TYPE is set to 1b (APDO).

Register	Name	Description
PDO_V6_H, Bits D[7:0]	PDO6_MAXIMUM_VOLTAGE	Sets the maximum PDO6 voltage in 100mV increments. The default is 0xA0 (16V).
PDO_V6_L, Bits D[7:0]	PDO6_MINIMUM_VOLTAGE	Sets the minimum PDO6 voltage in 100mV increments. The default is 0x21 (3.3V).

**PDO\_I6**

Address: 0x12

Type: Read/Write

Bits	Name	Description
D[7:0]	PDO6_CURRENT_SETTING	Sets PDO6's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 3A and APDO. When this bit is set to exceed 3A, the MPQ4242 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

**PDO\_V7\_L and PDO\_V7\_H**

Address: 0x13, 0x14

Type: Read/Write

If PDO7\_TYPE is set to 0b (fixed PDO).

Register	Name	Description
PDO_V7_L, Bits D[7:0]	PDO7_VOLTAGE_SETTING	Sets the PDO7's output voltage in 100mV units.

If PDO7\_TYPE is set to 1b (APDO).

Register	Name	Description
PDO_V7_H, Bits D[7:0]	PDO7_MAXIMUM_VOLTAGE	Sets the maximum PDO7 voltage in 100mV increments. The default is 0xD2 (21V).
PDO_V7_L, Bits D[7:0]	PDO7_MINIMUM_VOLTAGE	Sets the minimum PDO7 voltage in 100mV increments. The default is 0x21 (3.3V).

**PDO\_I7**

Address: 0x15

Type: Read/Write

Bits	Name	Description
D[7:0]	PDO7_CURRENT_SETTING	Sets PDO7's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 3A and APDO. When this bit is set to exceed 3A, the MPQ4242 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

**PD\_CTL1**

Address: 0x16

Type: Read/Write

Bits	Name	Default	Description															
D[7]	CDP_EN	0b	Selects the CDP mode. If this bit is set to 1, all the DCP, QC, and Apple modes are disabled. The device only works in CDP handshaking mode. The default is 0.															
D[6:5]	LEGACY_CHARGING_MODE_SEL	00b	Sets certain values based on the truth table below. <table border="1" data-bbox="568 1543 1469 1774"> <thead> <tr> <th>CDP_EN</th> <th>1</th> <th>0</th> <th>0</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>LEGACY_CHARGING_MODE_SEL</td> <td>X</td> <td>00</td> <td>01</td> <td>10/11</td> </tr> <tr> <td>Mode</td> <td>CDP mode</td> <td>All DCP modes are active</td> <td>Apple mode and BC1.2 mode are active</td> <td>Only BC1.2 is active; Apple mode and QC mode are disabled</td> </tr> </tbody> </table>	CDP_EN	1	0	0	0	LEGACY_CHARGING_MODE_SEL	X	00	01	10/11	Mode	CDP mode	All DCP modes are active	Apple mode and BC1.2 mode are active	Only BC1.2 is active; Apple mode and QC mode are disabled
CDP_EN	1	0	0	0														
LEGACY_CHARGING_MODE_SEL	X	00	01	10/11														
Mode	CDP mode	All DCP modes are active	Apple mode and BC1.2 mode are active	Only BC1.2 is active; Apple mode and QC mode are disabled														
D[4]	USBCOMMUNICATE	0b	Sets whether USB communication is supported. The default is 0b. 0b: USB communication is not supported 1b: USB communication is supported															



D[3]	NTC_CTL_RP	0b	<p>Selects whether the device enters USB Type-C 3A or 1.5A mode if an NTC or over-temperature warning (OTW) event occurs. In 5V @ 3A USB Type-C mode, the R<sub>P</sub> pull-up current is 330μA and the R<sub>D</sub> detection range is between 0.8V and 2.6V. The default is 0.</p> <p>0b: PDP &lt;15W, and R<sub>P</sub> = 1.5A, otherwise, R<sub>P</sub> = 3A            1b: The device enters 1.5A USB Type-C mode if an NTC or OTW1/OTW2 condition occurs</p>
D[2:1]	TOUCH_TEMP	00b	<p>Sets the touch temperature default value to 0, 1 or 2. These bits are defined in SOURCE_CAPABILITIES_EXTENDED Message byte 20, bits[1:0]. These bits are set to 00b by default</p>
D[0]	TYPE-C_MODE	0b	<p>Selects 3A or 1.5A Type-C mode. In 5V @ 3A USB Type-C mode, the R<sub>P</sub> pull-up current is 330μA and the R<sub>D</sub> detection range is between 0.85V and 2.45V. The default is 0.</p> <p>0b: 3A Type-C mode            1b: 1.5A Type-C mode</p>

**PD\_CTL2**

Address: 0x17

Type: Read/Write

Bits	Name	Default	Description
D[7]	HDRST	0b	<p>Sends a hard reset command. The default is 0b.</p> <p>0b: Normal state.            1b: Send a hard reset command to the sink. After the HDRST message is sent, this bit automatically resets to 0b</p>
D[6]	USB_SUSPEND	0b	<p>Sets whether the USB suspend function is supported. The default is 0b.</p> <p>0b: Not supported            1b: Supported</p>
D[5:3]	TOUCH_CURRENT	000b	<p>Sets the TOUCH_CURRENT, bits[2:0]. These bits are defined in SOURCE_CAPABILITIES_EXTENDED Message byte 13, bits[2:0]. These bits are set to 000b by default. Bit D[5] indicates TOUCH_CURRENT, bit 2</p>
D[2:0]	COMPLIANCE	101b	<p>Sets the values of bits[2:0] of the Compliance byte, defined in SOURCE_CAPABILITIES_EXTENDED Message byte 12, bits[2:0]. Bit D[2] sets the compliance value for bit 2.</p>

**PWR\_CTL1**

Address: 0x18

Type: Read/Write

Bits	Name	Default	Description
D[7]	EN	1b	<p>Determines the I<sup>2</sup>C control to turn the part on or off. When the external EN pin is low, the converter is off and the I<sup>2</sup>C shuts down. When the EN pin is high, the EN bit takes over. The default is 1.</p> <p>0b: The part is off but the I<sup>2</sup>C register does not reset. In addition, the USB Type-C logic is off, and the system clock turns off to save quiescent current (I<sub>Q</sub>)            1b: If the USB Type-C receptacle is disconnected, the system clock remains off to save I<sub>Q</sub></p>
D[6]	MODE	1b	<p>Sets the PWM mode. The default is 1.</p> <p>0b: Enables auto-PFM/PWM mode            1b: Forced PWM mode</p>

D[5:4]	FREQ	01b	Sets the switching frequency ( $f_{sw}$ ). The default is 01. 00b: 250kHz 01b: 420kHz 10b/11b: Reserved
D[3]	DITHER	0b	Enables the frequency spread spectrum function. The default is 0. 0b: Disabled 1b: Enabled
D[2:1]	LINE_DROP_COMP	00b	Sets the output voltage compensation vs. the load feature. The compensation amplitude is fixed for any output voltage. Set 0x1E, bit[6] = 1 to enable an additional compensation voltage. Line drop compensation has a maximum clamp at 800mV, regardless of the output current. Line drop compensation is disabled once the MPQ4242 enters PPS mode. Line drop compensation can be enabled in PPS mode through the factory OTP trim. The default is 00. 00b: No compensation 01b: $V_{OUT}$ compensates 150mV at a 3A Iout 10b: $V_{OUT}$ compensates 300mV at a 3A Iout 11b: $V_{OUT}$ compensates 600mV at a 3A Iout
D[0]	SLEW_RATE	1b	Sets the output slew rate to adjust $V_{OUT}$ . The default is 1. The slew rate can be calculated with the following equation: $V_{OUT} \text{ slew rate} = V_{REF} \text{ slew rate} \times \text{Feedback resistor ratio (12.5)}$ 0b: 0.4mV/ $\mu$ s $V_{REF}$ rising slew rate; 0.08mV/ $\mu$ s $V_{REF}$ falling slew rate 1b: 0.08mV/ $\mu$ s $V_{REF}$ rising slew rate; 0.08mV/ $\mu$ s $V_{REF}$ falling slew rate

**PWR\_CTL2**

Address: 0x19

Type: Read/Write

Bits	Name	Default	Description
D[7]	EN_VBUS	0b	Enables the power converter's output directly, even there is no USB Type-C sink device. The default is 0b. 0b: The power converter's on/off status is controlled by the USB Type-C controller 1b: The power converter is enabled
D[6]	PPS_MIN_SEL	1b	Sets the $V_{BUS}$ under-voltage (UV) threshold: This bit also controls the 3.3V or 5V minimum PPS voltage. The default is 1. 0b: The $V_{BUS}$ UV falling threshold is 4.5V with 5% accuracy for 5V minimum PPS voltage applications 1b: The $V_{BUS}$ UV falling threshold is 2.97V (3.135V maximum) with 4.5% accuracy for 3.3V minimum PPS voltage applications
D[5:3]	OTW1_THRESHOLD	100b	Sets the over-temperature warning (OTW1) threshold. The default is 100. The OTW threshold has a 20°C hysteresis for recovery. 000: Disable the OTW function 001b: 105°C 010b: 115°C 011b: 125°C 100b: 135°C 101b: 145°C 110b: 155°C 111b: 165°C

D[2:0]	OTP_THRESHOLD	010b	<p>Sets the OT shutdown threshold. The default is 010. OTP has a 20°C hysteresis for recovery.</p> <p>000b: 155°C            001b: 165°C            010b: 175°C            011b: 185°C            100b~111b: Reserved</p>
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### VOUT\_L and VOUT\_H

Address: 0x1A, 0x1B

Type: Read/Write

The VOUT\_L and VOUT\_H registers set  $V_{OUT}$  following an 11-bit direct format.

Name	VOUT															
Format	Direct, unsigned binary integer															
Register Name	N/A					VOUT_H D[7:0]							VOUT_L D[2:0]			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	N/A					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	N/A					Data bit high				Data bit low						
Default value (5V)	N/A					250 Integer										

The real-world  $V_{OUT}$  (in V) can be calculated with Equation (2):

$$V_{OUT} (V) = V / 100 + 2.5 \quad (2)$$

Where V is an 11-bit, unsigned binary integer from VOUT[10:0] (ranging between 0 and 2047). The  $V_{OUT}$  resolution (or minimum step) is 10mV. The MPQ4242 has a feedback network from the OUT pin to internal FB reference voltage. The feedback resistor ratio is  $V_{OUT} / V_{REF} = 12.5$ .

See the CTL\_SYS0 section below when changing  $V_{OUT}$ .

### IOUT\_LIM

Address: 0x1C

Type: Read/Write

Bits	Name	Default	Description
D[7]	RESERVED	-	Reserved.
D[6:0]	IOUT_LIM	0x48	Sets the CC current limit for the buck-boost output CC, in 50mA units. The default is 0x48 (3.6A). When changing IOUT_LIM, the internal IREF should have some slew rate control. The ramping slew rate is 1mA/μs.

### CTL\_SYS0

Address: 0x1D

Type: Read/Write

Bits	Name	Default	Description
D[7]	RESERVED	-	Reserved.
D[0]	GO_BIT	0b	<p>Controls when the MPQ4242 starts to change <math>V_{OUT} / I_{OUT\_LIM}</math>. Set GO_BIT to 1 to start the output / CC limit change based on VOUT / IOUT_LIM registers. When <math>V_{OUT} / I_{OUT\_LIM}</math> finishes changing (the internal <math>V_{REF}</math> steps to the target <math>V_{REF}</math>), GO_BIT automatically resets to 0. This prevents false operation of the VOUT/IOUT_LIM scaling. The default is 0.</p> <p>0b: <math>V_{OUT} / I_{OUT\_LIM}</math> do not change            1b: <math>V_{OUT} / I_{OUT\_LIM}</math> changes based on the VOUT / IOUT_LIM register settings</p>

**CTL\_SYS1**

Address: 0x1E

Type: Read/Write

Bits	Name	Default	Description								
D[7]	SEND_SRC_CAP	0b	Sends the source capability message. Write 1 to this bit to force the MPQ4242 to send a Src_Cap message. This bit automatically resets to 0 after the Src_Cap message is sent out. The default is 0b.								
D[6]	ADDITIONAL_LINE_DROP_COMPENSATION	0b	Enables an additional 150mV for line drop compensation based on the 0x18, bits[2:1] set-up. This bit is active only when line drop compensation is active. 0b: Disabled 1b: Enabled								
D[5:4]	EN_OFF_TIMER	000b	Sets the EN off time. There is a shutdown delay time after the EN pin goes low. If EN pulls high while the counter increases, the counter is reset. The default is 00. 00b: No delay 01b: 20 minutes 10b: 40 minutes 11b: 120 minutes								
D[3:0]	I2C_SLAVE_ADDRESS	0001b	Set the I <sup>2</sup> C slave address A4 to A1 bit. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="2">I<sup>2</sup>C Address (A7:A1)</th> </tr> <tr> <th>Binary</th> <th>Hex</th> </tr> </thead> <tbody> <tr> <td>1100 001 (Default)</td> <td>61h</td> </tr> <tr> <td>I<sup>2</sup>C adjustable for A4~A1</td> <td>Set by I2C_SLAVE_ADDRESS, bits D[3:0]</td> </tr> </tbody> </table>	I <sup>2</sup> C Address (A7:A1)		Binary	Hex	1100 001 (Default)	61h	I <sup>2</sup> C adjustable for A4~A1	Set by I2C_SLAVE_ADDRESS, bits D[3:0]
I <sup>2</sup> C Address (A7:A1)											
Binary	Hex										
1100 001 (Default)	61h										
I <sup>2</sup> C adjustable for A4~A1	Set by I2C_SLAVE_ADDRESS, bits D[3:0]										

**CTL\_SYS2**

Address: 0x1F

Type: Read and Write

Bits	Name	Default	Description
D[7:5]	GPIO1	000b	Sets the GPIO1 pin function. The default is 000. 000b: POWER_SHARE1. See the GPIO1_POWER_SHARE section on page 28 for more details 001b: GATE. Provides a GND to battery short protection drive 010b: FAULT, open-drain output. Pulls low to indicate if a fault has occurred, such as OCP, OTP, and GND/DP/DM/CCx to battery short 011b: NTC2. When this function is selected, the power share input is controlled by NTC2. The NTC_MODE bit does not control the NTC2 behavior. NTC_HYSTERESIS sets the hysteresis 100/101b: ATTACH_FLT_ALT, open-drain output. This pin pulls low for 12μs at the connection rising edge if no fault event has occurred. Pulls low if a fault occurs 111b: Current monitor output. Represents the signal between ISENS+ and ISENS-

D[4:2]	GPIO2	000b	<p>Sets the GPIO2 pin function. The default is 000.</p> <p>000b: Reserved</p> <p>001b: POL, open-drain output. Indicates the USB Type-C plug's polarity. When CC1 is selected as the CC line, POL pulls low; when CC2 is selected as the CC line or disconnected, POL is an open drain</p> <p>010b: NTC. Functions as an input pin to sense the external thermal. See the NTC Function section on page 27 for more details</p> <p>011b: VCONN_IN. Apply a 5V / 1.5W power supply on this pin</p> <p>100b: LED_PWM output. It is a 25kHz PWM signal output with an adjustable duty cycle. See the CTL_SYS18 section on page 49 for more details</p> <p>101b: ATTACH. Indicates if the USB Type-C port is connected. Only high or low for two states</p> <p>110b: POWER_SHARE2. GPIO2 power sharing is triggered when the GPIO2 voltage exceeds 1.87V. See the GPIO2_POWER_SHARE section on page 29 for more details</p>
D[1]	I2C_CTL_VOUT_EN	0b	<p>Enables the I<sup>2</sup>C registers 0x1A, 0x1B, 0x1C, and 0x1D. The default is 0.</p> <p>0b: V<sub>OUT</sub> and I<sub>OUT_LIM</sub> do not change, even after sending commands to VOUT_L, VOUT_H, GO_BIT, and ILIMIT. V<sub>OUT</sub> is controlled by the USB PD engine</p> <p>1b: V<sub>OUT</sub> changes based on the VOUT/IOUT_CC register setting</p>
D[0]	RESERVED	-	Reserved.

### CTL\_SYS3 and CTL\_SYS4

Address: 0x20 to 0x21

Type: Read and Write

Bits	Name	Default	Description
D[7:0]	PS_PDP_THD	0x5A	<p>Sets the threshold to which the PDO power rating is reduced. When the GPIOx pin (if set to the POWER_SHARE function) pulls low, the MPQ4242's PD power drops to the values set by PS_PDP_THD. The default is 45W.</p> <p>0x01: 0.5W</p> <p>0xFF: 127.5W</p>
D[7:0]	PS_PDP_THD_PDO_SELECT	0xBE	<p>Selects which voltage is enabled in the PDO list. See Table 4 on page 29 for more details. The final PDO current is determined by PS_PDP_THD. The default means 4 fixed PDOs: 5V/9V/15V/20V and 3 APDOs: 3.3V to 5.9V/3.3V to 11V/3.3V to 16V.</p>

### CTL\_SYS5

Address: 0x22

Type: Read/Write

Bits	Name	Default	Description
D[7]	RESERVED	-	Reserved.
D[6]	PPS_3A_5A	0b	<p>Sets the maximum current for APDO after entering a power sharing, V<sub>BATT</sub> low, OTW, or NTC state. The default is 0b.</p> <p>0b: 3A</p> <p>1b: 5A (requires 5A cable)</p>
D[5:4]	CC_BLANK_TIMER	10b	<p>Sets the blank time when the output CC over-current condition is reached. The default is 10b.</p> <p>00b: No additional CC blank timer</p> <p>01b: 2ms</p> <p>10b: 16ms</p> <p>11b: 32ms</p>

D[1:0]	PD_CAP_ PEAK_CURRENT	11b	<p>Enables the peak current 1, 2, and 3 capability in the SOURCE_CAP_EXTEND message. The default is 11.</p> <p>00b: Not support 01b: Support peak current 1 10b: Support peak currents 1 and 2 11b: Support peak currents 1, 2 and 3</p>
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**CTL\_SYS6~CTL\_SYS13**

Address: 0x23~0x2A

Type: Read/Write

Bits	Name	Default	Description
D[7:0]	VBATT_LOW1_ PDP	0x5A	<p>Sets the maximum power rating when <math>V_{BATT}</math> drops below its first threshold. PDP is reduced to the value set by these bits. The default is 45W.</p> <p>0x01: 0.5W 0xFF: 127.5W</p>
D[7:0]	VBATT_L1_ PDO_SELECT	0xBE	<p>Selects which voltage is enabled in the PDO list. See Table 4 on page 29 for more details. The final PDO current is determined by PDP_L. The default means 4 fixed PDOs: 5V/9V/15V/20V and 3 APDOs: 3.3V to 5.9V/3.3V to 11V/3.3V to 16V.</p>
D[7:0]	VBATT_LOW2_ PDP	0x1E	<p>Sets the maximum power rating when <math>V_{BATT}</math> drops below its second threshold. PDP is reduced to the value set by these bits. The default is 15W.</p> <p>0x01: 0.5W 0xFF: 127.5W</p>
D[7:0]	VBATT_L2_ PDO_SELECT	0xBE	<p>Selects which voltage is enabled in the PDO list. See Table 4 on page 29 for more details. The final PDO current is determined by PDP_L. The default means 4 fixed PDOs: 5V/9V/15V/20V and 3 APDOs: 3.3V to 5.9V/3.3V to 11V/3.3V to 16V.</p>
D[7:0]	OTW1_PDP	0x5A	<p>Sets the maximum power rating when the die temperature drops below its threshold. PDP is reduced to the value set by these bits. The default is 45W.</p> <p>0x01: 0.5W 0xFF: 127.5W</p>
D[7:0]	OTW1_PDO_ SELECT	0xBE	<p>Selects which voltage is enabled in the PDO list. See Table 4 on page 29 for more details. The final PDO current is determined by PDP_L. The default means 4 fixed PDOs: 5V/9V/15V/20V and 3 APDOs: 3.3V to 5.9V/3.3V to 11V/3.3V to 16V.</p>
D[7:0]	OTW2_NTC_ PDP	0x3C	<p>Sets the maximum power rating when the die temperature drops below its threshold. PDP is reduced to the value set by these bits. The default is 30W.</p> <p>0x01: 0.5W 0xFF: 127.5W</p>
D[7:0]	OTW2_NTC_ PDO_SELECT	0xBE	<p>Selects which voltage is enabled in the PDO list. See Table 4 on page 29 for more details. The final PDO current is determined by PDP_L. The default means 4 fixed PDOs: 5V/9V/15V/20V and 3 APDOs: 3.3V to 5.9V/3.3V to 11V/3.3V to 16V.</p>

**CTL\_SYS14 and CTL\_SYS15**

Address: 0x2B, 0x2C

Type: Read/Write

Bits	Name	Default	Description																																					
D[7:4]	VBATT_LOW_THLD1	0100b	Sets the threshold for input voltage detection. The default is 0100b. See the Low Battery Operation section on page 28 for more details. <table border="1" data-bbox="669 409 1393 898"> <thead> <tr> <th>D[3:0]</th> <th>Input Voltage Falling</th> <th>Hysteresis</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>This function is disabled</td> <td>This function is disabled</td> </tr> <tr> <td>0001</td> <td>12.6V</td> <td rowspan="14">800mV</td> </tr> <tr> <td>0010</td> <td>12.2V</td> </tr> <tr> <td>0011</td> <td>11.8V</td> </tr> <tr> <td>0100</td> <td>11.4V</td> </tr> <tr> <td>0101</td> <td>11V</td> </tr> <tr> <td>0110</td> <td>10.6V</td> </tr> <tr> <td>0111</td> <td>10.2V</td> </tr> <tr> <td>1000</td> <td>9.8V</td> </tr> <tr> <td>1001</td> <td>9.4V</td> </tr> <tr> <td>1010</td> <td>9V</td> </tr> <tr> <td>1011</td> <td>8.6V</td> </tr> <tr> <td>1100</td> <td>8.2V</td> </tr> <tr> <td>1101</td> <td>7.8V</td> </tr> <tr> <td>1110</td> <td>7.4V</td> </tr> <tr> <td>1111</td> <td>7V</td> </tr> </tbody> </table>	D[3:0]	Input Voltage Falling	Hysteresis	0000	This function is disabled	This function is disabled	0001	12.6V	800mV	0010	12.2V	0011	11.8V	0100	11.4V	0101	11V	0110	10.6V	0111	10.2V	1000	9.8V	1001	9.4V	1010	9V	1011	8.6V	1100	8.2V	1101	7.8V	1110	7.4V	1111	7V
D[3:0]	Input Voltage Falling	Hysteresis																																						
0000	This function is disabled	This function is disabled																																						
0001	12.6V	800mV																																						
0010	12.2V																																							
0011	11.8V																																							
0100	11.4V																																							
0101	11V																																							
0110	10.6V																																							
0111	10.2V																																							
1000	9.8V																																							
1001	9.4V																																							
1010	9V																																							
1011	8.6V																																							
1100	8.2V																																							
1101	7.8V																																							
1110	7.4V																																							
1111	7V																																							
D[3:0]	VBATT_LOW_THLD2	1000b	Sets the threshold for input voltage detection. The default is 1000b. See the Low Battery Operation section on page 28 for more details. <table border="1" data-bbox="680 982 1382 1472"> <thead> <tr> <th>D[3:0]</th> <th>Input Voltage Falling</th> <th>Input Voltage Rising</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>This function is disabled</td> <td>This function is disabled</td> </tr> <tr> <td>0001</td> <td>11.8V</td> <td rowspan="14">800mV</td> </tr> <tr> <td>0010</td> <td>11.4V</td> </tr> <tr> <td>0011</td> <td>11V</td> </tr> <tr> <td>0100</td> <td>10.6V</td> </tr> <tr> <td>0101</td> <td>10.2V</td> </tr> <tr> <td>0110</td> <td>9.8V</td> </tr> <tr> <td>0111</td> <td>9.4V</td> </tr> <tr> <td>1000</td> <td>9V</td> </tr> <tr> <td>1001</td> <td>8.6V</td> </tr> <tr> <td>1010</td> <td>8.2V</td> </tr> <tr> <td>1011</td> <td>7.8V</td> </tr> <tr> <td>1100</td> <td>7.4V</td> </tr> <tr> <td>1101</td> <td>7V</td> </tr> <tr> <td>1110</td> <td>6.6V</td> </tr> <tr> <td>1111</td> <td>6.2V</td> </tr> </tbody> </table>	D[3:0]	Input Voltage Falling	Input Voltage Rising	0000	This function is disabled	This function is disabled	0001	11.8V	800mV	0010	11.4V	0011	11V	0100	10.6V	0101	10.2V	0110	9.8V	0111	9.4V	1000	9V	1001	8.6V	1010	8.2V	1011	7.8V	1100	7.4V	1101	7V	1110	6.6V	1111	6.2V
D[3:0]	Input Voltage Falling	Input Voltage Rising																																						
0000	This function is disabled	This function is disabled																																						
0001	11.8V	800mV																																						
0010	11.4V																																							
0011	11V																																							
0100	10.6V																																							
0101	10.2V																																							
0110	9.8V																																							
0111	9.4V																																							
1000	9V																																							
1001	8.6V																																							
1010	8.2V																																							
1011	7.8V																																							
1100	7.4V																																							
1101	7V																																							
1110	6.6V																																							
1111	6.2V																																							



D[7:4]	VBATT_LOW_THLD3	1010b	Those bits set the threshold of input voltage detection. The default is 1010b. See the Low Battery Operation section on page 28 for more details.																																					
			<table border="1"> <thead> <tr> <th>D[3:0]</th> <th>Input Voltage Falling</th> <th>Input Voltage Rising</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>This function is disabled</td> <td>This function is disabled</td> </tr> <tr> <td>0001</td> <td>9.8V</td> <td rowspan="14">800mV</td> </tr> <tr> <td>0010</td> <td>9.4V</td> </tr> <tr> <td>0011</td> <td>9V</td> </tr> <tr> <td>0100</td> <td>8.6V</td> </tr> <tr> <td>0101</td> <td>8.2V</td> </tr> <tr> <td>0110</td> <td>7.8V</td> </tr> <tr> <td>0111</td> <td>7.4V</td> </tr> <tr> <td>1000</td> <td>7V</td> </tr> <tr> <td>1001</td> <td>6.6V</td> </tr> <tr> <td>1010</td> <td>6.2V</td> </tr> <tr> <td>1011</td> <td>5.8V</td> </tr> <tr> <td>1100</td> <td>5.4V</td> </tr> <tr> <td>1101</td> <td>5V</td> </tr> <tr> <td>1110</td> <td>4.6V</td> </tr> <tr> <td>1111</td> <td>4.2V</td> </tr> </tbody> </table>	D[3:0]	Input Voltage Falling	Input Voltage Rising	0000	This function is disabled	This function is disabled	0001	9.8V	800mV	0010	9.4V	0011	9V	0100	8.6V	0101	8.2V	0110	7.8V	0111	7.4V	1000	7V	1001	6.6V	1010	6.2V	1011	5.8V	1100	5.4V	1101	5V	1110	4.6V	1111	4.2V
			D[3:0]	Input Voltage Falling	Input Voltage Rising																																			
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1100	5.4V																																							
1101	5V																																							
1110	4.6V																																							
1111	4.2V																																							
D[3:2]	VBATT_LOW_BLK	10b	Sets the $V_{BATT}$ low 1, and $V_{BATT}$ low 2, and $V_{BATT}$ low 3 blank times. The default is 10b. 00b: 10ms 01b: 160ms 10b: 320ms 11b: 640ms																																					
D[1:0]	RESERVED	-	Reserved.																																					

**CTL\_SYS16**

Address: 0x2D

Type: Read/Write

Bits	Name	Default	Description												
D[7]	RESERVED	-	Reserved.												
D[6:4]	EXT_HS_FET_RON	000b	Sets the $R_{(DS)ON}$ for external N-channel MOSFET at 10V $V_{GS}$ . Select $R_{(DS)ON}$ such that matches MOSFET's actual $R_{(DS)ON}$ at 10V $V_{GS}$ . The default is 000b. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>D[6:4]</th> <th><math>R_{(DS)ON}</math> (m<math>\Omega</math>)</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>This function is disabled</td> </tr> <tr> <td>001</td> <td>5</td> </tr> <tr> <td>010</td> <td>7.5</td> </tr> <tr> <td>011</td> <td>10</td> </tr> <tr> <td>100</td> <td>12.5</td> </tr> </tbody> </table>	D[6:4]	$R_{(DS)ON}$ (m $\Omega$ )	000	This function is disabled	001	5	010	7.5	011	10	100	12.5
			D[6:4]	$R_{(DS)ON}$ (m $\Omega$ )											
			000	This function is disabled											
			001	5											
			010	7.5											
011	10														
100	12.5														
D[3:1]	OTW2_THRESHOLD	110b	Sets the over-temperature warning (OTW) threshold. The default is 110b. OTW has a 20°C hysteresis for recovery.  000b: Disable OTW 001b: 105°C 010b: 115°C 011b: 125°C 100b: 135°C 101b: 145°C 110b: 155°C 111b: 165°C												
			D[0]	RESERVED	-	Reserved.									

**CTL\_SYS17**

Address: 0x2E

Type: Read/Write

Bits	Name	Default	Description										
D[7:6]	PEAK_CL	11b	Sets the high-side peak current limit in boost mode. The default is 11b. <table border="1" data-bbox="841 380 1219 527" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>D[7:6]</th> <th>Peak Limit</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>8A</td> </tr> <tr> <td>01</td> <td>12A</td> </tr> <tr> <td>10</td> <td>16A</td> </tr> <tr> <td>11</td> <td>20A</td> </tr> </tbody> </table>	D[7:6]	Peak Limit	00	8A	01	12A	10	16A	11	20A
D[7:6]	Peak Limit												
00	8A												
01	12A												
10	16A												
11	20A												
D[4]	NTC_HYSTERESIS	1b	Sets the NTC thermal recovery hysteresis. This bit controls both NTC and NTC2. The default is 1b. 0b: 10% 1b: 20%										
D[3]	NTC_MODE	0b	Sets the behavior if the NTC function is triggered. The default is 0b. 0b: Shut down the MPQ4242 1b: Reduce the PD power to the value set by OTW2_NTC_PDP										
D[1:0]	VBUS_VOLTAGE	10b	Sets the default VBUS voltage. The default is 10b. 00b: 5V 01b: 5.05V 10b: 5.1V 11b: 5.15V										

**CTL\_SYS18**

Address: 0x2F

Type: Read/Write

Bits	Name	Default	Description
D[7]	OTP_PROGRAM	0x0	Configures the I <sup>2</sup> C register value into the OTP memory cell. A password is required before using the OTP. The OTP can be configured once. Only the MPQ4242-0000 and OTP_PAGE = 0 can be used to configure the OTP. Write 1 to this bit to implement OTP configurations. After configuring is complete, this bit automatically resets to 0. Apply a 12V V <sub>IN</sub> while configuring the OTP.
D[6:0]	LED_PWM_DUTY	0x32	Sets the LED_PWM output duty cycle. The minimum value is 5%; the maximum is 100%. 0x05: 5% 0x64: 100%

**STATUS1**

Address: 0x30

Type: Read-Only

This register is latch-off, and it is cleared when it is read.

Bits	Name	Description
D[7]	ATTACHED	Returns whether the sink is connected. 0b: Disconnected 1b: Connected
D[6]	NTC2_ENTER	Returns whether an NTC2 event has occurred. 0b: No NTC2 event has occurred 1b: An NTC2 event has occurred

D[5]	POL	Indicates the USB Type-C polarity. 0b: CC1 is selected as the CC line 1b: CC2 is selected as the CC line
D[4]	SHORT_VBATT	Indicates the output bus voltage status. 0b: Normal state 1b: DP, DM, CC1, CC2 or USB_GND is shorted with the battery voltage
D[3]	FAULT	FAULT function indicates a fault has happened. Fault conditions include OCP, OTP, and GND/DP/DM/CCx to battery shorts. 0b: No fault has occurred 1b: One or more fault events have occurred
D[2]	OTP_PAGE	Indicates the current OTP page index. 0b: Page 0. No OTP configurations 1b: Page 1
D[1]	CC_CV	Indicates the output power status. 0b: The output is in a CV state 1b: The output is in a CC current limit state
D[0]	NTC_ENTER	Returns whether an NTC event has occurred. 0b: No NTC event has occurred 1b: An NTC event has occurred

## STATUS2

Address: 0x31

Type: Read-Only

This register is latch-off, and it is cleared when it is read.

Bits	Name	Description
D[7]	VBATT_LOW1_FLAG	Indicates if $V_{IN}$ is below its first lower threshold. 0b: $V_{IN}$ is not below its threshold 1b: $V_{IN}$ is below its threshold
D[6]	VBATT_LOW2_FLAG	Indicates if $V_{IN}$ is below its second lower threshold. 0b: $V_{IN}$ is not below its threshold 1b: $V_{IN}$ is below its threshold
D[5]	OTW1	Indicates if the device is in an over-temperature warning (OTW1) state. 0b: No OTW1 state has been detected 1b: The device is in an OTW1 state
D[4]	OTW2	Indicates if the device is in an over-temperature warning (OTW2) state. 0b: No OTW2 state has been detected 1b: The device is in an OTW2 state
D[3:1]	SELECTED_PDO_INDEX	Returns the sink's selected PDO index. 0: No PD contract 1~7: PDO1~ 7 has been selected
D[0]	PDO_TYPE	Indicates if the sink's selected PDO is fixed PDO or APDO (PPS). 0b: Fixed PDO 1b: APDO

**STATUS3**

Address: 0x32

Type: Read-Only

This register reflects an instantaneous value. It is a non-latch register.

Bits	Name	Description
D[7:0]	CONTRACT_POWER	Returns the PD contracted power in 0.5W units. Calculate the fixed PDO value with the following equation: $\text{Fixed PDO} = \text{Voltage} \times \text{Maximum Current};$ Calculate the PPS with the following equation: $\text{PPS: Max Voltage} \times \text{Max Current}.$ If there is no PD contract, the value is 7.5W or 15W depending on R <sub>p</sub> .

**ID1**

Address: 0x33

Type: Read-Only

Bits	Name	Description
D[7:0]	OTP_SUFFIX_CODE	"0x00" represents the MPQ4242-0000. "0x01" represents the MPQ4242-0001.

**ID2**

Address: 0x34

Type: Read-Only

Bits	Name	Description
D[7:0]	OTP_SOFTWARE_REVISION_NO	Stores the revision number, which is the OTP value.

**FW\_REV**

Address: 0x35

Type: Read-Only

Bits	Name	Description
D[7]	MISMATCH	Indicates if the sink request sets a mismatch bit. Defined in the PD specification. 0b: The MISMATCH bit is set to 0 1b: The MISMATCH bit is set to 1
D[6]	GIVEBACK_FLAG	This bit is set if the sink requests a GIVEBACK flag.
D[5]	CABLE_CAP	0b: The cable can handle 3A only 1b: 5A cable
D[4:0]	FIRMWARE_REVISION	Returns the PD firmware revision number.

**MAX\_REQ\_CUR**

Address: 0x36

Type: Read-Only

Bits	Name	Description
D[7:0]	MAX_REQ_CUR	Sink requested maximal operation current (MISMATCH bit = 1) in 20mA unit, only valid when GIVEBACK_FLAG = 0 and fixed PDO is selected.

**MFR\_ID**

Address: 0x37

Type: Read-Only

Bits	Name	Description
D[7:0]	MANUFACTURER_ID	Returns the manufacturer ID. The default is 0000 1001b.

**DEV\_ID**

Address: 0x38

Type: Read-Only

Bits	Name	Description
D[7:0]	DEVICE_ID	Returns the device ID. The default is 0101 1000b.

**CLK\_ON**

Address: 0x39

Type: Write-Only

Bits	Name	Description
D[7:0]	CLOCK_ON	Enables the digital clock. Write 0x01 to enable the digital clock. No I <sup>2</sup> C registers can be modified before the digital clock is enabled. This bit automatically resets to 0 after the clock is enabled. The digital clock is enabled when a USB Type-C device is connected. Write 0 to 0x39, set the EN bit to 0, or pull down the EN pin and VIN pin below their UVLO thresholds to disable the digital clock again.

**GPIO1 and GPIO2 Options**

<b>GPIO1 Options</b>	GATE	POWER_SHARE1	FAULT	NTC2	ATTACH_FLT_ALT	IMON
<b>GPIO2 Options</b>	POL	NTC	VCONN_IN (max 5.25V)	LED_PWM	ATTACH	POWER_SHARE2

## APPLICATION INFORMATION

### COMPONENT SELECTION

#### Selecting the Inductor

In a buck-boost topology, the inductor must support buck applications with the maximum input voltage ( $V_{IN}$ ) and boost applications with the minimum  $V_{IN}$ . Two critical inductance values can be determined according to the buck mode and boost mode current ripple. The first inductance value ( $L_{MIN\_BUCK}$ ) can be calculated with Equation (3):

$$L_{MIN\_BUCK} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{REQ} \times \Delta I_L} \quad (3)$$

The second inductance value ( $L_{MIN\_BOOST}$ ) can be calculated with Equation (4):

$$L_{MIN\_BOOST} = \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{V_{OUT} \times f_{REQ} \times \Delta I_L} \quad (4)$$

Where  $f_{REQ}$  is the switching frequency, and  $\Delta I_L$  is the peak-to-peak inductor current ripple.

Typically, the peak-to-peak ripple can be set at 1A to 3A of the inductor current. In addition to the inductance value, the inductor must support the peak current in buck and boost applications to avoid saturation. The peak current in buck mode can be calculated with Equation (5):

$$I_{PEAK\_BUCK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{2 \times V_{IN(MAX)} \times f_{REQ} \times L} \quad (5)$$

The peak current in boost mode can be

calculated with Equation (6):

$$I_{PEAK\_BOOST} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN(MIN)}} + \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{2 \times V_{OUT} \times f_{REQ} \times L} \quad (6)$$

Where  $\eta$  is the estimated efficiency of the MPQ4242

#### Selecting the Input Capacitor

It is recommended to use ceramic capacitors plus an electrolytic capacitor for the input and output capacitors. This filters the input and output ripple current and helps achieve stable operation. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For automotive applications, a 100 $\mu$ F electrolytic capacitor and two 10 $\mu$ F + 0.1 $\mu$ F ceramic capacitors are recommended.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional, high-quality ceramic capacitors as close to  $V_{IN}$  as possible.

#### Selecting the Output Capacitor

The device requires an output capacitor ( $C_{OUT}$ ) to maintain the DC output voltage. Typically, a 100 $\mu$ F polymer or hybrid electric capacitor and two 10 $\mu$ F + 0.1 $\mu$ F ceramic output capacitors are recommended for excellent loop stability and transient response.

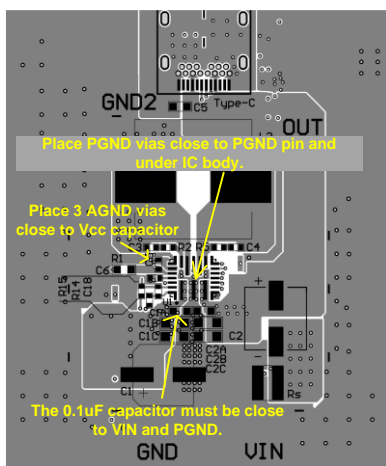
The E-capacitor's ESR must be smaller than 50m $\Omega$  for excellent loop stability, transient response, and efficiency.

In GND to battery short applications, the output E-capacitor's negative node must be connected to the current-sense resistor (see Figure 24 on page 55).

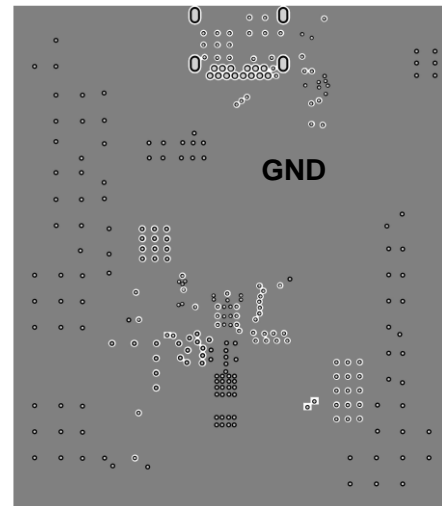
### PCB Layout Guidelines

Efficient PCB layout is critical for standard operation and thermal dissipation. For the best results, refer to Figure 23 and follow the guidelines below:

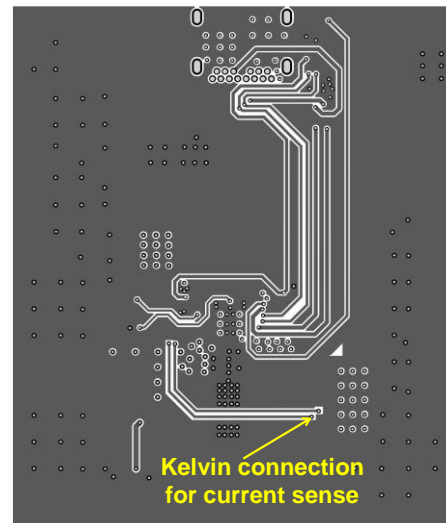
1. Use short, direct, and wide traces to connect OUT. Adding vias under the IC, then route the OUT trace on both PCB layers.
2. Place a large copper plane for PGND. Add multiple vias to improve thermal dissipation. Connect AGND to PGND.
3. Place PGND vias close to PGND pin and under the IC's body.
4. Place the VCC decoupling capacitor as close as possible to the VCC pin. Place 3 vias close to the VCC decoupling capacitor's AGND terminal.
5. Place a large copper plane for SW .
6. Place two ceramic input decoupling capacitors as close as possible to VIN, VOUT, and PGND to improve EMI performance.
7. Place an input filter at the bottom layer to improve EMI performance.
8. Use Kelvin connections for the output current sense traces (ISENS+ and ISENS-).
9. Place the input capacitor also close to the VIN pin as possible. Especially the 0.1 $\mu$ F capacitor should be placed close to the VIN pin and PGND.
10. Make the HS\_G trace wide and short.



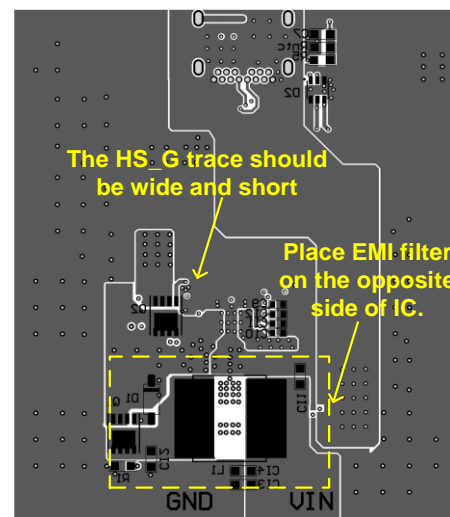
**Top Layer**



**Mid-Layer 1**



**Mid-Layer 2**



**Bottom Layer**

**Figure 23: Recommended PCB Layout**

## TYPICAL APPLICATION CIRCUITS

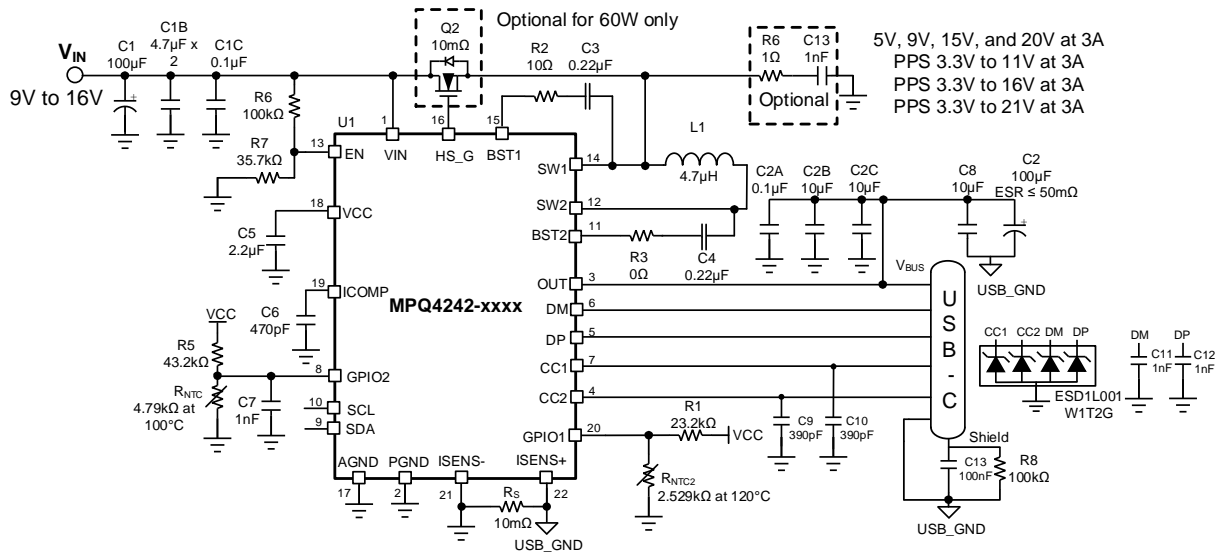


Figure 24: MPQ4242 60W PD Application

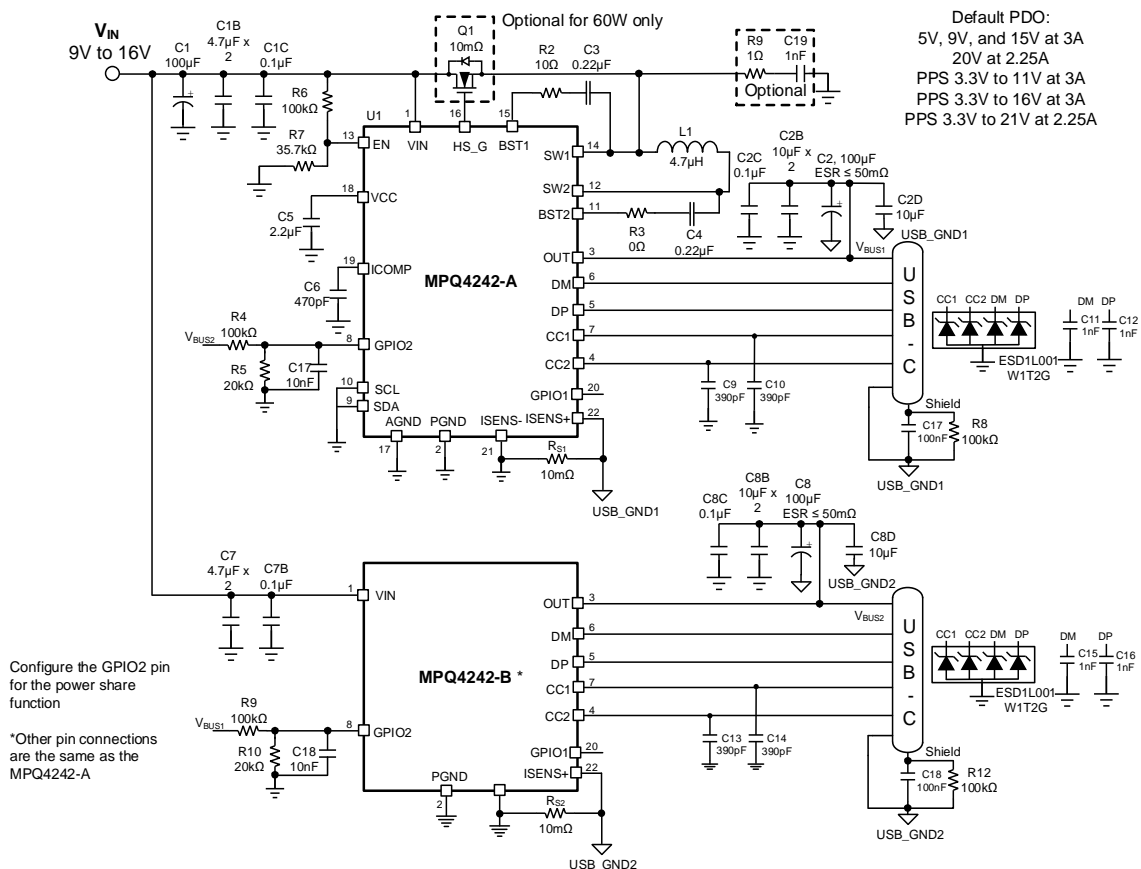


Figure 25: MPQ4242 Dual-Channel 45W PD Application with GPIO2\_POWER\_SHARE (18) (19) (20)

**Notes:**

- 18) See Table 5 on page 29 for the GPIO2 power share PDP management.  $V_{BUS}$  exceeds 11.2V to trigger power share function (GPIO2 input voltage > 1.87V).
- 19) GPIO1 can be configured as a gate drive for the external low-side N-channel power MOSFET used for USB\_GND short to battery protection.
- 20) TVS diodes are required to pass the  $\pm 8kV$  contact  $\neq$   $\pm 15kV$  air discharge per IEC ESD specifications.



**MPQ4242GQV-0000 CONFIGURATION TABLE**

OTP Items(PDO)	Enabled/Disabled	PDO Type	Voltage Setting	Current Setting
PDO1	Enabled	Fixed PDO	5V	3A
PDO2	1b: Enabled (default)	0b: Fixed PDO (default)	9V (default)	3A
PDO3	1b: Enabled (default)	0b: Fixed PDO (default)	15V (default)	3A
PDO4	1b: Enabled (default)	0b: Fixed PDO (default)	20V (default)	3A
PDO5	1b: Enabled (default)	1b: APDO (default)	3.3V to 11V	3A
PDO6	1b: Enabled (default)	1b: APDO (default)	3.3V to 16V	3A
PDO7	1b: Enabled (default)	1b: APDO (default)	3.3V to 21V	3A

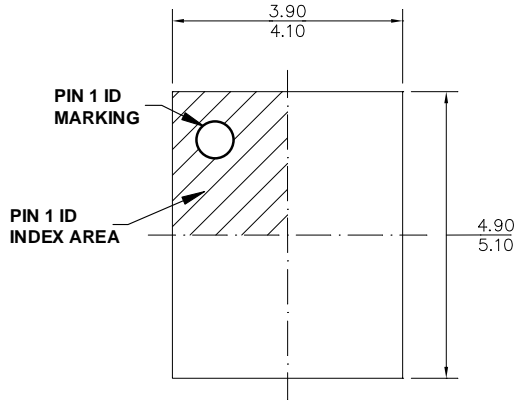
**Table 7: OTP Descriptions**

OTP Items	Description	Value
GPIO1	Configures the GPIO1 pin's function.	000b: POWER_SHARE function (default)
GPIO2	Configures the GPIO2 pin's function.	000b: Reserved
OTP_THRESHOLD	Sets the over-temperature shutdown threshold.	010b: 175°C (default)
OTW1_THRESHOLD	Sets-the over temperature warning threshold.	100b: 135°C (default)
OTW1_PDP	Sets the maximum power rating when the die temp drops below its threshold.	45W (default)
OTW1_PDO_SELECT	Selects which voltage is enabled in the PDO list.	0xBE (default)
OTW2_THRESHOLD	Sets the over-temperature warning threshold.	110b: 155°C (default)
OTW2_NTC_PDP	Set the maximum power rating when the die temperature drops below its threshold.	30W (default)
OTW2_NTC_PDO_SELECT	Selects which voltage is enabled in the PDO list.	0xBE (default)
NTC_HYSTERESIS	Sets the NTC thermal recovery hysteresis.	1b: 20%( default)
NTC_MODE	Sets the MPQ4242 behavior when the NTC is triggered.	1b: Reduce PD power to the value set by OTW2_NTC_PDP
VBATT_LOW_THLD1	Sets the first threshold for V <sub>IN</sub> detection.	0100b: 11.4V (default)
VBATT_LOW_THLD2	Sets the second threshold for V <sub>IN</sub> detection.	1000b: 9V (default)
VBATT_LOW_THLD3	Sets the third threshold for V <sub>IN</sub> detection. The device shuts down after this threshold is triggered.	1010b: 6.2V (default)
VBATT_LOW_BLK	Sets the V <sub>BATT</sub> low 1 and V <sub>BATT</sub> low 2 blank times.	10b: 320ms (default)
VBATT_LOW1_PDP	Sets the maximum power rating when V <sub>BATT</sub> falls below its first threshold.	45W (default)
VBATT_L1_PDO_SELECT	Select s the voltage that is enabled in the PDO list.	0xBE (default)
VBATT_LOW2_PDP	Sets the maximum power rating when V <sub>BATT</sub> falls below its second threshold.	15W (default)
VBATT_L2_PDO_SELECT	Selects the voltage that is enabled in the PDO list.	0xBE (default)
PS_PDP_THD	Set the thresholds to which the PDO power rating is reduced.	45W (default)
PS_PDP_THD_PDO_SELECT	Selects which voltage is enabled in the PDO list.	0xBE (default)
VBUS_VOLTAGE	Sets the default VBUS voltage.	10b: 5.1V (default)

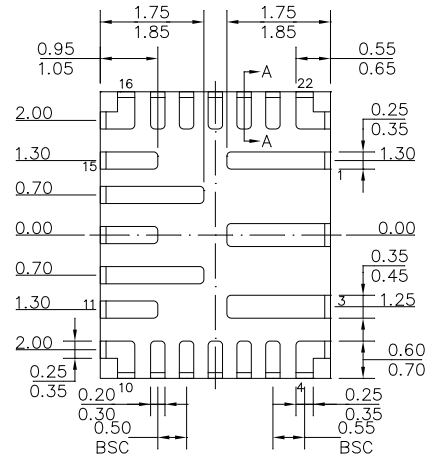
MODE	Sets the PFM/PWM mode.	1b: Forced PWM mode (default)
FREQ	Sets the switching frequency	01b: 420kHz (default)
DITHER	Sets the spread spectrum feature	0b: No frequency spread spectrum (default)
EN_OFF_TIMER	Sets the EN off timer.	000b: No delay (default)
LINE_DROP_COMP	Sets the output voltage compensation vs load feature.	00b: No compensation (default)
SLEW_RATE	Sets the output slew rate to adjust $V_{OUT}$ .	1b: 0.08mV/ $\mu$ s $V_{REF}$ rising slew rate, 0.08mV/ $\mu$ s $V_{REF}$ falling slew rate (default)
PEAK_CL	Sets the high-side peak current limit in boost mode.	11b: 20A (default)
RSENS	Sets the external CC limit $R_{SENS}$ resistor value.	1b: 10m $\Omega$
EXT_HS_FET RON	Sets the $R_{DS(ON)}$ of the external N-channel MOSFET at 10V $_{GS}$ .	000b: This function is disabled (default)
CC_BLANK_TIMER	Sets the blank time when the output CC over-current condition is reached.	01b: 2ms (default)
LEGACY_CHARGING_MODE_SEL	Selects QC 3.0/DCP short mode / Divider mode.	00b: All DCP modes are active (default)
I2C_SLAVE_ADDRESS	Sets the MPQ4242's I <sup>2</sup> C slave address.	61h (default)
VIN_OVP	Enables the VIN_OVP function. When $V_{IN} > 22V$ , the MPQ4242 shuts down.	0b: Disable VIN_OVP function

PACKAGE INFORMATION

QFN-22 (4mmx5mm)



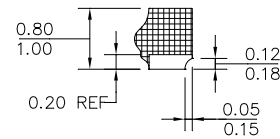
**TOP VIEW**



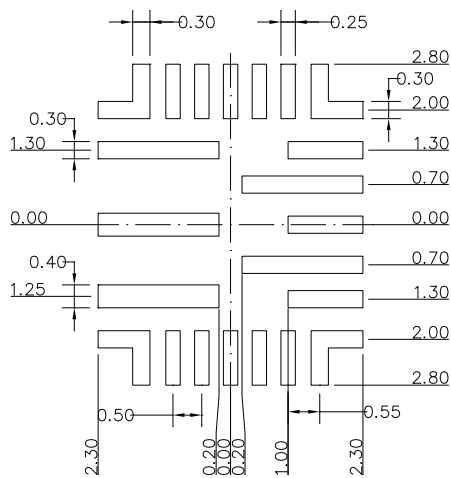
**BOTTOM VIEW**



**SIDE VIEW**



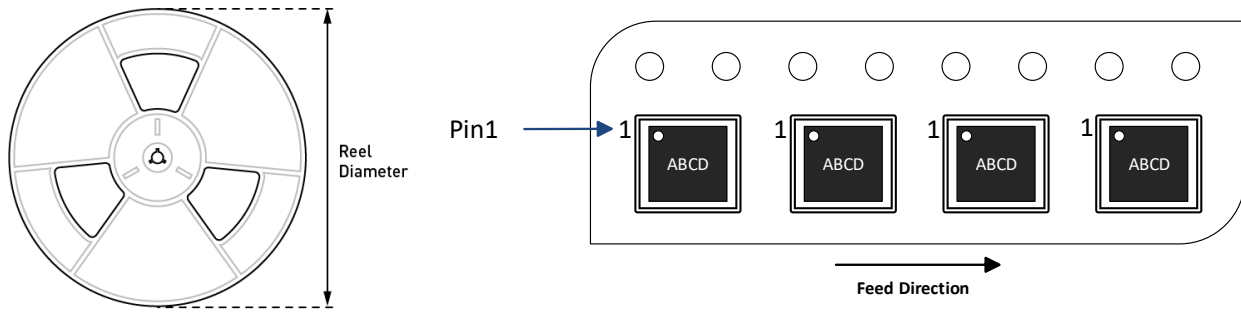
**SECTION A-A**



**RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

**CARRIER INFORMATION**


Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4242GVE-0000-AEC1-Z	QFN-22 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4242GVE-0001-AEC1-Z	QFN-22 (4mmx5mm)						
MPQ4242GVE-0015-AEC1-Z	QFN-22 (4mmx5mm)						
MPQ4242GVE-xxxx-AEC1-Z	QFN-22 (4mmx5mm)						

## REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/10/2022	Initial Release	-

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