DESCRIPTION

The MPM4730 is a synchronous, four-switch integrated buck-boost module with a 2.8V to 22V input voltage (V$_{IN}$) range. The device regulates the output voltage (V$_{OUT}$) with high efficiency, and provides integrated V$_{OUT}$ scaling and output current (I$_{OUT}$) limit functions.

The MPM4730 uses constant-on-time (COT) control in buck mode and constant-off-time control in boost mode, providing a fast load transient response and smooth buck-boost mode transients. The MPM4730 features automatic pulse-frequency modulation (PFM)/pulse-width modulation (PWM) or forced PWM switching modes. It also provides a selectable switching frequency (f$_{SW}$) and configurable soft start.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The MPM4730 is available in an ECLGA-18 (3mmx3mm) package.

FEATURES

- 2.8V to 22V Operating Input Voltage (V$_{IN}$) Range
- 0.08V to 1.637V Reference Voltage (V$_{REF}$) Range with 0.8mV Resolution via the I²C [1] (Default 1V V$_{REF}$)
- Configurable Output Voltage (V$_{OUT}$) via the FB Pin
- 1A Max Output Current (I$_{OUT}$)
- 500kHz/750kHz Selectable Switching Frequency (f$_{SW}$)
- Output Over-Voltage Protection (OVP) and Short-Circuit Protection (SCP) with Hiccup Mode
- Over-Temperature Warning (OTW) and Shutdown
- I²C Interface with ALT Pin
- One-Time Programmable (OTP) Non-Volatile Memory (NVM)
- I²C-Configurable Pulse-Frequency Modulation (PFM)/Pulse-Width Modulation (PWM) Mode, Soft Start, Over-Current Protection (OCP), and OVP
- Configurable EN Shutdown Discharge
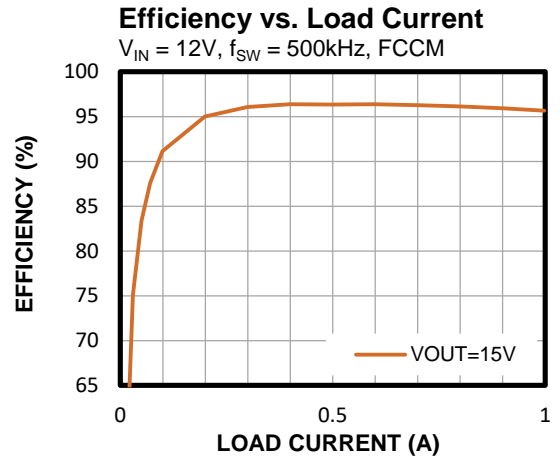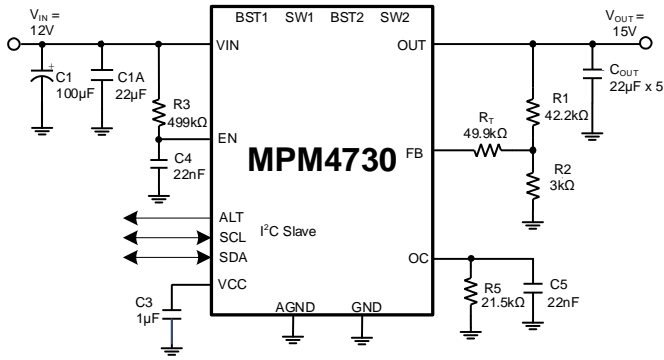- Available in an ECLGA-18 (3mmx3mmx1.86mm) Package

APPLICATIONS

- Server Power Supply Units (PSUs)
- Buck-Boost Bus Supplies

Note:

1) For applications where V$_{OUT}$ is below 3V, the switching frequency decreases.

TYPICAL APPLICATION

Efficiency vs. Load Current
V$_{IN}$ = 12V, f$_{SW}$ = 500kHz, FCCM

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL
MPM4730GPQ-xxxx**	ECLGA-18 (3mmx3mmx1.86mm)	*See Below*	3
MPM4730GPQ-0000	ECLGA-18 (3mmx3mmx1.86mm)	*See Below*	3

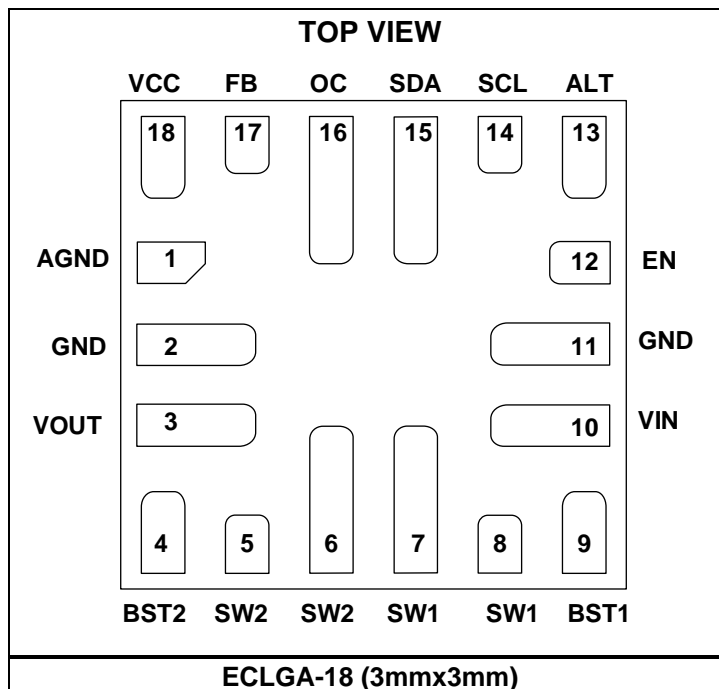* For Tape & Reel, add suffix -Z (e.g. MPM4730GPQ-xxxx-Z).

** The 4-digit suffix code "xxxx" is the configuration identifier for the register settings stored in the multiple-time programmable (MTP) memory. For the default configuration, the code is "0000". See Table 2 on page 30 and Table 3 on page 30 for the detailed configuration information. For customized configurations, contact an MPS FAE to assign a 4-digit suffix code.

TOP MARKING

$\overline{\text{BXLY}}$
LLL

BXL: Product code of MPM4730GPQ
Y: Year code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW

	VCC	FB	OC	SDA	SCL	ALT	
	18	17	16	15	14	13	
AGND	1					12	EN
GND	2					11	GND
VOUT	3					10	VIN
	4	5	6	7	8	9	
	BST2	SW2	SW2	SW1	SW1	BST1	

ECLGA-18 (3mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	AGND	**Analog ground.** Connect AGND to GND.
2, 11	GND	**Power ground.** The GND pin is the reference ground of the regulated output voltage (V$_{OUT}$). GND requires extra consideration during PCB layout. Connect GND with copper traces and vias.
3	VOUT	**Output power pin.** Place the output capacitor close to VOUT and GND.
4	BST2	**Test pin.** The BST2 pin can be floated.
5, 6	SW2	**Test pin.** The internal switches are connected to SW2. This is a test pin that can be floated.
7, 8	SW1	**Test pin.** The internal switches are connected to SW1. This is a test pin that can be floated.
9	BST1	**Test pin.** The BST1 pin can be floated.
10	VIN	**Supply voltage.** The VIN pin is the drain of the internal power device, and it provides power to the entire chip. The MPM4730 operates from a 2.8V to 22V input voltage (V$_{IN}$). An input capacitor (C$_{IN}$) is required to prevent large voltage spikes from appearing at the input. Place C$_{IN}$ as close to the IC as possible.
12	EN	**On/off control for the entire chip.** Drive the EN pin high to turn the device on. Drive EN low or float EN to turn it off. EN has an internal 2MΩ pull-down resistor connected to ground.
13	ALT	**Alert output.** If the ALT pin pulls to logic low, a fault or warning has occurred.
14	SCL	**Clock pin of the I²C interface.** The SCL pin can support an I²C clock up to 3.4MHz. If not used, SCL should be pulled up to VCC.
15	SDA	**Data pin of the I²C interface.** If the SDA pin is not used, SDA should be pulled up to VCC.
16	OC	**Output constant current limit setting pin.**
17	FB	**Feedback.** An external resistor divider from the output to AGND (tapped to FB) sets V$_{OUT}$.
18	VCC	**Internal 3.65V low-dropout (LDO) regulator output.** Decouple the VCC pin with a 1µF capacitor.

ABSOLUTE MAXIMUM RATINGS [2]

Supply voltage (V_{IN}) 26V
V_{OUT}.. 24V
$V_{SW1/SW2}$ (DC) ....-0.3V to +24.3V
$V_{SW1/SW2}$ (10ns)................................-7V to +26V
$V_{BST1/BST2}$ .... V_{SWx} + 4V
V_{EN}...-0.3V to +26V
V_{ALT}...-0.3V to +5.5V
All other pins ....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) [3] [6]
.... 4.36W
Junction temperature (T_J) ....150°C
Lead temperature ....260°C
Storage temperature............... -65°C to +150°C

ESD Ratings [4]

Human body model (HBM) ....±2kV
Charged-device model (CDM)....................±1kV

Recommended Operating Conditions [5]

Operating input voltage (V_{IN}) range……………...
……………………………………………2.8V to 22V
Output voltage (V_{OUT}) range...........1V to 20.47V
Output current (I_{OUT}).............................. Max 1A
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

ECLGA-18 (3mmx3mm)
MPM4730 [6]…………………28.7....10.63..°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101. The JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. The JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on the MPM4730 evaluation board, a 4-layer PCB, 51mmx51mm.

ELECTRICAL CHARACTERISTICS

V$_{IN}$ = 12V, V$_{EN}$ = 5V, T$_J$ = -40°C to +125°C [7], typical value is tested at T$_J$ = 25°C, unless otherwise noted.
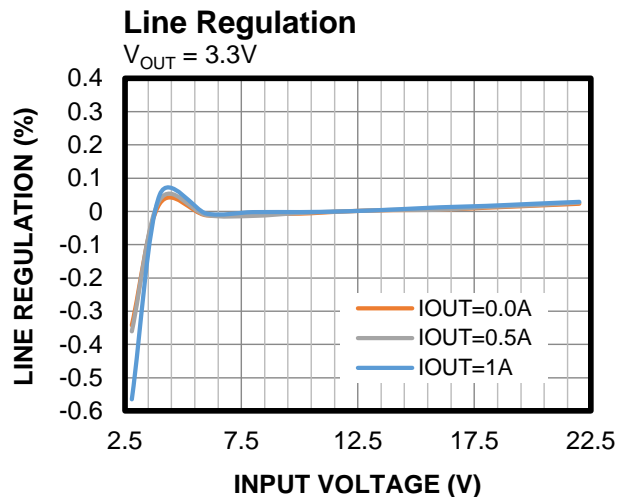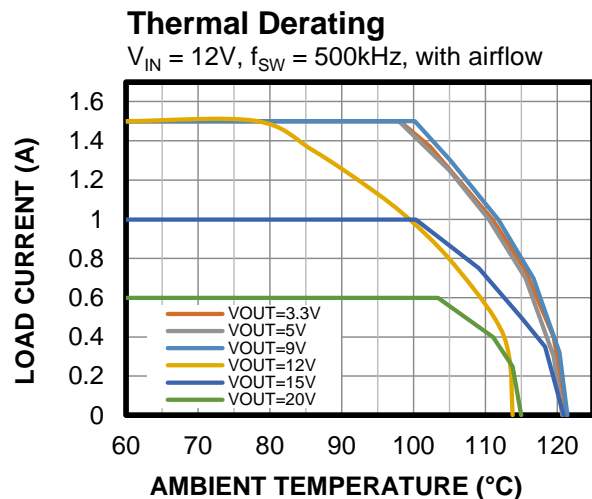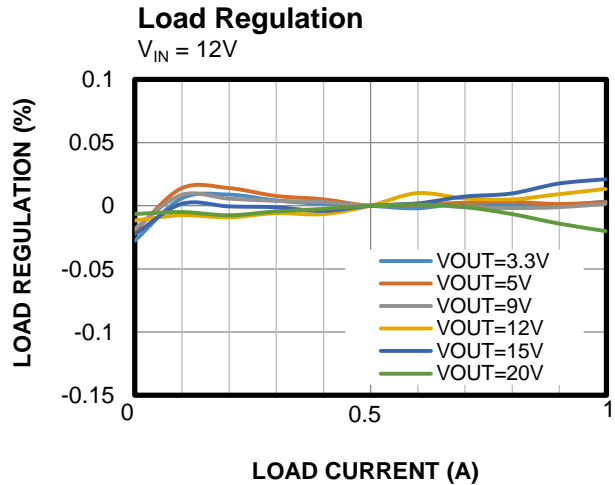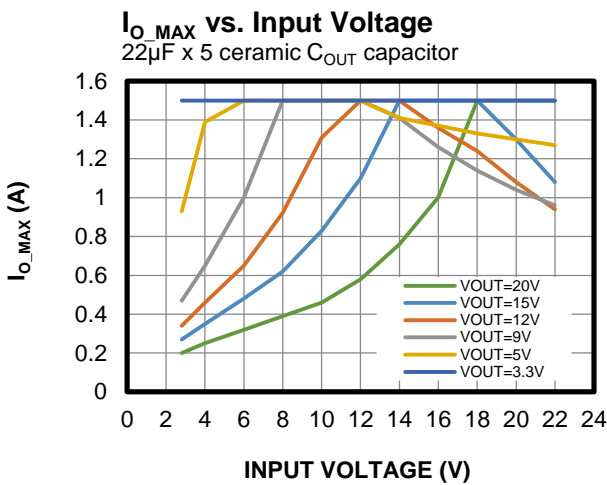
Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I$_{IN}$	V$_{EN}$ = 0V		0	3	µA
Quiescent supply current	I$_Q$	Non-switching, I²C sets PFM mode		1		mA
EN rising threshold	V$_{EN\_RISING}$		1	1.1	1.2	V
EN hysteresis	V$_{EN\_HYS}$			110		mV
EN-to-ground resistance	R$_{EN}$	V$_{EN}$ = 2V		2		MΩ
EN on to output voltage (V$_{OUT}$) > 90% delay	t$_{DELAY}$	See Figure 9 on page 18		3.6		ms
VCC regulator	V$_{CC}$		3.3	3.65	4	V
VCC load regulation	V$_{CC\_LOG}$	I$_{CC}$ = 10mA			1	%
Input voltage (V$_{IN}$) under-voltage lockout (UVLO) rising threshold	V$_{IN\_UVLO}$		2.5	2.65	2.8	V
V$_{IN}$ UVLO threshold hysteresis	V$_{UVLO\_HYS}$			160		mV
Power Converter						
Feedback voltage	V$_{FB}$	T$_J$ = 25°C	-1%	1000	+1%	mV
		T$_J$ = -40°C to +125°C	-1.5%	1000	+1.5%	mV
Feedback current	I$_{FB}$	V$_{FB}$ = 1.05V		10		nA
Output discharge resistance	R$_{DIS}$			60	100	Ω
Switch leakage	I$_{SWLKG}$	V$_{EN}$ = 0V, V$_{SW1/SW2}$ = 22V, T$_J$ = 25°C			1	µA
Oscillator frequency	f$_{SW1}$	Set FREQ = 500kHz via I²C, T$_J$ = 25°C	-20%	520	+20%	kHz
	f$_{S2W}$	Set FREQ = 750kHz via I²C, T$_J$ = 25°C		750		kHz
Minimum on time [8]	t$_{ON\_MIN1}$	Switch A, B, C, D		160		ns
Maximum duty cycle [8]	D$_{MAX}$	Buck mode, FREQ = 500kHz		85		%
Minimum duty cycle [8]	D$_{MIN}$	Boost mode, FREQ = 500kHz		15		%
Soft-start time	t$_{SS}$	Can be changed by I²C, V$_{REF}$ from 0V to 1V, default SS time		3.5		ms
Protections						
Output over-voltage protection (OVP)	V$_{OVP\_R}$		150%	160%	170%	V$_{REF}$
Output OVP recovery	V$_{OVP\_F}$		130%	140%	150%	V$_{REF}$
Output current (I$_{OUT}$) limit threshold [8]	I$_{OUT\_LIMT}$			2		A
Output under-voltage (UV) threshold	V$_{UVP}$	20µs deglitch, UV falling	45%	50%	55%	V$_{REF}$
ALT sink current capability	V$_{ALT\_LOW}$	Sink 4mA		0.2	0.4	V

ELECTRICAL CHARACTERISTICS *(continued)*

V$_{IN}$ = 12V, V$_{EN}$ = 5V, T$_J$ = -40°C to +125°C [7]**, typical value is tested at T$_J$ = 25°C, unless otherwise noted.**

Parameter	Symbol	Condition	Min	Typ	Max	Units
ALT leakage	I$_{ALT\_LKG}$	V$_{PULL}$ = 5V			1	µA
Thermal shutdown rising threshold [8]	T$_{STD}$			150		°C
Thermal hysteresis [8]	T$_{STD\_HYS}$			20		°C
I²C Specifications [8]						
Input logic high	V$_{IH}$	I²C pull-up V$_{DD}$ can be 1.8V to 5V	1.4			V
Input logic low	V$_{IL}$				0.4	V
Output voltage logic low	V$_{OUT\_L}$	Sink current = 4mA			0.4	V
SCL clock frequency	f$_{SCL}$			400	3400	kHz
SCL high time	t$_{HIGH}$		60			ns
SCL low time	t$_{LOW}$		160			ns
Data set-up time	t$_{SU\_DAT}$		10			ns
Data hold time	t$_{HD\_DAT}$		0	60		ns
Set-up time for (repeated) start command	t$_{SU\_STA}$		160			ns
Hold time for (repeated) start command	t$_{HD\_STA}$		160			ns
Bus free time between a start and a stop command	t$_{BUF}$		160			ns
Set-up time for stop command	t$_{SU\_STO}$		160			ns
SCL and SDA rising time	t$_R$		10		300	ns
SCL and SDA falling time	t$_F$		10		300	ns
Pulse width of suppressed spike	t$_{SP}$		0		50	ns
Capacitance for each bus line	C$_B$				400	pF

Notes:

7) Not tested in production. Guaranteed by over-temperature (OT) correlation.
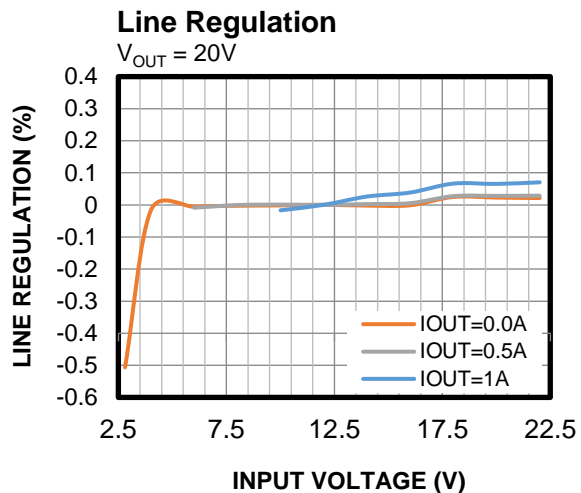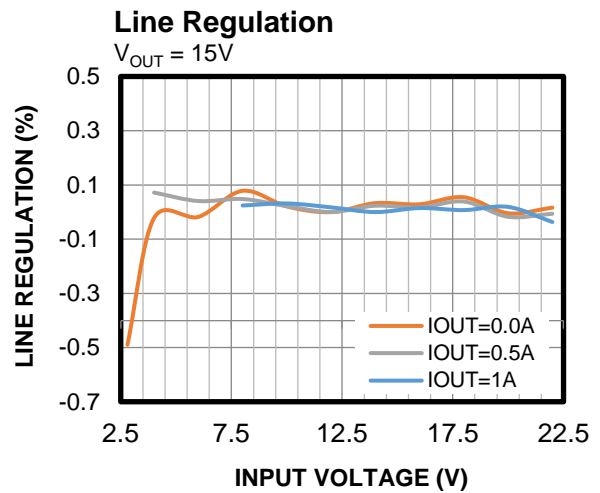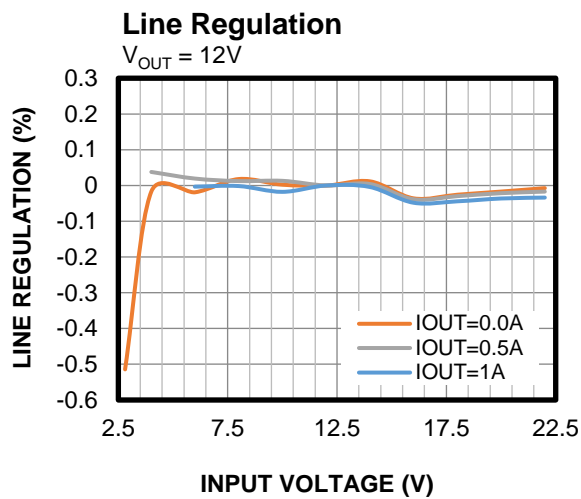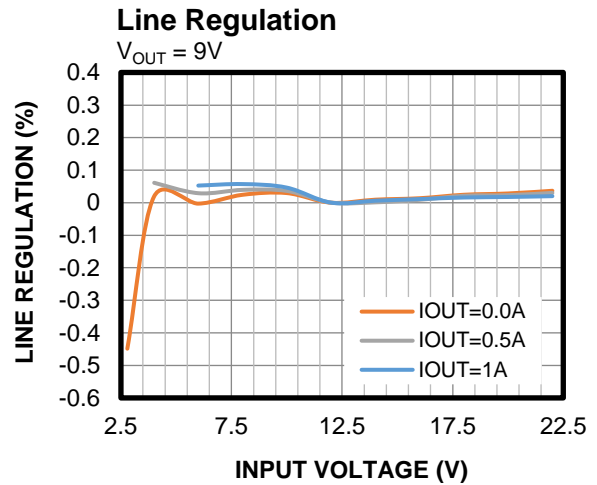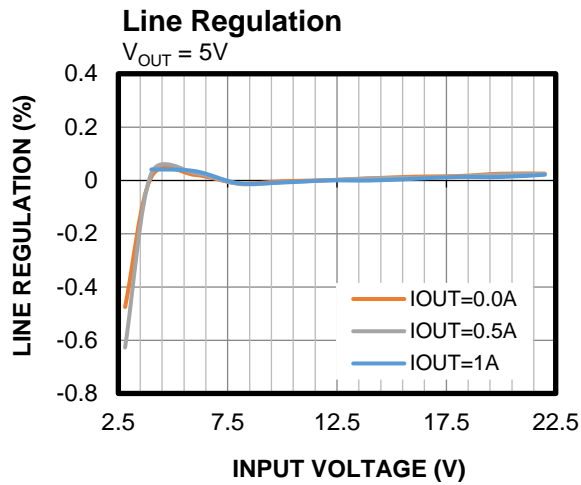8) Guaranteed by engineering sample characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 5V, FCCM, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

Efficiency vs. Load Current
V_{IN} = 12V, f_{SW} = 500kHz, FCCM

Thermal Derating
V_{IN} = 12V, f_{SW} = 500kHz, no airflow

I_{O_MAX} vs. Input Voltage
22µF x 5 ceramic C_{OUT} capacitor

Load Regulation
V_{IN} = 12V

Thermal Derating
V_{IN} = 12V, f_{SW} = 500kHz, with airflow

Line Regulation
V_{OUT} = 3.3V

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V$_{IN}$ = 12V, V$_{OUT}$ = 5V, FCCM,   **f$_{SW}$ = 500kHz, T$_A$ = 25°C, unless otherwise noted.**

Line Regulation
V$_{OUT}$ = 5V

Line Regulation
V$_{OUT}$ = 9V

Line Regulation
V$_{OUT}$ = 12V

Line Regulation
V$_{OUT}$ = 15V

Line Regulation
V$_{OUT}$ = 20V
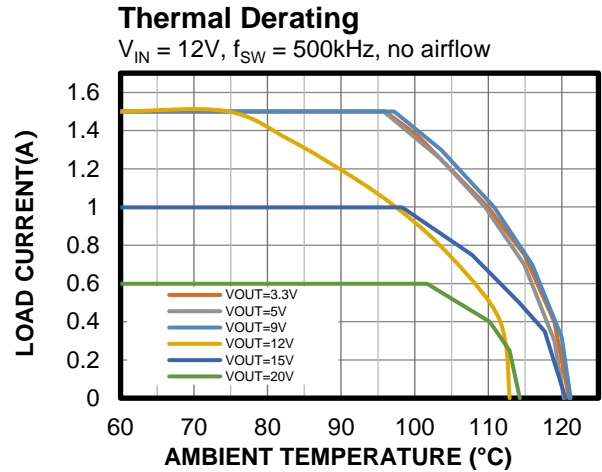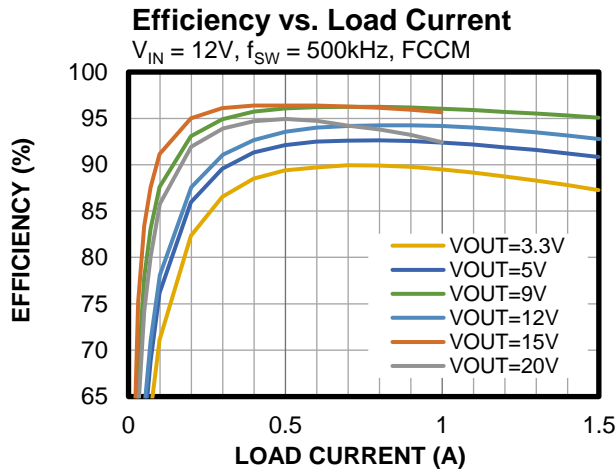
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V$_{IN}$ = 12V, V$_{OUT}$ = 5V, FCCM,   f$_{SW}$ = 500kHz, T$_A$ = 25°C, unless otherwise noted.

EN Bit Enabled via the I²C
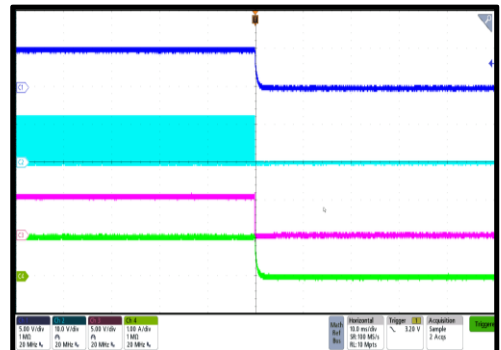I$_{OUT}$ = 0A

CH1: V$_{OUT}$
5V/div.

CH2: SW1
10V/div.

CH3: SW2
5V/div.
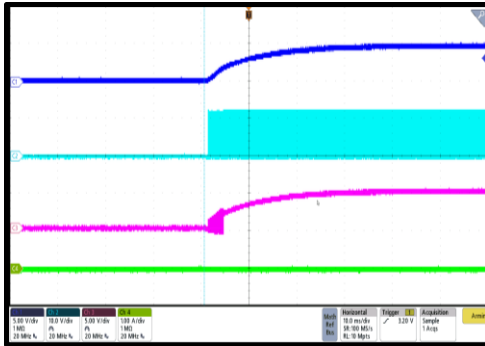
CH4: I$_{OUT}$
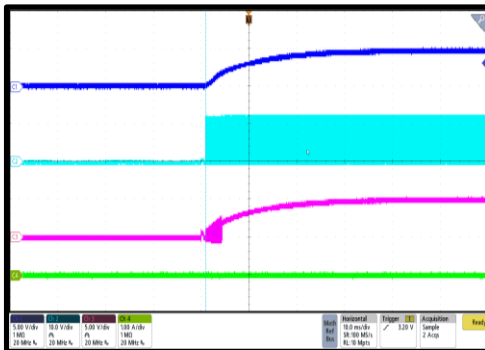1A/div.

EN Bit Enabled via the I²C
I$_{OUT}$ = 1A

CH1: V$_{OUT}$
5V/div.

CH2: SW1
10V/div.

CH3: SW2
5V/div.
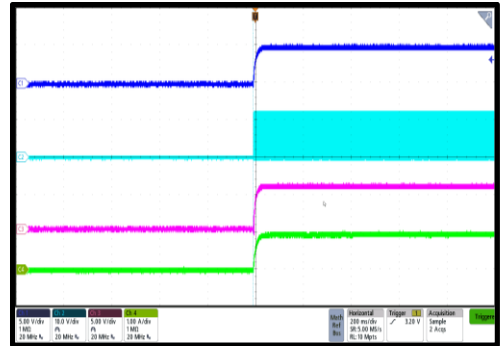
CH4: I$_{OUT}$
1A/div.

EN Bit Shutdown via the I²C
I$_{OUT}$ = 0A

CH1: V$_{OUT}$
5V/div.

CH2: SW1
10V/div.

CH3: SW2
5V/div.
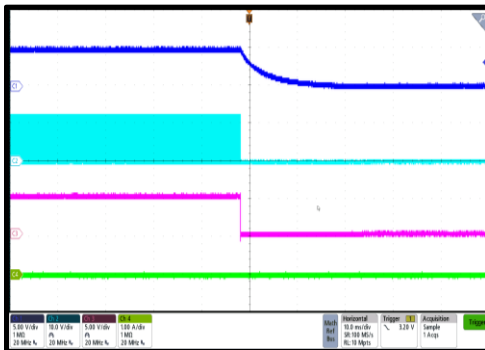
CH4: I$_{OUT}$
1A/div.

EN Bit Shutdown via the I²C
I$_{OUT}$ = 1A

CH1: V$_{OUT}$
5V/div.

CH2: SW1
10V/div.

CH3: SW2
5V/div.

CH4: I$_{OUT}$
1A/div.
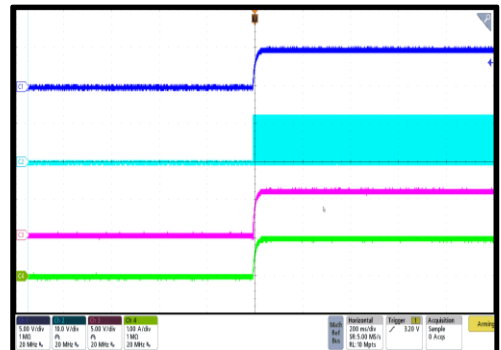
EN Pin Enabled
I$_{OUT}$ = 0A

CH1: V$_{OUT}$
5V/div.

CH2: SW1
10V/div.

CH3: SW2
5V/div.

CH4: I$_{OUT}$
1A/div.

EN Pin Enabled
I$_{OUT}$ = 1A

CH1: V$_{OUT}$
5V/div.

CH2: SW1
10V/div.

CH3: SW2
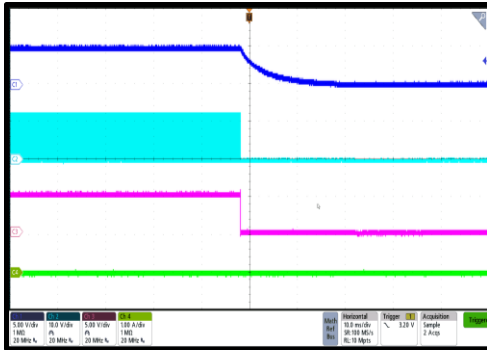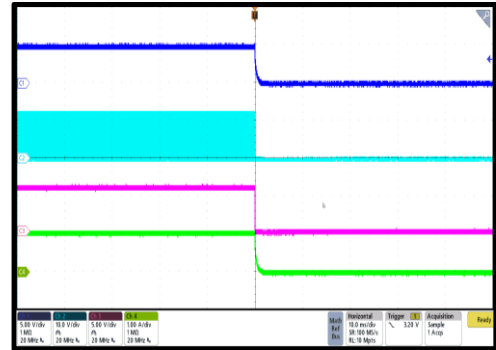5V/div.

CH4: I$_{OUT}$
1A/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V$_{IN}$ = 12V, V$_{OUT}$ = 5V, FCCM,   f$_{SW}$ = 500kHz, T$_A$ = 25°C, unless otherwise noted.

EN Pin Disabled
I$_{OUT}$ = 0A

CH1: V$_{OUT}$
5V/div.

CH2: SW1
10V/div.

CH3: SW2
5V/div.

CH4: I$_{OUT}$
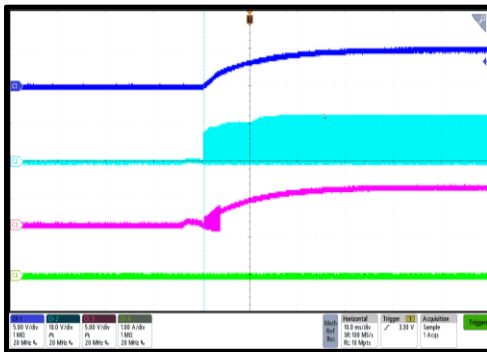1A/div.

EN Pin Disabled
I$_{OUT}$ = 1A

CH1: V$_{OUT}$
5V/div.

CH2: SW1
10V/div.

CH3: SW2
5V/div.

CH4: I$_{OUT}$
1A/div.

Start-Up through VIN
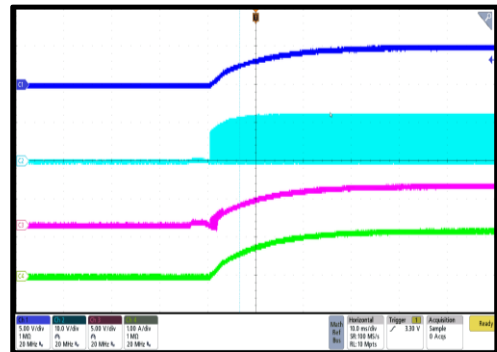I$_{OUT}$ = 0A

CH1: V$_{OUT}$
5V/div.

CH2: SW1
10V/div.

CH3: SW2
5V/div.

CH4: I$_{OUT}$
1A/div.

Start-Up through VIN
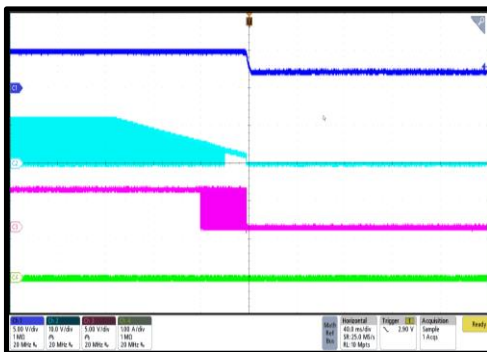I$_{OUT}$ = 1A

CH1: V$_{OUT}$
5V/div.

CH2: SW1
10V/div.

CH3: SW2
5V/div.

CH4: I$_{OUT}$
1A/div.

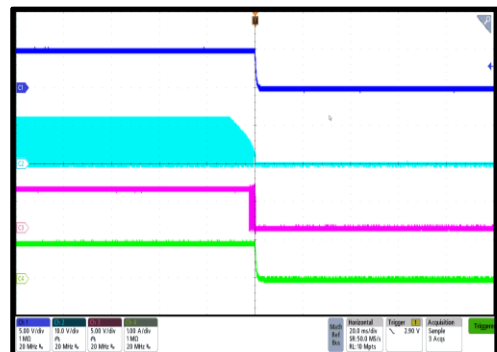**Shutdown through VIN**
I$_{OUT}$ = 0A

CH1: V$_{OUT}$
5V/div.

CH2: SW1
10V/div.

CH3: SW2
5V/div.

CH4: I$_{OUT}$
1A/div.

Shutdown through VIN
I$_{OUT}$ = 1A

CH1: V$_{OUT}$
5V/div.

CH2: SW1
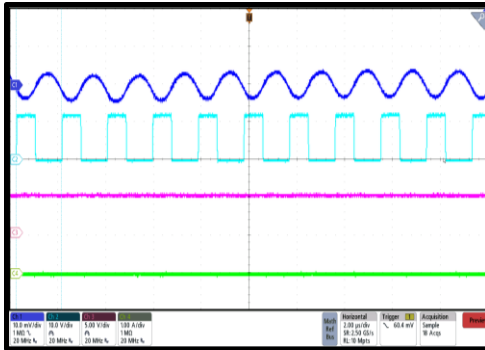10V/div.

CH3: SW2
5V/div.

CH4: I$_{OUT}$
1A/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V$_{IN}$ = 12V, V$_{OUT}$ = 5V, FCCM,   f$_{SW}$ = 500kHz, T$_A$ = 25°C, unless otherwise noted.

Steady State
f$_{SW}$ = 500kHz, 0A

CH1: V$_{OUT/AC}$
10mV/div.
CH2: SW1
10V/div.

CH3: SW2
5V/div.
CH4: I$_{OUT}$
1A/div.

Steady State
f$_{SW}$ = 500kHz, 1A

CH1: V$_{OUT/AC}$
10mV/div.
CH2: SW1
10V/div.

CH3: SW2
5V/div.
CH4: I$_{OUT}$
1A/div.
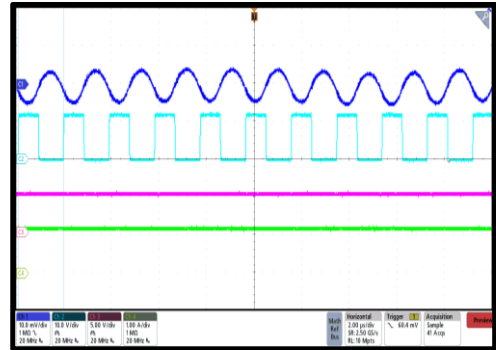
Steady State
f$_{SW}$ = 750kHz, 0A

CH1: V$_{OUT/AC}$
10mV/div.
CH2: SW1
10V/div.

CH3: SW2
5V/div.
CH4: I$_{OUT}$
1A/div.
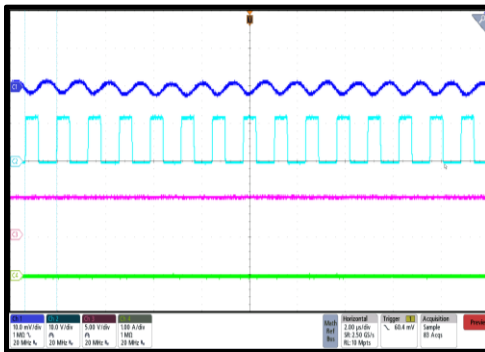
Steady State
f$_{SW}$ = 750kHz, 1A

CH1: V$_{OUT/AC}$
10mV/div.
CH2: SW1
10V/div.

CH3: SW2
5V/div.
CH4: I$_{OUT}$
1A/div.
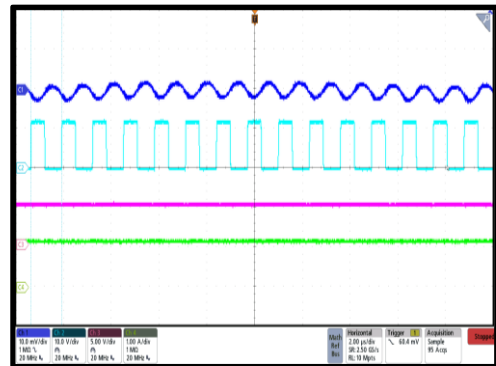
I^{2}C VID
V$_{OUT}$ = 5V to 12V, I$_{OUT}$ = 0A

CH1: V$_{OUT}$
10V/div.
CH2: SW1
10V/div.

CH3: SW2
10V/div.
CH4: I$_{OUT}$
1A/div.

I^{2}C VID
V$_{OUT}$ = 12V to 5V, I$_{OUT}$ = 0A

CH1: V$_{OUT}$
10V/div.
CH2: SW1
10V/div.

CH3: SW2
10V/div.
CH4: I$_{OUT}$
1A/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V$_{IN}$ = 12V, V$_{OUT}$ = 5V, FCCM, f$_{SW}$ **= 500kHz, T$_A$ = 25°C, unless otherwise noted.**

I²C VID
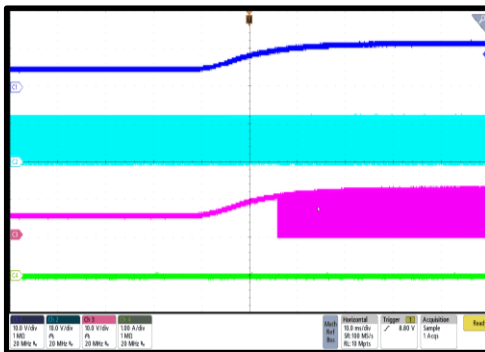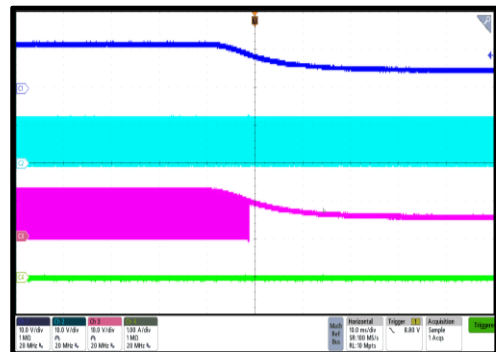V$_{OUT}$ = 5V to 12V, I$_{OUT}$ = 1A

CH1: V$_{OUT}$
10V/div.

CH2: SW1
10V/div.

CH3: SW2
5V/div.

CH4: I$_{OUT}$
1A/div.

I²C VID
V$_{OUT}$ =12V to 5V, I$_{OUT}$ = 1A

CH1: V$_{OUT}$
10V/div.

CH2: SW1
10V/div.

CH3:SW2
5V/div.
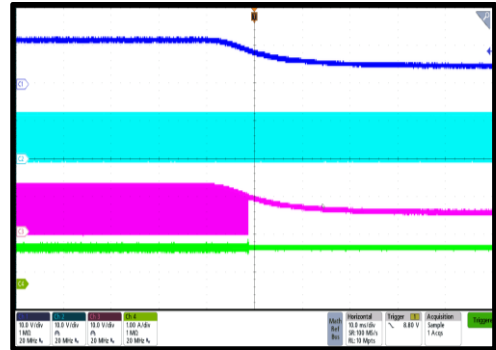
CH4:I$_{OUT}$
1A/div.

Load Transient Response
V$_{IN}$ = 12V, V$_{OUT}$ = 5V, no line drop compensation, 0A to 0.5A, 150mA/µs

CH1: V$_{OUT/AC}$
100mV/div.

CH4:I$_{OUT}$
1A/div.

Load Transient Response
V$_{IN}$ = 12V, V$_{OUT}$ = 5V, no line drop compensation, 0.5A to 1A, 150mA/µs

CH1: V$_{OUT/AC}$
100mV/div.
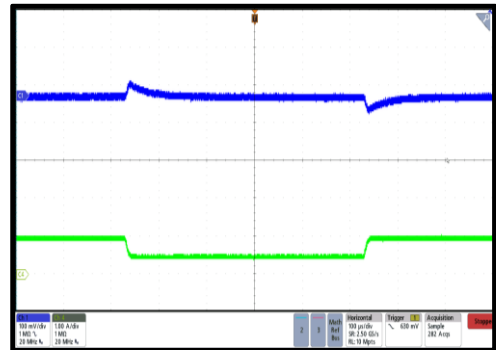
CH4:I$_{OUT}$
1A/div.

Short-Circuit Protection Entry with Latch-Off Mode

CH1: V$_{OUT}$
5V/div.

CH2: SW1
10V/div.

CH3: SW2
5V/div.
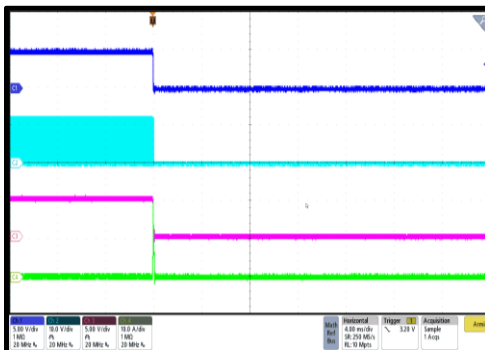
CH4: I$_{OUT}$
1A/div.

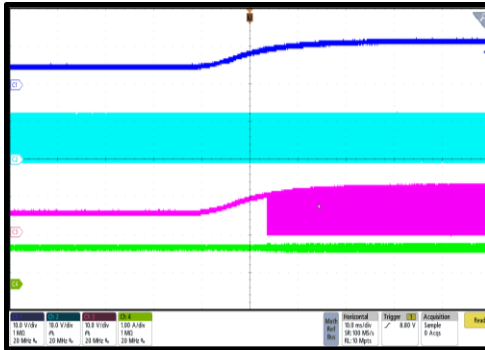**Short-Circuit Protection Entry with Hiccup Mode**
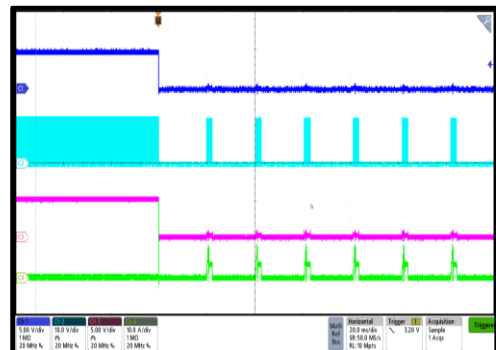
CH1: V$_{OUT}$
5V/div.

CH2: SW1
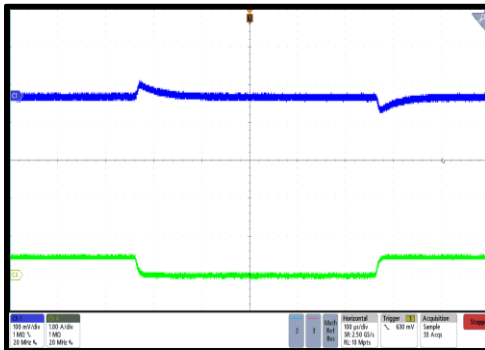10V/div.

CH3: SW2
5V/div.

CH4: I$_{OUT}$
1A/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V$_{IN}$ = 12V, V$_{OUT}$ = 5V, FCCM,   f$_{SW}$ = 500kHz, T$_A$ = 25°C, unless otherwise noted.

Short-Circuit Protection Recovery with Hiccup Mode

CH1: V$_{OUT}$
5V/div.
CH2: SW1
10V/div.
CH3: SW2
5V/div.
CH4: I$_{OUT}$
10A/div.
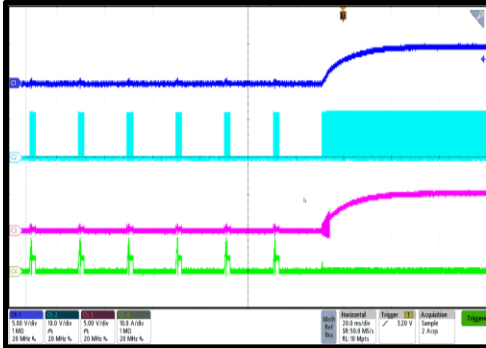
V$_{OUT}$ OVP with Hiccup Mode

CH1: V$_{OUT}$
5V/div.
CH2: SW1
10V/div.
CH3: SW2
5V/div.
CH4: I$_{OUT}$
1A/div.
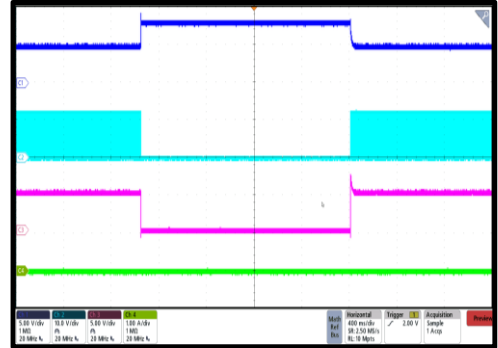
V$_{OUT}$ OVP with Latch-Off Mode

CH1: V$_{OUT}$
5V/div.
CH2: SW1
10V/div.
CH3: SW2
5V/div.
CH4: I$_{OUT}$
1A/div.
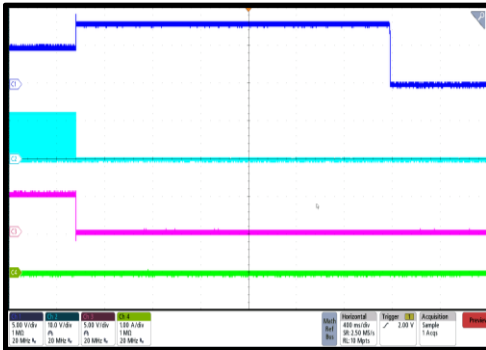
FUNCTIONAL BLOCK DIAGRAM
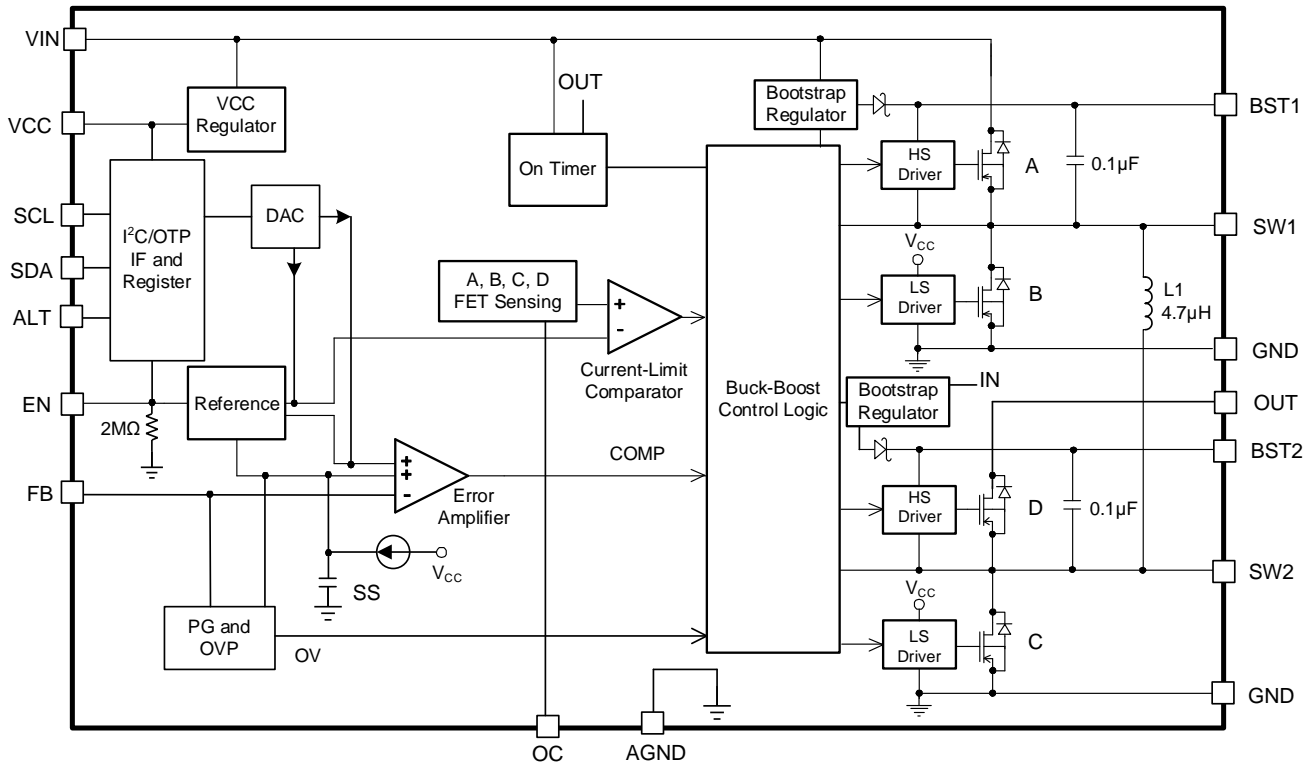
Figure 1: Functional Block Diagram

OPERATION

The MPM4730 is a four-switch, integrated inductor buck-boost module that can work in constant-on-time (COT) control mode with a fixed frequency. This provides fast transient response for the buck, boost, and buck-boost modes. A special buck-boost control strategy provides high efficiency across the full input range and smooth transients between different modes.

Buck-Boost Operation

The MPM4730 can regulate the output voltage (V$_{OUT}$) to be above, equal to, or below the input voltage (V$_{IN}$). Figure 2 shows a power structure with one inductor and the four switches.
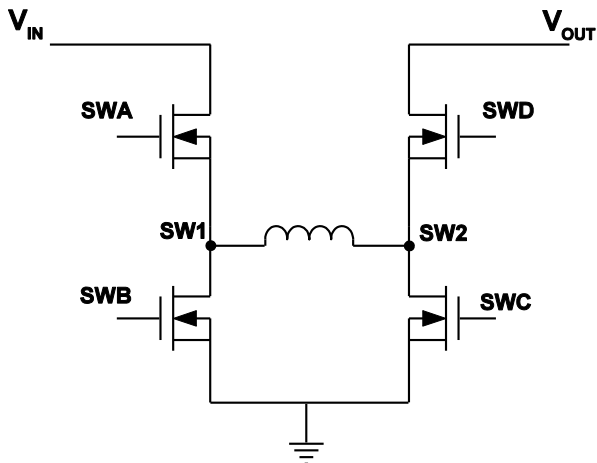
Figure 2: Buck-Boost Topology

The MPM4730 can operate in buck mode, boost mode, or buck-boost mode with different V$_{IN}$ inputs (see Figure 3).
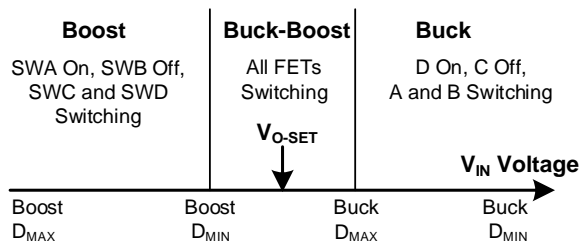

Figure 3: Buck-Boost Operation Range

Buck Mode

When V$_{IN}$ is significantly higher than V$_{OUT}$, the MPM4730 works in buck mode. In buck mode, SWA and SWB switch for buck regulation. SWC is off, and SWD remains on to conduct the inductor current (I$_L$).

SWA works with COT control logic, and SWB turns on as a complement of SWA. In each cycle, SWB turns on to conduct the inductor current.

When I$_L$ drops to the COMP voltage (V$_{COMP}$), SWB turns off and SWA turns on. SWA turns on for a fixed on time before turning off. Then SWB turns on again, and the operation repeats. The COMP signal is the error amplifier's (EA) output from the V$_{OUT}$ feedback and internal FB reference voltage (see Figure 4).
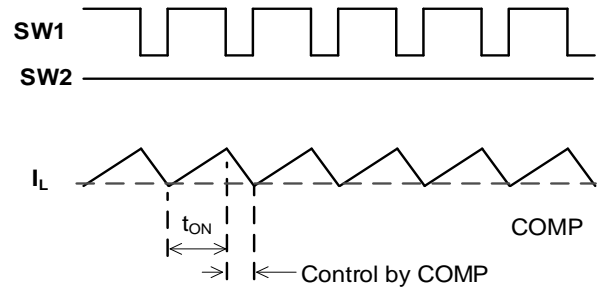
Figure 4: Buck Waveform

Boost Mode

When V$_{IN}$ is significantly lower than V$_{OUT}$, the MPM4730 works in boost mode. In boost mode, SWC and SWD switch for boost regulation. SWB is off, and SWA remains on to conduct I$_L$.

During each period, SWC remains off with COT control, while SWD turns on as a complement of SWC to boost I$_L$ to the output. In each cycle, SWC turns on to conduct I$_L$. When I$_L$ rises and reaches V$_{COMP}$, SWC turns off and SWD turns on. SWC turns off with a fixed off time before turning on again. During this period, SWD turns on for the current freewheel (see Figure 5).
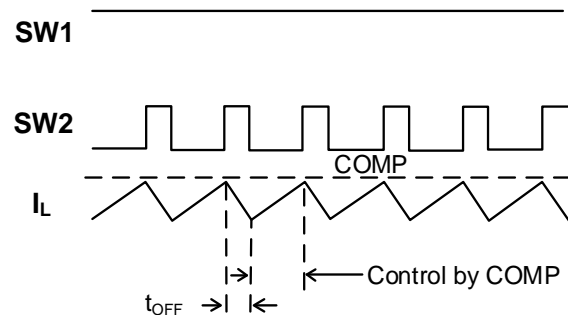
Figure 5: Boost Waveform

Buck-Boost Mode

When V$_{IN}$ is almost equal to V$_{OUT}$, the MPM4730 cannot provide enough energy to operate in buck mode due to SWA's minimum off time, or it supplies too much power to V$_{OUT}$ in boost mode due to SWC's minimum on time. The IC uses buck-boost control to regulate V$_{OUT}$ under these conditions.

If V$_{IN}$ drops and the SWA off period is close to the minimum buck off time in buck mode, buck-boost mode is engaged. When the next cycle starts after the SWA and SWD on time (the buck high-side MOSFET (HS-FET) on period), boost mode starts with SWA and SWC on (boost low-side MOSFET (LS-FET) on).

SWA and SWD turn on again for the resting period in boost mode (boost HS-FET is on). After the boost period elapses, the buck period starts, and SWB and SWD remain on until I$_L$ drops to V$_{COMP}$. Then SWA and SWD turn on until the next boost period begins. Buck and boost switching operate within a one-interval period. This is called buck-boost mode.

If V$_{IN}$ rises, and the SWC on period is close to the boost minimum on time in boost mode, buck-boost mode is enabled. After the boost constant-off-time period (SWA and SWD on), SWB and SWD remain on until the I$_L$ signal drops to V$_{COMP}$, just like a buck off-time period control.

After the I$_L$ signal triggers V$_{COMP}$, SWA and SWD turn on for the buck on time, which is followed by boost switching (SWA and SWC on). Buck and boost switching operate within a one-interval period. Figure 6 shows the buck-boost waveform when V$_{IN}$ exceeds V$_{OUT}$.
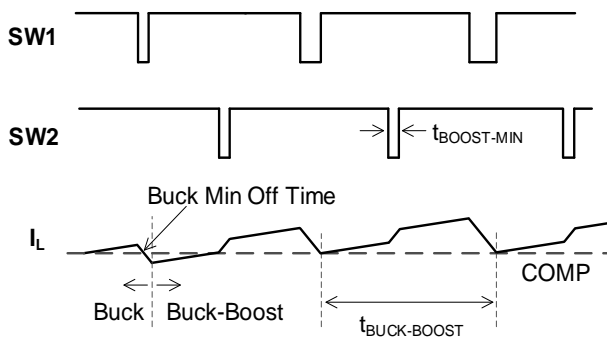
Figure 6: Buck to Buck-Boost Transient

Figure 7 shows the buck-boost waveform when V$_{OUT}$ exceeds V$_{IN}$.

If V$_{IN}$ exceeds 130% of V$_{OUT}$ in buck-boost mode, the MPM4730 switches from buck-boost mode to buck mode. If V$_{IN}$ drops below 20% of V$_{OUT}$, the MPM4730 switches from buck-boost mode to boost mode.
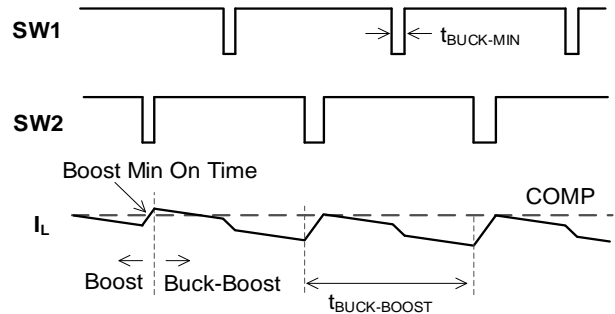
Figure 7: Buck-Boost Waveform

Working Mode Selection

The MPM4730 works with a fixed frequency under heavy-load conditions. When the load current decreases, the MPM4730 can work in forced continuous conduction mode (FCCM) or pulse-skip mode (PSM) based on the MODE register setting.

Forced Continuous Conduction Mode (FCCM) or Forced Pulse-Width Modulation (PWM) Mode

In FCCM, the buck on time and boost off time are determined by the internal circuit. This achieves a fixed frequency based on the V$_{IN}$ / V$_{OUT}$ ratio. When the load decreases, the average input current drops, and I$_L$ may go negative from V$_{OUT}$ to V$_{IN}$ during the off time (SWD on). This forces the inductor current to work in continuous conduction mode (CCM) with a fixed frequency, producing a lower V$_{OUT}$ ripple than in PSM mode.

Pulse-Skip Mode (PSM) and Automotive Pulse-Frequency Modulation (PFM)/PWM Mode

If I$_L$ drops to 0A in PSM, SWD turns off to prevent the current from flowing from V$_{OUT}$ to V$_{IN}$, forcing I$_L$ to work in discontinuous conduction mode (DCM). Meanwhile, the internal off time clock stretches once the MPM4730 enters DCM. The switching frequency drops when the inductor current conduction period decreases, which helps save power loss and reduce the V$_{OUT}$ ripple.

If V$_{COMP}$ drops to the PSM threshold (even if the IC decreases the frequency), the MPM4730 stops switching to further decrease the switching power loss.

The MPM4730 recovers switching once V$_{COMP}$ exceeds the PSM threshold. The switching pulse skips based on V$_{COMP}$ under very light-load conditions. PSM has a much higher efficiency than FCCM under light loads, but the V$_{OUT}$ ripple may be higher due to the group switching pulse.

Internal VCC Regulator

The 3.65V internal regulator powers most of the internal circuitries. This regulator takes VIN and operates across the full V$_{IN}$ range. When V$_{IN}$ exceeds 3.65V, the output of the regulator is in full regulation. If V$_{IN}$ drops below 3.65V, the output decreases with V$_{IN}$. VCC requires an external 1µF ceramic capacitor for decoupling.

Enable (EN) Control

The MPM4730 has an enable (EN) control pin. Pull EN high to enable the IC. Pull EN low or float EN to disable the IC.

If EN is pulled down when the output discharge function is enabled, the MPM4730 shuts down after 55ms. The MPM4730's I^{2}C register value is reset to its default only after the MPM4730 experiences this type of shutdown. If EN is pulled high within 55ms, the I^{2}C register is not reset, and the MPM4730 enables the output with the previous register setting.

If the output discharge function is disabled, the MPM4730 shuts down once EN is pulled down for more than 100µs, and the MPM4730 I^{2}C register is reset after a 100µs delay (see Figure 8).
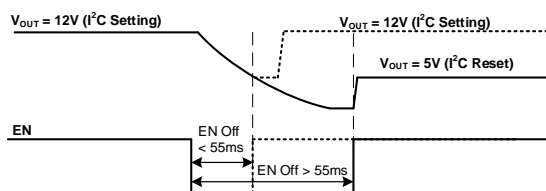
Figure 8: EN On/Off Logic for I^{2}C Register Reset

If EN is pulled high, there is a delay time (t$_{DELAY}$) before V$_{OUT}$ reaches 90% of V$_{REF}$ (see Figure 9).
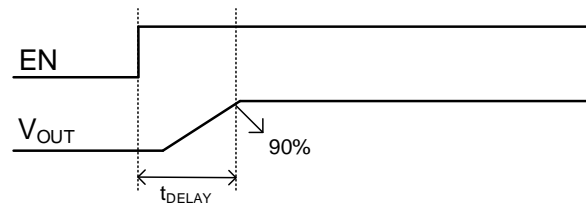
Figure 9: EN On to V$_{OUT}$ > 90% Delay

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors V$_{IN}$ and enables or disables the entire IC.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates an SS voltage that ramps up from 0V to 3.65V. If the SS voltage (V$_{SS}$) is below V$_{REF}$, the error amplifier uses V$_{SS}$ as the reference. If V$_{SS}$ exceeds V$_{REF}$, the error amplifier uses V$_{REF}$ as the reference.

If the MPM4730's output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the internal SS capacitor exceeds the internal V$_{FB}$.

Over-Current Protection (OCP)

The MPM4730 has a constant-current limit control loop to limit the output average current. The current information is sensed from switches A, B, C, and D. Then an average algorithm calculates the output current.

When the output current exceeds the current-limit threshold, V$_{OUT}$ starts to drop.

There are two conditions that activate this condition:

1. V$_{OUT}$ exceeds 3V, V$_{FB}$ drops below 50% of V$_{REF}$, and V$_{OUT}$ drops below 3V. The MPM4730 then enters hiccup mode or latch-off mode according to the I^{2}C setting.

2. V$_{OUT}$ is set below or equal to 3V, and V$_{OUT}$ drops below the under-voltage (UV) threshold (typically 50% below V$_{REF}$). The MPM4730 then enters hiccup mode or latch-off mode according to the I^{2}C setting.

In hiccup mode, the MPM4730 stops switching and recovers automatically with a 12.5% duty

cycle. In latch-off mode, the MPM4730 stops switching until the IC restarts (power cycling on VIN or EN, or EN bit toggling).

Over-Voltage Protection (OVP)

The MPM4730 monitors a resistor-divided V$_{FB}$ to detect output over-voltage (OV) conditions. When the feedback voltage exceeds 160% of the target voltage, the over-voltage protection (OVP) comparator output goes high. The OUT-to-ground discharge resistor turns on.

The OUT pin has an absolute OVP function. Once V$_{OUT}$ exceeds the absolute OVP threshold (23V), the MPM4730 stops switching and turns on the OUT-to-ground discharge resistor.

Start-Up and Shutdown

If both VIN and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN going low, V$_{IN}$ going low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid fault triggers. Then V$_{COMP}$ and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Output Discharge

The MPM4730 has an output discharge function that provides a resistive discharge path for the external output capacitor. The function is active when the part is disabled (input voltage is under UVLO or enable off), the discharge path is turned off when V$_{OUT}$ < 50mV or waits for the 50ms maximum timer to pass. This function can also be disabled via the I²C.

Thermal Warning (TSW) and Thermal Shutdown (TSD)

Thermal warning and thermal shutdown prevent the part from operating at exceedingly high temperatures. When the silicon die temperature exceeds 120°C, the MPM4730 sets the OTW bit (STATUS (09h), bit [D5]) to 1. When the temperature falls below its lower threshold (typically 100°C), the OTW bit is set to 0.

When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled. This is a non-latch protection.

I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence.

The MPM4730 interface is an I²C slave that supports fast mode (400kHz) and high-speed mode (3.4MHz). The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled instantaneously via the I²C interface.

When the master sends the address as an 8-bit value, the 7-bit address should be followed by a 0 to indicate a write operation, or 1 to indicate a read operation.

Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and end of an I²C transfer. The start (S) command is defined as the SDA signal transitioning from high to low while the SCL is high.

The stop (P) command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 10). The master then generates the SCL clocks and transmits the device address and the read/write (R/W) direction bit on the SDA line.

Transfer Data

Data is transferred in 8-bit bytes by an SDA line. Each byte of data should be followed by an acknowledge (ACK) bit.

I²C Update Sequence

The MPM4730 requires a start command, a valid I²C address, a register address byte, and a data byte for a single data update. The MPM4730 acknowledges that it has received each byte by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPM4730. The MPM4730 performs an update on the falling edge of the least significant bit (LSB) byte. Figure 11 on page 20, and Figure 12, Figure 13 on page 21 show examples of I²C write and read sequences.

I²C Start-Up Timing

I²C functionality is enabled once EN is active and V$_{IN}$ exceeds its UVLO threshold. The I²C works during OCP, OVP, and thermal shutdown.
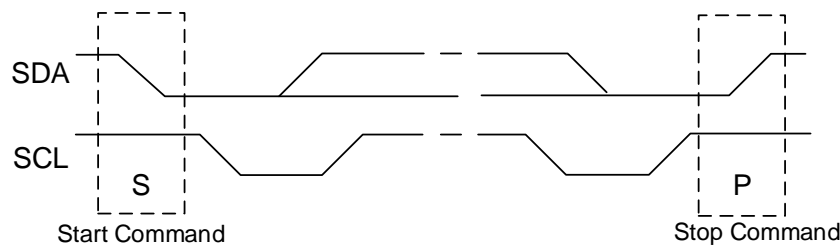
Figure 10: Start and Stop Commands

Figure 11: I²C Write Example (Write Single Register)

8 Bits				8 Bits		8 Bits							
S	Slave Address	WR	A	Register Address K	A	Write Data K	A	Write Data K + 1	A	•••	Write Data K + N	A	P

Multi-byte write executed from current register location (the read-only register is skipped)

☐ Master to Slave   A = Acknowledge (SDA = Low)   S = Start Command   WR Write = 0

☐ Slave to Master   NA = Not Acknowledge (SDA = High)   P = Stop Command   RD Read = 1

Figure 12: I²C Write Example (Write Multi-Register)

8 Bits				8 Bits			8 Bits			8 Bits		
S	Slave Address	WR	A	Register Address K	A	Sr	Slave Address	RD	A	Read Data K	NA	P

Register address to read specified   Read register data from current register location

☐ Master to Slave   A = Acknowledge (SDA = Low)   S = Start Command   Sr = Repeat Start Command   WR Write = 0

☐ Slave to Master   NA = Not Acknowledge (SDA = High)   P = Stop Command   RD Read = 1

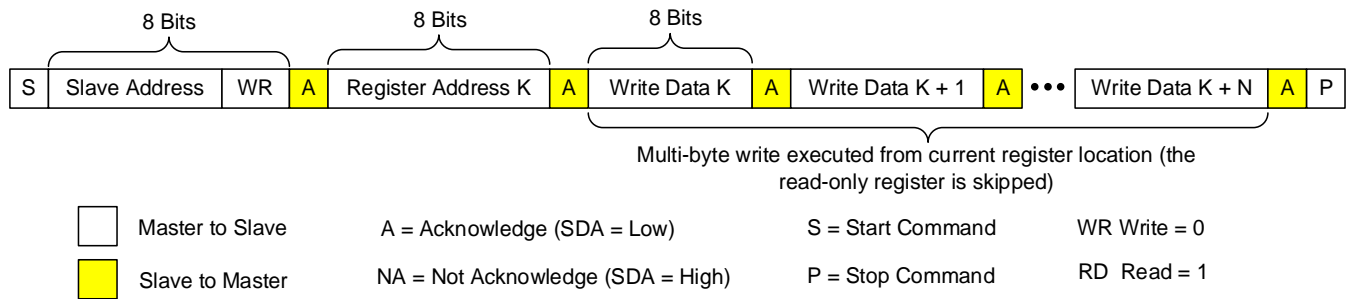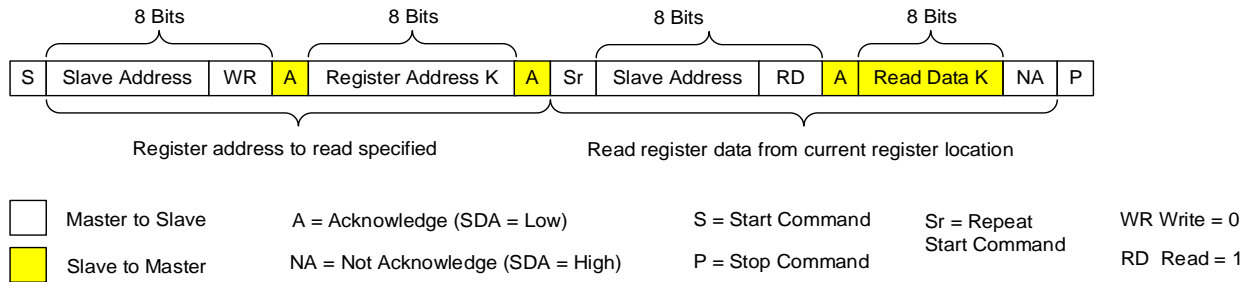**Figure 13: I²C Read Example (Read Single Register)**

I²C REGISTER MAP

Add (Hex)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VREF_L	R/W	RESERVED						VREF DATA BIT LOW [2:0] [9]	
01	VREF_H	R/W	VREF DATA BIT HIGH [10:3] [9]							
02	VREF_GO	R/W	RESERVED						PG_DELAY_EN [9]	GO_BIT
03	IOUT_LIM	R/W	RESERVED	RESERVED						
04	CTL1	R/W	EN [9]	HICCUP OCP_OVP [9]	DISCHG_EN [9]	MODE [9]	FREQ [9]		RESERVED	
05	CTL2	R/W	RESERVED		SS [9]		RESERVED			
06	RESERVED	R	RESERVED, all "0"						RESERVED	
07	RESERVED	R	RESERVED							
08	RESERVED	R	RESERVED							
09	STATUS	R	PG	OTP	OTW	CC_CV	RESERVED			
0A	INTERRUPT	W1C	OTEMPP_ENTER	OT WARNING_ENTER	OC_ENTER	OC_RECOVER	UVP_FALLING	OTEMPP_EXIT	OT WARNING_EXIT	PG_RISING
0B	MASK	R/W	RESERVED			OTPMSK [9]	OTWMSK [9]	OC_MSK [9]	UVP_MSK [9]	PG_MSK [9]
0C	ID1	R	OTP configuration code. "0x00" means the default MPM4730.							
27	MFR_ID	R	Manufacturer ID: b '0000 1001'							
28	DEV_ID	R	Device ID: b '0101 1000'							
29	IC_REV	R	IC revision: b '0000 0001'							

Note:

9) These items have one-time programmable (OTP) non-volatile memory (NVM). The OTP is reloaded to the I²C register when V$_{IN}$ exceeds the under-voltage lockout (UVLO) threshold, or during EN shutdown.

REGISTER DESCRIPTION

I²C Bus Slave Address

The MPM4730 I²C slave address is fixed to 60h.

VREF_H (00h) and VRE_L (01h) (Output Reference Voltage Setting)

The VREF_L and VREF_H registers set the reference voltage (V$_{REF}$) and follow the 11-bit direct format.

Name	VREF														
Format	Direct, unsigned binary integer														
Register Name	N/A					VREF_H D[7:0]								VREF_L D[2:0]		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	N/A					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	N/A					Data Bit High								Data Bit Low		
Default Value (1000mV)	N/A					1250 Integer										

V$_{REF}$ can be calculated with Equation (1):

$$V_{REF}(mV) = V \times 0.8 \qquad (1)$$

Where V is an 11-bit unsigned binary integer from VREF[10:0] that ranges between 0 and 2047. The V$_{REF}$ resolution is 0.8mV/LSB. The V$_{REF}$ changing slew rate is fixed at 1mV/μs. See the GO_BIT section below to change the reference voltage.

VREF_GO (02h)

Format: Unsigned binary

The VREF_GO command sets the control instruction of V$_{REF}$ beings to change and PG_DELAY_EN

Bits	Access	Bit Name	Default	Description
D [7:2]	N/A	RESERVED	N/A	Reserved.
D [1]	R/W	PG_DELAY_EN	1b'0	Enables PG delay. 1: Enables. PG experiences a 100μs rising delay 0: Disabled. There is no PG delay
D [0]	R/W	GO_BIT	1b'0	Controls whether the output reference changes. The MPM4730 can be controlled when V$_{REF}$ begins to change. Set GO_BIT to 1 to start the output reference change based on the VREF register. When the V$_{REF}$ change is complete (internal V$_{REF}$ reaches its target value), GO_BIT auto-resets to 0. This prevents a false operation of V$_{REF}$ scaling. Write to the reference voltage (0x00 and 0x01 registers) first, and then set GO_BIT = 1. V$_{REF}$ changes based on the new register setting. GO_BIT resets to 0 when V$_{REF}$ reaches a new value. The host can read GO_BIT to determine whether V$_{REF}$ scaling has completed. The VOUT-to-ground discharge function is enabled when GO_BIT = 1. This can ramp V$_{OUT}$ from high to low under light-load conditions. 1: Enabled. V$_{REF}$ begins to change based on the VREF register setting. After V$_{REF}$ scaling finishes, GO_BIT is automatically reset to 0. 0: Disabled. V$_{REF}$ does not change

CTL1 (04h)

Format: Unsigned binary

The CTL1 command sets the EN function, the over-current protection (OCP) and over-voltage protection (OVP) modes, the output discharge function, the pulse-frequency modulation (PFM)/pulse-width modulation (PWM) mode, and the switching frequency.

Bits	Access	Bit Name	Default	Description
D [7]	R/W	EN	1b'1	Turns the part on and off. When the external EN pin is low, the converter is off, and the I²C shuts down. When EN is high, the EN bit takes over. 1: Enable the part 0: Disable the part
D [6]	R/W	HICCUP_OCP_OVP	1b'1	Selects the mode for OCP and OV). 1: Hiccup mode 0: Latch-off mode
D [5]	R/W	DISCHG_EN	1b'1	Enables the output discharge function. 1: Output discharge occurs during EN or VIN shutdown 0: No output discharge occurs during shutdown
D [4]	R/W	MODE	1b'1	Enables PFM/PWM mode. The default is PWM mode under light-load conditions. 0: Enables auto-PFM/PWM mode 1: Sets forced PWM mode
D [3:2]	R/W	FREQ	2b'00	Sets the switching frequency. 00: 500kHz 01: 750kHz 10: Reserved 11: Reserved
D [1:0]	N/A	RESERVED	N/A	Reserved.

CTL2 (05h)

Format: Unsigned binary

The CTL2 command sets the soft-start time.

Bits	Access	Bit Name	Default	Description
D [7:6]	N/A	RESERVED	N/A	Reserved.
D [5:4]	R/W	SS	2b'10	Sets the output start-up soft-start timer (from 0% to 100% of V$_{REF}$) if the reference voltage is 1V. 00: 1.1ms 01: 2.2ms 10: 3.5ms 11: 4.4ms The SS slew rate is constant, but SS time changes with different V$_{REF}$ values. For example, the SS time = 3.5ms for a 1V V$_{REF}$, and the SS time = 5.25ms for a 1.5V V$_{REF}$.
D [3:0]	N/A	RESERVED	N/A	Reserved.

STATUS (09h)

Format: Direct

The STATUS command monitors the power good (PG), over-temperature protection (OTP), and over-temperature warning (OTW) statuses. It also enables constant-current (CC) or constant-voltage (CV) mode. These status bits indicate instantaneous values.

Bits	Access	Bit Name	Default	Description
D [7]	R	PG	N/A	Indicates the output PG status. 0: Output power is not good 1: Output power is good
D [6]	R	OTP	N/A	Indicates whether OTP has occurred. 0: OTP has not occurred 1: OTP has occurred
D [5]	R	OTW	N/A	Indicates whether OTW has occurred. 0: OTW has not occurred 1: OTW has occurred
D [4]	R	CC_CV	N/A	Enables CC output mode or CV output mode. 0: CV mode 1: CC mode
D [3:0]	N/A	RESERVED	N/A	Reserved.

INTERRUPT (0Ah)

Format: Direct

The INTERRUPT command monitors the statuses of OTEMPP_ENTER, OTWARNING_ENTER, OC_ENTER, OC_RECOVER, UVP_FALLING, OTEMPP_EXIT, OTWARNING_EXIT, and PG_RISING.

Each bit in this command is latched once triggered. Write 0xFF to this register to reset the interrupt and the ALT pin's state.

Bits	Access	Bit Name	Description
D [7]	W1C	OTEMPP_ ENTER	Indicates when the device enters over-temperature protection (OTP). When this bit is high, the IC enters thermal shutdown. This bit is not masked, even if OTPMSK = 1. Setting OTPMSK to 1 only masks the interrupt pin's output (ALT).
D [6]	W1C	OTWARNING_ ENTER	Indicates when the device enters the die temperature early warning condition. When this bit is high, the die temperature exceeds 120°C. This bit is not masked, even if OTWMSK = 1. Setting OTWMSK to 1 only masks the interrupt pin's output (ALT).
D [5]	W1C	OC_ENTER	Indicates when the device enters over-current (OC) or constant-current (CC) current-limit mode. THE OC_MSK bit can enable or disable the OC_ENTER and OC_RECOVER ALERT outputs.
D [4]	W1C	OC_RECOVER	Indicates when the device recovers from constant-current (CC) current-limit mode. If the device recovers from a hiccup, it does not trigger this interrupt signal.
D [3]	W1C	UVP_FALLING	Indicates when the reference voltage is within its under-voltage protection (UVP) threshold.
D [2]	W1C	OTEMPP_EXIT	Indicates when OTP ends. OTPMSK can mask off the ALT signals of this bit.

| D [1] | W1C | OTWARNING_EXIT | Indicates when the device exits the die temperature early warning condition. When the die temperature is below 100°C, this bit is set to 1. This bit is not masked, even if OTWMSK = 1. Setting OTWMSK to 1 only masks the interrupt pin's output (ALT). |
| D [0] | W1C | PG_RISING | Output power good rising edge. |

MSK (0Bh)

Format: Unsigned binary

The MSK command masks over-temperature protection (OTP), over-temperature warning (OTW), over-current (OC), under-voltage protection UVP, and power good (PG).

Bits	Access	Bit Name	Default	Description
D [7:5]	N/A	RESERVED	N/A	Reserved.
D [4]	R/W	OTPMSK	1b'0	Set OTPMSK to 1 to mask]the over-temperature protection (OTP) alert. Setting OTPMSK to 1 only masks the interrupt pin's output (ALT). This is not the interrupt register, but it is similar for other mask bits.
D [3]	R/W	OTWMSK	1b'0	Masks the OTW.
D [2]	R/W	OC_MSK	1b'0	Masks both over-current (OC) and constant current (CC) entry and recovery.
D [1]	R/W	UVP_MSK	1b'0	Masks the output under-voltage protection (UVP) interrupt.
D [0]	R/W	PG_MSK	1b'0	Masks the PG indication function on ALT. 1: The ALT pin does not indicate a PG event 0: The ALT indicates a PG rising event

Figure 14 shows the ALT pin's behavior during OTP, OTW, and OC recovery.
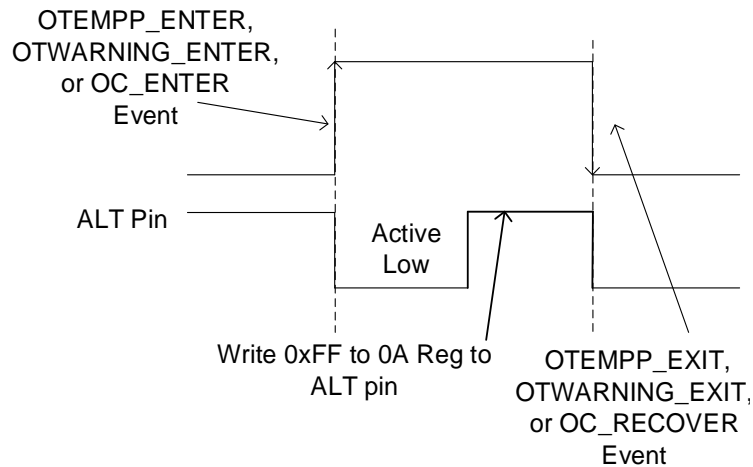

Figure 14: ALT Behavior during OTP, OTW, and OC Recovery

APPLICATION INFORMATION

Setting the Output Voltage (V$_{OUT}$)

The external resistor divider sets V$_{OUT}$. R1 can be calculated with Equation (1):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \qquad (1)$$
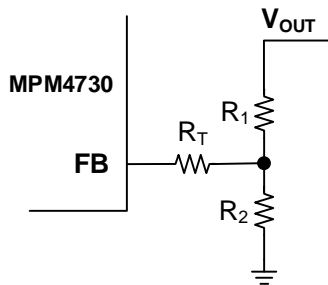
Figure 11 shows the feedback circuit.

Figure 15: Feedback Network

Table 1 lists the recommended resistors and inductor values for common output voltages. If the I²C is not used to set V$_{OUT}$, then set V$_{OUT}$ using the resistors below.

Table 1: Resistor Selection for Common Output Voltages

V$_{OUT}$ (V)	R1 (kΩ)	R2 (kΩ)	R$_T$ (kΩ)
5	43	10.7	49.9
9	40.2	4.99	49.9
12	43	3.9	49.9
15	42.2	3	49.9
20	42.2	2.2	49.9

Selecting the Input and Output Capacitors

It is recommended to use ceramic capacitors with an electrolytic capacitor at the input to filter the input ripple current and achieve stable operation.

Since the input capacitor (C$_{IN}$) absorbs the input switching current, it requires sufficient capacitance. For most applications, a 100µF electrolytic capacitor and a 22µF ceramic capacitor are sufficient.

The output capacitor (C$_{OUT}$) stabilizes the DC output voltage. A sufficient capacitor value is recommended to limit the output voltage ripple. The minimum ceramic C$_{OUT}$ should be 22µF x 5.

The input and output ceramic capacitors must be placed as close the device as possible.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best performance, refer to Figure 16 and Figure 17, and follow the guidelines below:

1. Place the input MLCC capacitors as close to the VIN and PGND pins as possible.

2. Place all signal traces far away from SW.

3. Maximize the VIN and PGND copper plane to minimize parasitic impedance.

4. Ensure that the high-current paths (PGND, VIN, and VOUT) have short, direct, and wide traces.

5. Place as many PGND vias as possible close to PGND to minimize parasitic impedance and thermal resistance.

6. Place the external feedback resistors and R$_T$ next to FB.
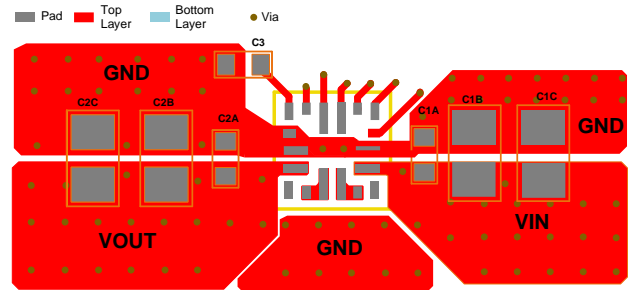
7. Route the feedback network away from the switching node.
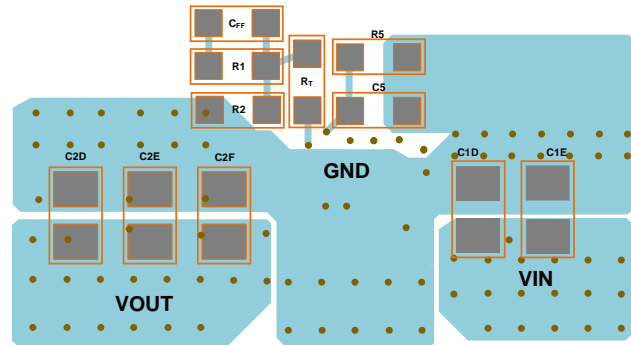

Figure 16: Recommended PCB Layout (Top)

Figure 17: Recommended PCB Layout (Bottom)
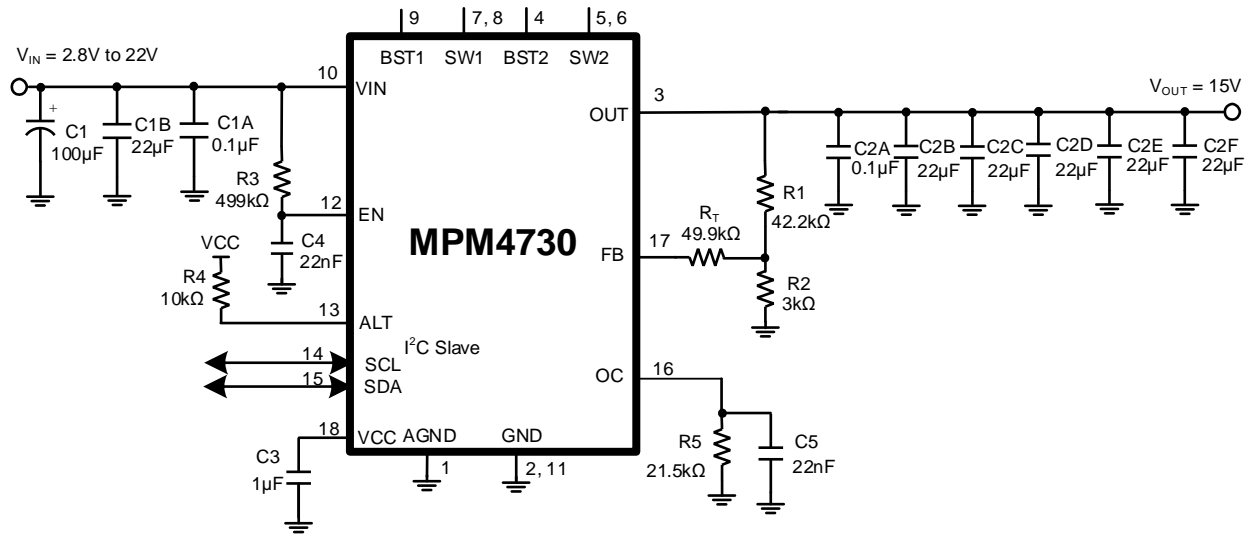
TYPICAL APPLICATION CIRCUIT

Figure 18: Typical Application Circuit (V_OUT = 15V)

DEFAULT OTP CONFIGURATION
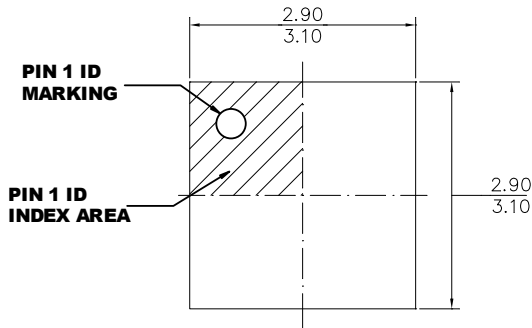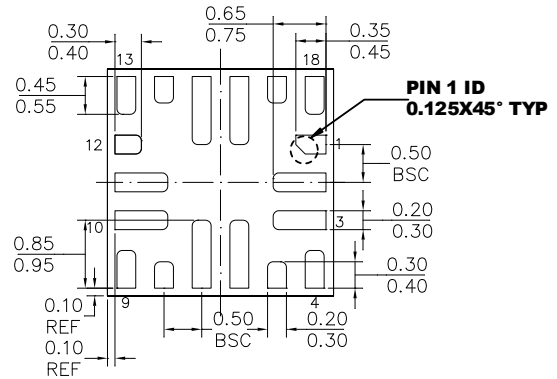
Table 2: 0000 Suffix Code Configuration

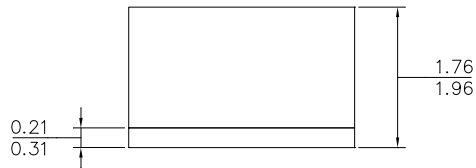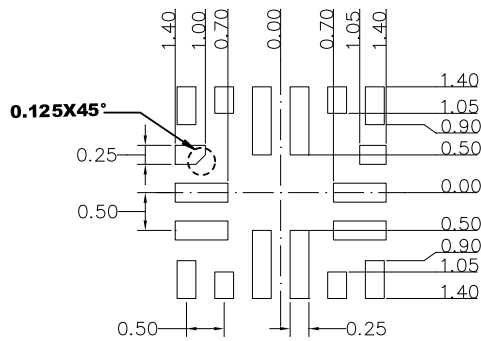| OTP Items	Default
Output Voltage	15V
Reference Voltage	1V
Initial On/Off	On
Mode	FCCM
Soft-Start Time	3.5ms
Output Discharge EN	Enabled
OCP/OVP Mode	Hiccup mode
Switching Frequency	500kHz
PG Delay EN	Disabled
OTP Mask	Off
OTW Mask	Off
OC Mask	Off
UVP Mask	Off
PG Mask	Off
Software Initial I^{2}C Slave Address	0x60

Table 3: 0000 Suffix Register Value

Register	Hex Value
0x00	02h
0x01	9Ch
0x02	00h
0x04	F0h
0x05	20h
0x09	80h
0x0A	01h
0x0B	00h
0x0C	00h
0x27	09h
0x28	58h
0x29	01h

PACKAGE INFORMATION

ECLGA-18 (3mmx3mm)

PIN 1 ID
MARKING

PIN 1 ID
INDEX AREA

$\frac{2.90}{3.10}$

$\frac{2.90}{3.10}$

TOP VIEW

$\frac{0.30}{0.40}$

$\frac{0.65}{0.75}$

$\frac{0.35}{0.45}$

$\frac{0.45}{0.55}$

PIN 1 ID
0.125X45° TYP

0.50
BSC

$\frac{0.20}{0.30}$

$\frac{0.85}{0.95}$

$\frac{0.30}{0.40}$

$\frac{0.10}{REF}$

$\frac{0.50}{BSC}$

$\frac{0.20}{0.30}$

0.10
REF

BOTTOM VIEW

$\frac{1.76}{1.96}$

$\frac{0.21}{0.31}$

SIDE VIEW

1.40
1.00
0.70
0.00
0.70
1.05
1.40

0.125X45°

0.25

0.50

1.40
1.05
0.90
0.50
0.00
0.50
0.90
1.05
1.40

0.50   0.25

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION

Pin1 →

Feed Direction
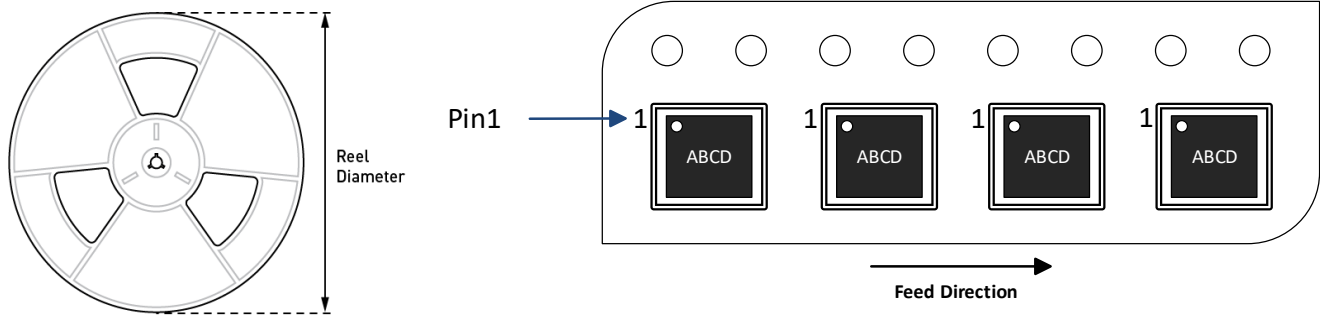
Part Number	Package Description	Quantity/Reel	Quantity/Tube	Quantity/Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM4730GPQ-Z	ECLGA (3mmx3mmx 1.86mm)	2500	N/A	N/A	13in	12mm	8mm
MPM4730GPQ-0000-Z	ECLGA (3mmx3mmx 1.86mm)	2500	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/11/2024	Initial Release	-