36V, 6A, Low Quiescent Current, Synchronous Step-Down Converter with Integrated Input Capacitors, AEC-Q100 Qualified

DESCRIPTION

The MPQ4326M is a configurable-frequency (200kHz to 2.5MHz), synchronous, step-down switching regulator with integrated internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). It features integrated input capacitors to optimize EMI performance, and can provide up to 6A of highly efficient output current (I_{OUT}) with peak current mode control.

The MPQ4326M can maintain a regulated output voltage (V_{OUT}) across a wide input voltage (V_{IN}) range up to 36V. Over-voltage protection (OVP) allows it to survive load dumps up to 42V. A 1µA shutdown mode quiescent current (I_Q) allows this device to be used in battery-powered applications. High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) at light loads to reduce switching and gate driver losses.

An open-drain power good (PG) signal indicates whether V_{OUT} is within 94.5% to 105.5% of its nominal voltage. Frequency foldback helps prevent inductor current (I_L) runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation. High duty cycle and low-dropout mode are provided for automotive cold-crank conditions.

The MPQ4326M is available in a QFN-14 (4mmx4mm) package, and is AEC-Q100 qualified.

FEATURES

- Designed for Automotive Applications
  - Survives 42V Load Dump
  - Operating Input Voltage (V_{IN}) Up to 36V
  - 6A Continuous Output Current (I_{OUT})
  - Low-Dropout Mode
  - 50ns Minimum On Time
  - -40°C to +150°C Operating Junction Temperature (T_J)
  - Available in AEC-Q100 Grade 1

FEATURES *(continued)*

- Increased Battery Life
  - 1µA Low Shutdown Supply Current
  - 24µA Sleep Mode Quiescent Current (I_Q), 28µA I_Q with Switching
  - Advanced Asynchronous Modulation (AAM) Mode Increases Efficiency under Light Loads
- High Performance for Improved Thermals
  - Internal 45mΩ HS-FET, 25mΩ LS-FET
- Optimized for EMC and EMI
  - Integrated Input Capacitors
  - 200kHz to 2.5MHz Configurable f_{SW}
  - Frequency Spread Spectrum Modulation
  - Symmetric VIN Pinout
  - CISPR25 Class 5 Compliant
  - MeshConnect™ Flip-Chip Package
- Additional Features
  - Fixed Output Options (1): 1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, 5V
  - Power Good (PG) Output
  - Synchronizable to an External Clock
  - Hiccup Over-Current Protection (OCP)
  - QFN-14 (4mmx4mm) Package with Wettable Flanks
- Functional Safety System Design Capable
  - MPSafe™ QM – Documentation Available

MPSafe™ QM

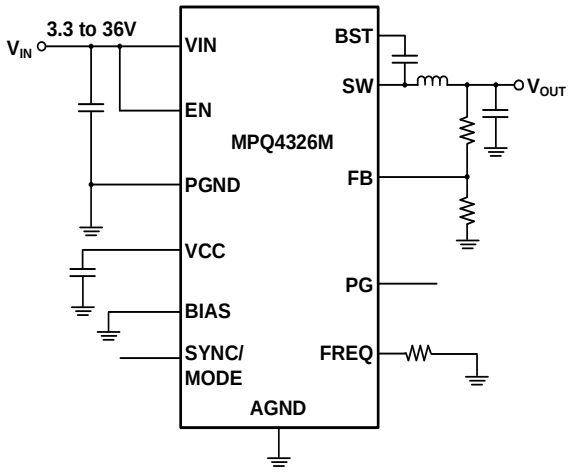
APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Advanced Driver-Assistance Systems (ADAS)
- Industrial Power Systems

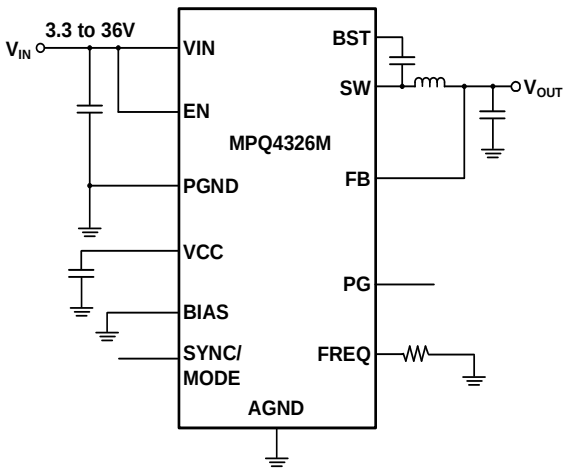
Note:

1) Refer to the Ordering Information section for availability for each fixed-output version. Additional output voltages may be available. Contact MPS for details.

TYPICAL APPLICATION



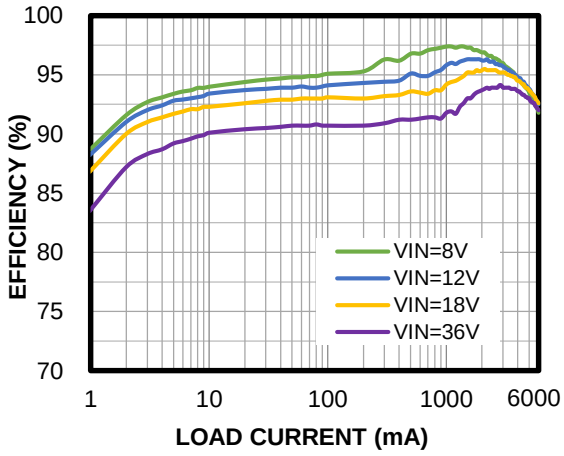
Adjustable-Output Version



Fixed-Output Version

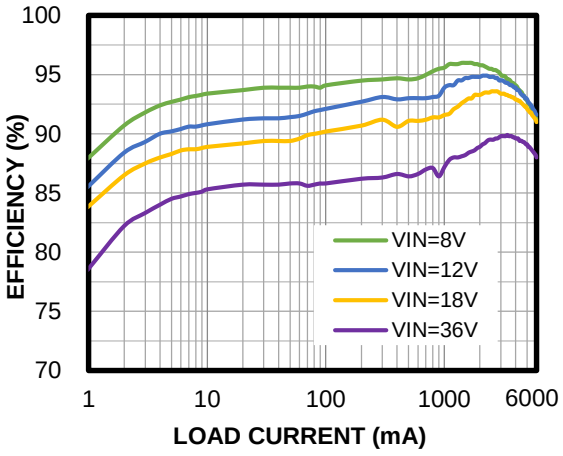
Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), AAM mode



Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), AAM mode



ORDERING INFORMATION

Part Number [2]*	Package	Top Marking	MSL Rating**
MPQ4326MGRE-AEC1***	QFN-14 (4mmx4mm)	*See Below*	Level 1

* For Tape & Reel, add suffix -Z (e.g. MPQ4326MGRE-AEC1-Z).

** Moisture Sensitivity Level Rating
*** Wettable flank

Note:

2) Contact MPS for details regarding fixed-output versions.

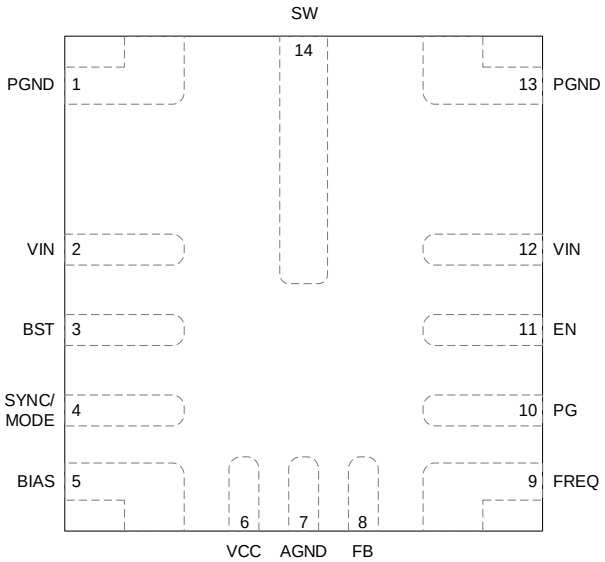
TOP MARKING

MPSYWW
M4326M
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
M4326M: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

TOP VIEW



QFN-14 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 13	PGND	**Power ground.**
2, 12	VIN	**Input supply.** The VIN pin supplies power to all of the internal control circuitry and the power MOSFET connected to SW. The two VIN pins are connected internally. Place decoupling capacitors connected to ground, close to each VIN pin to minimize the input voltage (V_{IN}) ripple and (ΔV_{IN}) switching spikes. For the MPQ4326M, two 0.1µF capacitors are integrated between the VIN and PGND pins inside the chip.
3	BST	**Bootstrap.** The BST pin is the positive power supply for the high-side MOSFET (HS-FET) driver connected to SW. Connect a bypass capacitor between BST and SW. See the Application Information section on page 37 to select the capacitance.
4	SYNC/MODE	**SYNC input and mode select pin.** Pull the SYNC/MODE pin below the specified threshold (0.4V) to select advanced asynchronous modulation (AAM) mode; pull it above the specified threshold (1.4V) to select forced continuous conduction mode (FCCM). Tie this pin to an external 200kHz to 2.5MHz clock source to synchronize the converter with the external clock and force it to operate in FCCM. This pin has one 100kΩ internal pull-down resistor. If this pin is left floating, the part will operate in AAM mode.
5	BIAS	**External bias.** Connect the BIAS to a 5V output voltage (V_{OUT}) supply for a lower quiescent current (I_Q). For the 5V output version, tie this pin directly to V_{OUT}. For other output versions, connect this pin to an external 5V source or ground. Ensure that V_{IN} is supplied before providing the external bias voltage. Do not float this pin.
6	VCC	**Internal bias supply.** The VCC pin is the internal regulator's output, and supplies power to the internal control circuit and gate drivers. VCC is typically 5V. Place a minimum 1µF decoupling capacitor connected to ground as close as possible to VCC.
7	AGND	**Analog ground.**
8	FB	**Feedback input.** For the fixed-output versions, connect this pin directly to V_{OUT}. For the adjustable-output version, connect this pin to the middle point of the external feedback divider between V_{OUT} and AGND to set V_{OUT}. The feedback voltage (V_{FB}) threshold is 0.8V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
9	FREQ	**Switching frequency setting.** Connect a resistor from this pin to ground to set the switching frequency (f_{SW}).
10	PG	**Power good output.** The PG pin's output is an open drain. If PG is used, it must be connected to a power source via a pull-up resistor. If V_{OUT} is within 94.5% to 105.5% of the nominal voltage, PG goes high; if V_{OUT} is above 107% or below 93% of the nominal voltage, PG goes low. Float this pin if it is not used.
11	EN	**Enable.** Pull the EN pin below the specified threshold (0.85V) to shut down the chip. Pull EN above the specified threshold (1.02V) to enable the chip. Do not float this pin.
14	SW	**Switch node.** The SW pin is the HS-FET source and the low-side MOSFET (LS-FET) drain.

ABSOLUTE MAXIMUM RATINGS (3)

VIN, EN…….....-0.3V to +40V
VIN, EN…..…...42V for automotive load dump (4)
SW…… -0.3V to $V_{IN(MAX)}$ + 0.3V
BST……..V_{SW} + 5.5V
FREQ……...……-0.3V to +5.5V
All other pins……-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (5) (9)
QFN-14 (4mmx4mm) ……..... 4.86W
Junction temperature (T_J)…….....+150°C
Lead temperature……....+260°C
Storage temperature……..-65°C to +150°C

ESD Ratings

Human body model (HBM) ..... Class 2 (6)
Charged-device model (CDM).....Class C2b (7)

Recommended Operating Conditions

Continuous supply voltage (V_{IN})…...3.3V to 36V
Output voltage (V_{OUT})……...0.8V to 0.95 x V_{IN}
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-14 (4mmx4mm)
JESD51-7…..…..……..46.7.....7.9.... °C/W (8)
EVQ4326M-R-00A.....…..25.7..... °C/W (9)

Ψ_{JT}

QFN-14 (4mmx4mm)
JESD51-7 …..….....2.6.....°C/W (8)
EVQ4326M-R-00A …….....2.2.....°C/W (9)

Notes:

3) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
4) Refer to ISO16750.
5) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
6) Per AEC-Q100-002.
7) Per AEC-Q100-011.
8) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages, and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{JC} shows the thermal resistance from junction-to-case bottom, and the value of Ψ_{JT} shows the characterization parameter from junction-to-case top.
9) Measured on an MPS standard EVB: 8.3cmx8.3cm, 2oz. copper thickness, 4-layer PCB, and the value of Ψ_{JT} shows the characterization parameter from junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage (V_{IN})						
V_{IN} minimum operating voltage	V_{IN_MIN}				3.3	V
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		3.5	3.7	3.9	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		2.75	2.9	3.15	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			750		mV
VIN quiescent current	I_Q	FB = 0.85V, no load, (sleep mode), without BIAS connection, T_J = 25°C		24	35	µA
		FB = 0.85V, no load, (sleep mode), without BIAS connection, T_J = -40°C to +150°C		24	80	µA
		FB = 0.85V, no load, connect BIAS to 5V		3		µA
VIN quiescent current (switching)	I_{Q_SLEEP}	SYNC/MODE = GND (AAM mode), switching, no load		28		µA
VIN active current (non-switching)	I_{Q_ACTIVE}	SYNC/MODE = VCC (FCCM), non-switching		950		µA
VIN shutdown current	I_{SHDN}	EN = 0V		1	10	µA
V_{IN} over-voltage protection (OVP) threshold	$V_{IN\_OVP\_RISING}$		36	38	40	V
V_{IN} OVP hysteresis	$V_{IN\_OVP\_HYS}$			1		V
Switches and Frequency						
Switching frequency	f_{SW}	R_{FREQ} = 49.9kΩ	350	410	460	kHz
		R_{FREQ} = 19.6kΩ	900	1000	1100	kHz
		R_{FREQ} = 8.66kΩ	1980	2200	2420	kHz
Minimum on time (10)	t_{ON_MIN}			50	65	ns
Minimum off time (10)	t_{OFF_MIN}			40	55	ns
Switch leakage current	I_{SW_LKG}	T_J = 25°C		0.01	1	µA
		T_J = -40°C to +150°C		0.01	5	µA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{BST} - V_{SW} = 5V		45		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	V_{CC} = 5V		25		mΩ
BIAS						
BIAS voltage (V_{BIAS}) takeover threshold	V_{BIAS_RISING}			4.6		V
V_{BIAS} takeover hysteresis	V_{BIAS_HYS}			240		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output and Regulation						
FB voltage	V_{FB}	T_J = 25°C	794	800	806	mV
		T_J = -40°C to +150°C	790	800	810	mV
FB input current	I_{FB}			0	100	nA
V_{OUT} discharge current	$I_{DISCHARGE}$	EN = 0V, V_{OUT} = 0.3V	2			mA
Bootstrap (BST)						
BST - SW refresh rising threshold	$V_{UV\_BST-SW\_RISING}$		2.2	2.7	3.2	V
BST - SW refresh falling threshold	$V_{UV\_BST-SW\_FALLING}$		2	2.5	3	V
BST - SW refresh hysteresis	$V_{UV\_BST-SW\_HYS}$			0.2		V
Enable (EN)						
EN rising threshold	V_{EN_RISING}		0.97	1.02	1.07	V
EN falling threshold	$V_{EN\_FALLING}$		0.8	0.85	0.9	V
EN hysteresis voltage	V_{EN_HYS}			170		mV
Soft Start (SS) and VCC						
SS time	t_{SS}	EN high to PG high	4.5	6.0	7.5	ms
VCC voltage	V_{CC}	I_{VCC} = 0mA	4.7	5.0	5.3	V
VCC regulation		I_{VCC} = 30mA, AAM mode		1		%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	50	65		mA
SYNC/MODE						
SYNC/MODE voltage rising threshold	V_{SYNC_RISING}		1.4			V
SYNC/MODE voltage falling threshold	$V_{SYNC\_FALLING}$				0.4	V
SYNC/MODE timeout	t_{MODE}	SYNC/MODE low to discontinuous conduction mode (DCM)		55	80	µs
SYNCIN clock range	f_{SYNC}	% of freerunning frequency	90%		110%	fsw
SYNCIN clock locking time	t_{SYNC_LOCK}	SYNC clock locking time			128	cycles
SYNCIN clock duty	D_{SYNC_DUTY}	SYNC clock duty for minimum input clock pulse width >40ns	20		80	%
f_{SW} after SYNC		f_{SW} accuracy compared to f_{SYNC}	-5		+5	%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Good (PG)						
PG rising threshold	$V_{PG\_TH\_RISING}$	V_{OUT} rising	93%	94.5%	96%	V_{OUT}
		V_{OUT} falling	104%	105.5%	107%	V_{OUT}
PG falling threshold	$V_{PG\_TH\_FALLING}$	V_{OUT} falling	91.5%	93%	94.5%	V_{OUT}
		V_{OUT} rising	105.5%	107%	108.5%	V_{OUT}
PG trip threshold hysteresis	$V_{PG\_TH\_HYS}$			1.5%		V_{OUT}
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG start-up rising delay	$t_{PG\_R\_DELAY}$			1.2		ms
PG rising deglitch time	$t_{PG\_R\_DEGLITCH}$			160		µs
PG falling deglitch time	$t_{PG\_F\_DEGLITCH}$			160		µs
Protections						
High-side (HS) current limit	I_{LIMIT_HS}	Duty cycle = 30%	8.5	11	13	A
Low-side (LS) valley current limit	I_{LIMIT_LS}		6	7.5	9	A
Zero-current detection (ZCD) threshold	I_{ZCD}	AAM mode	0	200		mA
LS reverse current limit	$I_{LIMIT\_REVERSE}$	FCCM		3		A
Thermal shutdown (10)	T_{SD}		155	170	185	°C
Thermal shutdown hysteresis (10)	T_{SD_HYS}			20		°C

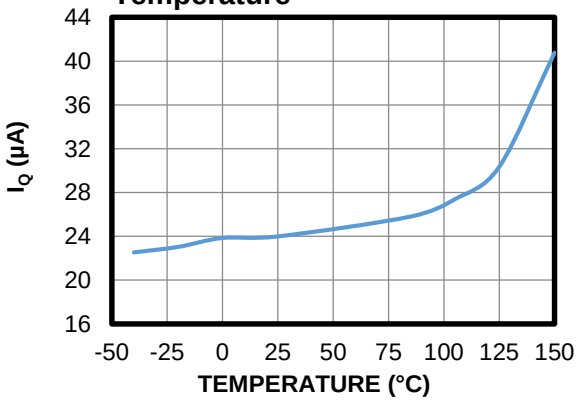
Note:

10) Not tested in production; guaranteed by design and characterization.

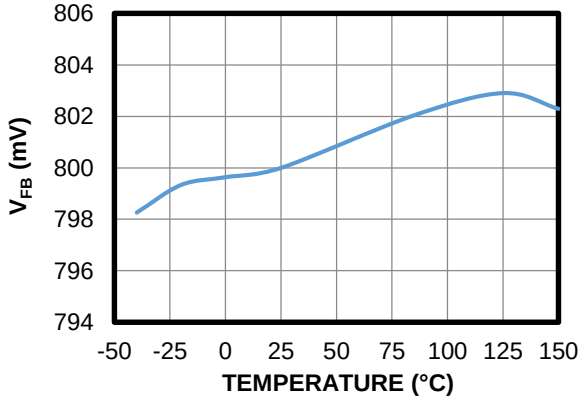
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

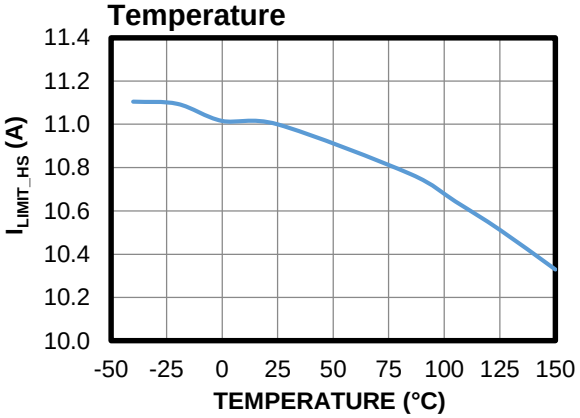
Quiescent Current vs. Temperature



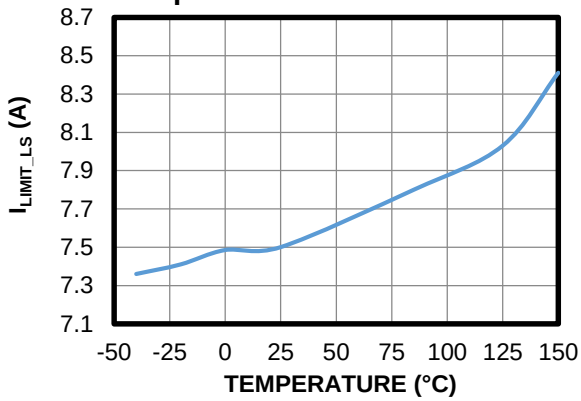
Feedback Voltage vs. Temperature



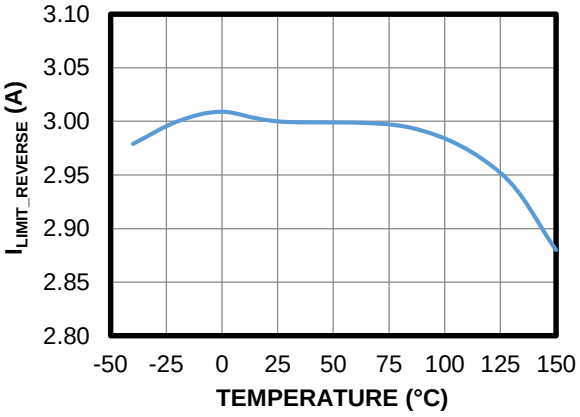
High-Side Current Limit vs. Temperature



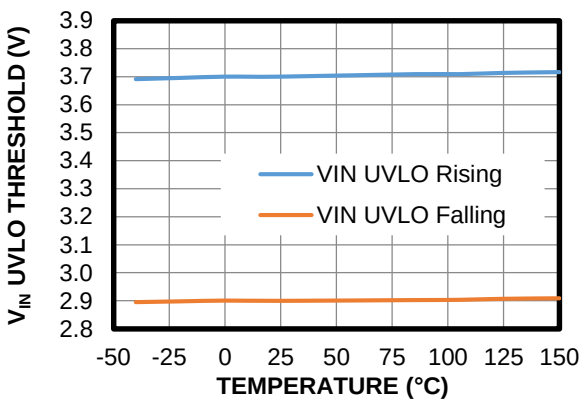
Low-Side Current Limit vs. Temperature



Reverse Current Limit vs. Temperature



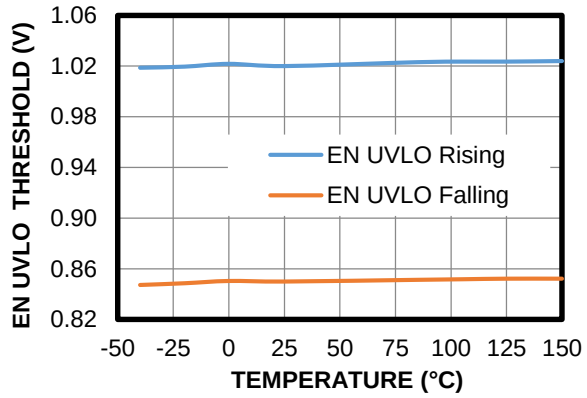
V_{IN} UVLO Threshold vs. Temperature



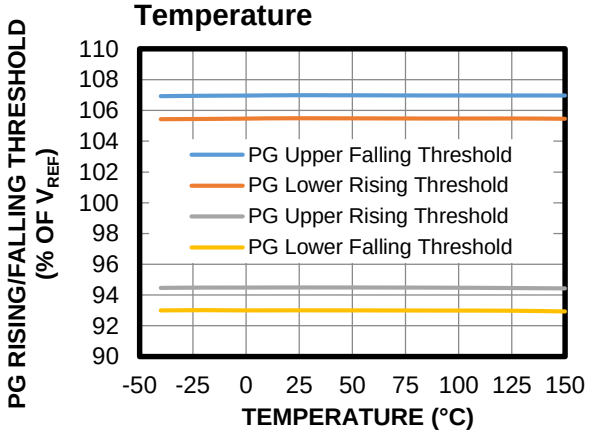
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

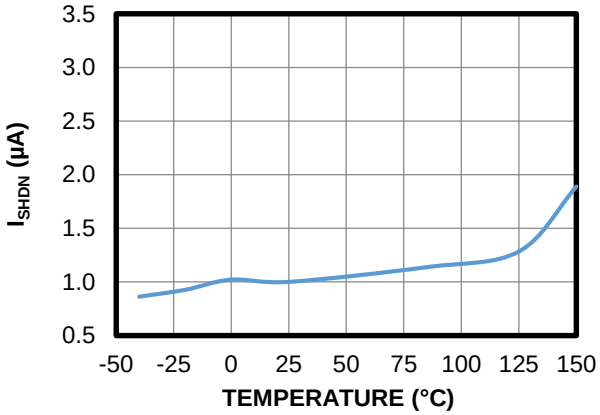
EN UVLO Threshold vs. Temperature



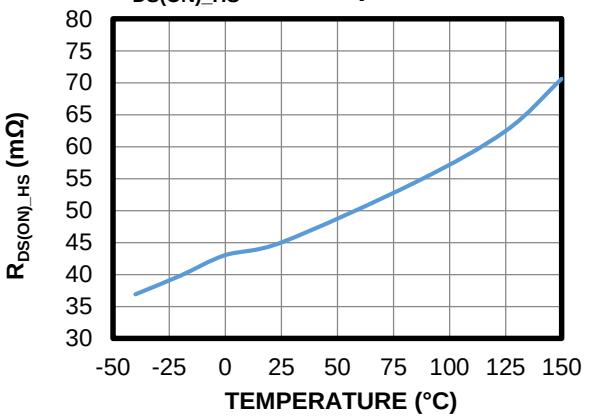
PG Rising/Falling Threshold vs. Temperature



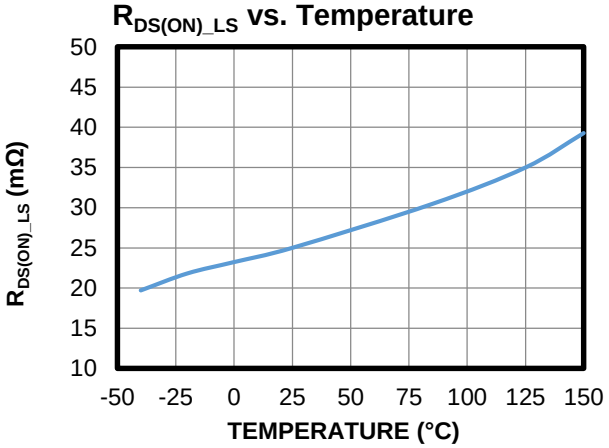
VIN Shutdown Current vs. Temperature



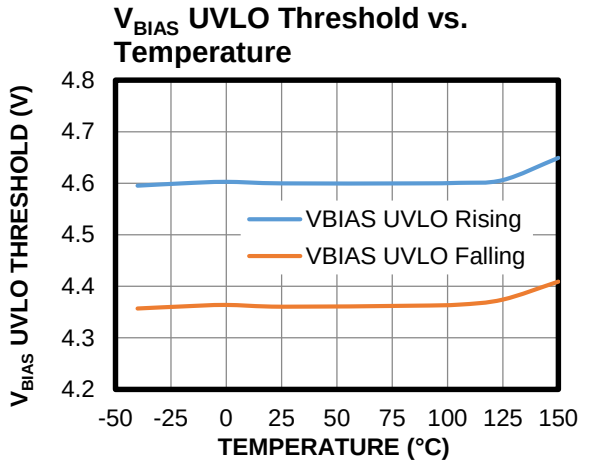
$R_{DS(ON)\_HS}$ vs. Temperature



$R_{DS(ON)\_LS}$ vs. Temperature



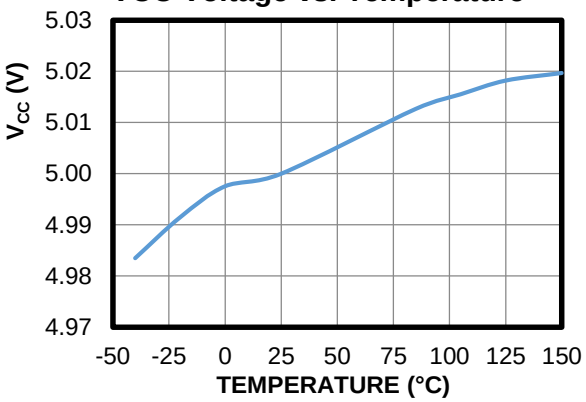
V_{BIAS} UVLO Threshold vs. Temperature



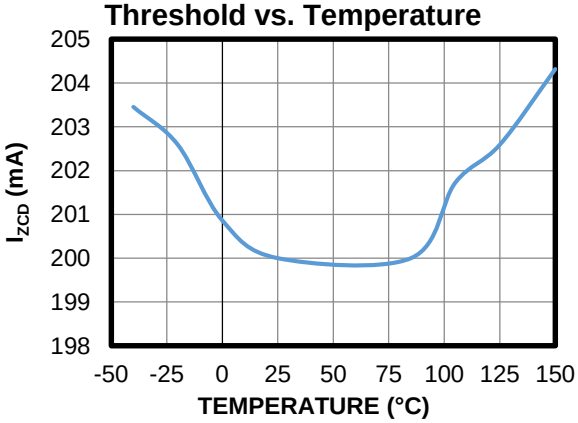
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

VCC Voltage vs. Temperature

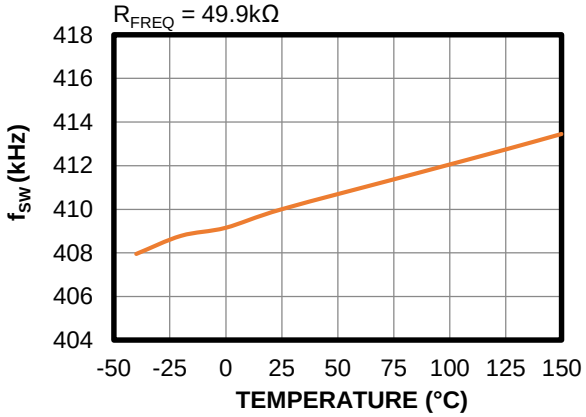


Zero-Current Detection Threshold vs. Temperature



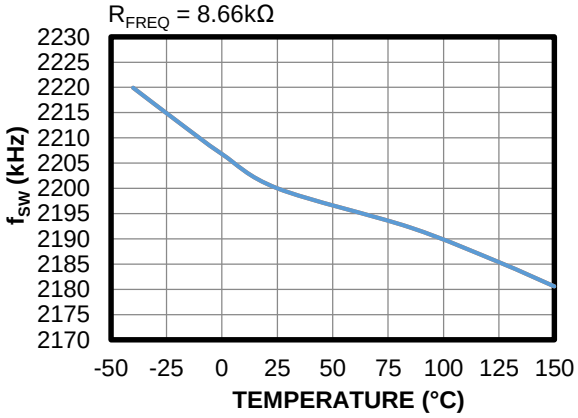
Switching Frequency vs. Temperature

R_{FREQ} = 49.9kΩ



Switching Frequency vs. Temperature

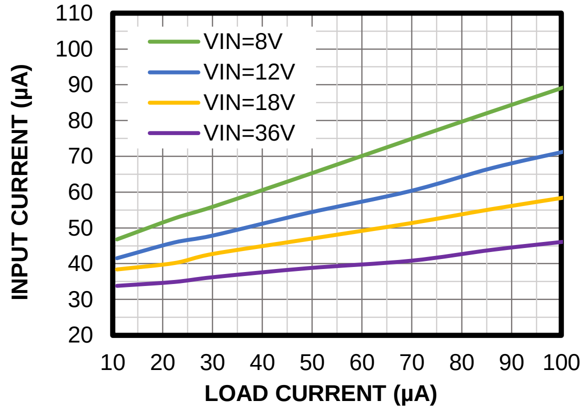
R_{FREQ} = 8.66kΩ



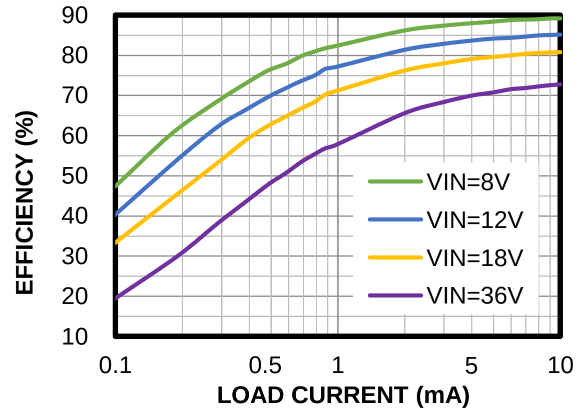
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

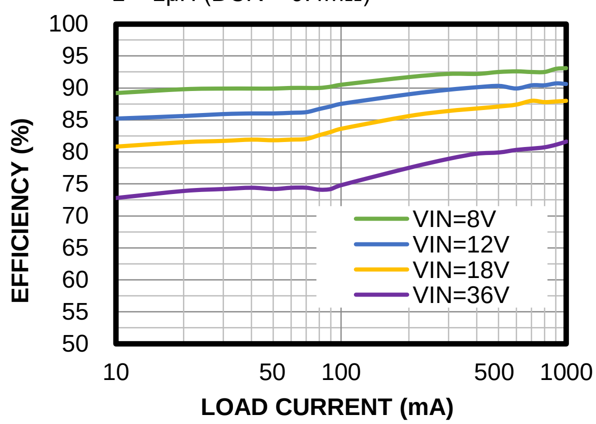
Input Current vs. Load Current
AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



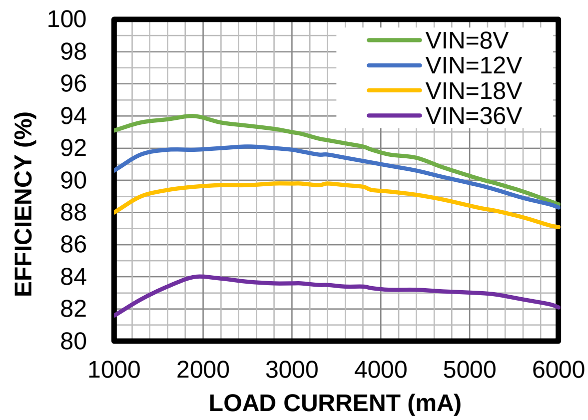
Efficiency vs. Load Current
AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



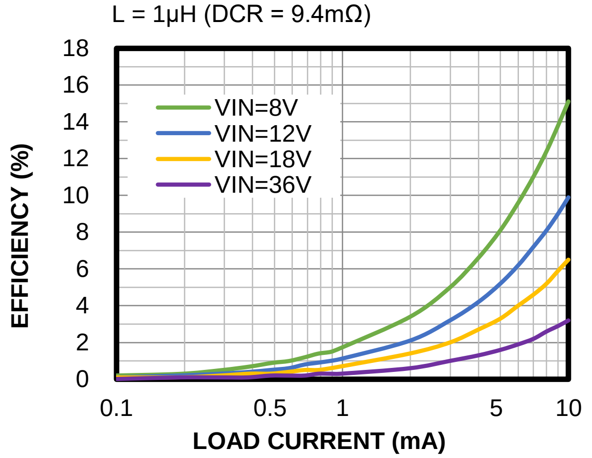
Efficiency vs. Load Current
AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



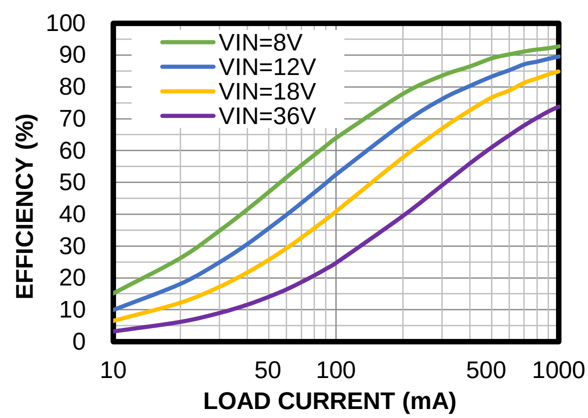
Efficiency vs. Load Current
AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)

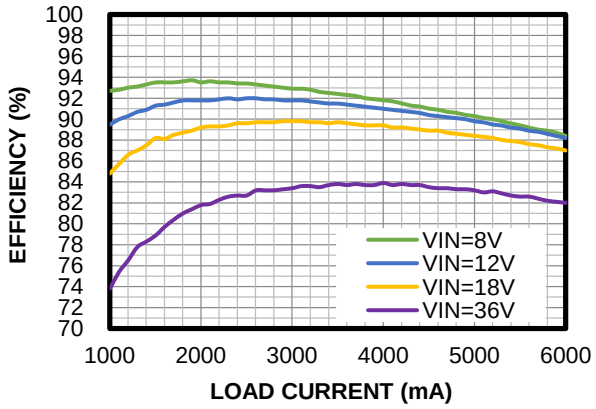


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

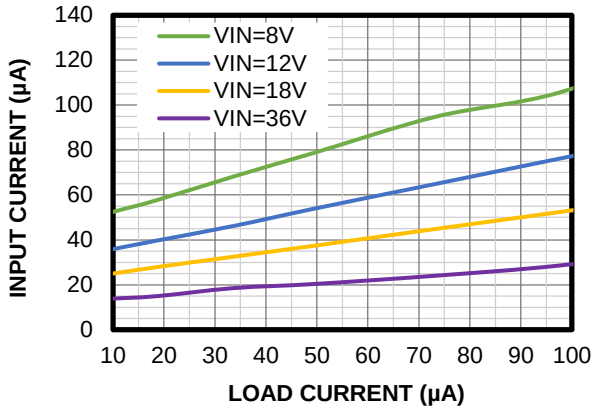
Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



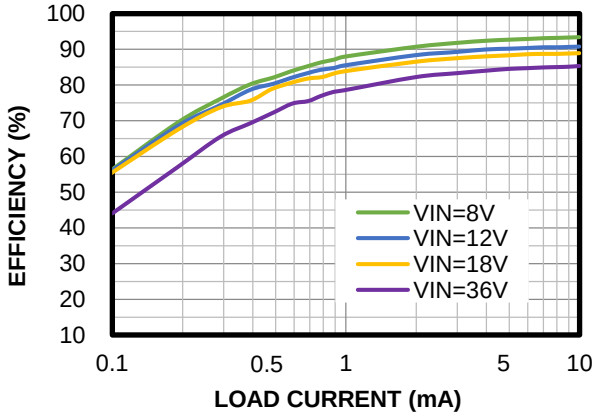
Input Current vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



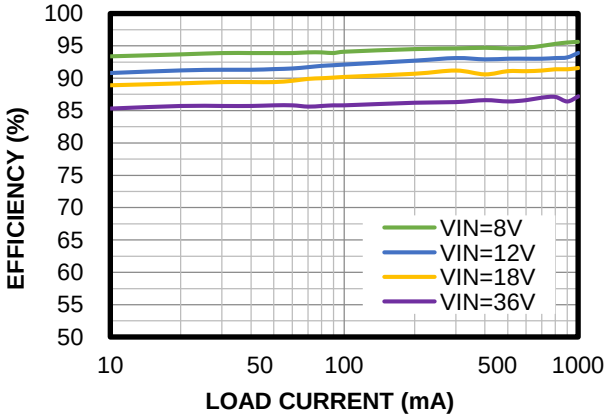
Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



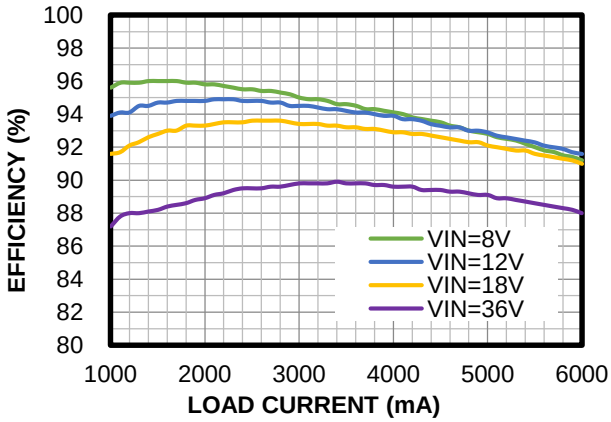
Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



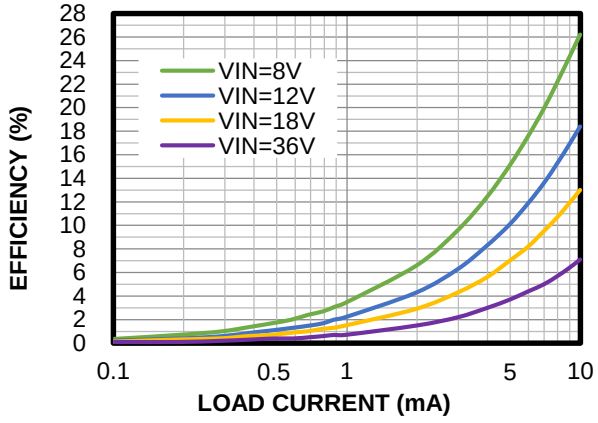
Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



Efficiency vs. Load Current

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)

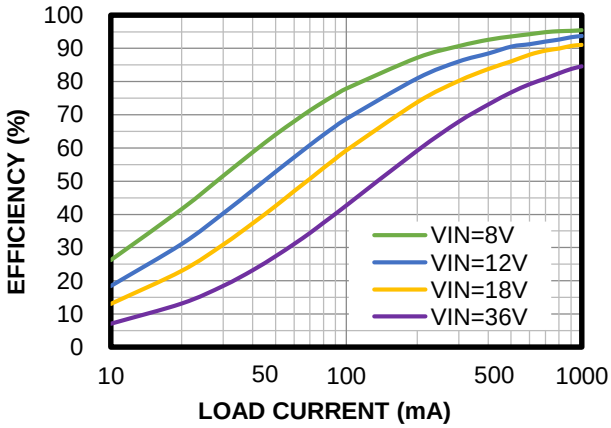


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

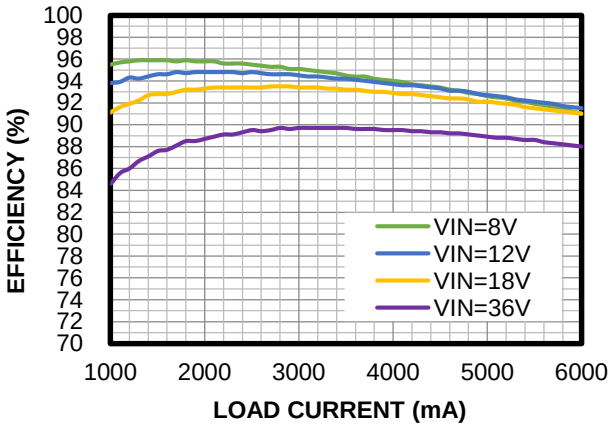
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 1µH (DCR = 9.4mΩ)



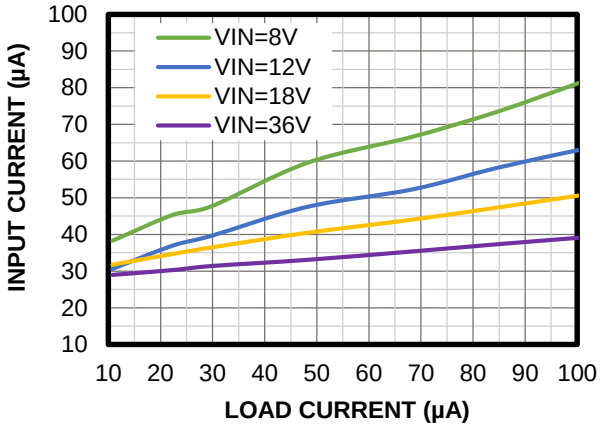
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 1µH (DCR = 9.4mΩ)



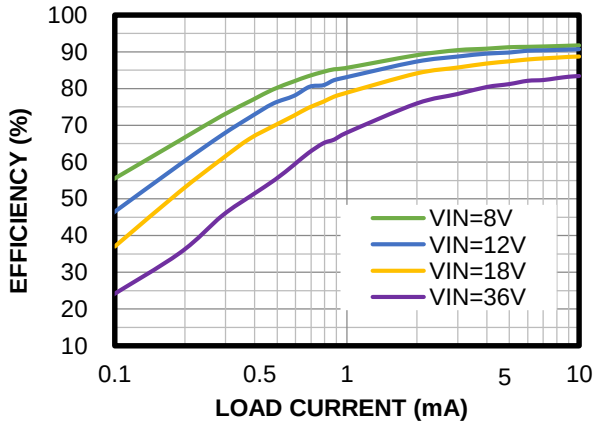
Input Current vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 4.7µH (DCR = 15mΩ)



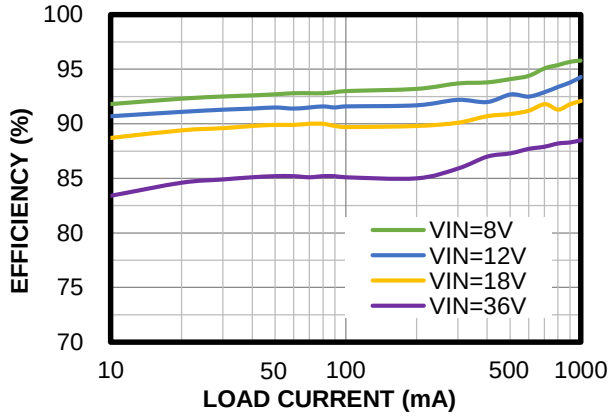
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 4.7µH (DCR = 15mΩ)



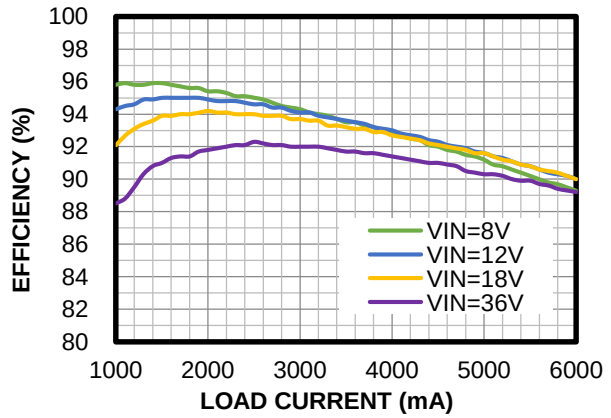
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 4.7µH (DCR = 15mΩ)



Efficiency vs. Load Current

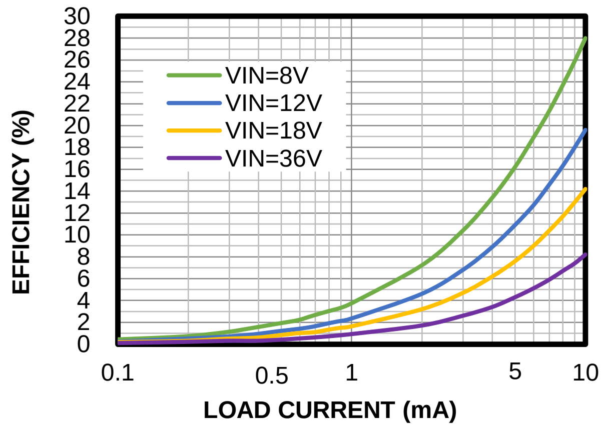
AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 4.7µH (DCR = 15mΩ)



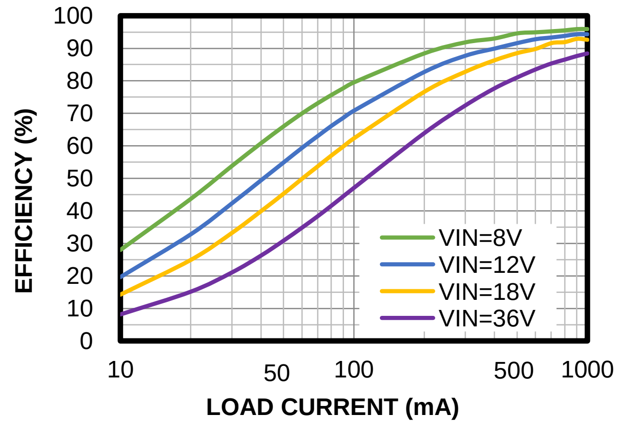
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

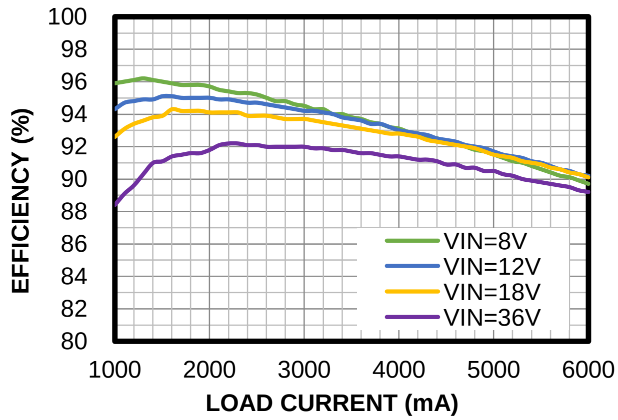
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



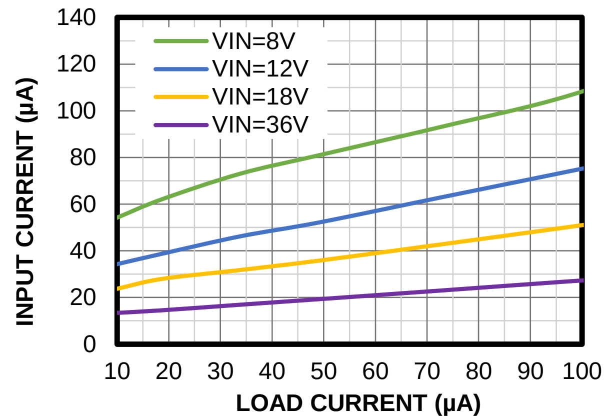
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



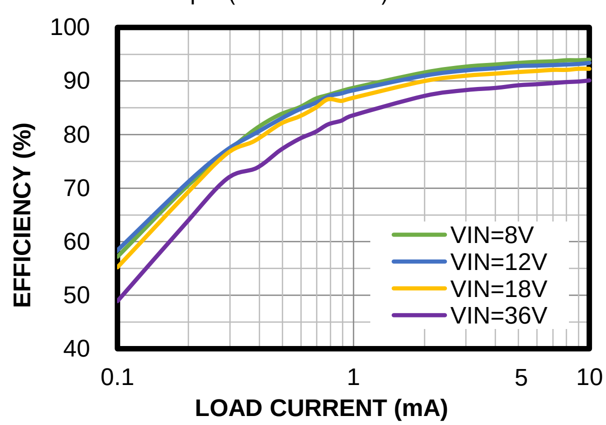
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



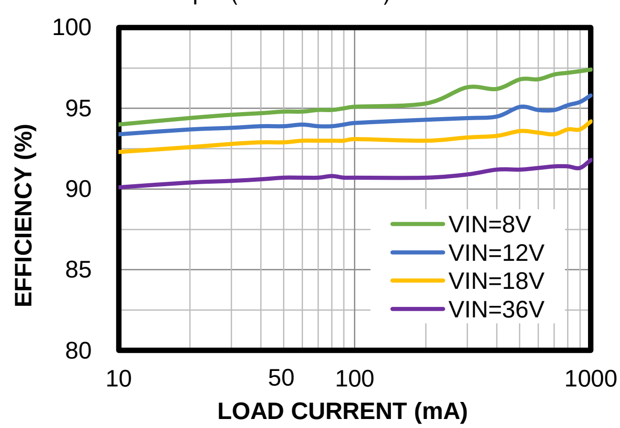
Input Current vs. Load Current
AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)

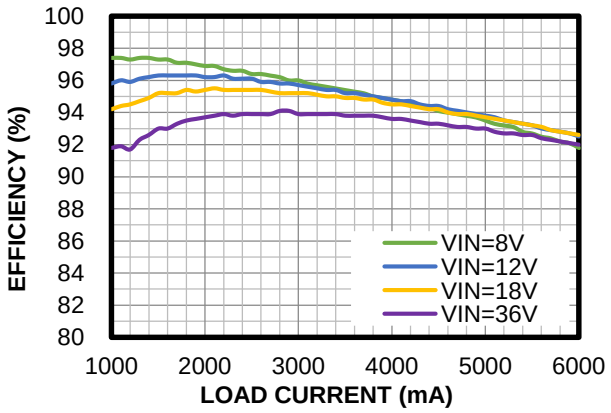


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

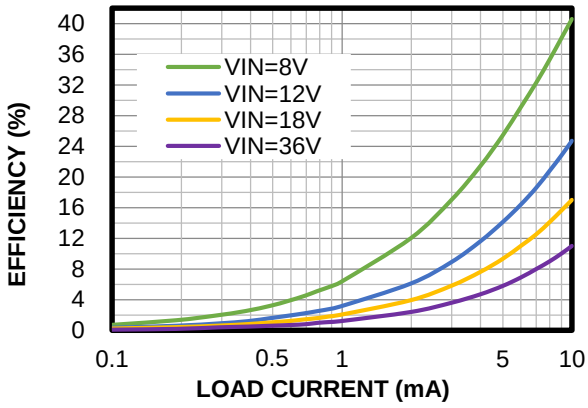
Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz, L = 4.7µH (DCR = 15mΩ)



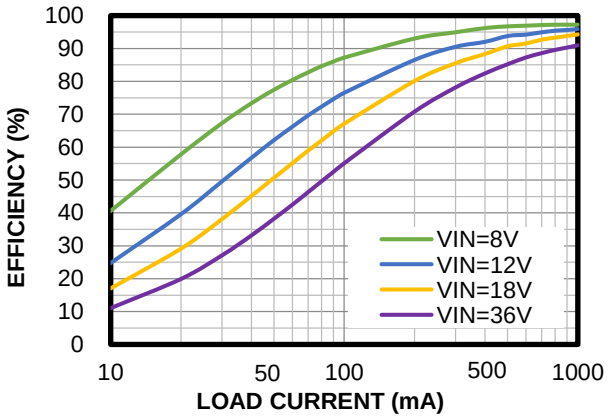
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V, f_{SW} = 410kHz, L = 4.7µH (DCR = 15mΩ)



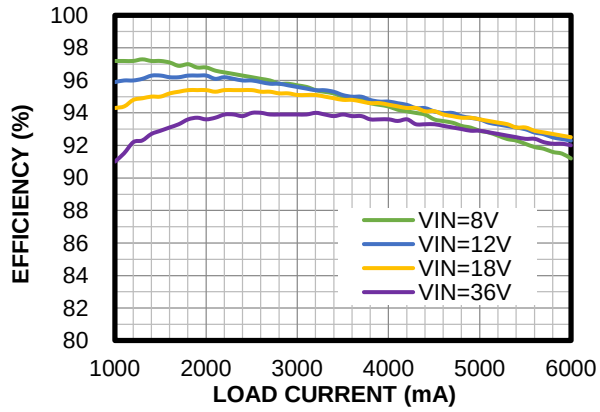
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V, f_{SW} = 410kHz, L = 4.7µH (DCR = 15mΩ)



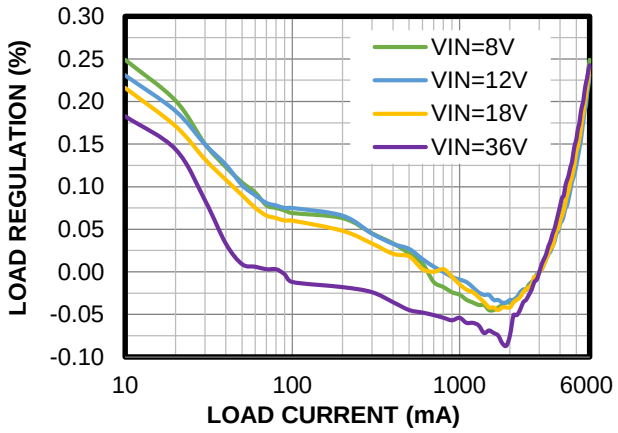
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V, f_{SW} = 410kHz, L = 4.7µH (DCR = 15mΩ)



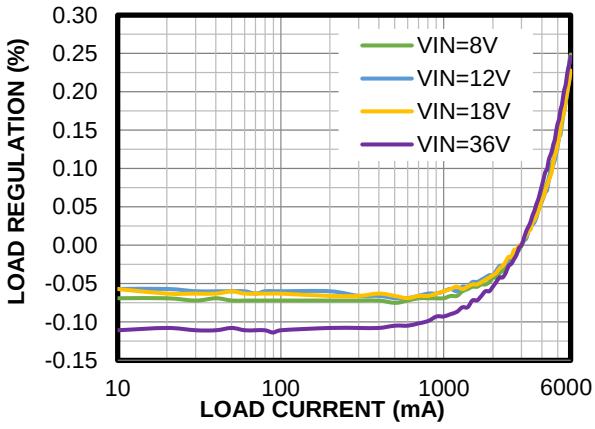
Load Regulation

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 1µH (DCR = 9.4mΩ)



Load Regulation

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 1µH (DCR = 9.4mΩ)

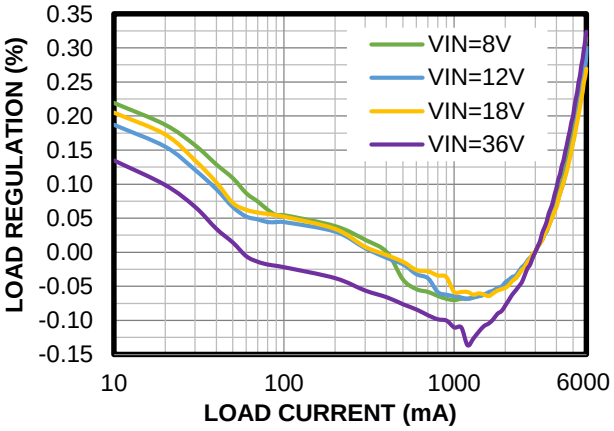


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

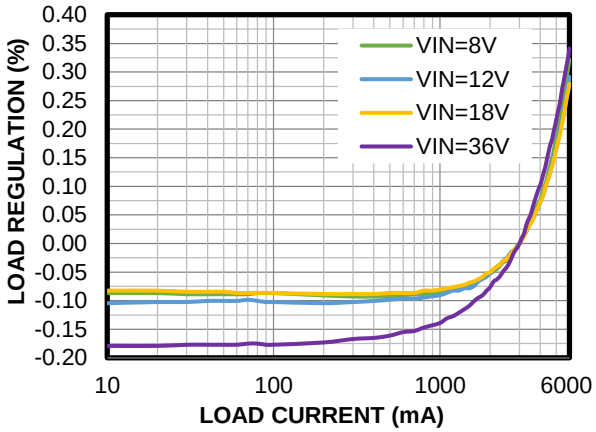
Load Regulation

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



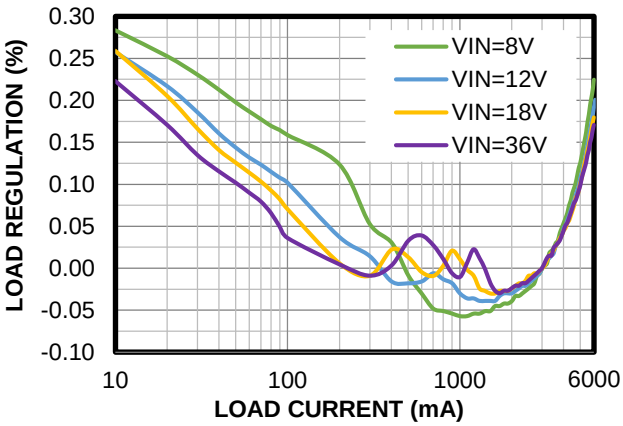
Load Regulation

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



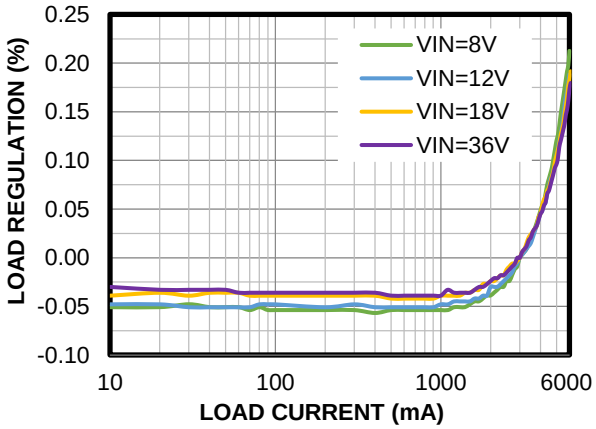
Load Regulation

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



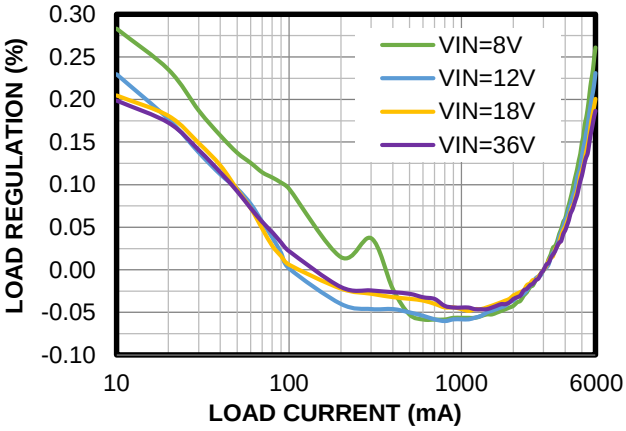
Load Regulation

FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



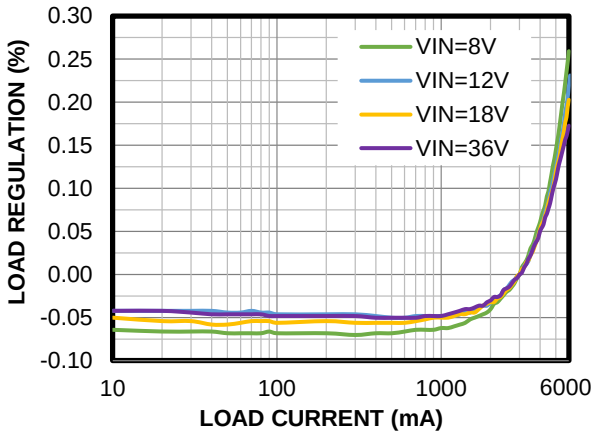
Load Regulation

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



Load Regulation

FCCM, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)

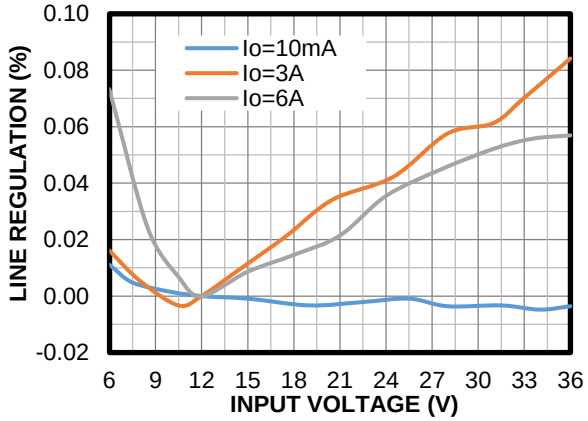


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

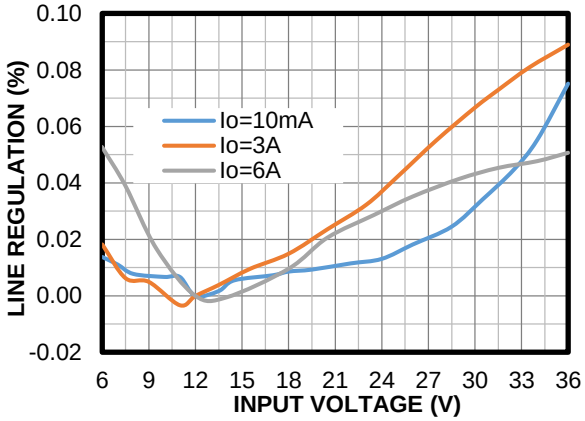
Line Regulation

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



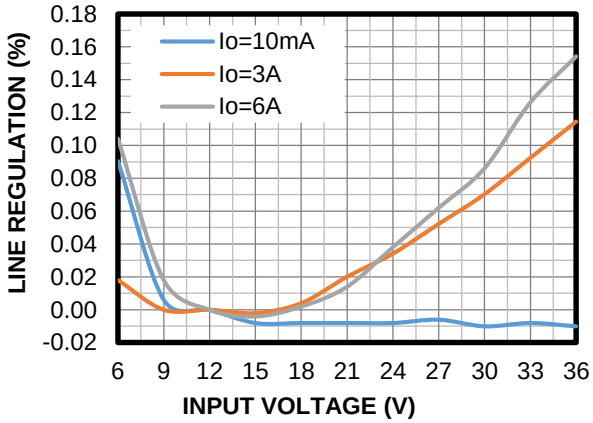
Line Regulation

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



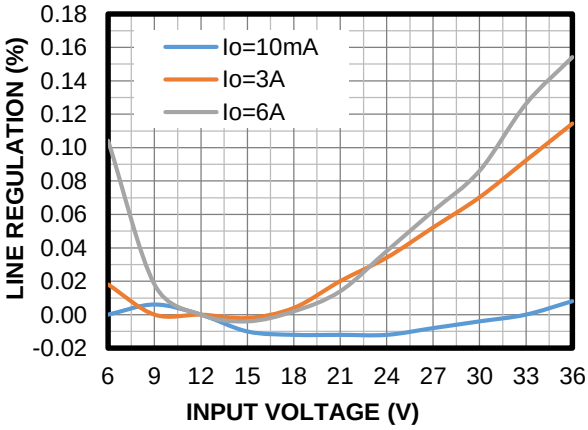
Line Regulation

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



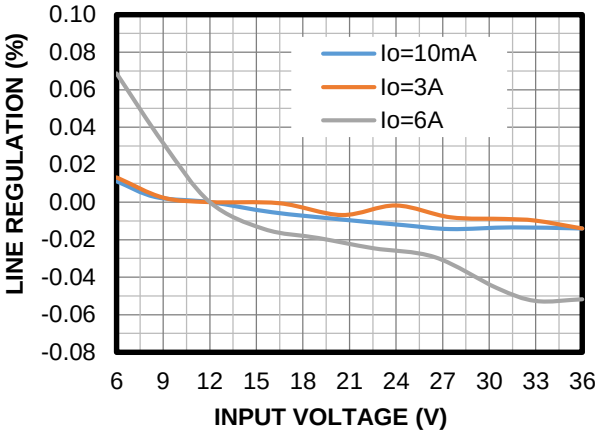
Line Regulation

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



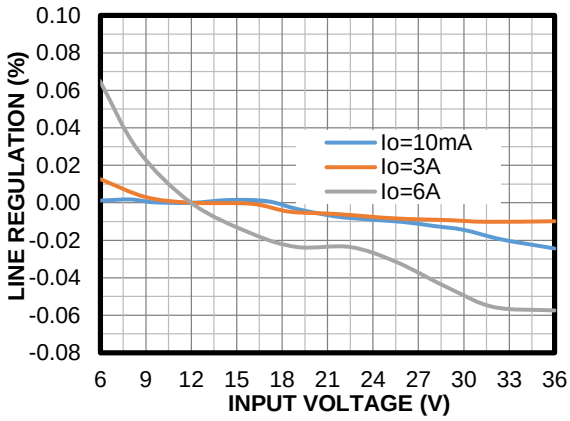
Line Regulation

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



Line Regulation

FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)

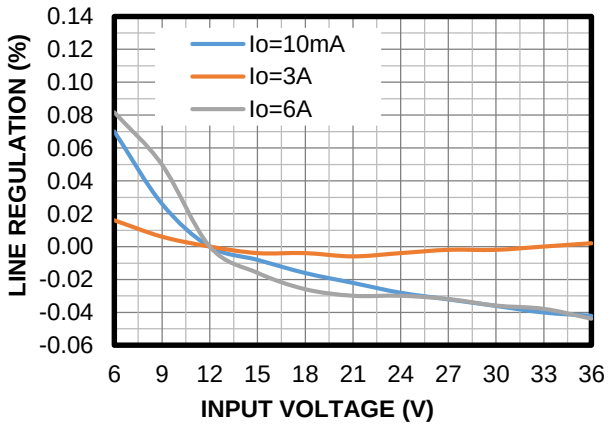


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

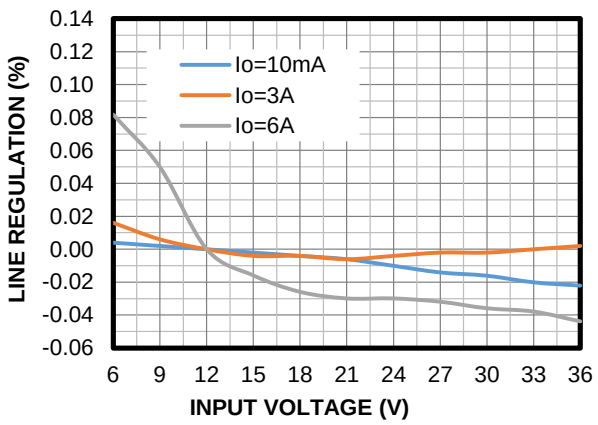
Line Regulation

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



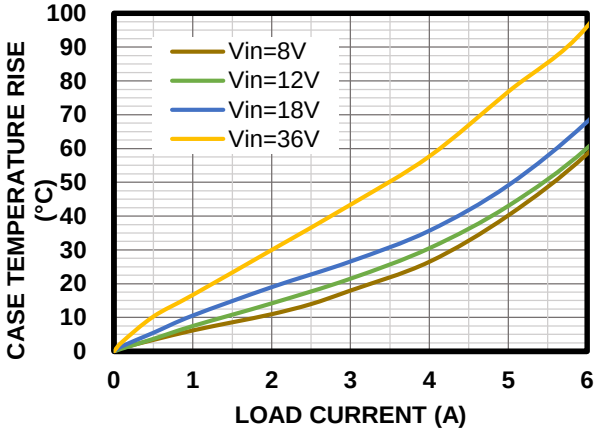
Line Regulation

FCCM, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



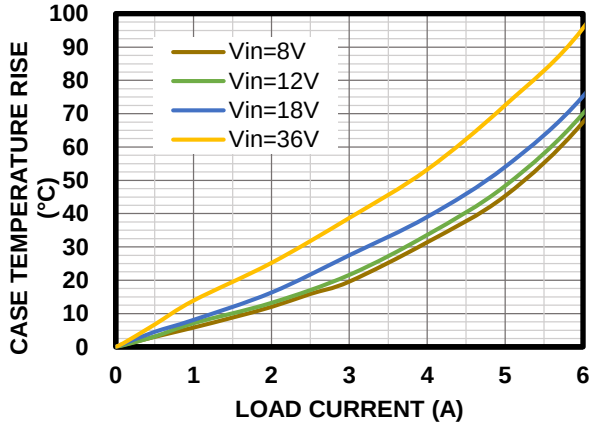
Case Temperature Rise

V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



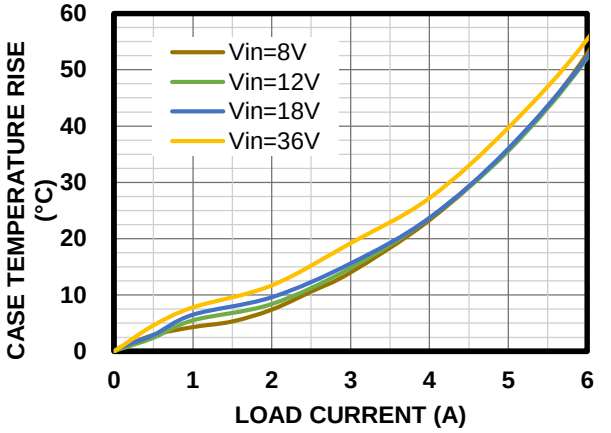
Case Temperature Rise

V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



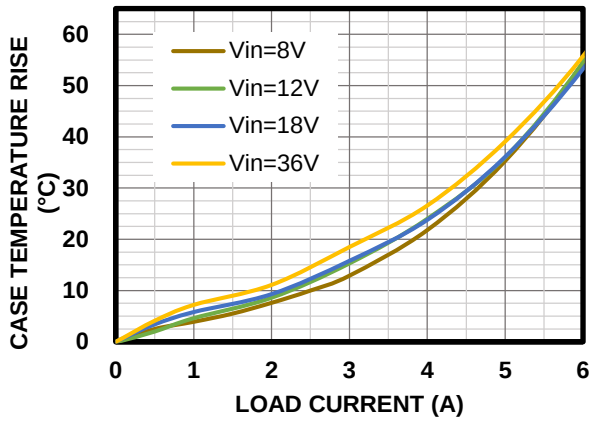
Case Temperature Rise

V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



Case Temperature Rise

V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)

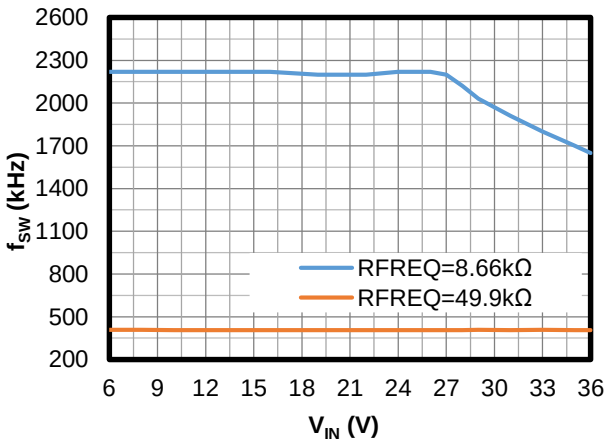


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

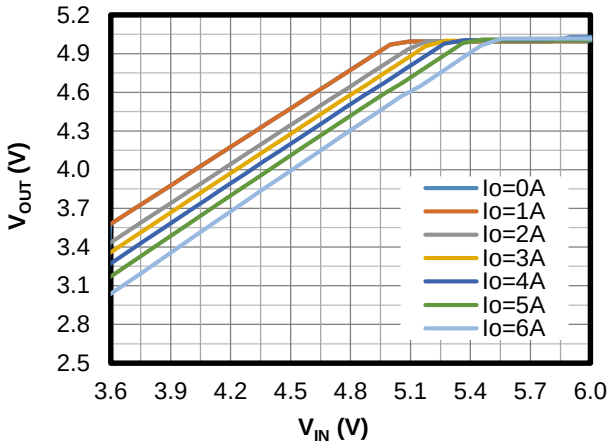
f_{SW} vs. V_{IN}

V_{OUT} = 3.3V



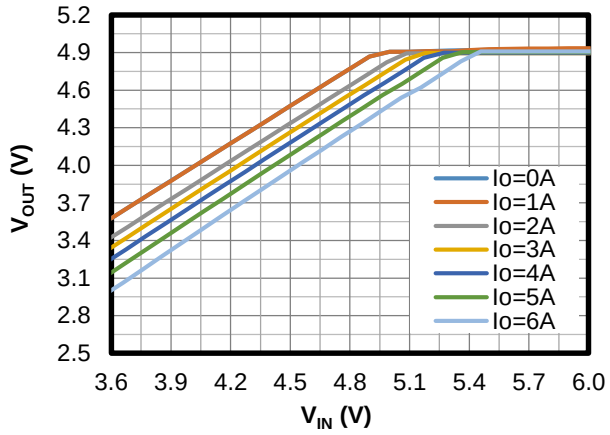
Low-Dropout Mode

V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



Low-Dropout Mode

V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)

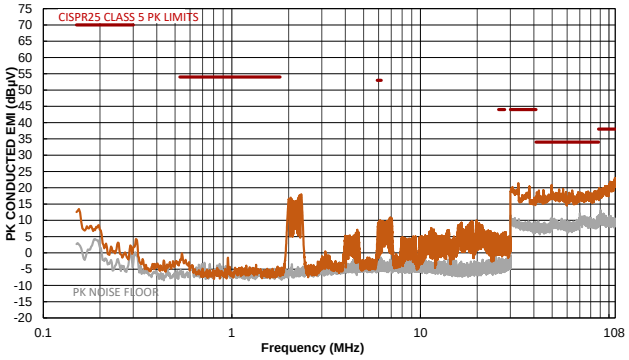


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, L = 1µH (11), f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted. (12)

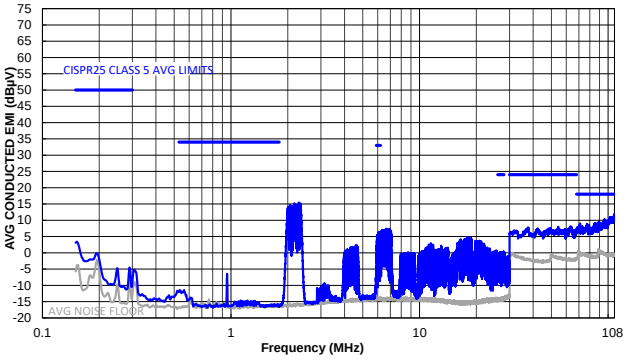
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



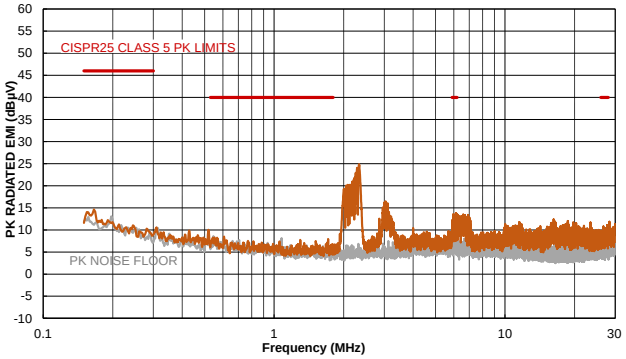
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



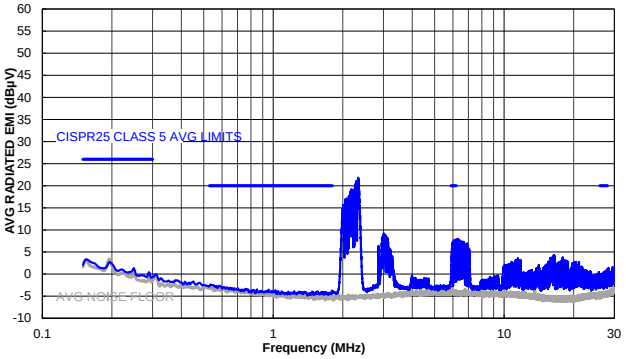
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



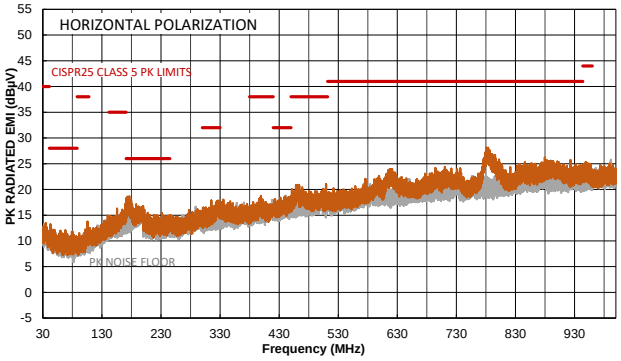
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



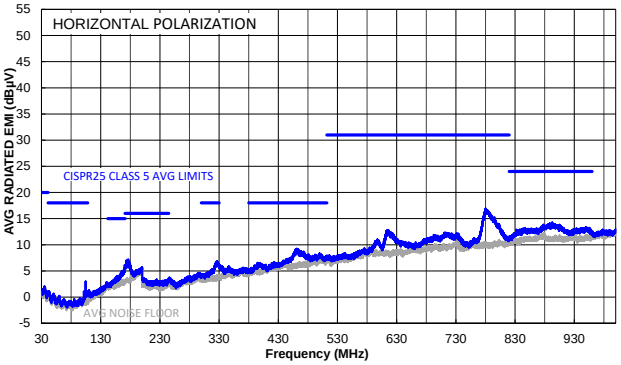
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

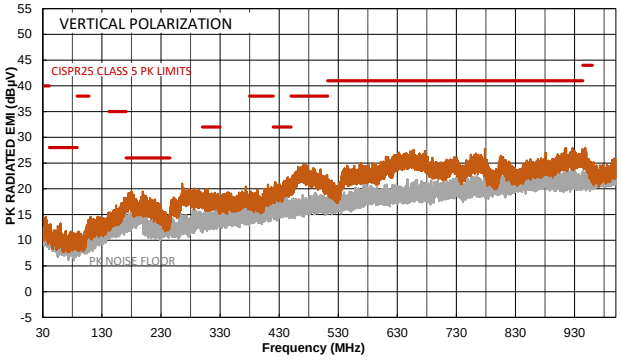


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, L = 1µH (11), f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted. (12)

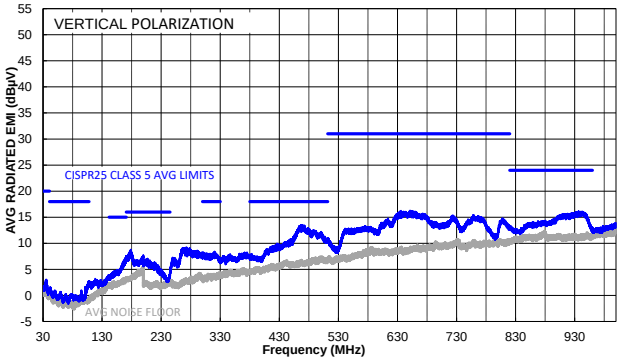
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Notes:

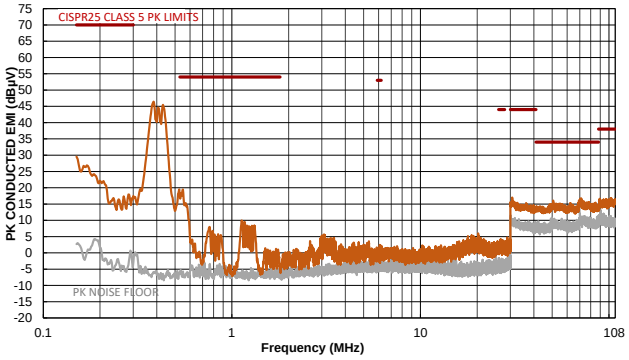
11) Inductor part number: XEL4020-102MEB; DCR = 14.6mΩ.
12) The EMC test results are based on the typical application circuit with EMI filters (see Figure 15 on page 44).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, L = 4.7µH (13), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted. (14)

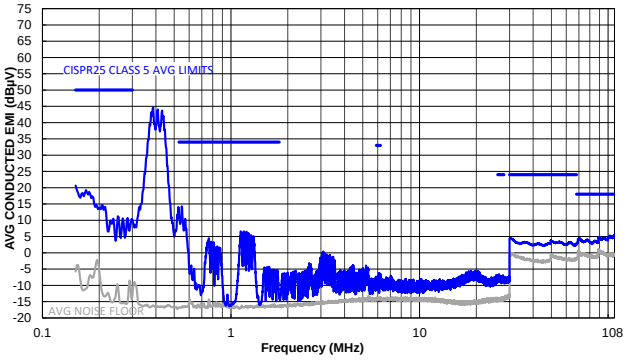
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



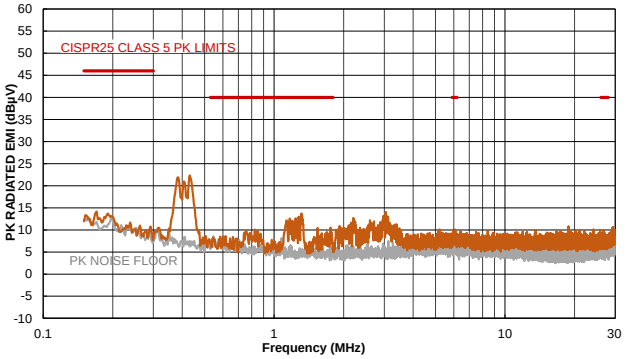
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



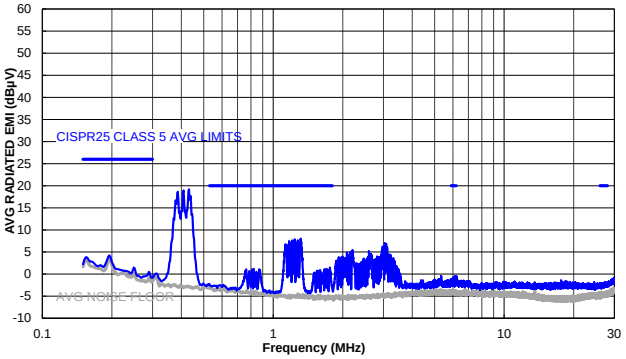
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



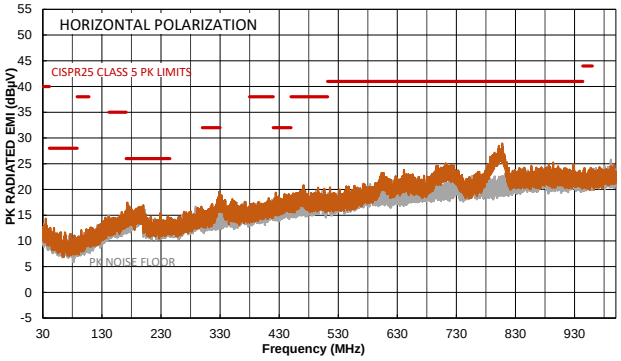
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



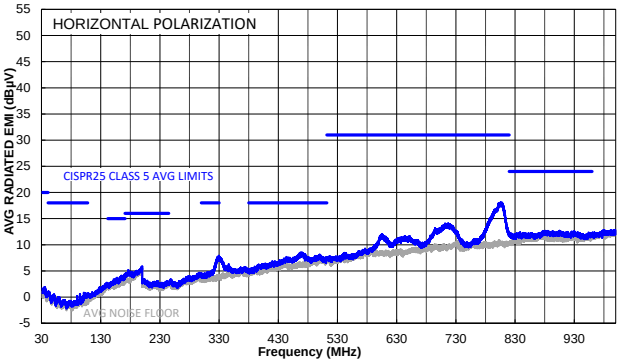
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

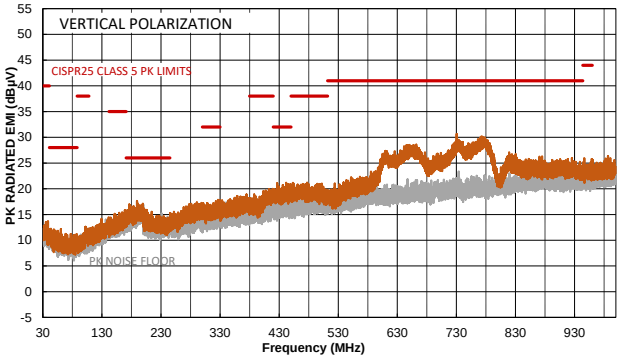


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, L = 4.7µH (13), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted. (14)

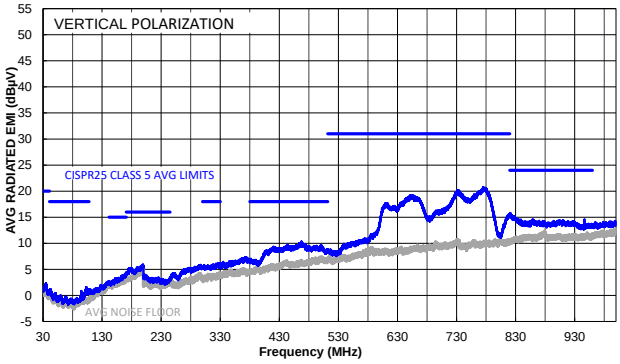
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Notes:

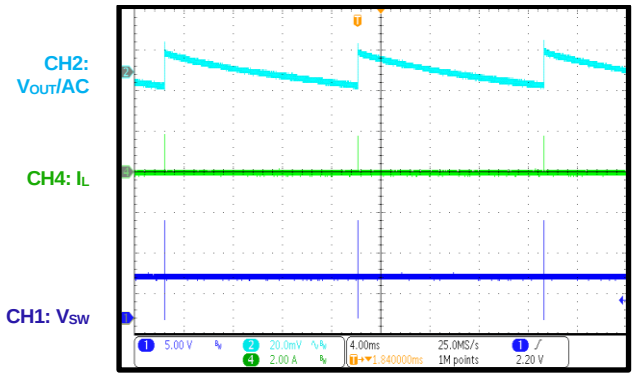
13) Inductor part number: XEL6060-472MEB/C; DCR = 15.02mΩ.

14) The EMC test results are based on the typical application circuit with EMI filters (see Figure 16 on page 45).

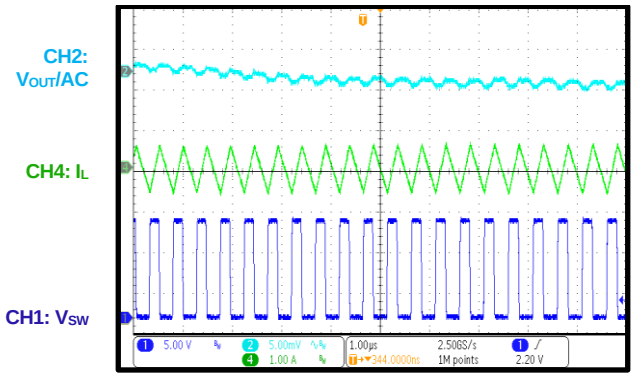
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

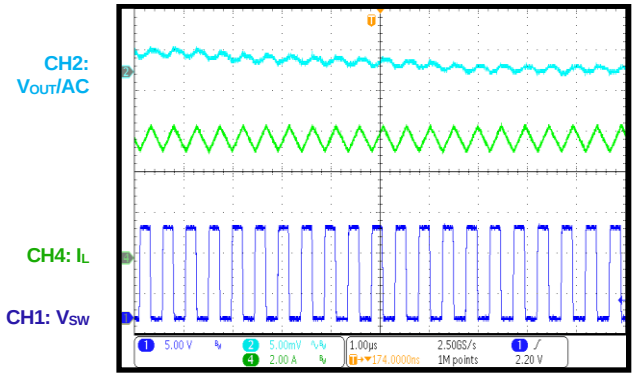
Steady State
I_{OUT} = 0A, AAM mode



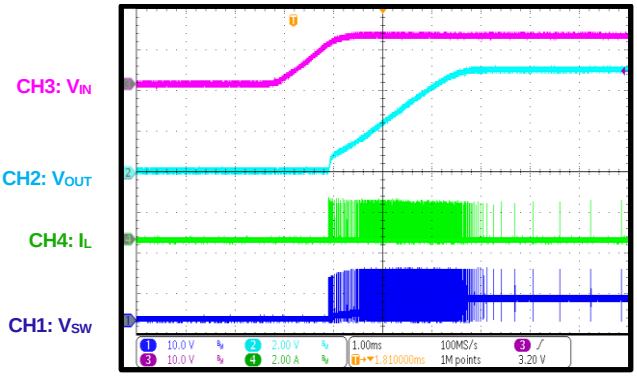
Steady State
I_{OUT} = 0A, FCCM



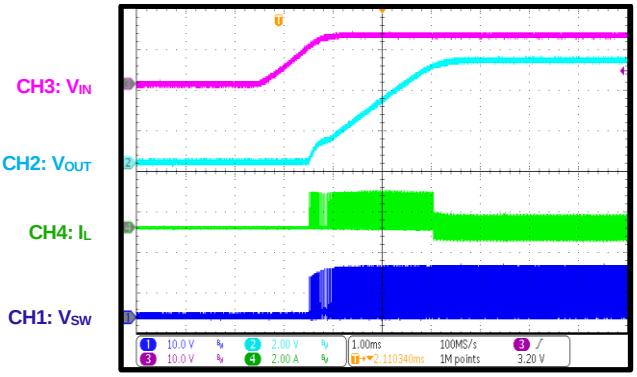
Steady State
I_{OUT} = 6A



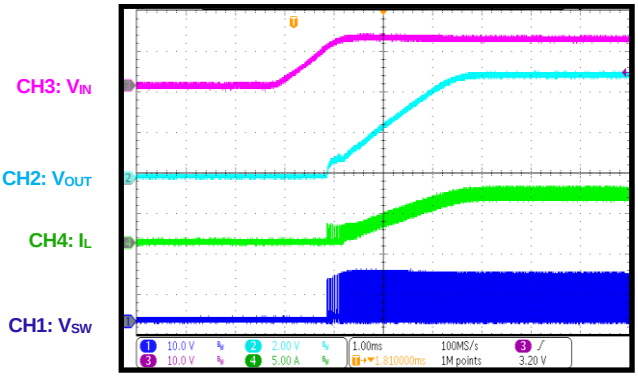
Start-Up through VIN
I_{OUT} = 0A, AAM mode



Start-Up through VIN
I_{OUT} = 0A, FCCM



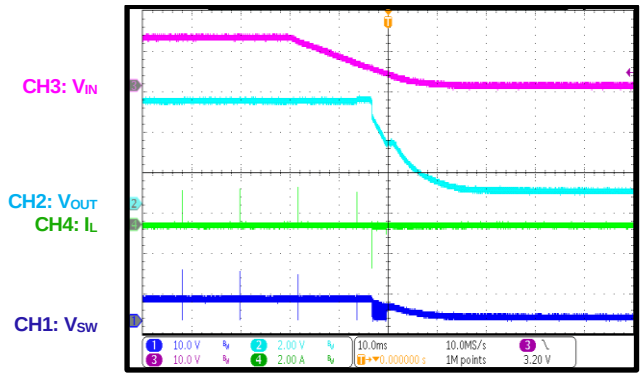
Start-Up through VIN
I_{OUT} = 6A



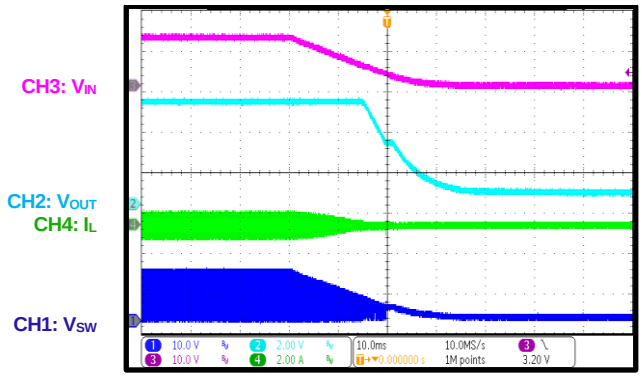
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

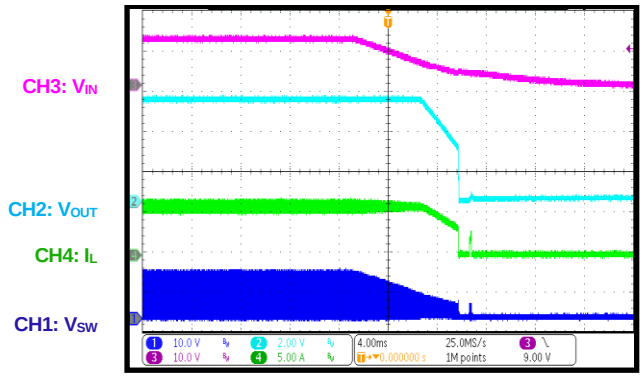
Shutdown through VIN
I_{OUT} = 0A, AAM mode



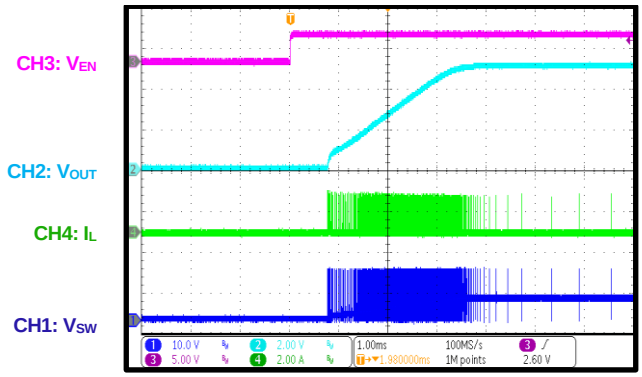
Shutdown through VIN
I_{OUT} = 0A, FCCM



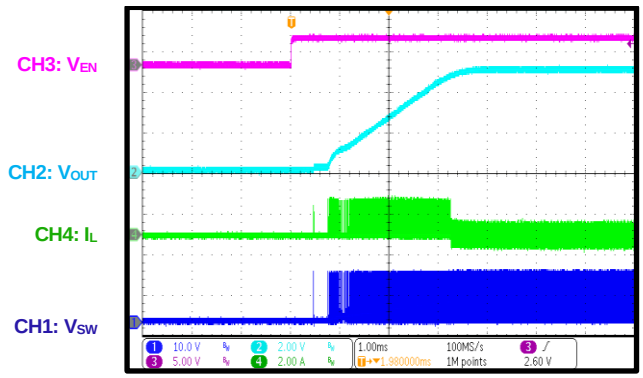
Shutdown through VIN
I_{OUT} = 6A



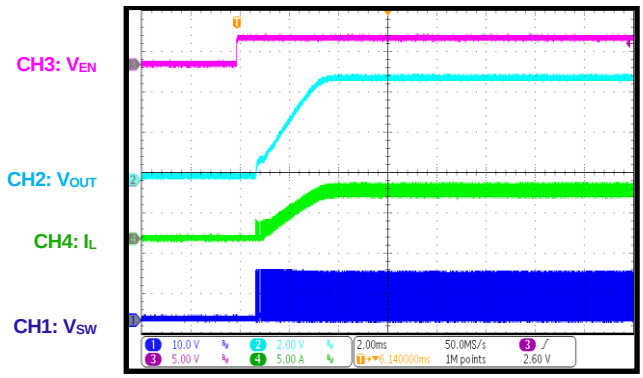
Start-Up through EN
I_{OUT} = 0A, AAM mode



Start-Up through EN
I_{OUT} = 0A, FCCM



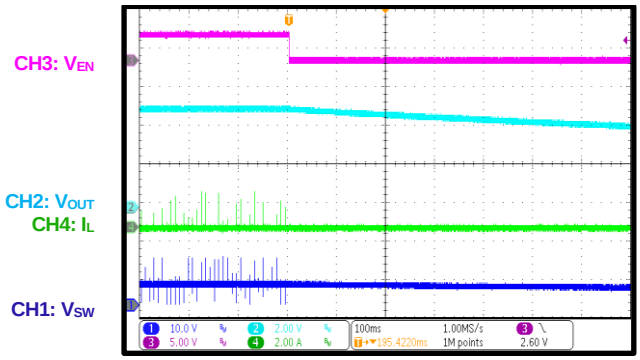
Start-Up through EN
I_{OUT} = 6A



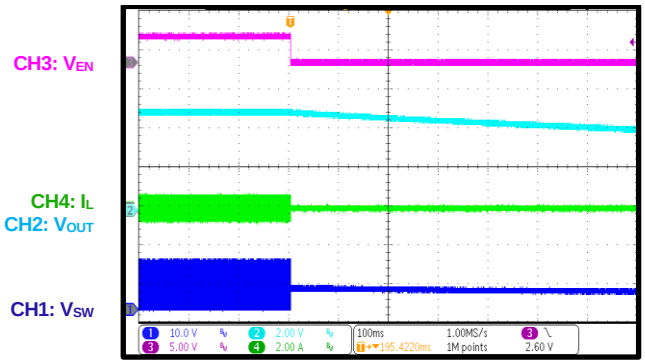
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

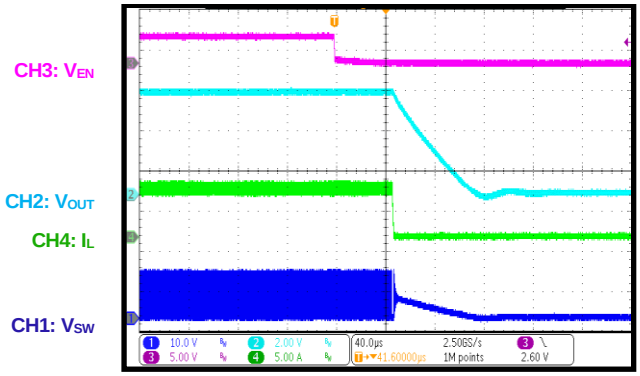
Shutdown through EN
I_{OUT} = 0A, AAM mode



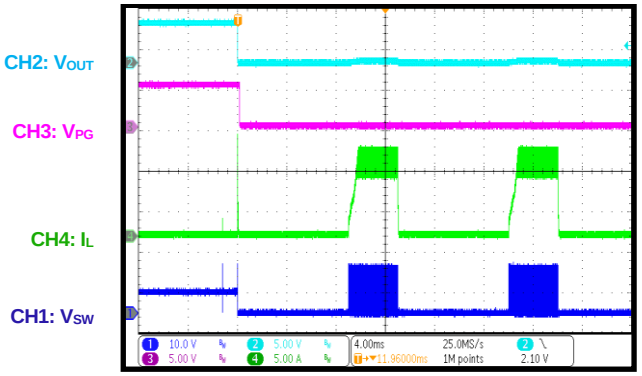
Shutdown through EN
I_{OUT} = 0A, FCCM



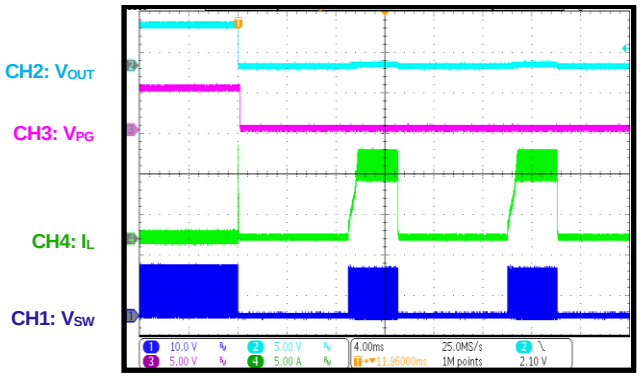
Shutdown through EN
I_{OUT} = 6A



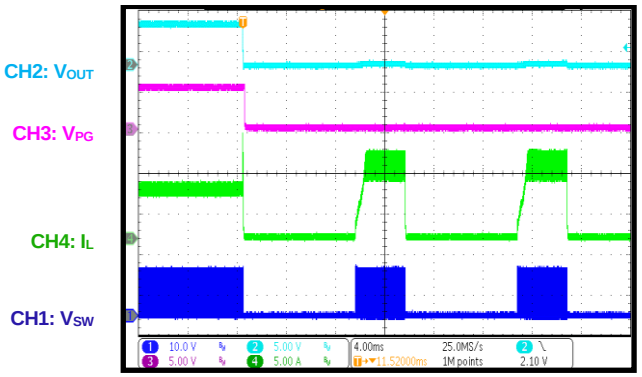
SCP Entry
I_{OUT} = 0A, AAM mode



SCP Entry
I_{OUT} = 0A, FCCM



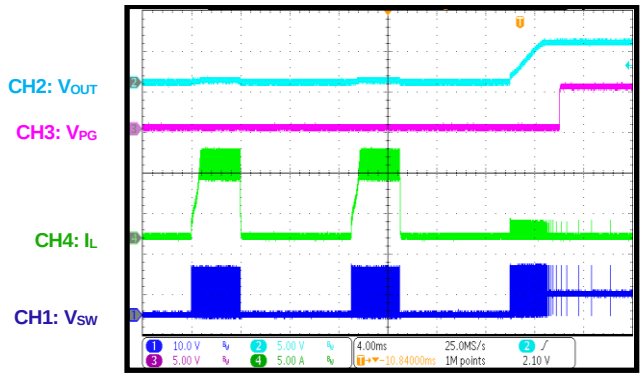
SCP Entry
I_{OUT} = 6A



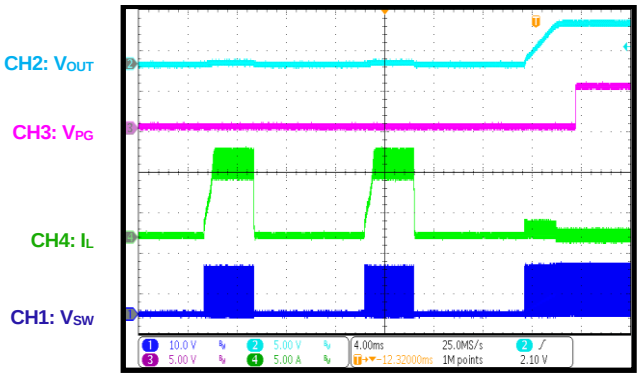
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

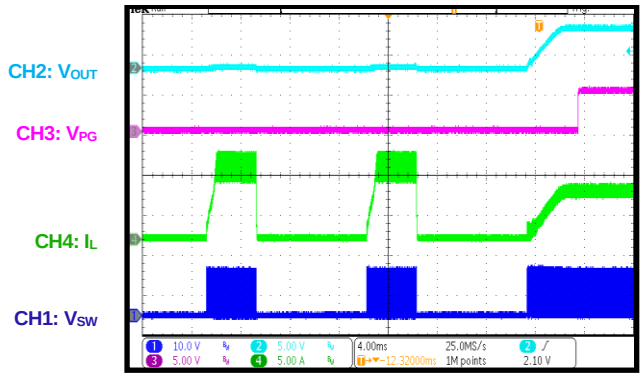
SCP Recovery
I_{OUT} = 0A, AAM mode



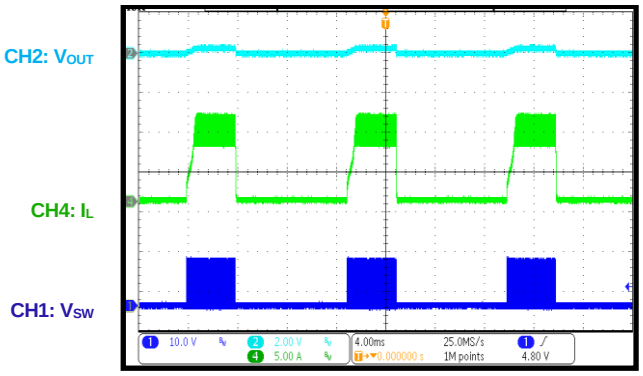
SCP Recovery
I_{OUT} = 0A, FCCM



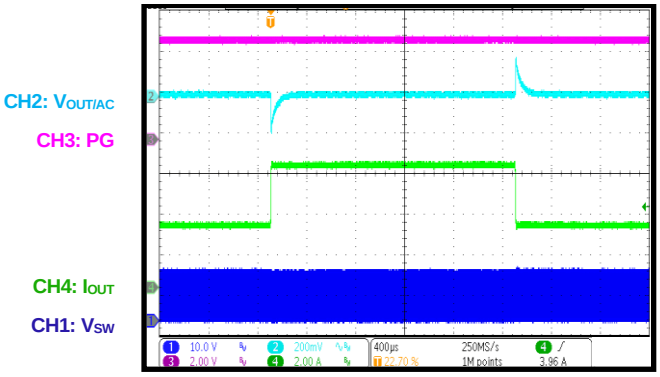
SCP Recovery
I_{OUT} = 6A



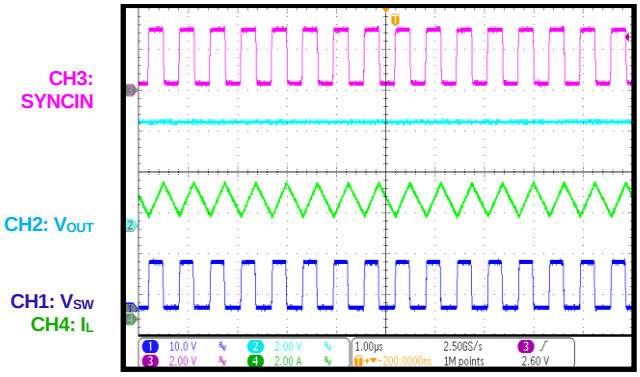
SCP Steady State



Load Transient
I_{OUT} = 3A to 6A, 2A/µs



SYNCIN Operation
I_{OUT} = 6A, SYNC frequency = 1600kHz

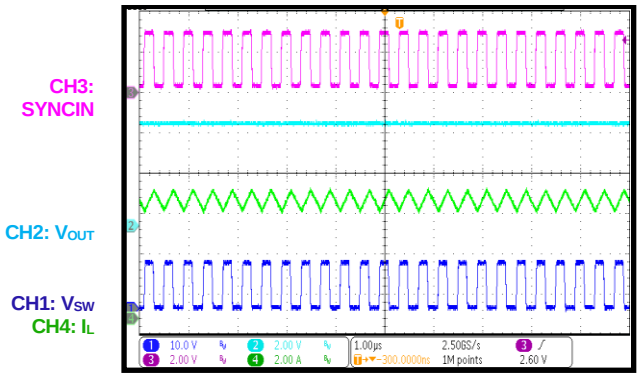


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

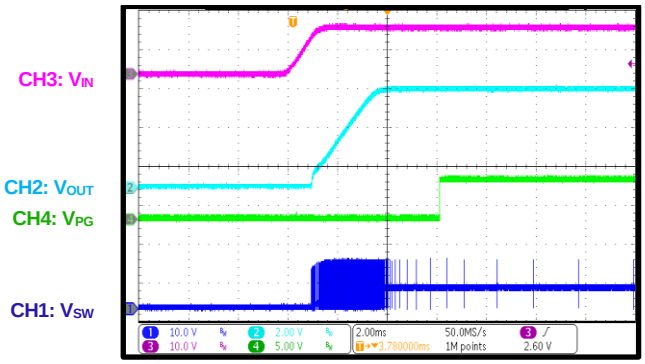
SYNCIN Operation

I_{OUT} = 6A, SYNC frequency = 2500kHz



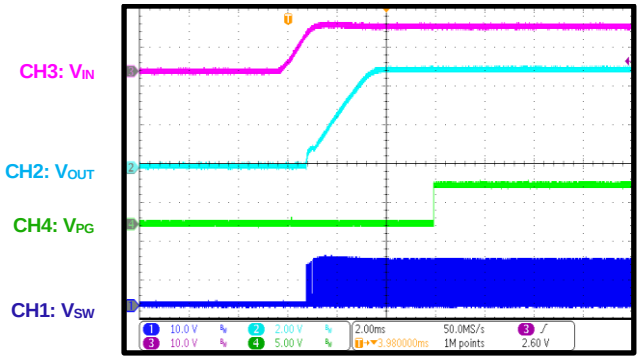
PG in Start-Up through VIN

I_{OUT} = 0A, AAM mode



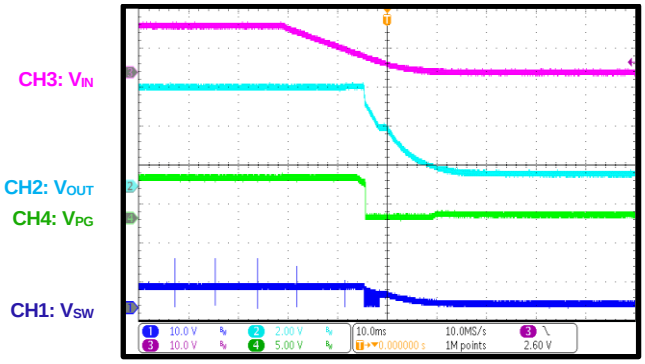
PG in Start-Up through VIN

I_{OUT} = 6A



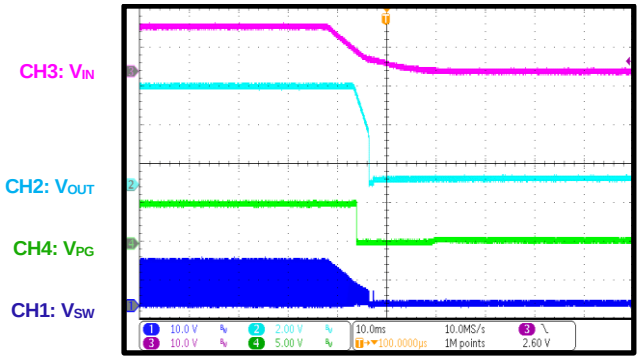
PG in Shutdown through VIN

I_{OUT} = 0A, AAM mode



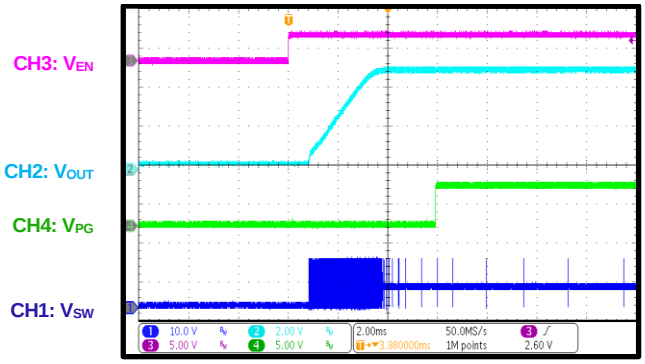
PG in Shutdown through VIN

I_{OUT} = 6A



PG in Start-Up through EN

I_{OUT} = 0A

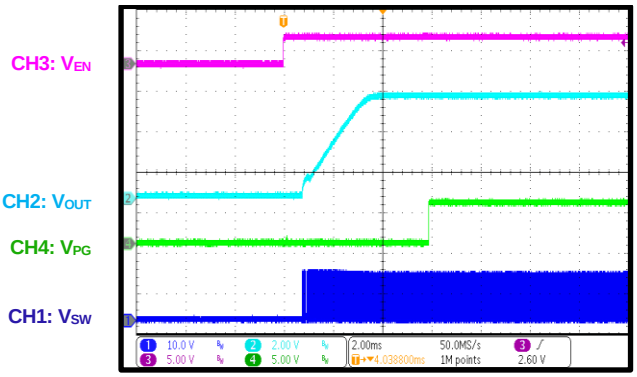


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

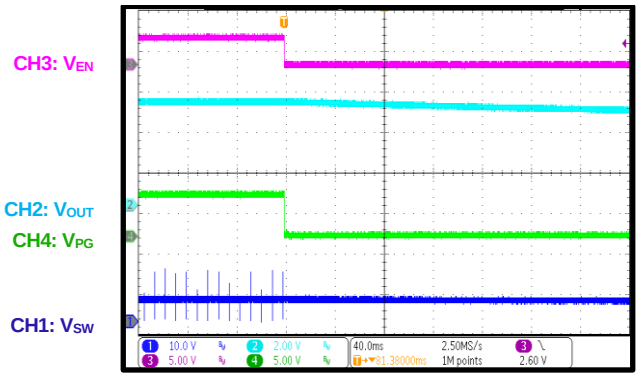
PG in Start-Up through EN

I_{OUT} = 6A



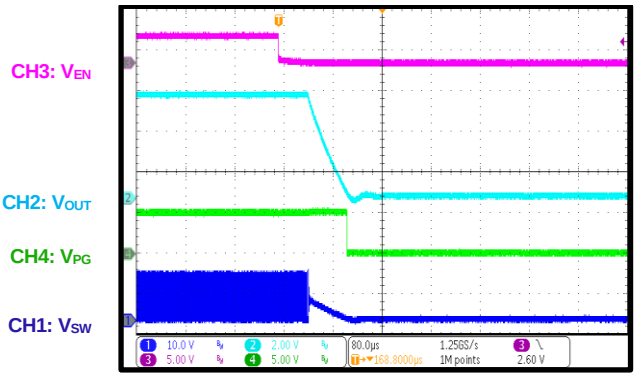
PG in Shutdown through EN

I_{OUT} = 0A



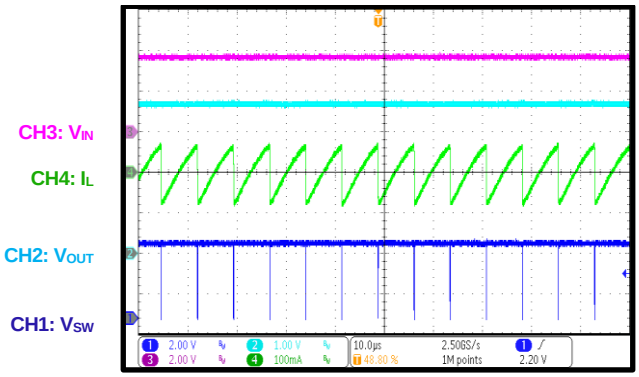
PG in Shutdown through EN

I_{OUT} = 6A



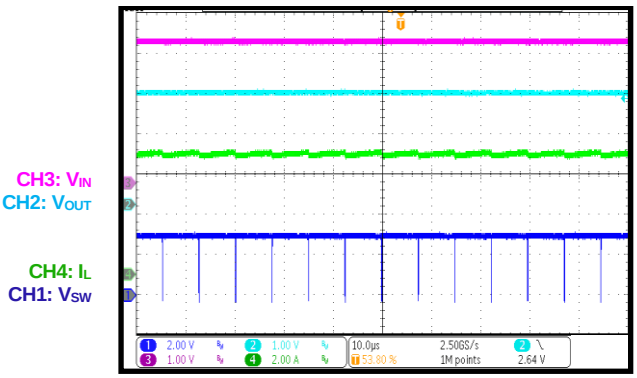
Low-Dropout Mode

V_{IN} = 3.7V, I_{OUT} = 0A



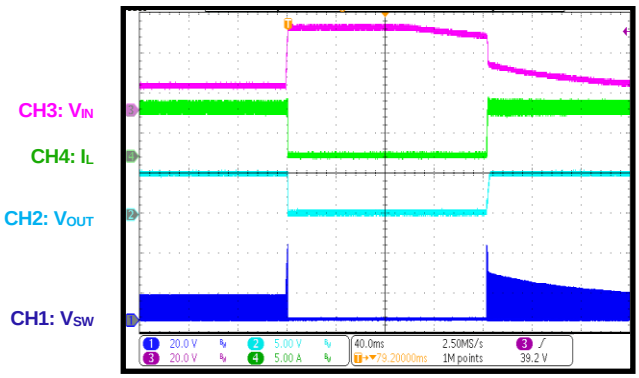
Low-Dropout Mode

V_{IN} = 3.7V, I_{OUT} = 6A



Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 6A

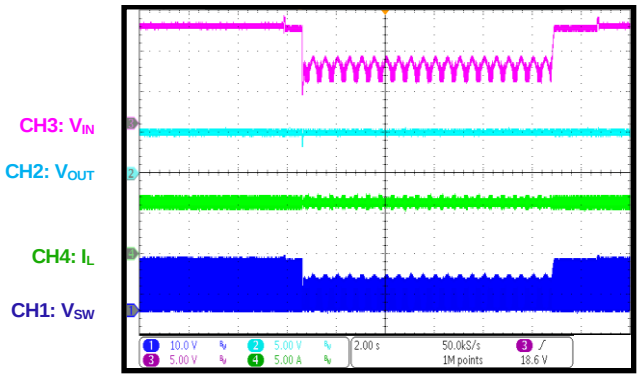


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

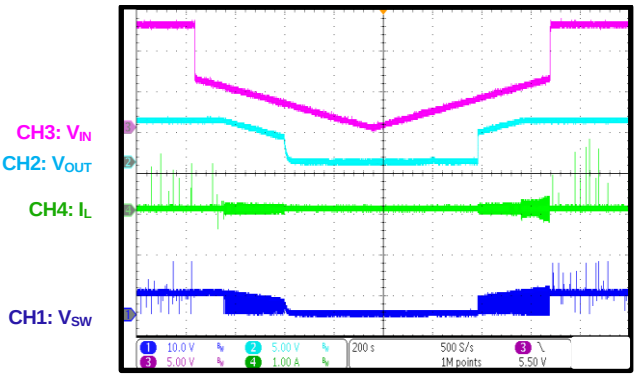
Cold Crank

V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 6A



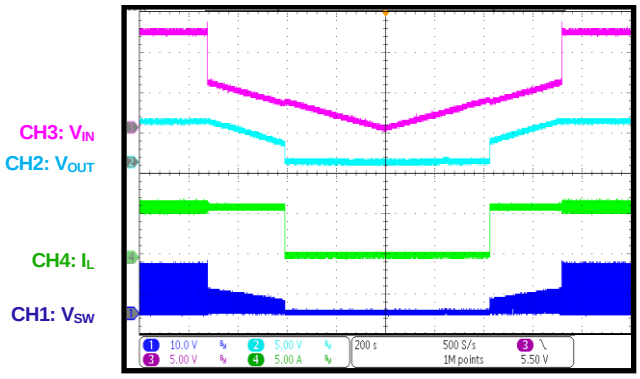
V_{IN} Ramping Down and Up

I_{OUT} = 0A, AAM mode



V_{IN} Ramping Down and Up

I_{OUT} = 6A



FUNCTIONAL BLOCK DIAGRAM

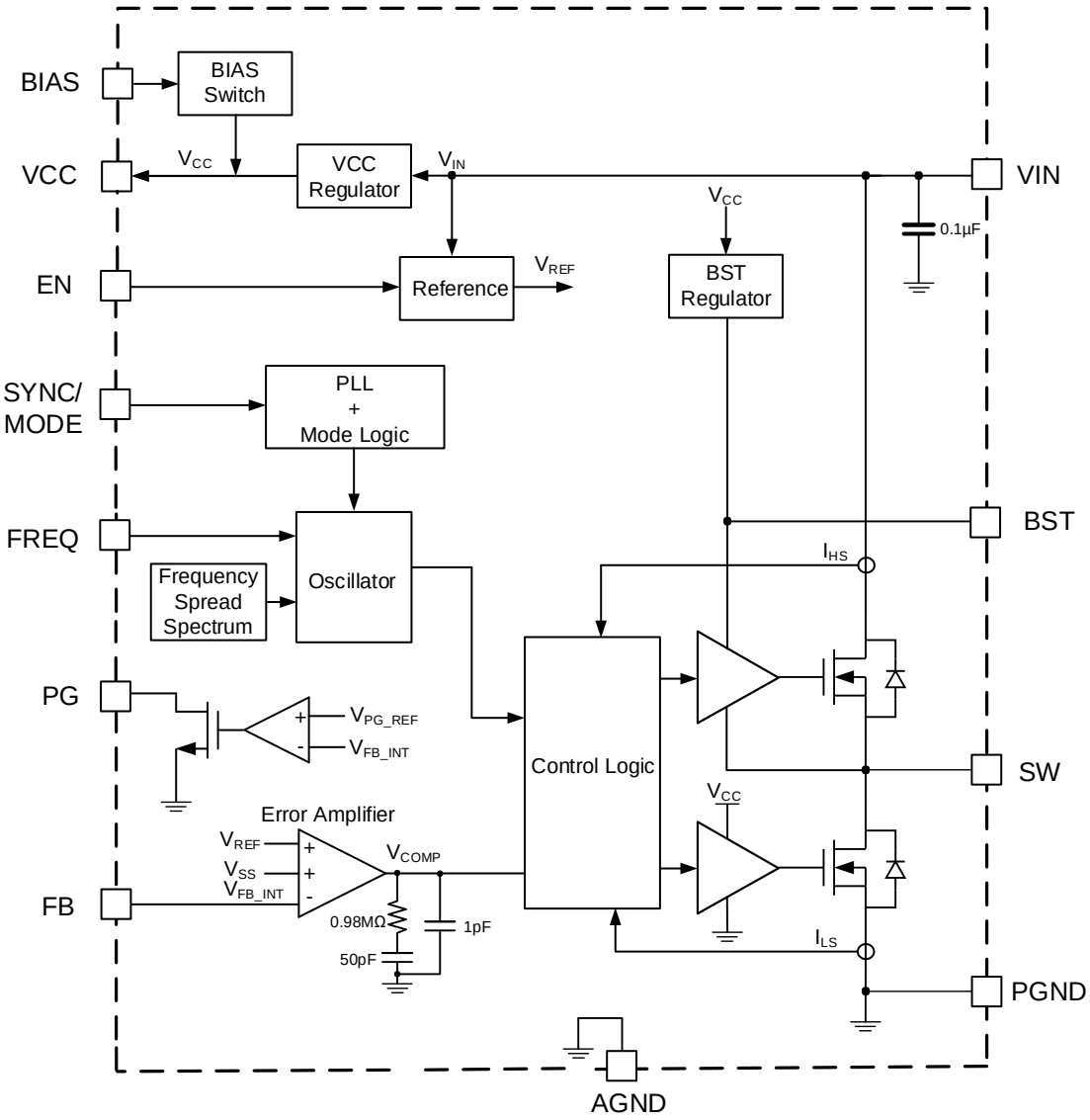


Figure 1: Adjustable-Output Version Functional Block Diagram

FUNCTION BLOCK DIAGRAM *(continued)*

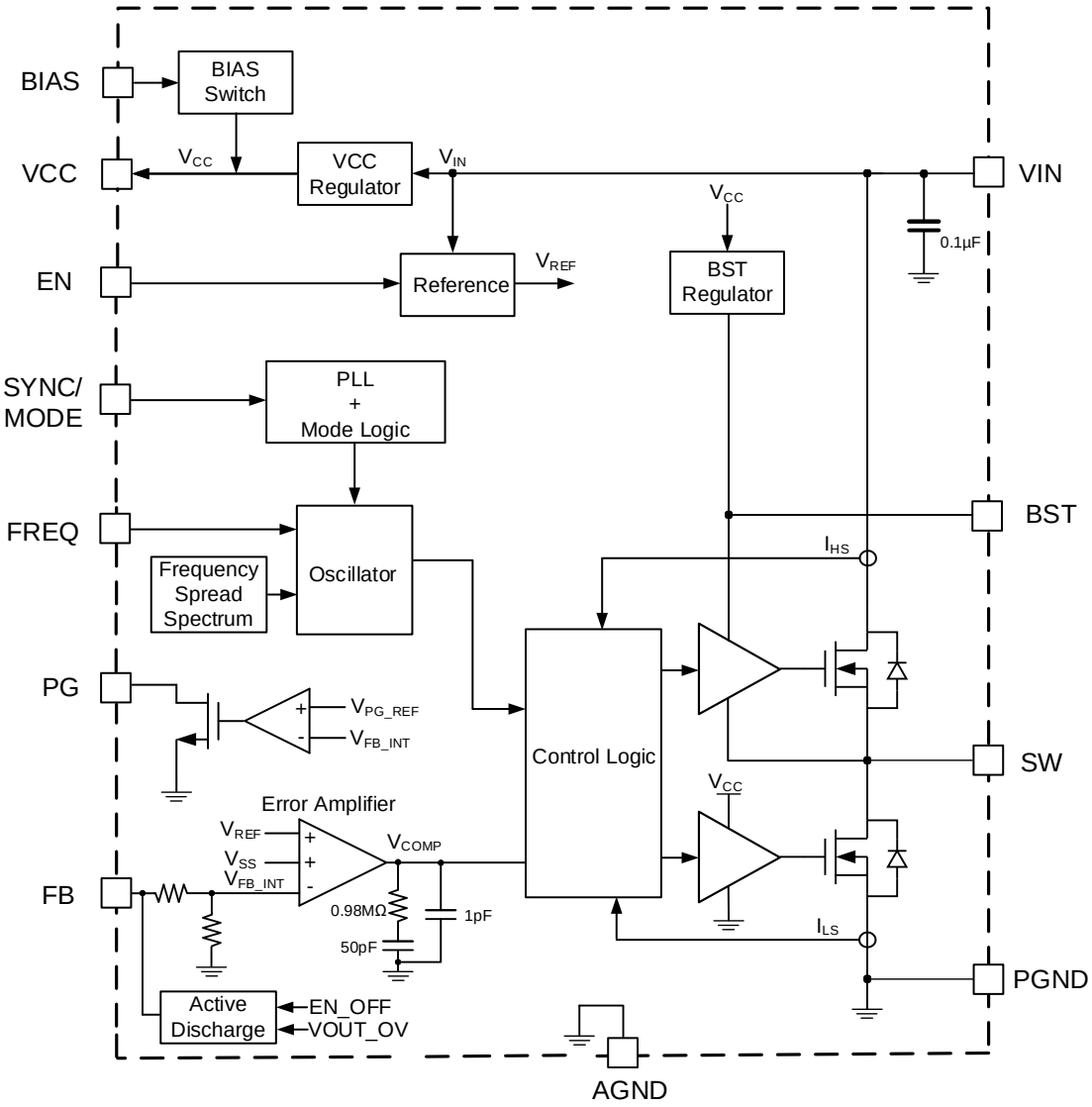


Figure 2: Fixed-Output Version Functional Block Diagram

OPERATION

The MPQ4326M is a synchronous, step-down switching regulator with an integrated, internal high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET). It also includes integrated input capacitors to optimize EMI performance, and provides up to 6A of highly efficient output current (I_{OUT}) with peak current mode control.

The device features wide input voltage (V_{IN}) range, configurable 200kHz to 2.5MHz switching frequency (f_{SW}), internal soft start (SS), and precision current limiting. The MPQ4326M's very low operational quiescent current (I_Q) makes it well-suited for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MPQ4326M operates in fixed-frequency, peak current control mode to regulate the output voltage (V_{OUT}). A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the clock's rising edge, the HS-FET turns on and remains on until the control signal reaches the value set by the internal COMP voltage (V_{COMP}).

When the HS-FET is off, the LS-FET turns on immediately and remains on until the next cycle starts, or until the inductor current (I_L) drops below the zero-current detection (ZCD) threshold. The LS-FET remains off for at least the minimum off time before the next cycle starts.

If the HS-FET current does not reach the value set by COMP within one PWM period, the HS-FET remains on and skips a turn-off operation. The HS-FET is forced off until the current reaches the value set by COMP, or its maximum on time (7µs) is reached. This operation mode extends the duty cycle, which achieves a very low dropout when V_{IN} is almost equal to V_{OUT}.

MODE Selection and Light-Load Operation

The MPQ4326M offers forced continuous conduction mode (FCCM) and advanced asynchronous modulation (AAM) mode, and supports on-the-fly mode selection (see Figure 3).

Under light-load conditions, the MPQ4326M can work in two different operation modes by configuring the SYNC/MODE pin. If SYNC/MODE is pulled above 1.4V or an external clock is used, the MPQ4326M works in FCCM.

In FCCM, the part operates with a fixed frequency across the no-load to full-load range. The advantage of FCCM is the constant frequency and lower output ripple under light loads.

If SYNC/MODE is pulled below 0.4V, the MPQ4326M operates in AAM mode to optimize efficiency under light-load and no-load conditions.

When I_L approaches 0A under light loads, the MPQ4326M enters non-synchronous operation. If the load decreases further and V_{COMP} drops below the set value, the MPQ4326M enters AAM mode. In AAM mode, the internal clock resets every time V_{COMP} crosses the set value, and the crossover time is used as a benchmark for the next clock. When the load increases and V_{COMP} exceeds the set value, the device operates in continuous conduction mode (CCM) or discontinuous conduction mode (DCM) with a constant f_{SW}.

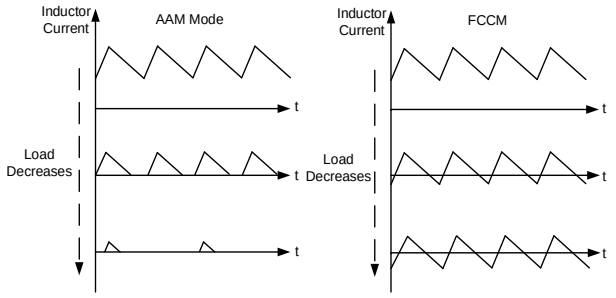


Figure 3: AAM Mode and FCCM

Error Amplifier (EA)

The error amplifier (EA) compares the feedback (FB) voltage (V_{FB}) to the internal reference voltage (V_{REF}, typically 0.8V), and outputs a current proportional to the difference between the two voltages. This current is used to charge the compensation network to form V_{COMP}, which controls the MOSFET's duty cycle.

During normal operation, the minimum V_{COMP} is clamped to 0.9V, and the maximum is clamped to 2V. If the IC shuts down, V_{COMP} is pulled down to ground internally.

Frequency Spread Spectrum (FSS)

The MPQ4326M uses a 7.5kHz modulation frequency with a 128-step triangular profile to spread the internal f_{SW} across a 20% (±10%)

window. The steps vary with f_{SW} to ensure that the exact f_{SW} steps cycle by cycle (see Figure 4).

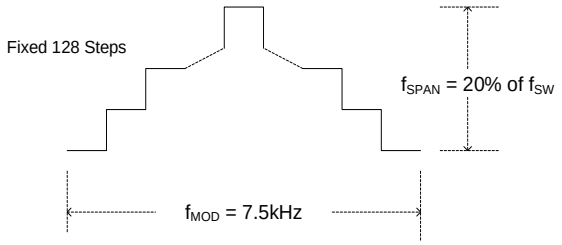


Figure 4: Frequency Spread Spectrum

Side bands are created by modulating f_{SW} via the triangle modulation waveform. The emission power of the fundamental f_{SW} and its harmonics are distributed into smaller pieces, which significantly reduces the peak EMI noise.

Low-Dropout Mode

To improve dropout, the MPQ4326M is designed to operate at close to a 100% duty cycle as long as the BST-to-SW voltage (V_{BST-SW}) is above 2.7V.

When the part exits low-dropout mode, the part reinitiates soft start (SS) to avoid V_{COMP} becoming too large during this period. Even when operating with a quickly rising V_{IN}, there are no large inductor spikes.

The duty cycle during the dropout period is mainly influenced by the voltage drops across the MOSFET, the inductor resistance, the low-side diode, and the PCB resistance.

Soft Start (SS)

Soft start (SS) is implemented to prevent V_{OUT} from overshooting during start-up. The soft-start time (t_{SS}) is fixed internally.

Once SS is initiated, the soft-start voltage (V_{SS}) rises from 0V to 1.2V with a set slew rate. If V_{SS} drops below the internal V_{REF} (0.8V), then V_{SS} takes over and the EA uses V_{SS} as its reference. If V_{SS} exceeds V_{REF}, the EA uses V_{REF} as its reference.

During SS time, the MPQ4326M operates in AAM mode regardless of the MODE setting for a smooth start-up.

During start-up through EN, the first pulse occurs after about 710µs. During this period, the VCC voltage (V_{CC}) is regulated, the internal bias is generated, and the compensation network is charged. After another 2.9ms, V_{OUT} ramps up and reaches its set value. SS is complete after another 2.3ms. PG is also pulled high after a 160µs deglitch time.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} during start-up (V_{FB} > V_{SS} - 150mV), this means that the output has a pre-biased voltage. The HS-FET and LS-FET both remain off until V_{SS} exceeds V_{FB}.

V_{IN} Over-Voltage Protection (OVP)

The MPQ4326M can operate across a wide V_{IN} range, up to 36V. If V_{IN} exceeds its over-voltage (OV) rising threshold (typically) 38V, the part stops switching. Once V_{IN} drops back to the OV falling threshold (typical 37V), it resumes normal operation. This allows the MPQ4326M to handle load dumps up to 42V.

Thermal Shutdown

Thermal shutdown prevents the device from operating at exceedingly high temperatures and protects it from thermal runaway. If the die temperature exceeds its upper threshold (about 170°C), the device shuts down, including the MOSFETs. Once the temperature drops below 150°C, the device restarts and resumes normal operation.

Start-Up and Shutdown

If both V_{IN} and the EN voltage (V_{EN}) exceed their respective thresholds, the IC starts up. The reference block starts up first to generate a stable V_{REF} and reference currents. Then the internal regulator is enabled to provide a stable supply for the remaining circuitries.

If the voltage between BST and SW (V_{BST-SW}) has not exceeded the BST refresh rising threshold (typically 2.7V) once the internal supply rail is up, the LS-FET turns on to charge V_{BST}. The HS-FET remains off during this time. When the soft-start block is enabled, V_{SS} is held low to ensure that the remaining circuits are ready, then slowly ramps up.

Three events can shut down the chip: EN going low, V_{IN} falling below its UVLO threshold, and thermal shutdown. During shutdown, the signaling path is blocked first to avoid any fault triggering. Then V_{COMP} is pulled down and the floating driver disables the HS-FET.

APPLICATION INFORMATION

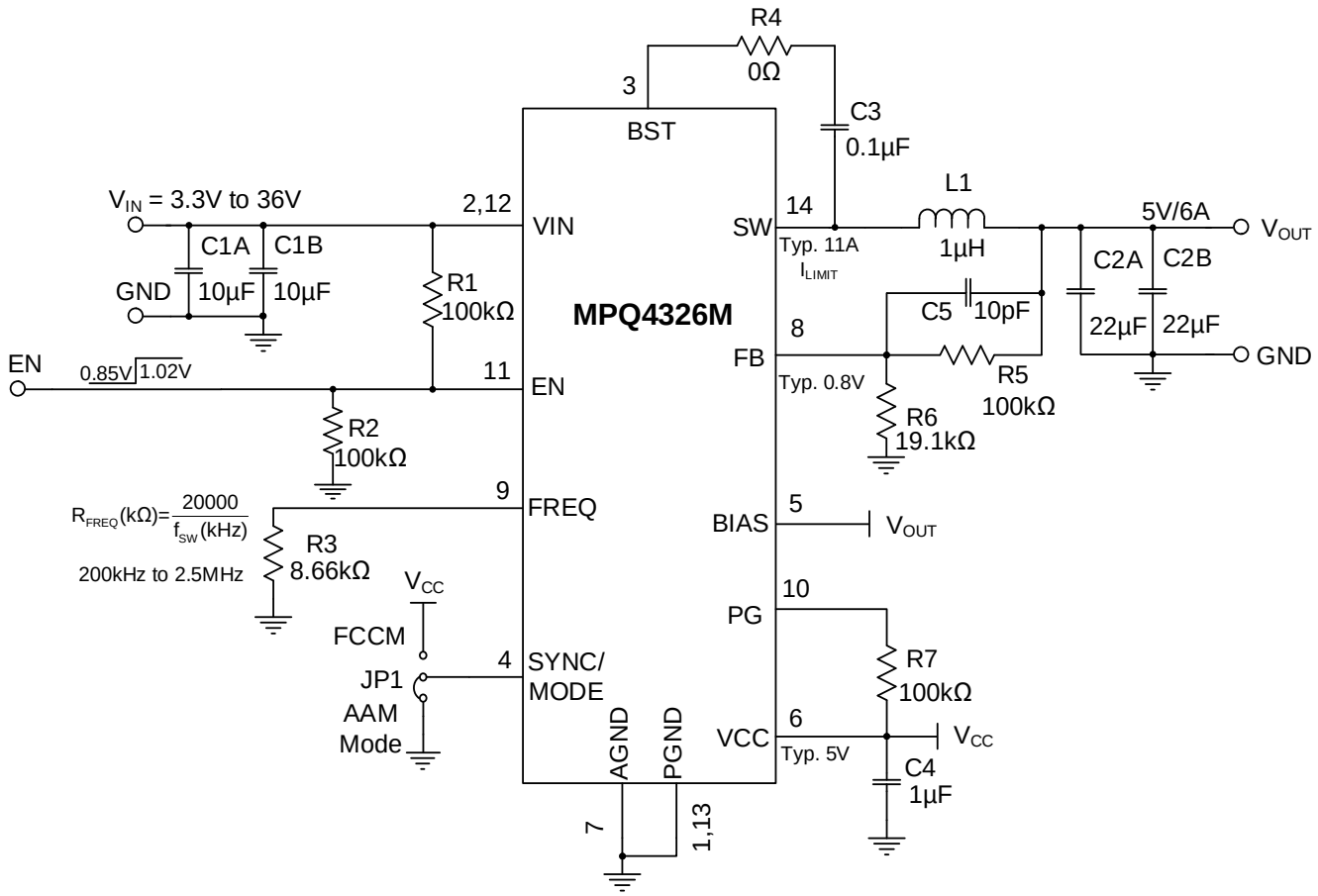


Figure 5: Typical Application Circuit for the MPQ4326M (V_{OUT} = 5V, f_{SW} = 2.2MHz)

Table 1: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
1, 13	PGND	-	GND Connection (Pins 1, 7, 13)
2, 12	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitors (VIN, Pins 2 and 12)
3	BST	R4, C3	Floating Driver and Bootstrap Charging (BST, Pin 3)
4	SYNC/MODE	-	SYNC Input and MODE Selection (SYNC/MODE, Pin 4)
5	BIAS	-	Setting the External Bias for Low Quiescent Current (BIAS, Pin 5)
6	VCC	C4	Input Bias Supply (VCC, Pin 6)
7	AGND	-	GND Connection (Pins 1, 7, 13)
8	FB	R5, R6, C5	Feedback (FB, Pin 8)
9	FREQ	R3	Setting the Switching Frequency (FREQ, Pin 9)
10	PG	R7	Power Good (PG) Indicator (PG, Pin 10)
11	EN	R1, R2	Enable and Under-Voltage Lockout (UVLO) (EN, Pin 11)
14	SW	L1, C2A, C2B	Selecting the Inductor (SW, Pin 14) Selecting the Output Capacitors (SW, Pin 14)

GND Connection (Pins 1, 7, 13)

See the PCB Layout Guidelines section on page 41 for more details.

Selecting the Input Capacitors (VIN, Pins 2 and 12)

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 4.7µF to 10µF capacitor is sufficient.

The MPQ4326M has two integrated 0.1µF, 0603 package capacitors between VIN and PGND, which help absorb high-frequency switching noise and optimize EMI performance.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in C_{IN} (I_{CIN}) can be estimated with Equation (1):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (1)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (2):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (2)$$

For simplification, choose an input capacitor with maximum load current (I_{LOAD_MAX}). C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (3):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Floating Driver and Bootstrap Charging (BST, Pin 3)

The bootstrap capacitor (C3, also called C_{BST}) is recommended to be between 0.1nF and 0.22nF.

It is not recommended to place a resistor (R_{BST}) in series with C_{BST}, unless there is a strict EMI requirement. R_{BST} reduces EMI and voltage stress at high input voltages. A higher resistance is better for switching spike reduction, but compromises efficiency. When R_{BST} is necessary, it should be less than 5Ω.

The voltage between the BST and SW pins (V_{BST-SW}) is regulated to about 5V by the dedicated internal bootstrap regulator. If V_{BST-SW} falls below its regulated value, an N-channel MOSFET pass transistor connected between VCC and BST turns on to charge C_{BST}. The external circuit should provide enough voltage headroom to facilitate charging.

When the HS-FET is on, V_{BST} is higher than V_{CC}, so C_{BST} cannot charge. At higher duty cycles, the time available for BST charging is shorter, so C_{BST} may not charge sufficiently. If the external circuit has an insufficient voltage and time to charge C_{BST}, additional external circuitry can be used to ensure that V_{BST} remains within its normal operating range.

If V_{BST} falls below its UVLO threshold, then the HS-FET turns off and the LS-FET turns on for t_{OFF_MIN} to refresh V_{BST} via the set f_{SW}.

SYNC Input and Mode Selection (SYNC/MODE, Pin 4)

f_{SW} can be synchronized to the rising edge of a clock signal applied at SYNCIN. The recommended SYNCIN frequency range is 200kHz to 2.5MHz.

The MPQ4326M's switching can be synchronized to an external clock within a SCYNCIN clock locking time (128 cycles), ranging from ±10% of the setting clock frequency.

When this pin is used for mode selection, pull it high to force the part to operate in FCCM; pull it low to force the part operate in AAM mode. Table 2 on page 38 shows the detailed mode selection information.

Table 2: Mode Selection

SYNC/MODE Input	Operation Mode
<0.4V	AAM mode
>1.4V	FCCM
External clock in	FCCM

Setting the External Bias for Low Quiescent Current (BIAS, Pin 5)

The BIAS pin is the external bias pin. When this pin is connected to 5V, the internal LDO turns off, and the input supply current can be reduced to achieve higher efficiency. When the BIAS voltage (V_{BIAS}) exceeds 4.6V, BIAS starts working. When V_{BIAS} is below 4.36V, BIAS is disabled. For the 5V output version of the MPQ4326M, connect BIAS directly to V_{OUT}. For other lower (<4.6V) or higher (>6V) output versions, connect BIAS to the external 5V source for a lower input supply current, or connect BIAS to ground to turn off the bias function. When using an external V_{BIAS}, ensure that V_{IN} is supplied before providing V_{BIAS}.

Internal VCC (VCC, Pin 6)

The VCC capacitance (C4) is recommended to be 1µF. Most of the internal circuitry is powered by the internal, 5V VCC regulator. This regulator uses V_{IN} as its input and operates across the entire V_{IN} range. If V_{IN} exceeds 5V, then V_{CC} is in full regulation. If V_{IN} drops below 5V, then V_{CC} degrades.

Feedback (FB, Pin 8)

For the adjustable-output version, the typical feedback voltage (V_{FB}) is 0.8V. The external resistor dividers (R6 and R5) connected to FB set V_{OUT} (see Figure 6).

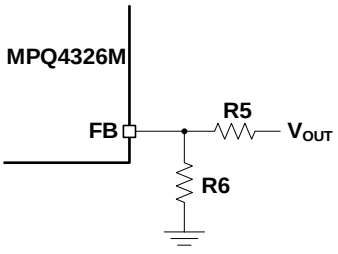


Figure 6: Feedback Divider Network for Adjustable-Output Version

Calculate the value of R6 with Equation (4):

$$R6 = \frac{R5}{\frac{V_{OUT}}{0.8V} - 1} \quad (4)$$

Table 3 lists the recommended feedback resistor values for common output voltages.

Table 3: Resistor Selection for Output Voltages

V_{OUT} (V)	R5 (kΩ)	R6 (kΩ)
3.3	100 (0.1%)	31.6 (0.1%)
5	100 (0.1%)	19.1 (0.1%)

For the fixed-output version, the FB resistor dividers (R_{FB1} and R_{FB2}) are integrated internally (see Figure 7). Connect FB directly to V_{OUT} to set V_{OUT}. The following fixed outputs can be selected: 1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, or 5V.

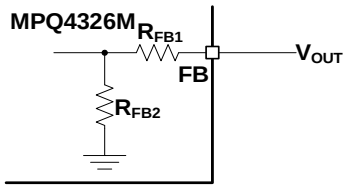


Figure 7: Feedback Divider Network for Fixed-Output Version

Table 4 shows the relationship between the internal R_{FB} and V_{OUT}.

Table 4: R_{FB} vs. V_{OUT}

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
1	64	256
1.8	320	256
2.5	544	256
3	704	256
3.3	800	256
3.8	960	256
5	1344	256

Setting the Switching Frequency (FREQ, Pin 9)

A frequency resistor (R3, also called R_{FREQ}) can be used to set the MPQ4326M's internal f_{SW} (see Figure 8 and Figure 9 on page 39).

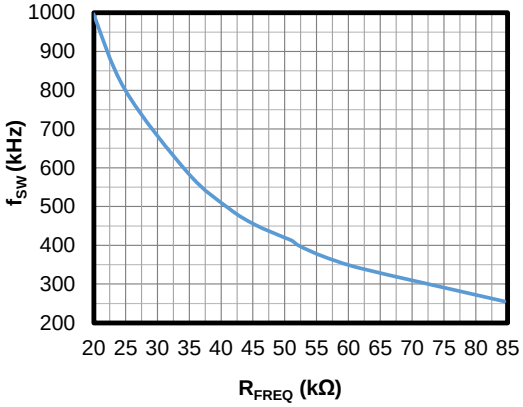


Figure 8: f_{SW} vs. R_{FREQ} (200kHz to 1000kHz)

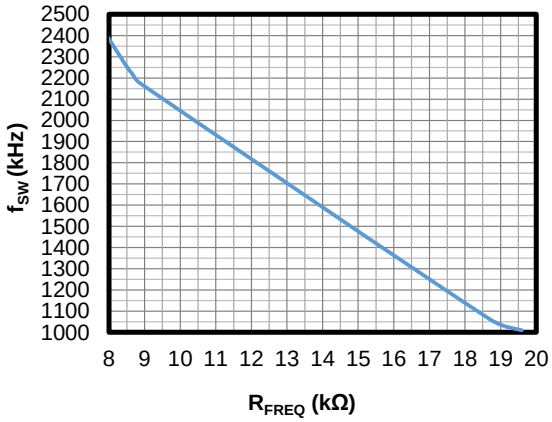


Figure 8: f_{SW} vs. R_{FREQ} (1000kHz-2500kHz)

Table 5 lists some common frequency to frequency resistor relationships as a quick reference for selecting f_{SW}.

Table 5: f_{SW} vs. R_{FREQ}

R_{FREQ} (kΩ)	f_{SW} (kHz)
7.87	2500
8.66	2200
14.3	1500
18.7	1060
19.6	1000
24.9	800
34.8	590
43.2	470
49.9	410
52.3	400
56.2	370
62	340
84.5	255
100	210

Power Good (PG) Indicator (PG, Pin 10)

The PG resistor (R7, also called R_{PG}) should have a resistance of about 100kΩ.

The MPQ4326M includes an open-drain power good (PG) output that indicates whether V_{OUT} is within its nominal range.

If using PG, connect it to a logic high power source via a pull-up resistor. If V_{OUT} is within 94.5% to 105.5% of the nominal voltage, PG goes high. if V_{OUT} is above 107% or below 93% of the nominal voltage, PG goes low. Float PG if it is not used.

Enable and Under-Voltage Lockout (UVLO) (EN, Pin 11)

The EN pin is a digital control pin that turns the regulator on and off.

Enabled by an External Logic High/Low Signal

If the EN voltage (V_{EN}) reaches 0.7V, the bandgap (BG) does not turn on until V_{IN} exceeds 2.7V. BG then provides an accurate reference voltage for the EN threshold. Pull EN above its rising threshold (about 1.02V) to enable the device. Pull EN below 0.85V to shut down the device.

There is no internal pull-up or pull-down resistor connected to the EN pin. Do not float EN. If the control signal cannot give an accurate high or low logic, an external pull-up or pull-down resistor is required.

Configurable V_{IN} Under-Voltage Lockout (UVLO) Threshold

The MPQ4326M has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3.7V, and the falling threshold is about 2.9V. For applications that require a higher UVLO point, place an external resistor divider between VIN and EN can be used to raise the equivalent UVLO threshold (see Figure 9).

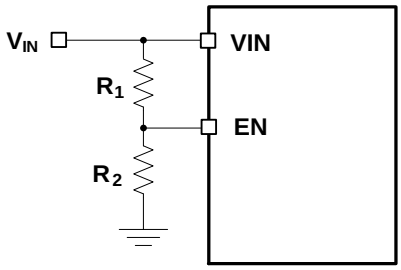


Figure 9: Adjustable UVLO Using EN Divider

The UVLO rising threshold ($V_{IN\_UVLO\_RISING}$) can be calculated with Equation (5):

$$V_{IN\_UVLO\_RISING} = (1+\frac{R_1}{R_2}) \times V_{EN\_RISING} \quad (5)$$

Where V_{EN_RISING} is 1.02V.

The UVLO falling threshold ($V_{IN\_UVLO\_FALLNG}$) can be calculated with Equation (6):

$$V_{IN\_UVLO\_FALLING} = (1+\frac{R_1}{R_2}) \times V_{EN\_FALLING} \quad (6)$$

Where $V_{EN\_FALLING}$ is 0.85V.

If EN is not used to turn the IC on and off, connect EN to a high-voltage source (e.g. VIN) to turn the device on by default.

Selecting the Inductor (SW, Pin 14)

The inductance (L) can be estimated with Equation (7):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

A 1µH to 10µH inductor with a DC current rating at least 25% greater than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage; however, it also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current.

The peak inductor current (I_{L_PEAK}) can be calculated with Equation (8):

$$I_{L\_PEAK} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Choose an inductor that does not saturate under I_{L_PEAK}.

The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor (C_{OUT}).

Selecting the Output Capacitors (SW, Pin 14)

The output capacitor (C_{OUT}) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep ΔV_{OUT} low.

For ceramic capacitors**,** the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, the output voltage ripple (ΔV_{OUT}) can be calculated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

When selecting C_{OUT}, consider the allowable overshoot in V_{OUT} if the load is suddenly removed. In this scenario, energy stored in the inductor is transferred to C_{OUT}, causing its voltage to rise. To achieve an optimal overshoot relative to the regulated voltage, C_{OUT} can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^2 \times L}{V_{OUT}^2 \times ((V_{OUT\_MAX} / V_{OUT})^2 - 1)} \quad (12)$$

Where V_{OUT_MAX} / V_{OUT} is the maximum allowable overshoot.

After calculating the capacitance that meets both the ripple and overshoot requirements, choose the larger capacitance. The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4326M can be optimized for a wide range of capacitances and ESR values.

Peak and Valley Current Limits

Both the HS-FET and LS-FET feature cycle-by-cycle current-limit protection. If the inductor current (I_L) reaches the high-side (HS) peak current limit (typically 11A) while the HS-FET is on, then the HS-FET is forced off immediately to prevent the current from rising further.

When the LS-FET is on, the next clock's rising edge is held until I_L drops below the low-side (LS) valley current limit (typically 7.5A). This allows I_L to drop to a sufficiently low value when the HS-FET turns on again. This current limit scheme prevents current runaway if an overload or short-circuit event occurs.

Short-Circuit Protection (SCP)

If the output is shorted to ground and V_{OUT} drops below 70% of its nominal value, then the MPQ4326M shuts down and begins discharging V_{SS}. Once V_{SS} is fully discharged, the device restarts with a full SS. This hiccup process repeats until the fault is removed. If V_{FB} reaches 50% of V_{REF} during the hiccup time, the part triggers SCP recovery, and restarts with SS to

prevent large voltage and current spikes. When applying SCP function, V_{IN} is recommended to be lower than 24V.

Output Over-Voltage Protection (OVP) and Discharge

If V_{OUT} exceeds 130% of its nominal voltage, the MPQ4326M stops switching. An internal 75Ω discharge path from FB to AGND discharges V_{OUT}. This discharge path is only active for the fixed-output version. Once V_{OUT} drops below 125% of its nominal voltage, the discharge path is disabled and the part resumes normal operation.

For the fixed-output version, the V_{OUT} discharge path is also activated if a shutdown through EN occurs. Once V_{CC} drops to its UVLO threshold, this path is deactivated.

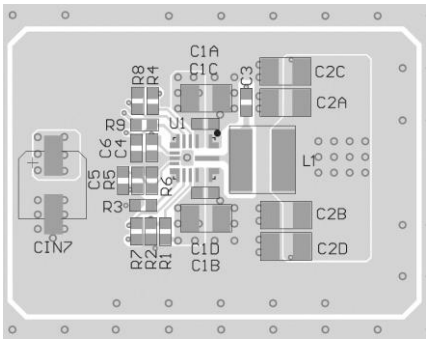
PCB Layout Guidelines (15)

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to achieve better thermal performance. For the best results, refer to Figure 10 and follow the guidelines below:

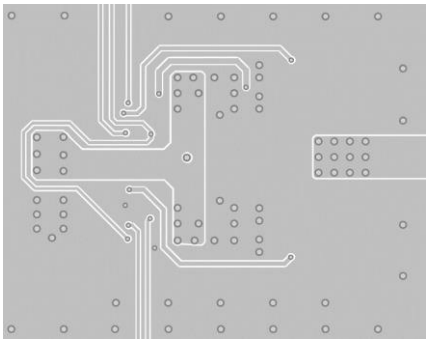
1. Place the symmetric input capacitors as close to VIN and PGND as possible.
2. Connect a large ground plane directly to PGND.
3. If the bottom layer is a ground plane, add vias near PGND.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Keep the connection between the input capacitor and VIN as short and wide as possible.
6. Place the VCC capacitor as close to VCC and AGND as possible.
7. Route SW and BST away from sensitive analog areas, such as FB.
8. Reduce SW node routing size for better EMI.
9. Place the feedback resistors close to the chip to ensure the trace that connects to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

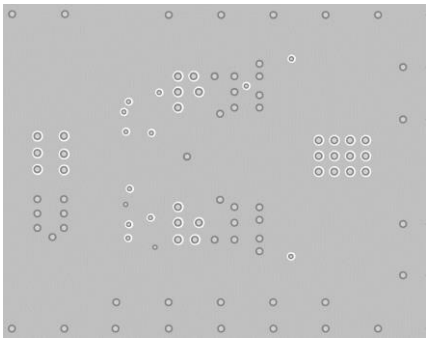
15) The recommended PCB layout is based on Figure 11 on page 42.



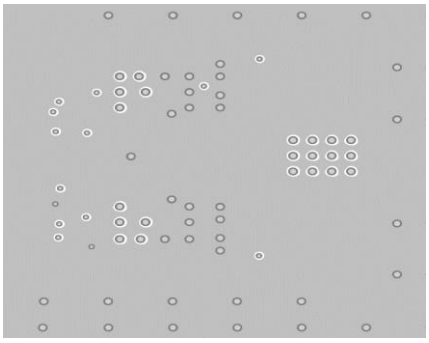
Top Layer



Mid-Layer 2



Mid-Layer 1



Bottom Layer

Figure 10: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

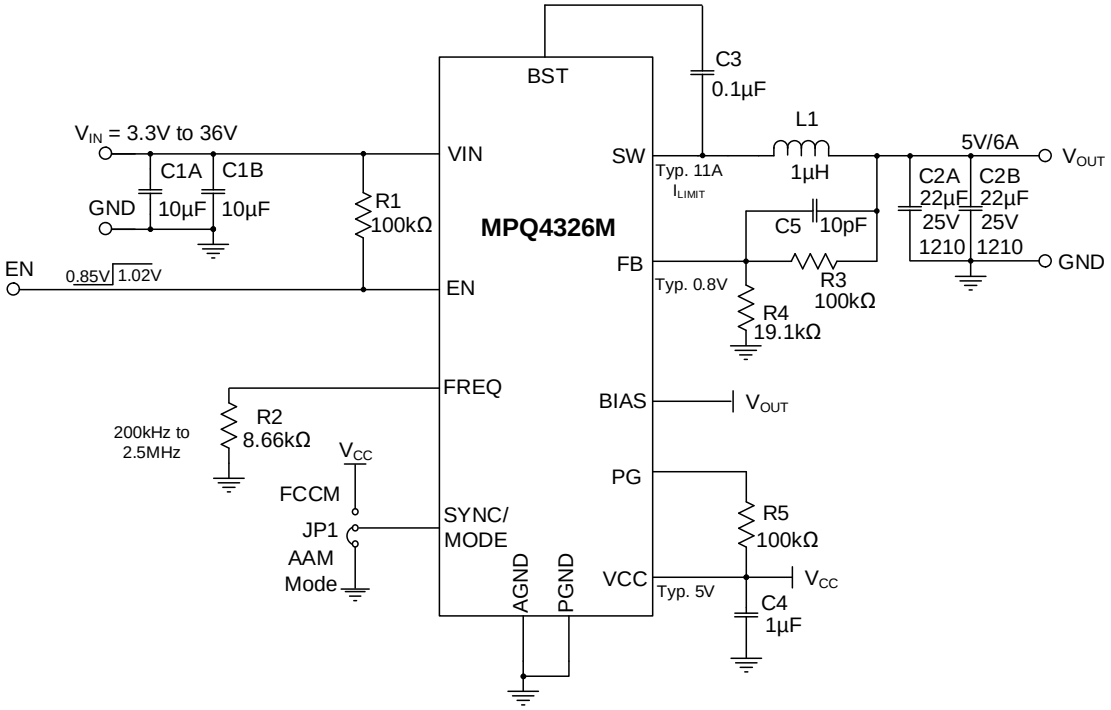


Figure 11: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz)

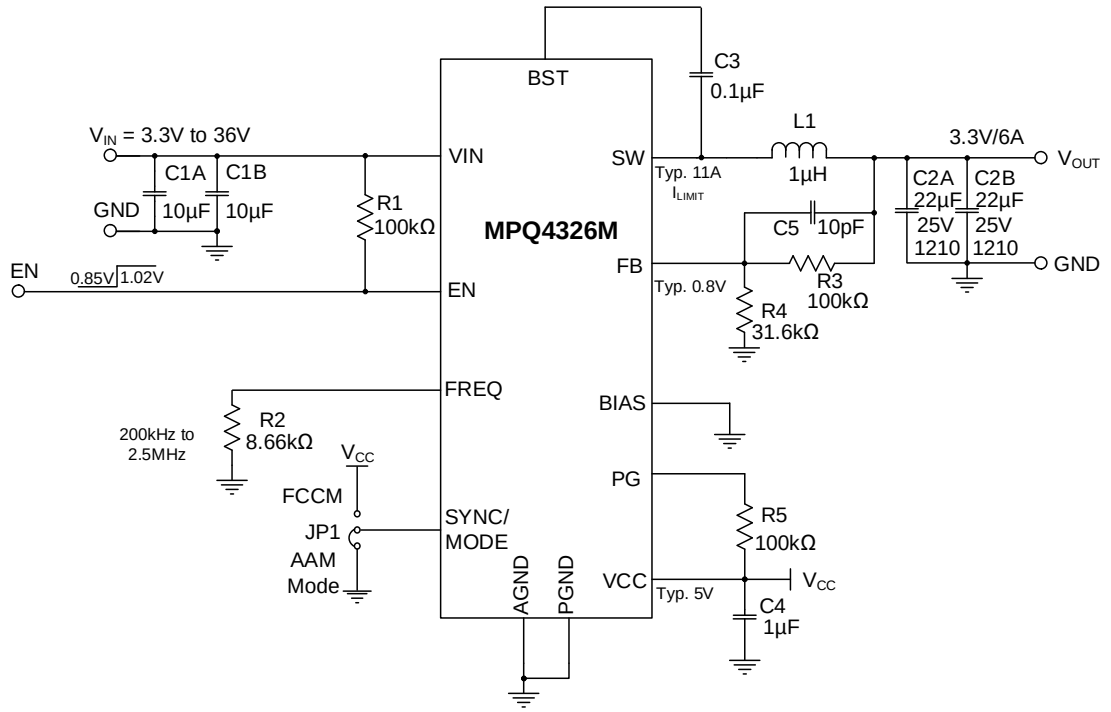


Figure 12: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 2.2MHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

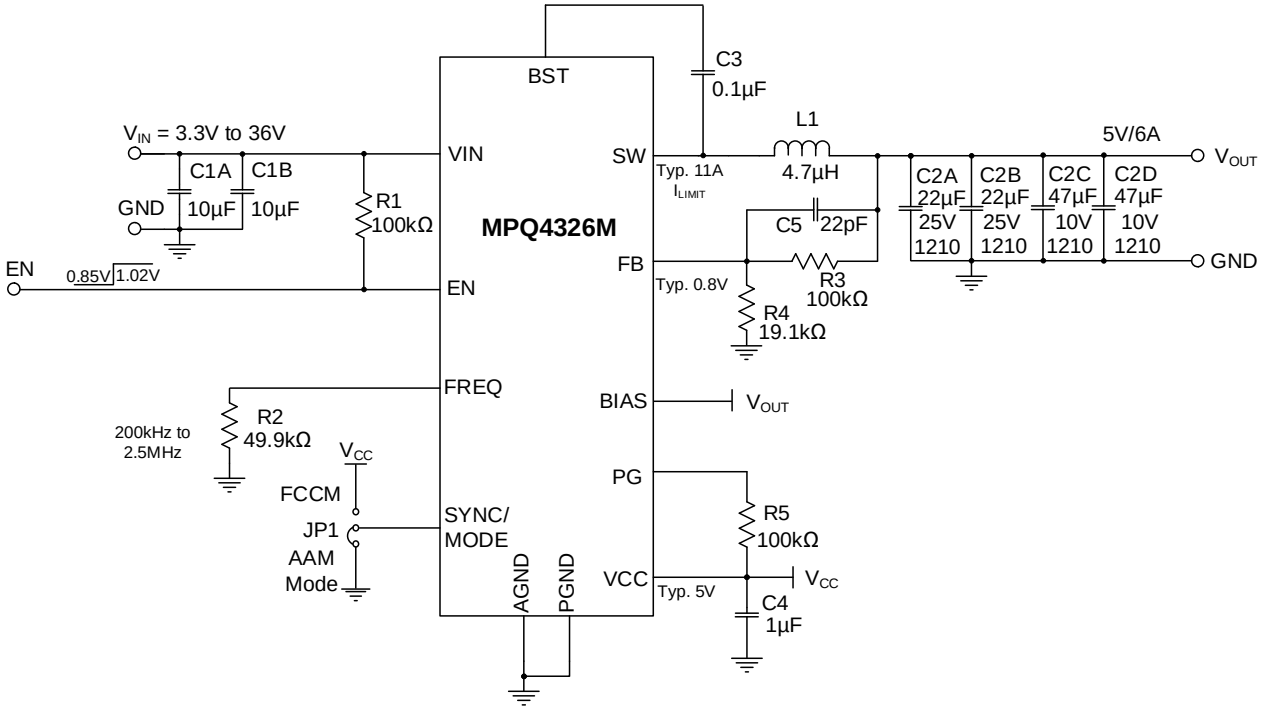


Figure 13: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 410kHz)

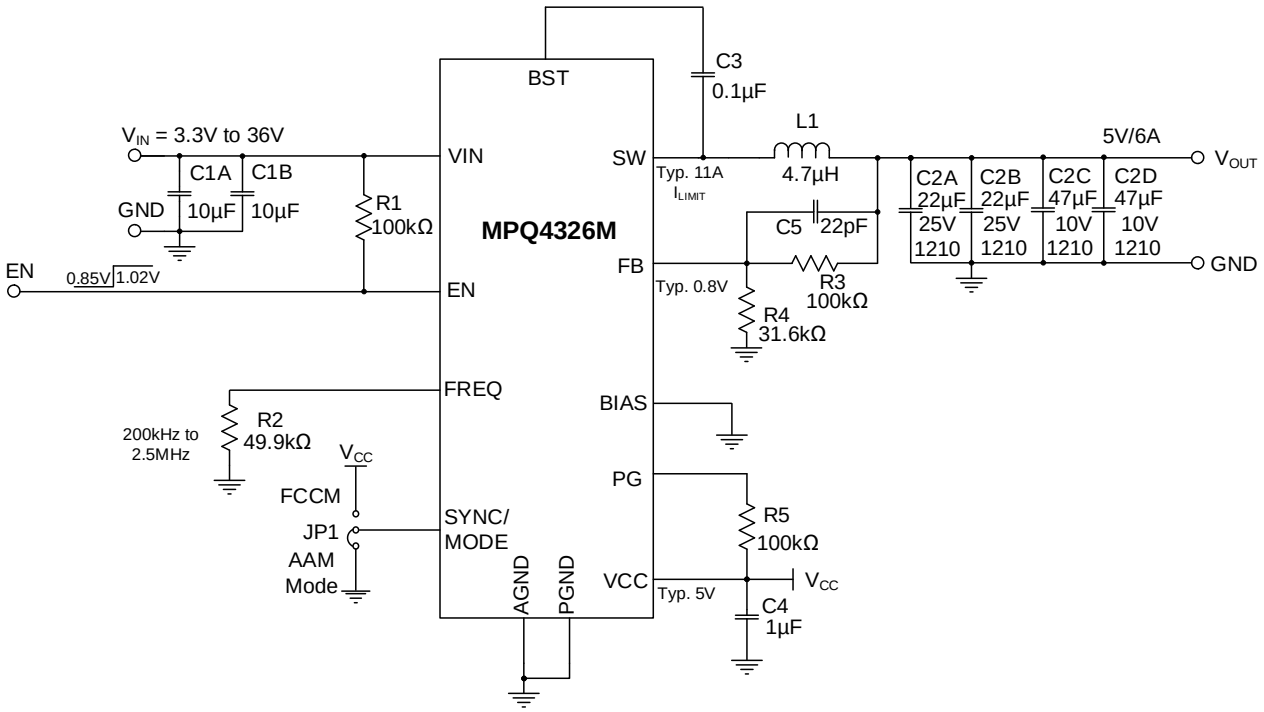


Figure 14: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 410kHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

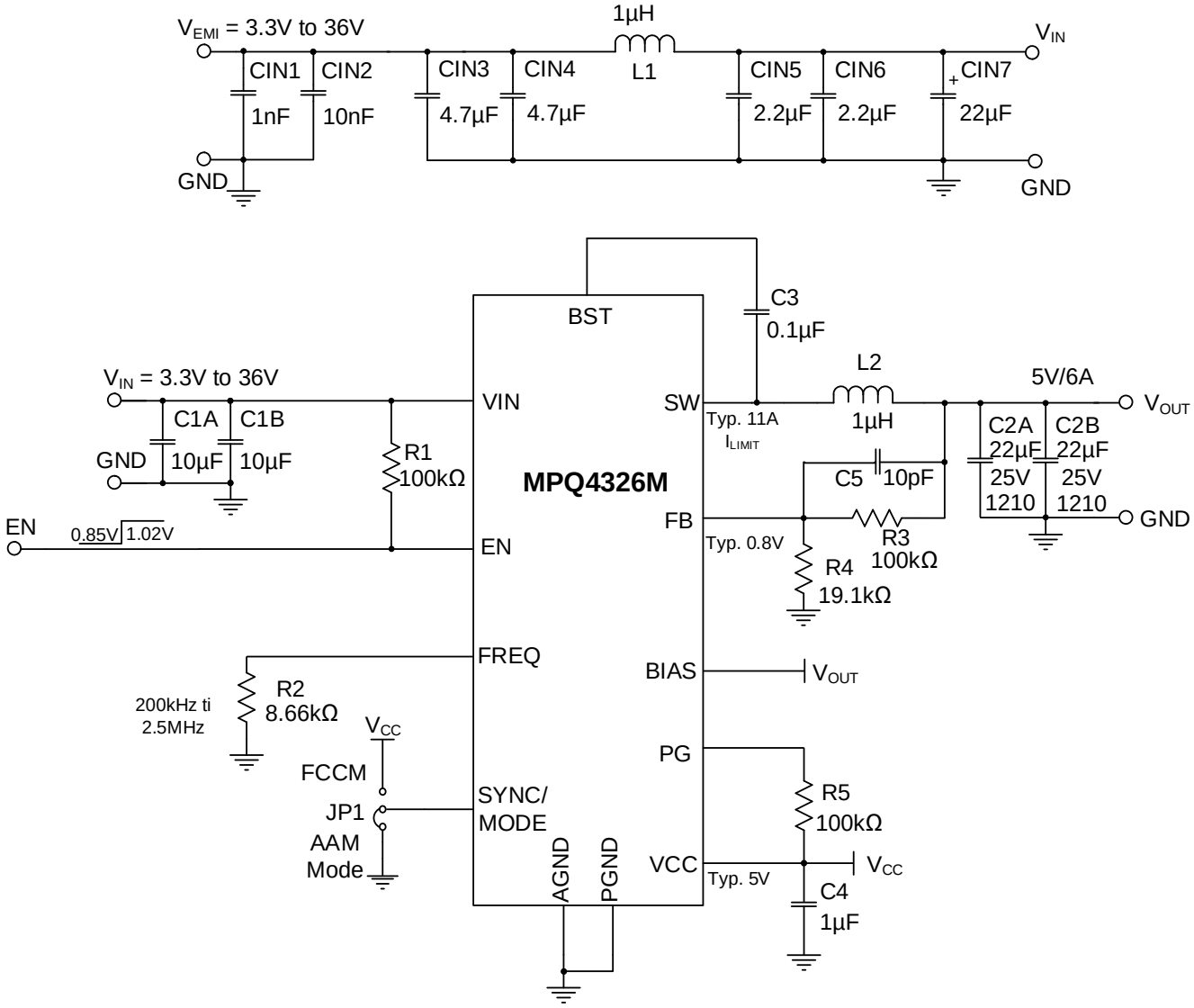


Figure 15: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz with EMI Filters)

TYPICAL APPLICATION CIRCUITS *(continued)*

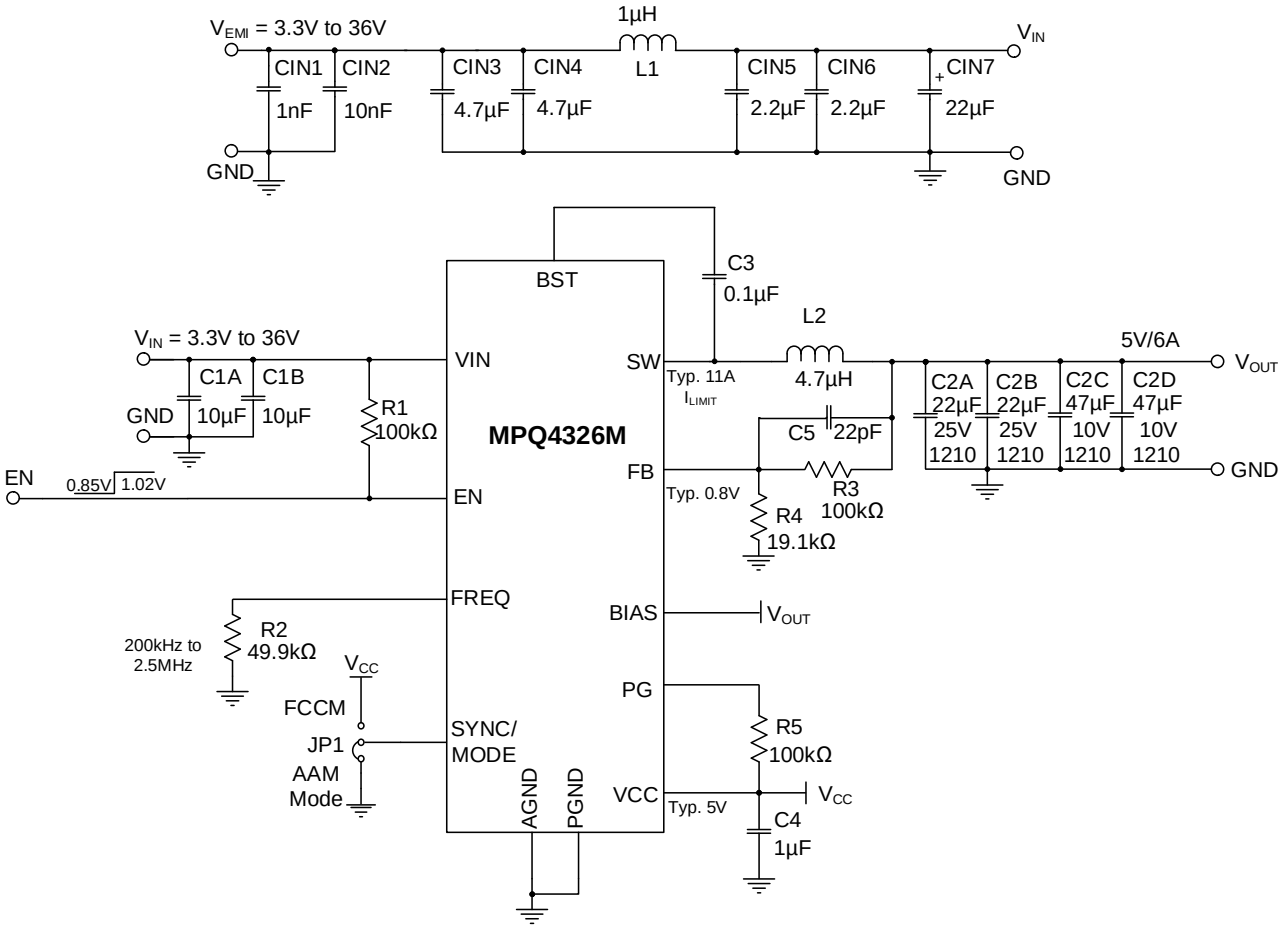
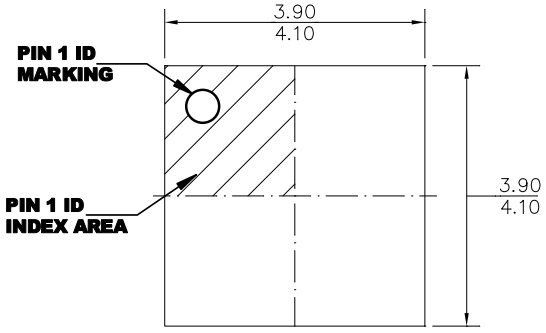


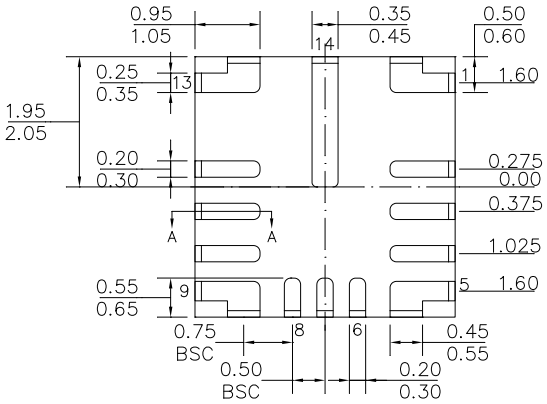
Figure 16: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 410kHz with EMI Filters)

PACKAGE INFORMATION

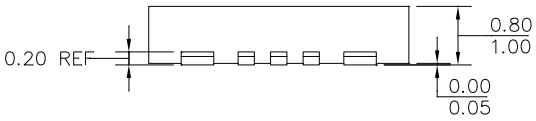
QFN-14 (4mmx4mm)
Wettable Flank



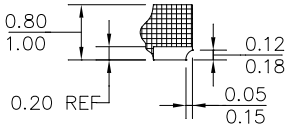
TOP VIEW



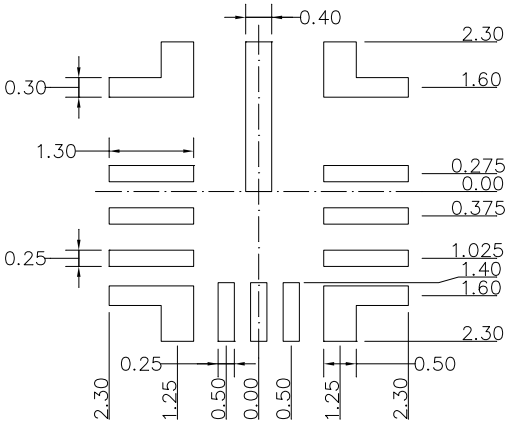
BOTTOM VIEW



SIDE VIEW



SECTION A-A

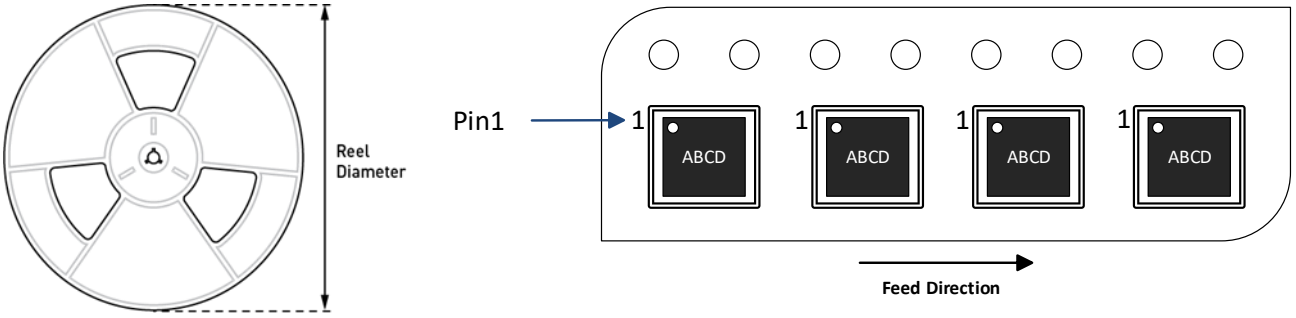


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (16)	Quantity /Tray (16)	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4326MGRE-AEC1-Z	QFN-14 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

16) N/A indicates “not available” in tube and tray. For 500-piece tape & reel prototype quantities, contact the factory. (The order code for a 500-piece partial reel order is “-P”. Tape & reel dimensions are the same as the full reel.)

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/11/2023	Initial Release	-