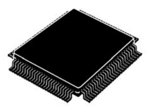
SR5 E1 line of Stellar electrification MCUs — 32-bit Arm® Cortex®-M7 automotive MCU 2x cores, 300 MHz, 2 MB flash, rich analog, 104 ps 24-ch high-resolution timer, HSM, and ASIL D

eTQFP100

(14 × 14 × 1.0 mm)

eTQFP144

(20 × 20 × 1.0 mm)



eLQFP176

(24 × 24 × 1.4 mm)

Product status link	
Part number	**Package**
SR5E1E3	eTQFP100
SR5E1E5	eTQFP144
SR5E1E7	eLQFP176

Features

- AEC-Q100 automotive qualification on going
- SR5 high-performance analog MCUs offering:
  - Digital and analog high-frequency control requested by new wide-bandgap technologies (silicon carbide and gallium nitride)
  - Superior real-time and functional safety performance (ASIL-D capability)
  - Built-in fast and cost-optimized OTA (over-the-air) reprogramming capability (with built-in dual-image storage)
  - High-speed security cryptographic services (HSM)

Cores

- 2× 32-bit Arm® Cortex®-M7 with double-precision FPU, L1 cache and DSP instructions running at up to 300 MHz to reach 1284 DMIPS/2.14 DMIPS/MHz/Core (Dhrystone 2.1)
  - Split-lock configuration, allowing either 2 cores in parallel or 1 core in lockstep configuration
- 2 DMA engines in lockstep configuration

Memories

- Up to 2 MB on-chip flash memory with read while write support
  - 1920 KB code flash memory split in two banks allowing 960 KB OTA reprogramming support
  - 160 KB HSM dedicated code flash memory
- 96 KB data flash memory (64 KB + 32 KB dedicated to HSM)
- 488 KB on-chip general-purpose SRAM:
  - 2× 32 KB instruction TCM + 2× 64 KB data TCM
  - 256 KB system RAM
  - 40 KB HSM dedicated system RAM

Security: hardware security module (HSM)

- On-chip high-performance security module with EVITA medium support with dedicated RAM and flash memory
- Based on Cortex®-M0+ core running at up to 150 MHz
- Hardware accelerator for symmetric cryptography

Safety: comprehensive new generation ASIL-D safety concept

- State of the art safety measures at all level of the architecture for most efficient implementation of ISO26262 ASIL-D functionalities
- FCCU for collection and reaction to failure notifications with enhanced configurability
- Memory error management unit (MEMU) for collection and reporting of error events in memories
- Cyclic redundancy check (CRC) unit

Enhanced peripherals for fast control loop capability

- 12 Timers:
  - 2× HRTIM (high-resolution and complex waveform builder): 12× 16-bit counters, up to 102 ps resolution, 24 PWM in total
  - 2× 16-bit 6-channel advanced control timers, with up to 12× PWM, in total
  - 2× 32-bit general purpose timers, with up to 8× IC/OC/PWM or pulse counter and quadrature encoder input in total
  - 4× 16-bit general purpose timers, with up to 11× PWM, 2 of which paired, in total
  - 2× 16-bit basic timers
- Enhanced analog-to-digital converter system with:
  - 5 separate 12-bit SAR analog converters, 8 channels each. Sampling rate up to 2.5 MSPS in single mode, 5 MSPS in dual mode
  - 2 separate 16-bit sigma-delta analog converters
- 12-bit digital-to-analog converters (DAC)
  - 2 buffered external channels 1 MSPS
  - 8 unbuffered internal channels 15 MSPS
- 8 rail-to-rail analog comparators, 50 ns propagation delay
- Hardware accelerator
  - 1× CORDIC for trigonometric functions acceleration

Communication interfaces

- 4 modular controller area network (MCAN) modules, all supporting flexible data rate (ISO CAN-FD)
- 3 UART modules with LIN functionality
- 4 serial peripheral interface (SPI) modules, 2 multiplexed with I²S interfaces
- 2 I²C modules

Advanced debug and trace for high-performance automotive application development

- Built around Arm® CoreSight™-600
- Debug interface: Arm® CoreSight™ JTAG (IEEE 1149.1) or SWD
- 4 KB embedded trace FIFO for both on- and off-chip tracing
- Trace port for off-chip tracing: parallel trace port configurable from 1 to 8 data lines

Others

- Power efficiency management, through separate power modes for any selected cores, peripherals or memories
- Boot assist flash (BAF) supports factory programming using a serial loader through CAN or UART
- Junction temperature range -40 °C to 150 °C
- Integrated power supply scheme:
  - Integrated internal SMPS regulator
  - 3.3 V supply & GPIOs

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SR5E1E3, SR5E1E5, SR5E1E7 microcontroller units (MCUs). For functional characteristics, refer to the device reference manual. This device is a preliminary and superset implementation of family devices. Contact your local STMicroelectronics sales or marketing representative to receive the information on feature removal, improvement or addition, versus upcoming SR6 family devices.

Note: For information on the Cortex®-M7 and Cortex®-M0+ cores, refer to the technical reference manuals, available from the www.arm.com website.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.2 Description

The SR5E1E3, SR5E1E5, SR5E1E7 MCU family has been designed to meet the enhanced digital control and high-performance analog requested by the new wide bandgap power technologies, silicon carbide and GAN, from power conversion applications such as on-board charger and DC/DC converters as well as advanced motor control like traction inverter applications.

SR5E1E3, SR5E1E5, SR5E1E7 also offer superior real-time and safe performance with the highest ASIL-D capability, security cryptographic services (HSM) and high efficiency OTA reprogramming capability.

1.3 Device features

The following table lists a summary of major features for the SR5E1E3, SR5E1E5, SR5E1E7. A detailed description of the functionality provided by each on-chip module is given later in this document.

Table 1. Features list

Feature	Description
Cores/memories	
Cortex®-M7	
Number of cores/checker cores	2 decoupled cores in split mode / 1 core with checker core in lock mode
Nominal frequency	300 MHz
Tightly coupled memory (TCM)	2× 32 KB instruction in split mode or 1× 64 KB instruction in lock mode 2× 64 KB data in split mode or 1× 128 KB data in lock mode
Floating-point unit	Single and double precision
Cache	8 KB instruction (2 ways) for each core 16 KB data (4 ways) for each core
System memories	
On-chip code flash memory	2 MB
On-chip data flash memory	64 KB
Built-in memory replication for OTA reprogramming	Up to 960 KB flash available
System RAM	2× 128 KB (not including HSM dedicated RAM - see HSM)
Others	
Multichannel eDMA (paired in lockstep)	2 DMA engines, 8 streams each
Interrupt broadcasting system in lockstep	Up to 190 sources
Watchdogs	2 independent and 2 window watchdogs

Feature	Description
Security: hardware security module (HSM)	
Core	Cortex®-M0 @ 150 MHz, as half device frequency.
C3 cryptography engine	Symmetric: • AES-128/256, ECB, CBC, CMAC, GCM • TRNG
Dedicated flash memory	160 KB
Dedicated system RAM	40 KB
Dedicated data flash	32 KB
Peripheral, IOs	
Timer modules	
High-resolution timer	2 modules, 6× 16-bit channels each, up to 102 ps resolution Up to 24× PWM signals (or 12× paired)
Advance control timer	2 modules, 16-bit timer Up to 8 input capture, 12 output compare (8 of which paired)
General purpose timer	2 modules, 32-bit timer. Up to 8 input capture/output compare 4 modules, 16-bit timer. Up to 11 input capture/output compare (2 of which paired)
Basic timer	2 modules, 16-bit timer
Enhanced analog-to-digital converter system	
12-bit SAR analog converters	5 modules, 8 channels each Fast conversion, up to 2.5 MSPS in single mode, 5 MSPS in dual mode
16-bit sigma-delta analog converters	2 modules, 2 channels each (available only in eLQFP176 and eTQFP144 packages) Output conversion rate of 333 ksps (OSR = 24)
12-bit analog comparators	8 modules, rail-to-rail, 50 ns propagation delay
12-bit digital-to-analog convertors	2 buffered external channels, 1 MSPS 8 unbuffered internal digital-to-analog channels, 15 MSPS
Hardware accelerator	
CORDIC (for trigonometric functions acceleration)	1 module
Communication interfaces	
UART modules (with LIN function)	3
MCAN supporting CAN-FD according to ISO 11898-1 2015	4 CAN shared message RAM: 4 KB / MCAN (16 KB in total)
Serial peripheral interface (SPI)	4
I²C	2
Software development/emulation features	
Arm® CoreSight™-600 libs	CoreSight™-600 libs for trace links, trace sink, and control components CoreSight™-400 libs for debug and trace source components
Debug interfaces	Arm® CoreSight™-600 compliant • Debug port (JTAG+SWD)
Trace types	Cortex®-M7 instruction and data trace
Off-chip trace	Arm® CoreSight™ parallel trace port (1 to 8 data lines, shared with user pins, not available in eTQFP100 package)
Advance cross-trigger and performance measurement	CoreSight™-600 CTI & CTM

Feature	Description
Timestamp distribution	Arm® CoreSight™ timestamp generator
Security	Arm® CoreSight™ authentication Password challenge with HSM
Debug controller	External tool-host CPU mailbox Host-based debugging Debug-under-reset
Others	
Low power mode	Clock gating management for selected cores, peripherals, and/or memories Smart wake-up mechanisms through events or interrupts
Temperature sensor	Yes
Self-test controller	Yes
PLL	2 individual PLLs: 1 with a stable clock source for peripherals and 1 supporting frequency modulation for cores
Power supply	Single internal SMPS regulator for 3.3 V supply and GPIOs
Boot assist flash (BAF)	Supports factory programming using a serial loader through the asynchronous CAN or UART
CRC channel(s)	1

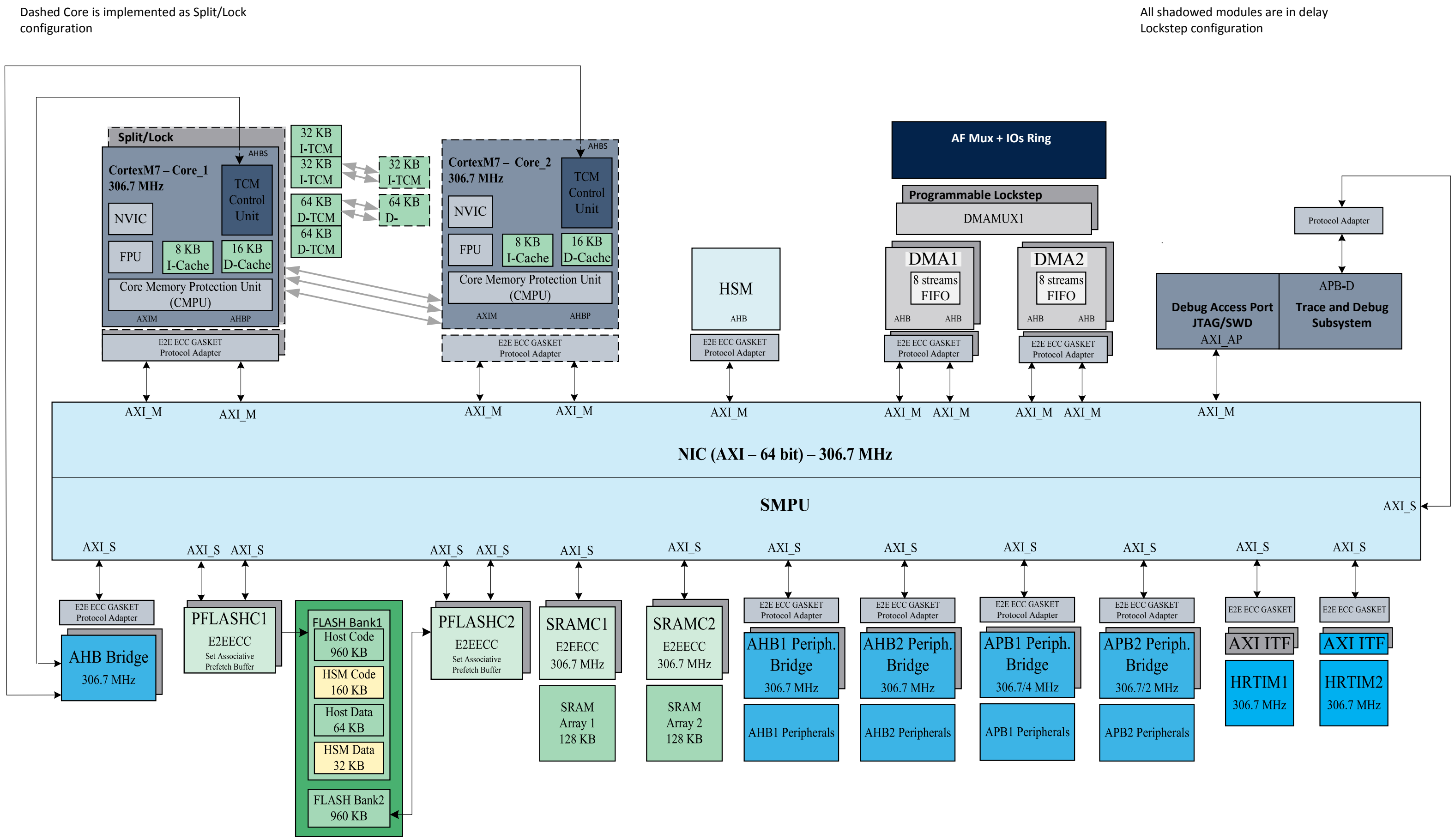
Table 2. SR5E1E3, SR5E1E5, SR5E1E7 product selector

Features		SR5E1E3, SR5E1E5, SR5E1E7
Cortex®-M7 cores		2 cores, either decoupled or in lockstep
Nominal frequency in MHz		300
Floating-point unit		Single and double precision
Cache (instruction/data) per core in Kbyte		8 / 16
Code flash in Mbyte	Overall included HSM in Mbyte	2
User code flash in Kbyte		1920
HSM code NVM in Kbyte		160
Code flash built-in memory replication for OTA reprogramming (not supported by HSM) in Kbyte		Up to 2× 960
Data flash in Kbyte	Overall included HSM	96
	User data flash	64
	HSM data flash	32
RAM in Kbyte	Overall	488
	TCM (instruction / data)	64 / 128
	User system RAM	256
	HSM system RAM	40
Hardware security module (HSM)		Yes
DMA engines (number of channels)	Engine	2
	Channel	2× 8
Low power mode and smart wake-up schemes		Yes
LIN and UART		3
CAN (with CAN-FD)		4
SPI		4
Timers	Advanced control	2 (16-bit)
	High-resolution	2 (16-bit)
	General purpose	2 (32-bit) 4 (16-bit)
	Basic	2 (16-bit)
12-bit SAR analog converters		5
16-bit sigma-delta analog converters		2
12-bit analog comparators (with internal DAC)		8
12-bit external DAC		2
Debug port	Main debug port (JTAG+SWD)	Yes
	Secondary debug port (SWD)	No
Max temperature (target)	Ambient temperature	125 °C
Junction temperature		150 °C
Packages	eTQFP100	X
	eTQFP144	X
	eLQFP176	X

1.4 Block diagram

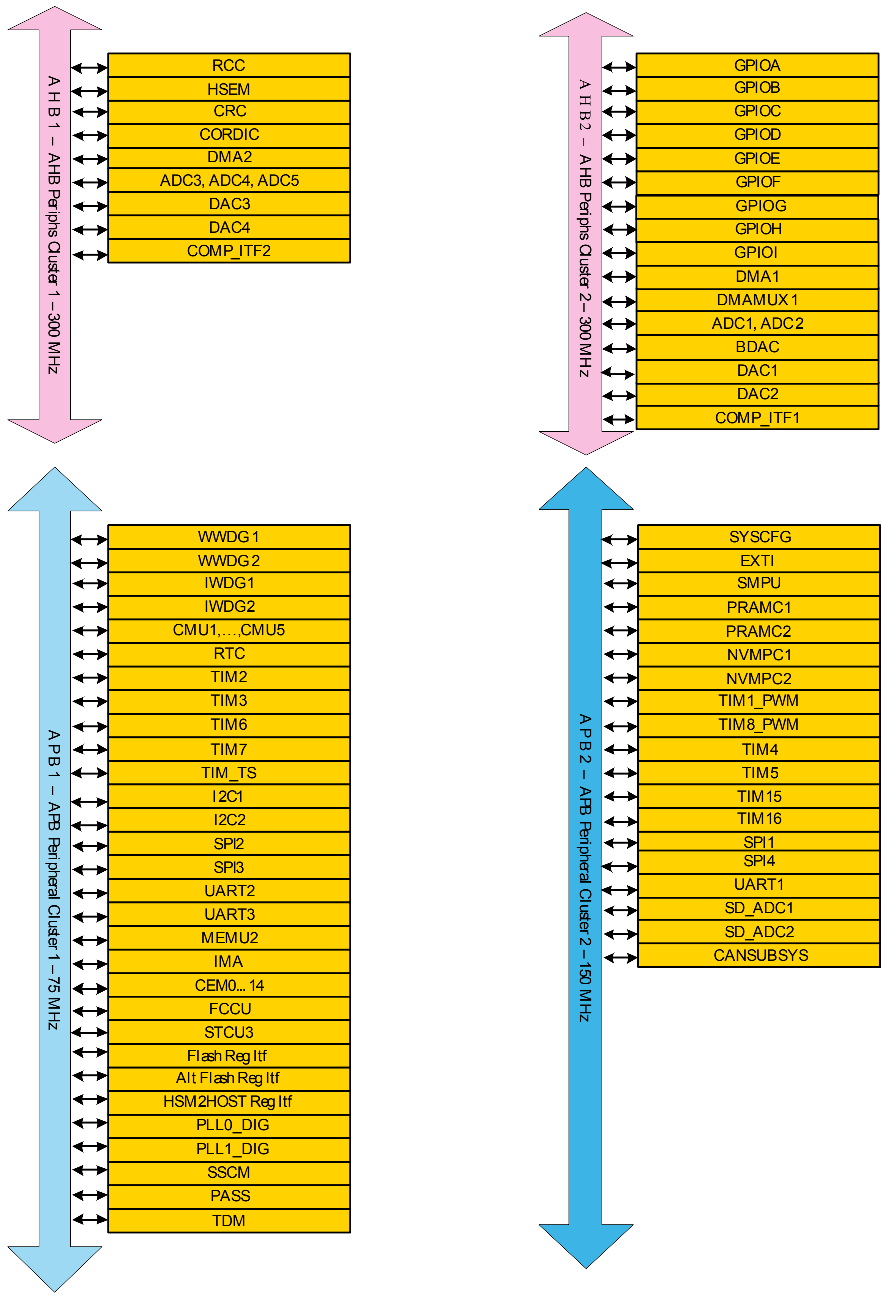
The figure below shows the top-level block diagram.

Figure 1. Block diagram



The figure below shows the peripheral block diagram.

Figure 2. Peripheral allocation



2 Package pinouts and signal descriptions

Refer to the SR5E1E3, SR5E1E5, SR5E1E7 IO definition technical note.

- Package pinouts
- Pin descriptions:
  - Power supply and reference voltage pins
  - System pins
  - Generic pins

3 Electrical characteristics

3.1 Introduction

The present document contains the target electrical specification for the 40 nm family 32-bit MCU SR5E1E3, SR5E1E5, SR5E1E7 products. Refer to the device reference manual for the details.

Note: This document provides target electrical specifications, based on previous designs, design simulations, or initial evaluation. Target electrical specification may not be guaranteed at this early stage of the product life cycle, however they are built to provide enough margin, ensuring production silicon meets customer requirements.

Finalized specifications are published after completion of device characterization and device qualifications.

Parts described in this document are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol "CC" (controller characteristics) is included in the "Symbol" column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol "SR" (system requirement) is included in the "Symbol" column.

The electrical parameters shown in this document are classified by various methods. To give the customer a better understanding, the classifications listed in the table below are used and the parameters are tagged accordingly in the tables where appropriate.

Table 3. Parameter classifications

Classification tag	Tag description
P	Those parameters are tested in production on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

3.2 Absolute maximum ratings

The table below describes the maximum ratings for the device. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

Table 4. Absolute maximum ratings

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{SS}	SR	D	Ground supply for the device. This is covering both VSS_LV and VSS_HV for the exposed pad device, unless specific notations.	—	-0.3	—	0.3	V
V_{DD_LV}	CC	D	Core voltage operating life range(1)	—	-0.3	—	1.45	V
$V_{SS\_HV\_OSC}$	SR	D	Ground supply for oscillator	—	-0.3	—	0.3	V
$V_{DD\_HV\_OSC}$	SR	D	High voltage power supply for oscillator	Reference to $V_{SS\_HV\_OSC}$	-0.3	—	3.6	V
$V_{DD\_HV\_IO}$	SR	D	I/O supply voltage and high voltage power supply for internal power management unit(2)	Reference to V_{SS}	-0.3	—	3.8	V
$V_{DD\_HV\_FLA}$	SR	D	High voltage power supply for flash	—	-0.3	—	3.8	V
$V_{DD\_HV\_SAR}$	SR	D	SAR ADC supply voltage	—	-0.3	—	3.8	V
$V_{DD\_HV\_SD\_DAC\_COMP}$	SR	D	High voltage power supply for SD ADC, DAC and comparator	—	-0.3	—	3.8	V
HV_REFL_SD	SR	D	SD ADC ground reference	—	-0.3	—	0.3	V
HV_REFH_SD	SR	D	SD ADC voltage reference	Reference to HV_REFL_SD	-0.3	—	3.8	V
HV_REFL_SD - V_{SS}	SR	D	SD ADC ground reference differential voltage	—	-0.3	—	0.3	V
HV_REFL_SAR	SR	D	SAR ADC ground reference and SAR ADC analog ground	—	-0.3	—	0.3	V
HV_REFH_SAR	SR	D	SAR ADC voltage reference	Reference to HV_REFL_SAR	-0.3	—	3.8	V
HV_REFL_SAR - V_{SS}	SR	D	SAR ADC ground reference differential voltage	—	-0.3	—	0.3	V
HV_REFL_DAC_COMP	SR	D	Ground reference for DAC and comparator	—	-0.3	—	0.3	V
HV_REFH_DAC_COMP	SR	D	Voltage reference for DAC and comparator	Reference to HV_REFL_DAC_COMP	-0.3	—	3.8	V
HV_REFL_DAC_COMP - V_{SS}	SR	D	DAC and comparator ground reference differential voltage	—	-0.3	—	0.3	V
V_{IN}	SR	D	I/O input voltage range(3)(4)	Relative to V_{ss}	-0.3	—	3.8	V
T_{TRIN}	SR	D	Digital input pad transition time(5)	—	—	—	TBD	ms
I_{INJ}	SR	T	Maximum DC injection current for each analog/digital PAD(6)	—	-5	—	5	mA
T_{STG}	SR	D	Maximum non-operating Storage temperature range	—	-55	—	125	°C
$T_{STORAGE}$	SR	D	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range -40 °C to 60 °C	—	—	20	years
T_{SDR}	SR	T	Maximum solder temperature Pb-free packaged(7)	—	—	—	260	°C
MSL	SR	T	Moisture sensitivity level(8)	—	—	—	3	—

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
T_{XRAY} dose	SR	T	Maximum cumulated XRAY dose	Typical range for X-rays source during inspection:80 - 130 KV; 20 - 50 µA	—	—	1	gray

1. *V_{DD_LV}: allowed 1.36 V - 1.45 V for 60 seconds cumulative time at the given temperature profile. Remaining time allowed 1.345 V - 1.36 V for 10 hours cumulative time at the given temperature profile. Remaining time as defined in Section 3.3: Operating conditions.*
2. *$V_{DD\_HV\_IO}$: allowed 3.45 V - 3.8 V for 60 seconds cumulative time at the given temperature profile, for 10 hours cumulative time with the device in reset at the given temperature profile. Remaining time as defined in Section 3.3: Operating conditions.*
3. *The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage is equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3 V can be used for nominal calculations.*
4. *Relative value can be exceeded if design measures are taken to ensure injection current limitation (parameter INJ).*
5. *This limitation applies to pads with digital input buffer enabled. If the digital input buffer is disabled, there are no maximum limits to the transition time.*
6. *The limits for the sum of all normal and injected currents on all pads within the same supply segment can be found in Section 3.8.3: I/O pad current specifications.*
7. *Solder profile per IPC/JEDEC J-STD-020D.*
8. *Moisture sensitivity per JDEC test method A112.*

Related links

3.3 Operating conditions on page 12
3.8.3 I/O pad current specifications on page 24
3.8.1 I/O input DC characteristics on page 18
3.12.1 ADC input description on page 35
3.12.2 SARADC 12-bit electrical specification on page 36

3.3 Operating conditions

The table below describes the operating conditions for the device, and for which all the specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded or the functionality of the device is not guaranteed.

Table 5. Operating conditions

Symbol (1)		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
F_{SYS}	SR	P	Operating system clock frequency(2)	—	—	—	306.7	MHz
T_J	SR	P	Operating Junction temperature	High temperature range	-40	—	150	°C
T_A	SR	P	Operating Ambient temperature	—	-40	—	125	°C
V_{DD_LV}	CC	D	Core supply voltage(3)	—	1.225(4)	1.285	1.345(5)	V
$V_{SS\_HV\_OSC}$	SR	C	Ground supply for oscillator	—	-0.3	—	0.3	V
$V_{DD\_HV\_OSC}$	SR	C	High voltage supply for oscillator	—	3.15(6)	—	3.45	V
$V_{DD\_HV\_IO}$	SR	P	IO supply voltage and high voltage power supply for internal power management unit	—	3.15(6)	—	3.45(7)	V
$V_{DD\_HV\_SAR}$	SR	P	SAR ADC supply voltage	—	3.15(6)	—	3.45(7)	V
$V_{DD\_HV\_SD\_DAC\_COMP}$	SR	P	High voltage power supply for SD ADC, DAC and comparator	—	3.15(6)	—	3.45(7)	V

Symbol [1]		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD\_HV\_FLA}$	SR	P	High voltage power supply for flash	—	3.15[6]	—	3.45[7]	V
HV_REFH_SD	SR	P	SD ADC supply reference voltage[8]	—	2.9	—	3.45	V
HV_REFH_SD - $V_{DD\_HV\_SD\_DAC\_COMP}$	SR	D	SD ADC reference differential voltage	—	—	—	0 (Not allowed)	mV
HV_REFL_SD	SR	P	SD ADC ground reference voltage	—	—	0	—	V
HV_REFL_SD - V_{SS}	SR	D	SD ADC ground differential voltage	—	–25	—	25	mV
HV_REFH_SAR	SR	P	SAR ADC supply reference voltage[9]	—	2.7	—	3.45	V
HV_REFH_SAR - $V_{DD\_HV\_SAR}$	SR	D	SAR ADC reference differential voltage	—	—	—	0 (Not allowed)	mV
HV_REFL_SAR	SR	P	SAR ADC ground reference voltage and SAR ADC analog ground	—	0	—	0.1	V
HV_REFL_SAR - V_{SS}	SR	D	SAR ADC ground differential voltage	—	–25	—	25	mV
HV_REFL_DAC_COMP	SR	P	Ground reference for DAC and comparator	—	—	0	—	V
HV_REFH_DAC_COMP	SR	P	Voltage reference for DAC and comparator	Reference to HV_REFL_DAC_COMP	3.0	—	3.45	V
HV_REFL_DAC_COMP - V_{SS}	SR	D	DAC and comparator ground reference differential voltage	—	–25	—	25	mV
V_{RAMP_HV}	SR	D	Slew rate on HV power supply	—	33	—	100	V/ms
V_{IN}	SR	P	I/O input voltage range and high voltage power supply for internal power management unit	—	0	—	$V_{DD\_HV\_IO}$	V
I_{INJ1}	SR	T	Injection current (per pin) without performance degradation [10][11][12]	Digital pins and analog pins	–3	—	3	mA
I_{INJ2}	SR	D	Dynamic injection current (per pin) with performance degradation[10][13]	Digital pins and analog pins	–10	—	10	mA

1. *The ranges in this table are design targets and actual data may vary in the given range.*
2. *Maximum operating frequency is applicable to the cores and platform of the device. Refer to the device reference manual, Clocking chapter, for more information on the clock limitations for the various IP blocks on the device.*
3. *Core voltage is measured on device pin to guarantee published silicon performance. This value is provided as information, but it is controlled internally by PMU. External low voltage supply is not supported in functional mode.*
4. *In the range [1.265-1.225] V the device functionality and specifications are guaranteed, but this interval is to be considered as a transient, in accordance with the mission profile, to guarantee the product reliability and to reduce the false LVD triggers recurrence. In the range [1.225-1.19] V, the device functionality is granted and the device is expected to receive a flag by the internal LVD119 monitors to warn that the regulator providing the VDD_LV supply, exited the expected operating conditions. If the internal LVD119 monitors are disabled by the application, then an external voltage monitor with minimum threshold of V_{DD_LV}(min) = 1.19 V measured at the device pad, has to be implemented. Refer to Section 3.13.3: Voltage monitors for the list of available internal monitors and to the device reference manual for the configurability of the monitors.*
5. *In the range [1.31-1.345] V the device functionality and specifications are guaranteed, but this interval is to be considered as a transient, in accordance with the mission profile, to guarantee the product reliability and to reduce the false HVD triggers recurrence. In the range [1.345-1.4] V the device functionality is granted and the device is expected to receive a flag by the internal HVD140 monitors to warn that the regulator providing the V_{DD_LV} supply, exited the expected operating conditions. Refer to Section 3.13.3: Voltage monitors for the list of available internal monitors and to the device reference manual for the configurability of the monitors. Possible permanent failure over 1.4 V.*

6. *In the range [3.02-3.15] V, the device functionality and specifications are guaranteed, but this interval is to be considered as a transient, in accordance with the mission profile, to guarantee the product reliability and to reduce the false LVD triggers recurrence. In the range [3.012-2.898] the device functionality and specifications are granted and the device is expected to receive a flag by the internal LVD290 monitors . Refer to Section 3.13.3: Voltage monitors for the list of available internal monitors and to the Reference Manual for the configurability of the monitors.*
7. *In the range [3.45-3.65]V, the device functionality and specifications are guaranteed, but this interval is to be considered as a transient, in accordance with the mission profile, to guarantee the product reliability and to reduce the false UVD triggers recurrence. In the range [3.651-3.799] the device functionality and specifications are granted and the device is expected to receive a flag by the internal UVD380 monitors . Refer to Section 3.13.3: Voltage monitors for the list of available internal monitors and to the Reference Manual for the configurability of the monitors.*
8. *To be always ensured $V_{DD\_HV\_SD\_DAC\_COMP} \geq$ HV_REFH_SD.*
9. *To be always ensured $V_{DD\_HV\_SAR} \geq$ HV_REFH_SAR.*
10. *The limits for the sum of all normal and injected currents on all pads within the same supply segment can be found in Section 3.8.3: I/O pad current specifications.*
11. *The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pins is above the supply rail, current is injected through the clamp diode to the supply rails. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.*
12. *Full device lifetime. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. Refer to Section 3.2: Absolute maximum ratings for maximum input current for reliability requirements.*
13. *Positive and negative dynamic current injection pulses are allowed up to this limit, with different specifications for I/O, ADC accuracy and analog input. Refer to the dedicated chapters for the different specification limits. See the Table 4. Absolute maximum ratings for maximum input current for reliability requirements. Refer to the following pulses definitions: Pulse1 (ISO 7637-2:2011), Pulse 2a(ISO 7637-2:2011 5.6.2), Pulse 3a (ISO 7637-2:2011 5.6.3), Pulse 3b (ISO 7637-2:2011 5.6.3).*

Table 6. TCM wait states configuration

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Core ITCM waitstates	CC	D	ITCM access wait state from own core	—		0		WS
Core DTCM waitstates	CC	D	DTCM access wait state from own core	—		0		WS

Table 7. PRAM wait states configuration

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
PRAMC MEMACC_WAIT	SR	D	System RAM read/write wait state	—	0	0	0	WS

Related links

3.2 Absolute maximum ratings on page 11
3.8.3 I/O pad current specifications on page 24
3.12.1 ADC input description on page 35
3.13.3 Voltage monitors on page 56

3.3.1 Power domains and power up/down sequencing

The following table shows the constraints and relationships for the different power domains. Supply1 (on rows) can exceed Supply2 (on columns), only if the cell at the given row and column is reporting ‘ok’. This limitation is valid during power-up and power-down phases, as well as during normal device operation.

Table 8. **Device supply relation during power-up/power-down sequence**

		Supply2							
		$V_{DD\_HV\_IO}$	$V_{DD\_HV\_OSC}$	$V_{DD\_HV\_FLA}$	$V_{DD\_HV\_SAR}$	$V_{DD\_HV\_SD\_DAC\_COMP}$	HV_REFH_SAR	HV_REFH_SD	HV_REFH_DAC_COMP
Supply1	$V_{DD\_HV\_IO}$		OK	OK	OK	OK	OK	OK	OK
	$V_{DD\_HV\_OSC}$	OK		OK	OK	OK	OK	OK	OK
	$V_{DD\_HV\_FLA}$	OK	OK		OK	OK	OK	OK	OK
	$V_{DD\_HV\_SAR}$	OK	OK	OK		OK	OK	OK	OK
	$V_{DD\_HV\_SD\_DAC\_COMP}$	Not allowed	OK	OK	OK		OK	OK	OK
	HV_REFH_SAR	OK	OK	OK	Not allowed	OK		OK	OK
	HV_REFH_SD	Not allowed	OK	OK	OK	Not allowed	OK		OK
	HV_REFH_DAC_COMP	OK	OK	OK	OK	Not allowed	OK	OK	

During power-up, all functional terminals are maintained in a known state as described in the device pinout Excel file attached to the SR5E1E3, SR5E1E5, SR5E1E7 IO definition technical note.

3.4 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device.

Table 9. **ESD ratings**

Symbol		C	Parameter (1)(2)	Conditions	Value			Unit
					Min	Typ	Max	
ESD_HBM	SR	T	ESD for human body model (HBM)(3)	All pins	—	—	2000	V
ESD_CDM	SR	T	ESD for field induced charged device model (CDM)(4)	All terminals	—	—	500	V
	SR	T		Corner terminals	—	—	750	V

1. *Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature. Maximum DC parametrics variation within 10% of maximum specification”.*
2. *All ESD testing is in conformity with CDF-AEC-Q100 stress test qualification for automotive grade integrated circuits.*
3. *This parameter tested in conformity with ANSI/ESD STM5.1-2007 electrostatic discharge sensitivity testing.*
4. *This parameter tested in conformity with ANSI/ESD STM5.3-1990 charged device model - component level.*

3.5 Electromagnetic emission characteristics

EMC measurements at integrated circuit level IEC standards can be requested to STMicroelectronics.

300 MHz nominal frequency is not suggested as operative frequency due to possible EMC emission in the GNSS band. Suggested operative (max) frequency is 306.7 MHz, refer to Reference Manual "Clock tree" and PLLs divider registers (PLL0DV and PLL1DV).

3.6 Temperature profile

The device is qualified in accordance to AEC-Q100 Grade1 and customers' requirements.

3.7 Device consumption

The total device consumption seen from the HV domain is the sum of the total dynamic current on the high voltage supply and the leakage current seen on the high voltage domain (from LV domain through SMPS) for the selected temperature. So, it is: $I_{TOT} = I_{DD\_HV} + I_{DD\_HV\_SMPS\_LKG}$.

The following table reports each single contributor factor to the device consumption.

Refer to Figure 3. Device consumption measurement to see where each contributor is measured.

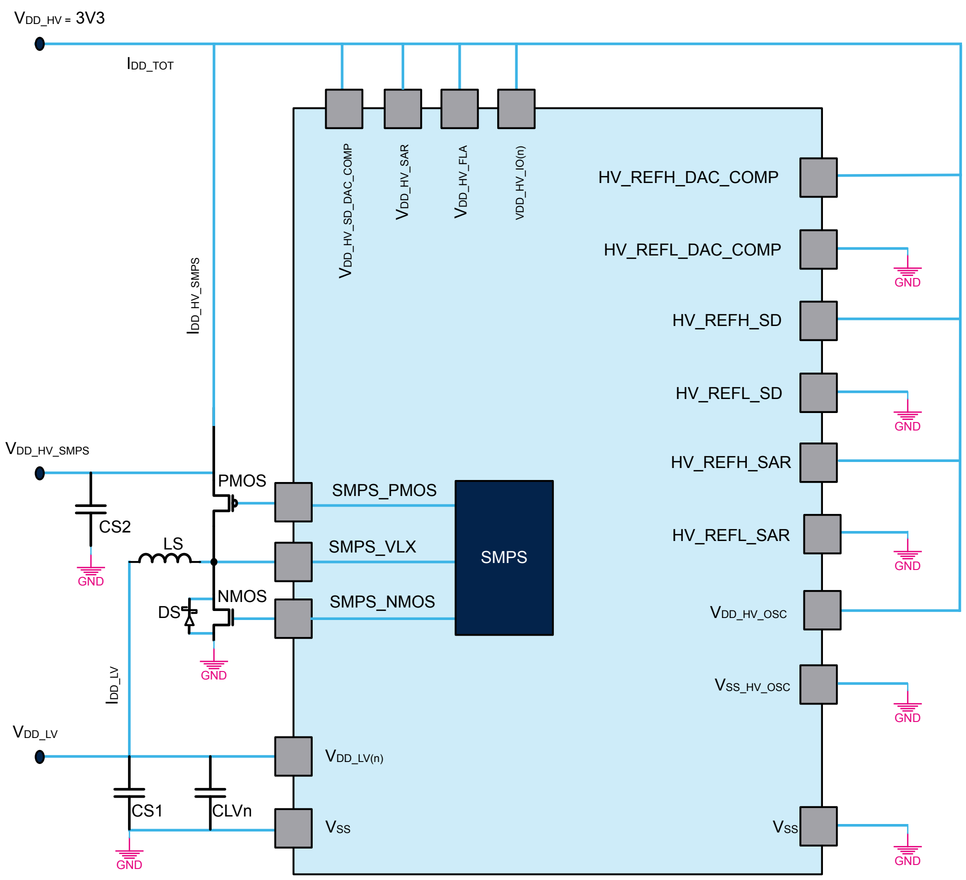
Table 10. Device consumption

Symbol[1]		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
High voltage domain (V_{DD_HV})								
I_{DD_HV}	CC	P	Total dynamic current on a high voltage supply (V_{DD_HV})	Motor control application profile[3] Freq = 300 MHz	—	105	150	mA
		P		Full case profile[4] Freq = 300 MHz	—	150	205	mA
$I_{DD\_HV\_SMPS\_LKG}$	CC	C	Leakage current is seen on the high voltage domain (from LV domain through SMPS)	Tamb = 25 °C	—	10	40	mA
		P		Tamb = 125 °C	—	105	430	
$I_{DD\_HV\_SMPS}$	CC	P	Dynamic current on external MOSFETs	Motor control application profile[3] Freq = 300 MHz	—	90	145	mA
		P		Full case profile[4] Freq = 300 MHz	—	125	190	mA
Low voltage domain (V_{DD_LV})								
I_{DD_LKG}[2][5]	CC	C	Leakage current on digital supply (V_{DD_LV})	Tamb = 25 °C	—	21	80	mA
		P		Tamb = 125 °C	—	170	750	
I_{DD_LV}[5]	CC	T	Dynamic current on digital supply (V_{DD_LV})	Motor control application profile[3] Freq = 300 MHz	—	205	240	mA
		T		Full case profile[4] Freq = 300 MHz	—	270	310	mA
$I_{DD\_MAIN\_m7}$	CC	T	Main core dynamic current	Motor control application based[6] Freq = 300 MHz	—	42	48	mA
$I_{DD\_MAIN\_Csleep}$	CC	T	Dynamic current reduction with main core in CSleep	Full case profile[7] Freq = 300 MHz	—	4	8	mA
I_{SPIKE}	CC	T	Maximum short term current spike	< 20 µs observation window	—	—	100	mA
dI	SR	D	Current difference ratio to average current (dI/avg(I))	20 µs observation window	—	—	20	%
I_{SR}[8]	CC	D	Current variation during power up/down	Refer to footnote[9]	—	—	200	mA
I_{DDOFF}	CC	T	Power-off current on high voltage supply rails[10]	V_{DD_HV} = 2.5 V	100	—	—	µA

1. *The ranges in this table are design targets and actual data may vary in the given range.*

2. *The leakage considered is the sum of core logic and RAM memories. The contribution of analog modules is not considered, and they are computed in the dynamic I_{DD_LV} and I_{DD_HV} parameters.*
3. *Motor control application configured to drive single field-oriented control (FOC) 3-phase permanent magnet motors with ICS topology power stage (in open-loop). Position sensors used are encoder and sensor-less algorithms. IPs involved: Single core, 2× ADC channels, 6× timer channels (PWM generation), 2× timer channels (encoder), UART, DAC, CORDIC, GPIOs.*
4. *Full case profile - 2× M7 cores in lockstep. IPs involved: 5× SARADCs, 2× SDADCs, COMPs, 6× timer channels (PWM generation), 24× HRTIM channels (PWM generation), UART, DAC, CORDIC, 2× SPIs, CAN, GPIOs.*
5. *I_{DD_LKG} (leakage current) and I_{DD_LV} (dynamic current) are reported as separate parameters, to give an indication of the consumption contributors. The tests used in validation, characterization and production are verifying that the total consumption (leakage+dynamic) is lower than or equal to the sum of the maximum values provided (I_{DD_LKG} + I_{DD_LV}). The two parameters, measured separately, may exceed the maximum reported for each, depending on the operative conditions and the software profile used.*
6. *Main core dynamic consumption contribution based on motor control profile. Dedicated I/D-caches and I/D-TCMs contribution are not included.*
7. *Dynamic current reduction with the main core in CSleep, based on the full case profile.*
8. *This specification is the maximum value and is a boundary for the dI specification.*
9. *Condition 1: for power, on period from 0 V up to normal operation with reset asserted. Condition 2: from reset asserting until PLL running free. Condition 3: increasing PLL from free frequency to full frequency. Condition 4: reverse order for power down to 0 V.*
10. *I_{DDOFF} is the minimum ensured consumption of the device during power-up.*

Figure 3. Device consumption measurement



3.8 I/O pad specification

The following table describes the different pad type configurations.

Table 11. I/O pad specification descriptions

Pad type	Description
Slow configuration	Provides a good compromise between transition time and low electromagnetic emission.
Medium configuration	Provides transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
Fast configuration	Provides fast transition speed; used for fast interface.
Very fast configuration	Provides maximum speed and controlled symmetric behavior for rise and fall transition. Used for fast interface requiring fine control of rising/falling edge jitter.
Input only pads	These low input leakage pads are associated with the ADC channels.

Note: Each I/O pin on the device supports specific drive configurations. Refer to the signal description table in the device reference manual for the available drive configurations for each I/O pin.

3.8.1 I/O input DC characteristics

The following table provides input DC electrical characteristics, as described in the following figure.

Figure 4. I/O input electrical characteristics

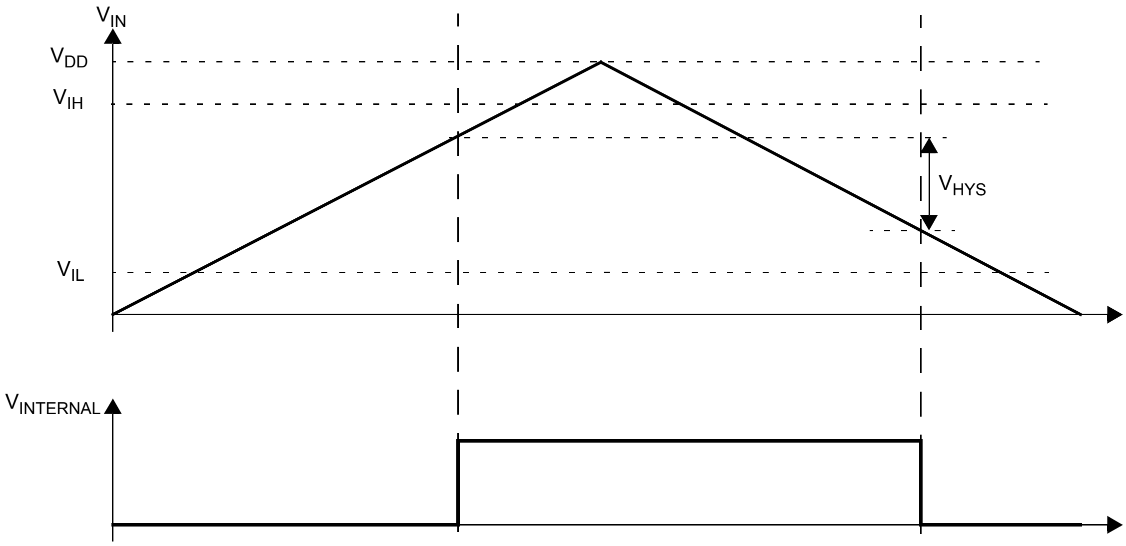


Table 12. I/O input electrical characteristics

Symbol	C		Parameter	Conditions	Value			Unit
					Min	Typ	Max	
TTL								
V_{ihttl}	SR	P	Input high level TTL(1)	—	2	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ilttl}	SR	P	Input low level TTL(1)	—	-0.3	—	0.8	V
V_{hysttl}	CC	C	Input hysteresis TTL(1)	—	0.3	—	—	V

Symbol	C		Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Automotive								
V_{ihaut}[2]	SR	P	Input high level AUTO	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	0.75 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ilaut}[3]	SR	P	Input low level AUTO	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	-0.3	—	0.35 * $V_{DD\_HV\_IO}$	V
V_{hysaut}[4]	CC	C	Input hysteresis AUTO	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	0.11 * $V_{DD\_HV\_IO}$	—	—	V
CMOS								
V_{ihcmos}	SR	P	Input high level CMOS[1]	—	0.65 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ilcmos}	SR	P	Input low level CMOS[1]	—	-0.3	—	0.35 * $V_{DD\_HV\_IO}$	V
$V_{hyscmos}$	CC	C	Input hysteresis CMOS[1]	—	0.10 * $V_{DD\_HV\_IO}$	—	—	V
Common								
I_{LKG}	CC	P	Pad input leakage[1]	INPUT-ONLY pads, static leakage characteristics $V_{DD\_HV\_IO}$ = 3.3 V ± 5% T_J = 150 °C	—	—	200	nA
		P		FAST pads, static leakage characteristics $V_{DD\_HV\_IO}$ = 3.3 V ± 5% T_J = 150 °C	—	—	800	
		P		VERY FAST pads, static leakage characteristics $V_{DD\_HV\_IO}$ = 3.3 V ± 5% T_J = 150 °C	—	—	1000	
C_{P1}	CC	D	Pad capacitance	—	—	—	3.5	pF
V_{drift}	CC	D	Input V_{il}/V_{ih} temperature drift	In a 1 ms period, with a temperature variation <30 °C	-50	—	+50	mV

1. *In case of current injection pulses on one pad under the conditions and limits described in I_{INJ2} parameter in Absolute maximum ratings, other pads of the same supply segment have a drift of 4 % above the maximum V_{il} and 4 % below the minimum V_{ih} limits. Similarly V_{hys} parameter is decreased of 4 %.*
2. *Good approximation of the variation of the minimum value with supply is given by formula: 3.3 V range: V_{IHAUT} = 0.75 × $V_{DD\_HV\_IO}$*
3. *Good approximation of the variation of the maximum value with supply is given by formula: 3.3 V range: V_{ILAUT} = 0.35 × $V_{DD\_HV\_IO}$*
4. *Good approximation of the variation of the minimum value with supply is given by formula: 3.3 V range: V_{HYSAUT} = 0.11 × $V_{DD\_HV\_IO}$*

Table 13. I/O pull-up/pull-down electrical characteristics

Symbol	C		Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{WPU}	CC	T	Weak pull-up current absolute value	V_{IN} = 1.1 V[1]	—	—	130	µA
		P		V_{IN} = 0.69 * $V_{DD\_HV\_IO}$ [2]	15	—	—	
R_{WPU}	CC	D	Weak pull-up resistance	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	24	—	45	KΩ
I_{WPD}	CC	T	Weak pull-down current absolute value	V_{IN} = 0.69 * $V_{DD\_HV\_IO}$[1]	—	—	130	µA
		P		V_{IN} = 0.9 V[2]	15	—	—	
R_{WPD}	CC	D	Weak pull-down resistance	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	20	—	38	KΩ

1. *Maximum current when forcing a change in the pin level opposite to the pull configuration.*
2. *Minimum current when keeping the same pin level state as the pull configuration.*

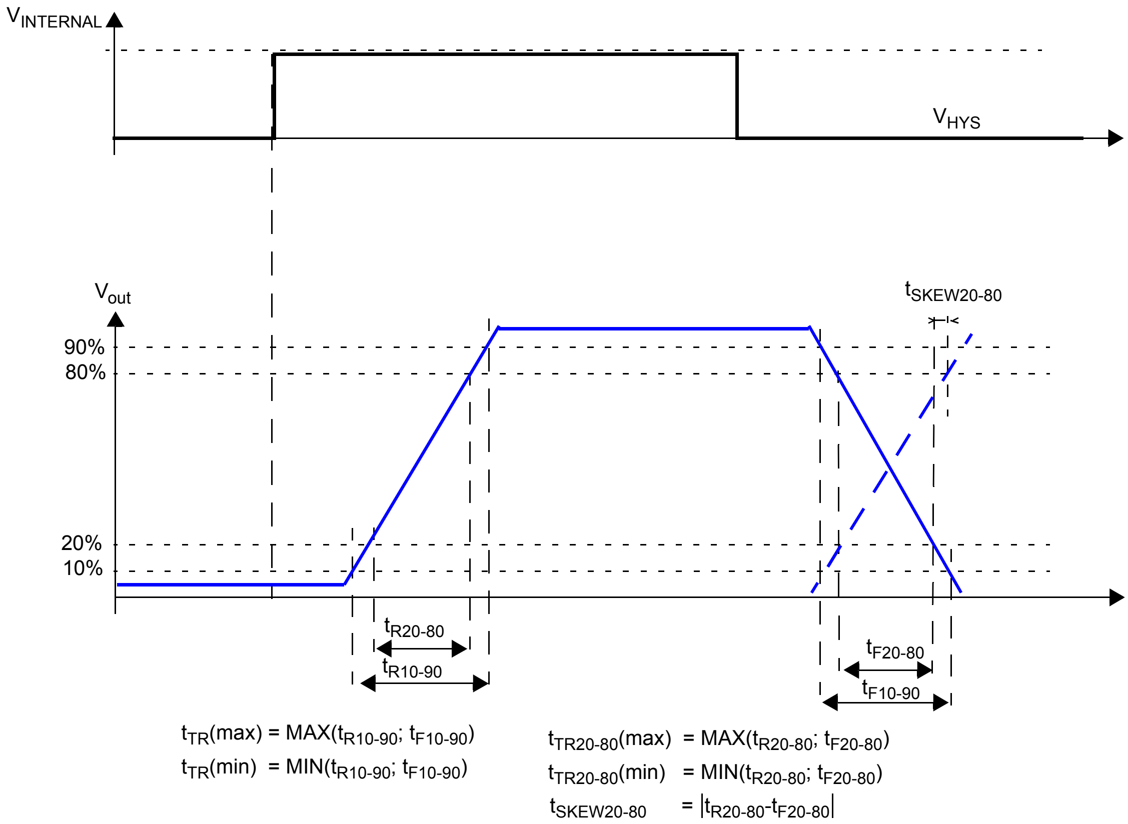
Related links

3.2 Absolute maximum ratings on page 11
3.12.1 ADC input description on page 35

3.8.2 I/O output DC characteristics

The figure below describes the output DC electrical characteristics.

Figure 5. I/O output DC electrical characteristics definition



The following tables provide DC characteristics for bidirectional pads.

Related links

3.15.1.2 JTAG interface timing on page 63

3.8.2.1 Slow I/O output characteristics

The following table provides output driver characteristics for I/O pads when in slow configuration.

Table 14. Slow I/O output characteristics

Symbol		C	Parameter	Conditions	Value Min	Typ	Max	Unit
V_{ol_S}	CC	D	Output low voltage for slow type pads	I_{ol} = 0.5 mA $V_{DD\_HV\_IO}$ = 3.3 V ± 5%	—	—	0.1 * $V_{DD\_HV\_IO}$	V
V_{oh_S}	CC	D	Output high voltage for slow type pads	I_{oh} = 0.5 mA $V_{DD\_HV\_IO}$ = 3.3 V ± 5%	0.9 * $V_{DD\_HV\_IO}$	—	—	V
$R_{\_S}$	CC	P	Output impedance for slow type pads	V_{OL} = 0.1 * $V_{DD\_HV\_IO}$ (static driver sink impedance)	256	—	600	Ω
				V_{OH} = 0.9 * $V_{DD\_HV\_IO}$ (static driver source impedance)	256	—	600	
F_{max_S}	CC	T	Maximum output frequency for slow type pads	$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 25 pF	—	—	2	MHz
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 50 pF	—	—	1	MHz
t_{TR_S}	CC	T	Transition time output pin slow configuration, 10%-90%	$V_{DD\_HV\_IO}$ = 3.3 V + 5% C_L = 25 pF	23	—	83	ns
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 50 pF	40	—	150	ns
$\lvert t_{SKEW\_S} \rvert$	CC	T	Rise / fall skew (Tr-Tf) / Max[Tr,Tf]	—	—	—	30	%
I_{DCMAX_S}	CC	D	Maximum DC current	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	—	—	0.5	mA

3.8.2.2 *Medium I/O output characteristics*

The following table provides output driver characteristics for I/O pads when in medium configuration.

Table 15. Medium I/O output characteristics

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
V_{ol_M}	CC	D	Output low voltage for medium type pads	I_{ol} = 2.0 mA $V_{DD\_HV\_IO}$ = 3.3 V ± 5%	—	—	0.1*$V_{DD\_HV\_IO}$	V
V_{oh_M}	CC	D	Output high voltage for medium type pads	I_{oh}=2.0 mA $V_{DD\_HV\_IO}$ = 3.3 V ± 5%	0.9*$V_{DD\_HV\_IO}$	—	—	V
$R_{\_M}$	CC	P	Output impedance for medium type pads	V_{OL} = 0.1 * $V_{DD\_HV\_IO}$ (static driver sink impedance)	64	—	150	Ω
				V_{OH} = 0.9 * $V_{DD\_HV\_IO}$ (static driver source impedance)	64	—	150	
F_{max_M}	CC	T	Maximum output frequency for medium type pads	$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 25 pF	—	—	12	MHz
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 50 pF	—	—	6	MHz
t_{TR_M}	CC	T	Transition time output pin medium configuration, 10%-90%	$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L =25 pF	6	—	20	ns
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 50 pF	11	—	40	ns
$\|t_{SKEW\_M}\|$	CC	T	Rise / fall skew (Tr-Tf) / Max[Tr,Tf]	—	—	—	30	%
I_{DCMAX_M}	CC	D	Maximum DC current	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	—	—	2	mA

3.8.2.3 *Fast I/O output characteristics*

The following table provides output driver characteristics for I/O pads when in fast configuration.

Table 16. Fast I/O output characteristics

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
V_{ol_F}	CC	D	Output low voltage for fast type pads	I_{ol} = 5.7 mA $V_{DD\_HV\_IO}$ = 3.3 V ± 5%	—	—	0.15*$V_{DD\_HV\_IO}$	V
V_{oh_F}	CC	D	Output high voltage for fast type pads	I_{oh} = 5.7 mA $V_{DD\_HV\_IO}$ = 3.3 V ± 5%	0.85*$V_{DD\_HV\_IO}$	—	—	V
$R_{\_F}$	CC	P	Output impedance for fast type pads	V_{OL} = 0.15 * $V_{DD\_HV\_IO}$ (static driver sink impedance)	28	—	66	Ω
				V_{OH} = 0.85 * $V_{DD\_HV\_IO}$ (static driver source impedance)	28	—	66	
F_{max_F}	CC	T	Maximum output frequency for fast type pads	$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 25 pF	—	—	50	MHz
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 50 pF	—	—	25	MHz
t_{TR_F}	CC	T	Transition time output pin, fast configuration, 10%-90%	$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 25 pF	2.5	—	7	ns
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 50 pF	4	—	10	
$\lvert t_{SKEW\_F} \rvert$	CC	T	Rise / fall skew (Tr-Tf) / Max[Tr,Tf]	—	—	—	30	%
I_{DCMAX_F}	CC	D	Maximum DC current	—	—	—	5.7	mA

3.8.2.4 *Very fast I/O output characteristics*

The following table provides output driver characteristics for I/O pads when in very fast configuration.

Table 17. Very fast I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_V}	CC	D	Output low voltage for very fast type pads	I_{ol} = 10 mA $V_{DD\_HV\_IO}$ = 3.3 V ± 5%	—	—	0.15*$V_{DD\_HV\_IO}$	V
V_{oh_V}	CC	D	Output high voltage for very fast type pads	I_{oh} = 10 mA $V_{DD\_HV\_IO}$ = 3.3 V ± 5%	0.85*$V_{DD\_HV\_IO}$	—	—	V
$R_{\_V}$	CC	P	Output impedance for very fast type pads	V_{OL} = 0.15 * $V_{DD\_HV\_IO}$ (static driver sink impedance)	16	—	38	Ω
				V_{OH} = 0.85 * $V_{DD\_HV\_IO}$ (static driver source impedance)	16	—	38	
F_{max_V}	CC	T	Maximum output frequency for very fast type pads	$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 25 pF	—	—	50	MHz
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 50 pF	—	—	25	MHz
t_{TR_V}	CC	T	10-90% threshold transition time output pin very fast configuration	$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 25 pF	1.3	—	4	ns
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% Tx line with Td = 0.6 ns C_L = 10 pF	1.0	—	6.5	
$t_{TR20\text{-}V\_20\_80}$	CC	T	20-80% threshold transition time output pin very fast configuration	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%, Tx line with Td = 0.6 ns C_L = 10 pF	0.5	—	Tr + Tf < 9Tr Tf = 4.5 ns	ns
I_{DCMAX_V}	CC	D	Maximum DC current	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	—	—	10	mA

3.8.3 I/O pad current specifications

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in the Excel file attached to the SR5E1E3, SR5E1E5, SR5E1E7 IO definition technical note.

The table below provides I/O consumption figures.

To ensure the device reliability, the average current of the I/O on a single segment should remain below the I_{RMSSEG} maximum value.

To ensure the device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Pad mapping on each segment can be optimized using the pad usage information provided on the I/O signal description table.

Table 18. I/O consumption

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Average consumption(1)								
I_{RMSSEG}	SR	D	Sum of all the DC I/O current within a supply segment(2)	—	—	—	120	mA
I_{RMS_S}	CC	D	RMS I/O current for Slow configuration	$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 25 pF, 2 MHz	—	—	1	mA
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 50 pF, 1 MHz	—	—	1	
I_{RMS_M}	CC	D	RMS I/O current for Medium configuration	$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 25 pF, 12 MHz	—	—	4.5	mA
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 50 pF, 6 MHz	—	—	4.5	
I_{RMS_F}	CC	D	RMS I/O current for Fast configuration	$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 25 pF, 50 MHz	—	—	15	mA
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 50 pF, 25 MHz	—	—	15	
I_{RMS_V}	CC	D	RMS I/O current for Very Fast configuration	$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 25 pF, 50 MHz	—	—	20	mA
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 10 pF, 25 MHz	—	—	8	
Dynamic consumption(3)								
I_{DYN_SEG}	SR	D	Sum of all the dynamic and DC I/O current within a supply segment	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	—	—	360	mA
I_{DYN_S}	CC	D	Dynamic I/O current for Slow configuration	$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 25 pF	—	—	6.6	mA
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 50 pF	—	—	6.6	
I_{DYN_M}	CC	D	Dynamic I/O current for Medium configuration	$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 25 pF	—	—	15	mA
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 50 pF	—	—	16	
I_{DYN_F}	CC	D	Dynamic I/O current for Fast configuration	$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 25 pF	—	—	34	mA
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 50 pF	—	—	36	
I_{DYN_V}	CC	D	Dynamic I/O current for Very Fast configuration	$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 25 pF	—	—	60	mA
				$V_{DD\_HV\_IO}$ = 3.3 V ± 5% C_L = 10 pF	—	—	48	

1. *Average consumption in one pad toggling cycle.*

2. *The IOs supply are well distributed around the device to sustain the different drive capability of each pad. The only limitation is related (for all packages) to the Very Fast configuration for the segment including JTAG pads till PAD_PG[5..12] pads: PAD_PG[5..12] can be configured in Very Fast mode, toggling in the same time, but JTAG pads to be not used, or vice versa.*
3. *Stated maximum values represent peak consumption that lasts only a few ns during I/O transition. When possible (timed output) it is recommended to delay transition between pads by few cycles to reduce noise and consumption.*

Related links

3.2 Absolute maximum ratings on page 11
3.3 Operating conditions on page 12

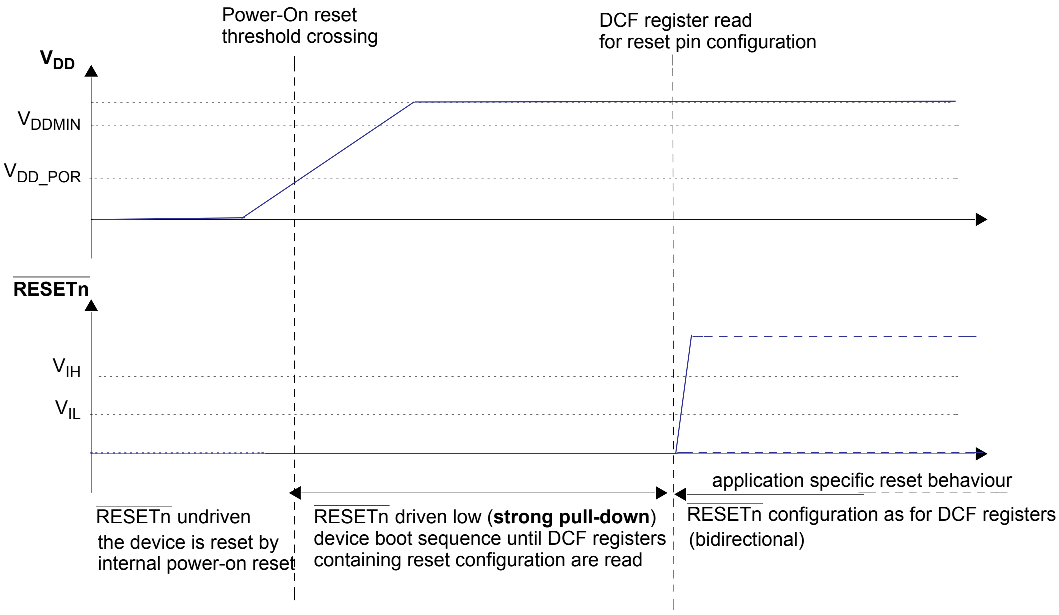
3.9 Reset pad (RESETn) electrical characteristics

The device implements a reset pin pad: RESETn is configured as Reset Input/Output.

Configuration is read during the boot initialization process as described in the device reference manual, Reset and boot chapter. When samples are delivered, in the default configuration, RESETn pin does not require active control.

The following figure describes RESETn behavior during the power-up sequence.

Figure 6. RESETn behavior during power-up sequence



The RESETn pin implements an input filtering mechanism. The following figure describes the possible conditions:

1. Low pulse has too low amplitude: it is filtered by input buffer hysteresis. The device remains in current state.
2. Low pulse has too short duration: it is filtered by low pass filter. The device remains in current state.
3. Low pulse is generating a reset:
   a. Signal is low but initially filtered during at least W_{FRST}. The device remains initially in current state.
   b. Signal potentially filtered until W_{NFRST}. The device state is unknown. It may be under reset or still be in the previous mode depending on extra condition (temperature, voltage, device).
   c. Signal asserted for longer than W_{NFRST}. The device is under reset.

Figure 7. Input reset filter

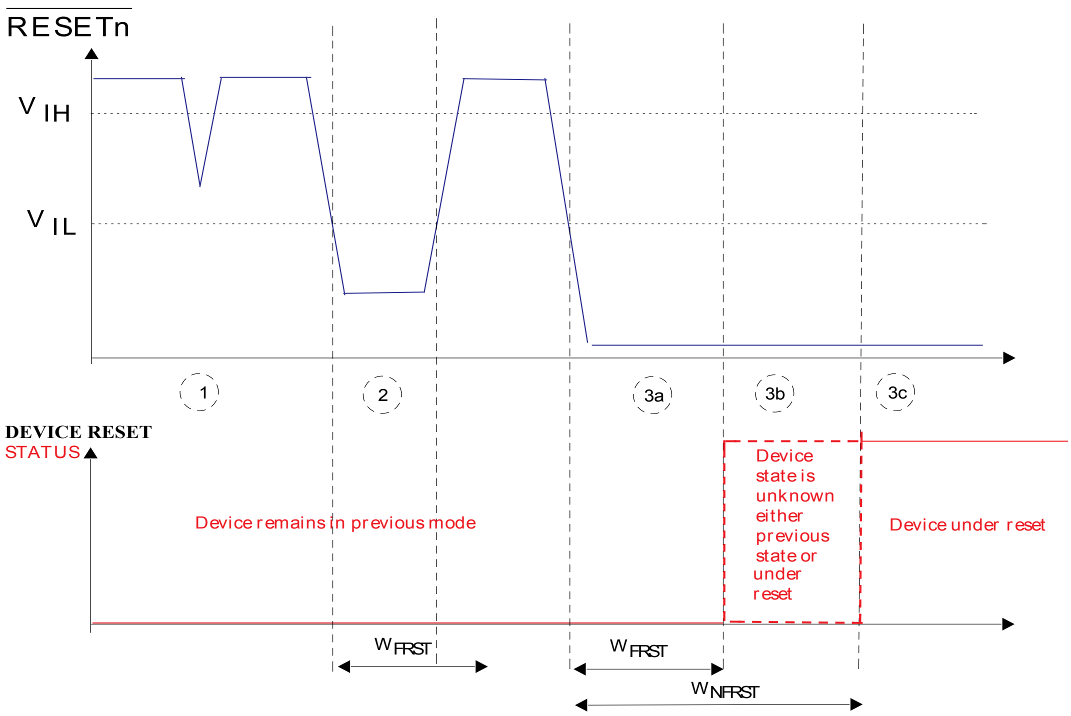


Table 19. Reset pad electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IHRES}	SR	P	Input high level TTL	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	2	—	$V_{DD\_HV\_IO}$+0.3	V
V_{ILRES}	SR	P	Input low level TTL	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	-0.3	—	0.8	V
V_{HYSRES}	CC	C	Input hysteresis TTL	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	0.3	—	—	V
V_{DD_POR}	CC	D	Minimum supply for strong pull-down activation	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	—	—	1.6	V
I_{OL_R}	CC	P	Strong pull-down current(1)	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	3	—	—	mA
I_{WPU}	CC	P	Weak pull-up current absolute value	V_{IN} = 1.1 V(2) $V_{DD\_HV\_IO}$ = 3.3 V ± 5%	15	—	130	µA
I_{WPD}	CC	P	Weak pull-down current absolute value	V_{IN} = 0.9 V(2)(3) $V_{DD\_HV\_IO}$ = 3.3 V ± 5%	15	—	130	µA
W_{FRST}	CC	P	Input filtered pulse	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	—	—	500	ns
W_{NFRST}	CC	P	Input not filtered pulse	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	2000	—	—	ns

1. *I_{OL_R} applies to RESETn: strong pull-down is active until the DCF containing the RESETn configuration is read. Refer to the device reference manual, Reset and boot chapter.*
2. *Maximum current when forcing a change in the pin level opposite to the pull configuration.*
3. *Minimum current when keeping the same pin level state as the pull configuration.*

Table 20. **RESETn settings**

Input conditions		Behavior (set at power-on)		
Life cycle	DCF RESET_CFG [RESN_PDOWN_EN] Description : RESETn pull-down enable	From power on till DCFs are read	Any non-power on reset phase (either destructive or functional) after internal RESETOUT release	SW Run time
ST production, customer delivery	NOT programmed	Strong pull-down	Bidirectional with weak pull-up Pad level as forced from outside	
OEM production, in-field, failure analysis	NOT programmed	Strong pull-down	Bidirectional with weak pull-down Pad level as forced from outside	
Don’t care	Programmed to 0	Strong pull-down	Bidirectional with weak pull-down Pad level as forced from outside	

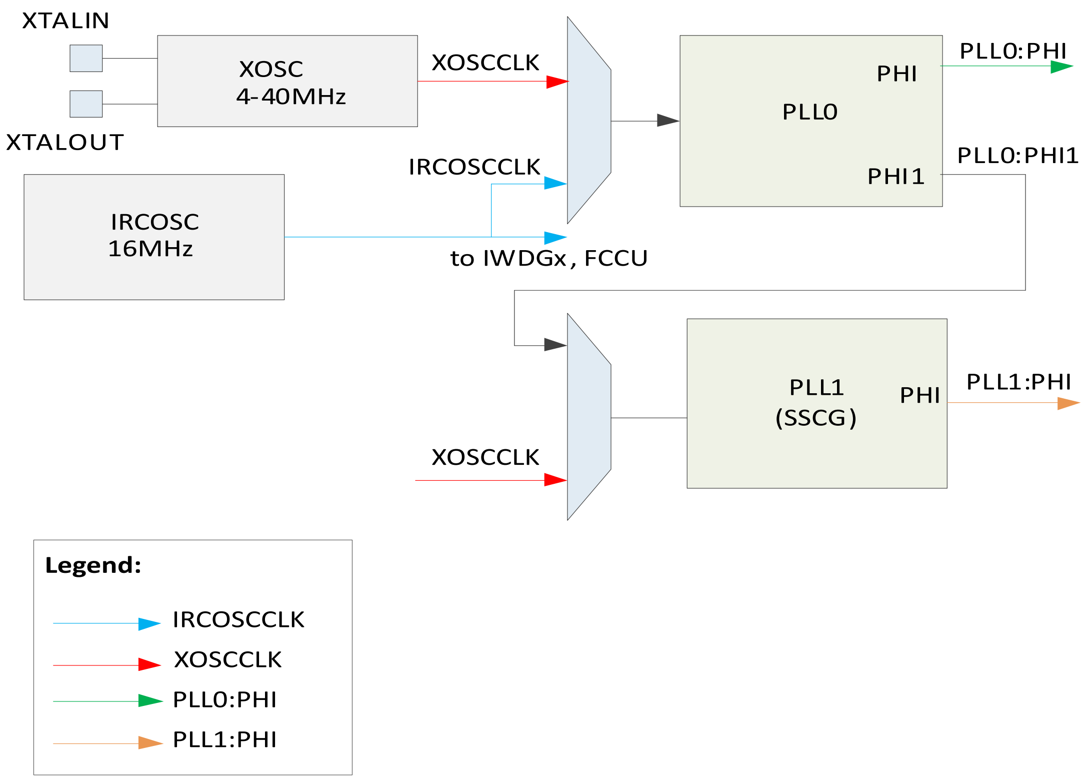
When the reset pin is configured as reset bidirectional with weak pull-down capability, it is possible to drive the pin with an external pull-up to ensure correct reset exit sequence. Recommended value is 4.7 KΩ.

3.10 PLLs

Two phase-locked loop (PLL) modules are implemented to generate system and auxiliary clocks on the device.

The figure below depicts the integration of the two PLLs. Refer to device reference manual for more detailed schematic.

Figure 8. PLLs integration



3.10.1 PLL0

Table 21. PLL0 electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{PLL0IN}	SR	—	PLL0 input clock[1]	—	8	—	56[2]	MHz
Δ_{PLL0IN}	SR	—	PLL0 input clock duty cycle[1]	—	40	—	60	%
f_{INFIN}	SR	C	PLL0 PFD (phase frequency detector) input clock frequency	—	8	—	20	MHz
$f_{PLL0VCO}$	CC	P	PLL0 VCO frequency	—	600	—	1400	MHz
$f_{PLL0PHI0}$	CC	D	PLL0 output frequency	—	4.7620	—	700	MHz
$f_{PLL0PHI1}$	CC	D	PLL0 output clock PHI1	—	20	—	175[3]	MHz
$t_{PLL0LOCK}$	CC	P	PLL0 lock time	—	—	—	100	µs
$\|\Delta_{PLL0PHISPJ}\|$	CC	T	PLL0_PHI single period jitter f_{PLL0IN} = 8 MHz (resonator)	$f_{PLL0PHI}$ = 16 MHz, 6-sigma pk-pk	—	—	435	ps
$\|\Delta_{PLL0PHI1SPJ}\|$	CC	T	PLL0_PHI1 single period jitter f_{PLL0IN} = 8 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma pk-pk	—	—	210	ps
$\Delta_{PLL0LTJ}$	CC	T	PLL0 output long term jitter f_{PLL0IN} = 8 MHz (resonator) VCO frequency = 640 MHz	long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk)	—	—	±500	ps
I_{PLL0}	CC	T	PLL0 consumption	FINE LOCK state	—	—	5.4	mA

1. *PLL0IN clock retrieved directly from either internal IRCOSC or external XOSC clock. Input characteristics are granted when using internal oscillator or external oscillator is used in functional mode.*
2. *Since XOSC max frequency is 40 MHz, the 40-56 MHz range can only be reached with external reference clock (XOSC bypass).*
3. *If the PLL0_PHI1 is used as an input for PLL1, then the PLL0_PHI1 frequency obeys to the maximum input frequency limit set for PLL1 (refer to f_{PLL1IN} in Table 22. PLL1 electrical characteristics).*

Related links

3.10.2 PLL1 on page 31

3.10.2 PLL1

PLL1 is a frequency modulated PLL with spread spectrum clock generation (SSCG) support.

Table 22. PLL1 electrical characteristics

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
f_{PLL1IN}	SR	—	PLL1 input clock[1]	—	37.5	—	87.5	MHz
Δ_{PLL1IN}	SR	—	PLL1 input clock duty cycle[1]	—	35	—	65	%
f_{INFIN}	SR	C	PLL1 PFD (phase frequency detector) input clock frequency	—	37.5		87.5	MHz
$f_{PLL1VCO}$	CC	P	PLL1 VCO frequency	—	600	—	1400	MHz
$f_{PLL1PHI}$	CC	D	PLL1 output clock PHI	—	4.762	—	700	MHz
$t_{PLL1LOCK}$	CC	P	PLL1 lock time	—	—	—	50	µs
$f_{PLL1MOD}$	CC	T	PLL1 modulation frequency	—	—	—	250	kHz
$\|\delta_{PLL1MOD}\|$	CC	T	PLL1 modulation depth (when enabled)	Center spread[2]	0.25	—	2	%
				Down spread	0.5	—	4	%
$\|\Delta_{PLL1PHISPJ}\|$	CC	T	PLL1_PHI single period peak to peak jitter with modulation activated (md = ± 2%)	$f_{PLL1PHI}$ = 300 MHz, 6-sigma pk-pk	—	—	250	ps
I_{PLL1}	CC	T	PLL1 consumption	FINE LOCK state	—	—	6.25	mA

1. *PLL1IN clock retrieved directly from either internal PLL0 or external FXOSC clock. Input characteristics are granted when using internal PPL0 or external oscillator is used in functional mode.*
2. *The device maximum operating frequency F_{SYS} (max) includes the frequency modulation. If center modulation is selected, the FSYS must be below the maximum by MD (modulation depth percentage), such that $FSYS(\max) = FSYS(1 + MD\,\%)$. Refer to the device reference manual for the PLL programming details.*

Related links

3.10.1 PLL0 on page 30

3.11 Oscillators

3.11.1 Low speed internal RC oscillator (LSI)

Table 23. 1024 kHz internal RC oscillator electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
F_{sirc}	CC	T	Slow internal RC oscillator frequency	—	—	1024	—	kHz
df_{var_T}	CC	P	Frequency variation across temperature	–40 °C < T < 150 °C	–9	—	+9	%
df_{var_V}	CC	P	Frequency variation across voltage	—	–5	—	+5	%
I_{sirc}	CC	D	Slow internal RC oscillator current	T = 55 °C	—	—	6	μA
T_{sirc}	CC	D	Start up time, after switching ON the internal regulator.	—	—	—	12	μS

3.11.2 External crystal oscillator 40 MHz (XOSC)

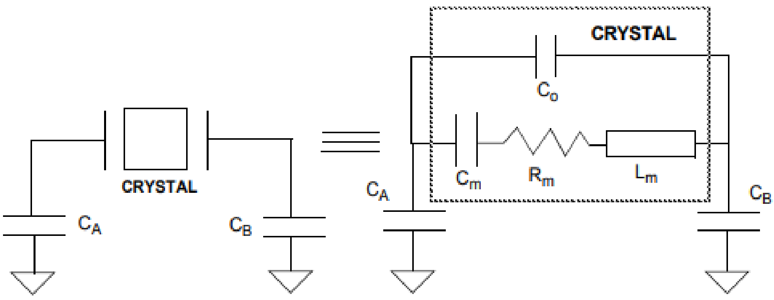
Table 24. External 40 MHz oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{XTAL}	CC	D	Crystal frequency range[1][2][3]	XOSC_freq_sel[1:0]= 00	4	—	10	MHz
				XOSC_freq_sel[1:0]= 01	10	—	20	
				XOSC_freq_sel[1:0]= 10	20	—	30	
				XOSC_freq_sel[1:0]= 11	30	—	40	
f_{EXTAL}	SR	T	External frequency range (bypass)	—	—	—	100	MHz
t_{cst}	CC	D	Crystal startup time[4][5]	4MHz-10MHz	—	—	12	ms
				10MHz-20MHz	—	—	7.5	
				20MHz-30MHz	—	—	6	
		T		30MHz-40MHz	—	—	5	
t_{rec}	CC	D	Crystal recovery time[6]	—	—	—	as startup time	ms
V_{IHEXT}	CC	D	EXTAL input high voltage (external reference)[7]	—	$V_{DD\_HV\_OSC}$ - 0.6	—	—	V
V_{ILEXT}	CC	D	EXTAL input low voltage (external reference)[7]	—	—	—	0.6	V
C_{S_EXTAL}	CC	D	Total on-chip stray capacitance on EXTAL pin[8]	Cpar = C_IPinternal + C_IOs	5.6	7	8.4	pF
C_{S_XTAL}	CC	D	Total on-chip stray capacitance on XTAL pin[8]	Cpar = C_IPinternal + C_IOs	5.6	7	8.4	pF
g_m	CC	P	Oscillator transconductance	T_J = –40 °C to 150 °C, f_{XTAL} = 4 - 10 MHz, XOSC_freq_sel[1:0]= 00	2.73	—	9.77	mA/V
		D		T_J = –40 °C to 150 °C f_{XTAL} = 10 - 20 MHz XOSC_freq_sel[1:0]= 01	5.70	—	20.50	
		D		T_J = –40 °C to 150 °C f_{XTAL} = 20 - 30 MHz XOSC_freq_sel[1:0]= 10	9.73	—	34.50	

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
g_m	CC	P	Oscillator transconductance	T_J = –40 °C to 150 °C f_{XTAL} = 30 - 40 MHz XOSC_freq_sel[1:0]= 11	12.70	—	46.15	mA/V
V_{XTAL}	CC	T	Oscillation amplitude on the XTAL pin after startup(9)	T_J = –40 °C to 150 °C, pk-pk @40MHz	0.5	—	$V_{DD\_HV\_OSC}$	V

1. *The range is selectable by UTEST miscellaneous DCF clients XOSC_FREQUENCY [1:0].*
2. *Refer to Table 25. Crystal parameters and load conditions for supported crystal parameters and load conditions.*
3. *The XTAL frequency, if used to feed the PLL0 (or PLL1), has to obey the minimum input frequency limit set for PLL0 (or PLL1).*
4. *Proper PC board layout procedures must be followed to achieve these specifications.*
5. *This value is determined by the crystal manufacturer and board design.*
6. *Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.*
7. *Applies to an external clock input and not to crystal mode.*
8. *See the crystal manufacturer's specification for recommended load capacitor (C_L) values. Total capacitance on XTAL net must be 2*C_L. On-chip stray capacitance (CS_EXTAL/CS_XTAL) and PCB capacitance must be accounted when selecting a load capacitor value. External capacitance or integrated load capacitor value can be used. Integrated load capacitance can be selected via software to match the crystal manufacturer's specification. The stray capacitance (Cpar) on chip value here reported, takes into account the sum of total parasitic capacitance inside the SOC (IP, routing inside SOC, IO pad) + package.*
9. *Amplitude on the XTAL pin after startup is determined by the automatic level control circuit (ALC) block. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation to reduce power, distortion, and RFI, and to avoid over driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.*

Figure 9. Equivalent mode of crystal



- C_0 is the shunt or static capacitance of the crystal. The parameter equals the sum of capacitance measured from pin to pin, including the electrode and the mounting structure. This capacitance is usually specified as a maximum value, for example, 2 pF maximum.
- L_m, R_m, and C_m are in the motional arm of the crystal. Their circuit affects only exist when the crystal is oscillating.
  - L_m, the motional inductance, is determined by the mechanical mass of quartz in motion.
  - C_m is determined by the stiffness of the quartz (constant), the area of the electrode, and the thickness and shape of the quartz wafer. C_m is dependent on the specified frequency of the crystal. C_m is usually less than 0.02 pF.
  - R_m is the equivalent series resistance when oscillating. It is a function of mechanical losses during vibration. Low resistance indicates low mechanical losses. The lower the resistance is, the more easily the crystal oscillates. R_m is usually specified as a maximum value, for example, 50 maximum.

Internal trimmable capacitance

Two capacitance blocks are connected between A and AGND and ZO and AGND inside the oscillator. For the internal capacitance array to be selected, ext_cload_en should be low.

Capacitance is implemented using metal fringe.

The capacitance offered by this array is decided by load_cap_sel[4:0].

The formula to calculate the capacitance offered is C_var = n.Cu

Where,

- Cu = unit capacitance (for a typical corner, Cu = 0.48 pF. Across the process, the variation is ± 10%)
- n = load_cap_sel[4] × 2^4 + load_cap_sel[3] × 2^3 + load_cap_sel[2] × 2^2 + load_cap_sel[1] × 2^1 + load_cap_sel[0] × 2^0

For example:

- For load_cap_sel[4:0]=00000, C_var = 0 pF at A & ZO each.
- For load_cap_sel[4:0]=10000, C_var = 7.68 pF at A & ZO each.
- For load_cap_sel[4:0]=11111, C_var = 14.88 pF at A & ZO each.

Refer to the UTEST miscellaneous DCF client described in the device reference manual (chapter Device configuration format DCF records).

Table 25. Crystal parameters and load conditions

Crystal frequency range (MHz)[1]	Maximum crystal ESR supported (Ω)[2]	C_0 (max) (pF)[2][3]	C_L (min) (pF)[2]	C_L (max) (pF)[2]	Drive level (max) (µW)
4-10	220	2	5	10	100
10-20	120	2	5	10	200
20-30	80	2	5	6	200
			7	8	250
			9	10	300
30-40	50	2	5	5	200
			6	7	250
			8	8	300

1. *Crystal frequency range values are related to F_{XTAL} defined by freq_sel[1:0] settings (refer to Table 24. External 40 MHz oscillator electrical specifications)*
2. *Where:*
   - $ESR = R_m \times \left(1 + \frac{C_0}{C_L}\right)^2$
   - *C_L is the load capacitance.*
   - *C_0 is the shunt capacitance.*
   - *$C_A = C_B = 2 \times C_L$.*
3. *C_A, C_B, and C_0 include the parasitic capacitance due to the crystal, PCB board traces, package parasitics etc.*

3.11.3 Internal RC 16 MHz oscillator (IRCOSC)

Table 26. Internal RC oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{Target}	CC	D	IRC target frequency	—	—	16	—	MHz
δf_{var_noT}	CC	P	IRC frequency variation without temperature compensation	T < 150 °C	-5	—	5	%
δf_{var_T}	CC	T	IRC frequency variation with temperature compensation	T < 150 °C	-3	—	3	%
δf_{var_SW}	—	T	IRC software trimming accuracy	Trimming temperature	-0.5	±0.3	0.5	%
T_{start_noT}	CC	T	Startup time to reach within f_{var_noT}	Factory trimming already applied	—	—	5	µs
T_{start_T}	CC	T	Startup time to reach within f_{var_T}	Factory trimming already applied	—	—	120	µs
I_{FIRC}	CC	T	Current consumption on analog power supply[1]	After T_{start_T}	—	—	1600	µA

1. *The additional contribution of the core logic clocked by the RCOSC16M affects the RCOSC16M consumption. This core logic cannot be turned off during the measurement at device level.*
   In any case, the design specifies the parameter at 1200 µA.

3.12 Analog subsystem

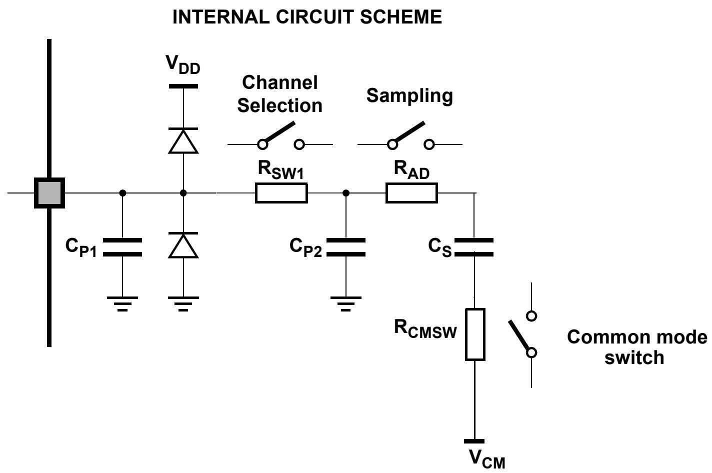
The SR5E1E3, SR5E1E5, SR5E1E7 analog subsystem contains:

- 5 SARADC modules with up to eight channels coming from pads,
- 2 SDADC modules,
- 8 Fast-DACs,
- 8 analog comparators,
- 2 buffered-DACs that is with buffer to bring analog output on pads,
- 1 temperature sensor,
- 1 ADCBIAS_COMP module to generate 4 reference voltages for runtime diagnosis of comparators,
- 1 ADCBIAS_SAR module to generate 4 reference voltages for runtime diagnosis of SAR_ADCs in single ended mode.

3.12.1 ADC input description

The figure below shows the input equivalent circuit for SARn channels.

Figure 10. Input equivalent circuit (Fast SARn channels)



R_{SW1}: Channel Selection Switch Impedance
R_{AD}: Sampling Switch Impedance
C_P: Pin Capacitance (two contributions, C_{P1} and C_{P2})
C_S: Sampling Capacitance
R_{CMSW}: Common mode switch
V_{CM}: Common mode voltage (~0.5 V_{DD})

The above figure can be used as approximation circuitry for external filtering definition.

Note:
- *For input leakage current, refer to I_{LKG} in Section 3.8.1: I/O input DC characteristics,*
- *For injection current 1, refer to I_{INJ1} in Section 3.3: Operating conditions,*
- *For pad capacitance 1, refer to C_{P1} in Section 3.8.1: I/O input DC characteristics.*

Table 27. ADC pin specification

Symbol (1)		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
C_{P2}	CC	D	Internal routing capacitance	SARn 12-bit channels	—	—	700	fF
C_S	CC	D	SAR ADC sampling capacitance	SARn 12-bit	—	—	2	pF
R_{SW1}	CC	D	Analog switches resistance	SARn 12-bit channels	0	—	3	kΩ
R_{AD}	CC	D	ADC input analog switches resistance	SARn 12-bit	—	—	1.2	kΩ
R_{CMSW}	CC	D	Common mode switch resistance	Sum of the two resistances	—	—	1	kΩ
R_{SAFEPD}	CC	D	Discharge resistance for ADC input-only pins (strong pull-down for safety)	$V_{DD\_HV\_IO}$ = 3.3 V ± 5%	—	—	3	kΩ

1. *All specifications in this table valid for the full input voltage range for the analog inputs.*

Related links

3.2 Absolute maximum ratings on page 11
3.3 Operating conditions on page 12
3.8.1 I/O input DC characteristics on page 18
3.12.2 SARADC 12-bit electrical specification on page 36
3.13.1 Power management integration on page 52

3.12.2 SARADC 12-bit electrical specification

The SARn ADCs are 12-bit successive approximation register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

Table 28. SARn ADC electrical specification

Symbol (1)		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IN}	SR	D	Full scale input range	Single ended	HV_REFL_SAR	—	HV_REFH_SAR	V
				Differential ended	2*(HV_REFH_SAR – HV_REFL_SAR)			$V_{PP\ DIFF}$
V_{IN_COM}	SR	D	Input signal common mode	Only in differential mode	[HV_REFH_SAR + HV_REFL_SAR/2] – 10%	[HV_REFH_SAR + HV_REFL_SAR/2]	[HV_REFH_SAR + HV_REFL_SAR/2] + 10%	V
f_{ADCK}	SR	P	Clock frequency	—(2)	—	—	40	MHz
$t_{ADCINIT}$	CC	D	Setting time	—	—	—	4	µs
$t_{ADCBIASINIT}$	CC	D	Bias setting time	—	—	—	4	µs
ΔV_{PRECH}	SR	D	Dis-charge voltage precision	T_J < 150 °C	0	—	TBD	V
$t_{ADCSAMPLE}$	SR	T	ADC sample time(3)	Fast channels	$3.5/f_{ADCK}$(4)	—	$640.5/f_{ADCK}$	µs
		T		Slow channels	$12.5/f_{ADCK}$	—		
		D		Conversion of BIAS test channels through 20 kΩ input.	$67/f_{ADCK}$	—		
$t_{ADCVREG\_STUP}$	CC	D	ADC voltage regulator start-up time	From enadc=L, enldo=L to enadc=L, enldo=H (LDO start-up Tup_ldo)	—	—	10	µs

Symbol [1]		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$t_{ADCEVAL}$[5]	SR	D	ADC evaluation time	12-bit configuration	$12.5/f_{ADCK}$	—	—	µs
		D		10-bit configuration	$10.5/f_{ADCK}$	—	—	
I_{ADV_S}	CC	P	$V_{DD\_HV\_SAR}$ power supply current	Run mode (for each ADC)	—	—	0.46	mA
		D		Power down mode (for each ADC)	—	—	0.01	
TUE_{12}[6]	CC	P	Total unadjusted error in 12-bit configuration[7]	T_J < 150 °C in all conditions	-7	—	7	LSB (12b)
TUE_{10}[6]	CC	D	Total unadjusted error in 10-bit configuration[7]	T_J < 150 °C in all conditions	-4	—	4	LSB (10b)
TUE_{INJ2}	CC	T	TUE degradation addition, due to current injection in I_{INJ2} range[8]	See Table 4. Absolute maximum ratings, I_{INJ2} parameter.	+10			LSB
DNL[7]	CC	P	Differential non-linearity	In all $V_{DD\_HV\_SAR}$ voltage range.	-1	—	2	LSB (12b)

1. *Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device. All specifications in this table are valid for one ADC operating at a time.*
2. *Max frequency can be reached under specific device clocks configuration. Refer to the device reference manual, Clocking chapter for details.*
3. *Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Refer to Figure 10. Input equivalent circuit (Fast SARn channels) for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.*
4. *The minimum sampling time of 2.5 ADC clock cycles requires the setting of the ADC_SMPR1.SMPPLUS bit to 1. The overal minimum sampling time is $3.5/f_{ADCK}$ µs.*
5. *It is referring to the "successive approximation time (Tsar)" defined in the device reference manual, ADC timing chapter.*
6. *After calibration.*
7. *TUE and DNL are granted with injection current within the range defined in Table 27. ADC pin specification for parameters classified as T and D.*
8. *All channels of all SARADC12bit are impacted with same degradation, independently from the ADC and the channel subject to current injection.*

Related links

3.2 Absolute maximum ratings on page 11
3.12.1 ADC input description on page 35

3.12.3 SDADC electrical specification

The SDn ADCs are sigma delta 16-bit analog-to-digital converters with up to 300 Ksps output rate.

Note: The SDADCs are not available in the eTQFP100 package.

Table 29. SDn ADC electrical specification

Symbol [1]		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
V_{IN_PK2PK} [2]	SR	D	Input range peak to peak $V_{IN\_PK2PK} = V_{INP}$[3] – V_{INM}[4]	Single ended $V_{INM} = V_{SS}$	$V_{DD\_HV\_SD\_DAC\_COMP}$/GAIN			V
		D		Single ended V_{INM} = 0.5*HV_REFH_SD GAIN = 1	±0.5*HV_REFH_SD			
		D		Single ended V_{INM} = 0.5*HV_REFH_SD GAIN = 2, 4, 8, 16	±HV_REFH_SD/GAIN			
		D		Differential, $0 < V_{IN} < V_{DD\_HV\_IO}$	±HV_REFH_SD/GAIN			
f_{ADCD_M}	SR	P	S/D modulator input Clock 3[5]	T_J < 150 °C	14.4	—	16	MHz
f_{IN}	SR	P	Input signal frequency	—	0.01	—	75[6]	KHz
f_{ADCD_S}	SR	D	Output conversion rate	Default filter mode[7] effective OSR = 24	—	—	333	ksps
				Bypass FIR Mode[7] effective OSR = 24	—	—	333	
—	CC	D	Oversampling ratio	Internal modulator	24	—	256	—
				External modulator	—	—	256	—
RESOLUTION	CC	D	S/D register resolution	2's complement notation	16			bit
GAIN	SR	D	ADC gain	Defined via ADC_SD[PGA] register. Only integer powers of 2 are valid gain values.	1	—	16	—
$\|\delta_{GAIN}\|$	CC	C	Absolute value of the ADC gain error[8](10)	Before calibration (applies to gain setting = 1)	—	—	1	%
		T		After calibration, ΔHV_REFH_SD < 10% $\Delta V_{DD\_HV\_SD\_DAC\_COMP}$ < 10% –40 °C < T_J < 150 °C	—	—	8	mV
V_{OFFSET}	CC	P	Conversion offset[8](9)(10)	Before calibration GAIN = 1	—	9*(1+1/gain)	20	mV
		T		Before calibration GAIN = 2, 4, 8, 16	—	10*(1+1/gain)	20	
		D		After calibration, ΔHV_REFH_SD < 10% –40 °C < T_J < 150 °C	—	—	5	mV
$SNR_{DIFF150}$	CC	P	Signal to noise ratio in differential mode 150 ksps output rate	In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 1 T_J < 150 °C	80[11]	—	—	dBFS

Symbol [1]		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$SNR_{DIFF150}$	CC	C	Signal to noise ratio in differential mode 150 ksps output rate	In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 2 T_J < 150 °C	77	—	—	dBFS
		C		In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 4 T_J < 150 °C	74	—	—	
		C		In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 8 T_J < 150 °C	71	—	—	
		D		In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 16 T_J < 150 °C	68	—	—	
$SNR_{DIFF333}$	CC	P	Signal to noise ratio in differential mode 333 ksps output rate	In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 1 T_J < 150 °C	71 [11]	—	—	dBFS
		C		In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 2 T_J < 150 °C	68	—	—	
		C		In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 4 T_J < 150 °C	65	—	—	
		C		In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 8 T_J < 150 °C	62	—	—	
		D		In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 16 T_J < 150 °C	60	—	—	

Symbol [1]		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
SNR_{SE333}	CC	P	Signal to noise ratio in single ended mode 333 ksps output rate	In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 1 T_J < 150 °C	65[11]	—	—	dBFS
		C		In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 2 T_J < 150 °C	62	—	—	
		C		In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 4 T_J < 150 °C	59	—	—	
		C		In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 8 T_J < 150 °C	56	—	—	
		D		In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 16 T_J < 150 °C	54	—	—	
SNR_{SE150}	CC	P	Signal to noise ratio in single ended mode 150 ksps output rate	In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 1 T_J < 150 °C	74[11]	—	—	dBFS
		C		In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 2 T_J < 150 °C	71	—	—	
				In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 4 T_J < 150 °C	68	—	—	
				In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 8 T_J < 150 °C	65	—	—	

Symbol [1]		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
SNR_{SE150}	CC	D	Signal to noise ratio in single ended mode 150 ksps output rate	In all $V_{DD\_HV\_SD\_DAC\_COMP}$ supply range. HV_REFH_SD = $V_{DD\_HV\_SD\_DAC\_COMP}$ GAIN = 16 T_J < 150 °C	62	—	—	dBFS
$\Delta_{SNRINJ2}$	CC	T	SNR degradation addition, due to current injection in I_{INJ2} range.	See Table 4. Absolute maximum ratings, I_{INJ2} parameter[12]	—	—	TBD	dBFS
SFDR	CC	P	Spurious free dynamic range	GAIN = 1	60	—	—	dBc
		C		GAIN = 2	60	—	—	
		C		GAIN = 4	60	—	—	
		C		GAIN = 8	60	—	—	
		D		GAIN = 16	60	—	—	
Z_{DIFF}	CC	D	Differential input impedance (f_{ADCD_M} = 8 MHz)	GAIN = 1	360	450	540	kΩ
		D		GAIN = 2	224	280	336	
		D		GAIN = 4	128	160	192	
		D		GAIN = 8	65	85	105	
		D		GAIN = 16	65	85	105	
Z_{CM}	CC	D	Common mode input impedance (f_{ADCD_M} = 8 MHz)	GAIN = 1	450	560	670	kΩ
		D		GAIN = 2	340	430	520	
		D		GAIN = 4	250	310	370	
		D		GAIN = 8	170	210	250	
		D		GAIN = 16	170	210	250	
R_{BIAS}	CC	D	Bias resistance	—	120	160	200	kΩ
ΔR_{BIAS}	CC	D	R_{BIAS} positive/negative terminal impedance mismatch	—	-5	—	+5	%
V_{BIAS}	CC	D	Bias voltage	—	—	$(V_{DD\_HV\_SD\_DAC\_COMP} - V_{SS})/2$	—	V
ΔV_{INTCM}	CC	D	Common mode input reference voltage	—	–12	$(V_{DD\_HV\_SD\_DAC\_COMP} + V_{SS})/2$	+12	%
δV_{BIAS}	CC	D	Bias voltage accuracy	—	–2.5	—	+2.5	%
V_{cmrr}	CC	T	Common mode rejection ratio	—	50	—	—	dB
R_{Caaf}	SR	D	Anti-aliasing filter	External series resistance	—	—	20	kΩ
	CC	D		Filter capacitances	180	—	—	pF
$f_{PASSBAND}$	CC	D	Pass band[13]	Default filter mode Bypass FIR mode	0.01	—	0.333 * f_{ADCD_S}	kHz
				Modified bandwidth mode		—	0.166 * f_{ADCD_S}	
				External filter mode (OSR = 75)		—	0.066 * f_{ADCD_S}	
				External filter mode (All OSR, expect 75)		—	0.083 * f_{ADCD_S}	

Symbol (1)		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
δ_{RIPPLE}	CC	D	Pass band ripple(14)	0.333 * f_{ADCD_S}	–1	—	1	%
$F_{rolloff}$	CC	D	Stop band attenuation Default filter mode(15)	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	1	—	—	dB
				[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	40	—	—	
				[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	47	—	—	
				[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	54	—	—	
				[2.5 * f_{ADCD_S}, f_{ADCD_M}/2]	64	—	—	
$F_{rolloff}$	CC	D	Stop band attenuation Modified bandwidth mode(15)	[0.25 * f_{ADCD_S}, 0.5 * f_{ADCD_S}]	40	—	—	dB
				[0.5 * f_{ADCD_S}, 0.75 * f_{ADCD_S}]	55	—	—	
				[0.75 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	86	—	—	
				[1.0 * f_{ADCD_S}, 1.25 * f_{ADCD_S}]	109	—	—	
				[1.25 * f_{ADCD_S}, f_{ADCD_M}/2]	99	—	—	
$F_{rolloff}$	CC	D	Stop band attenuation External filter mode(15)	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	2	—	—	dB
				[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	11	—	—	
				[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	31	—	—	
				[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	44	—	—	
				[2.5 * f_{ADCD_S}, f_{ADCD_M}/2]	39	—	—	
$F_{rolloff}$	CC	D	Stop band attenuation Bypass FIR mode(15)	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	3	—	—	dB
				[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	15	—	—	
				[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	41	—	—	
				[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	59	—	—	
				[2.5 * f_{ADCD_S}, f_{ADCD_M}/2]	52	—	—	
δ_{GROUP}	CC	D	Group delay Default filter mode(15)	Within pass band – Tclk is time period of f_{ADCD_M} /2 freq. = 2/ f_{ADCD_M}	—	—	—	—
				OSR = 24	—	—	197.9	Tclk
				OSR = 28	—	—	230	
				OSR = 32	—	—	262.1	
				OSR = 36	—	—	294.2	
				OSR = 40	—	—	326.3	
				OSR = 44	—	—	358.4	
				OSR = 48	—	—	390.4	
				OSR = 56	—	—	454.6	
				OSR = 64	—	—	518.8	
				OSR = 72	—	—	582.9	
				OSR = 80	—	—	647.1	
				OSR = 88	—	—	711.3	
				OSR = 96	—	—	775.4	
				OSR = 112	—	—	903.8	
				OSR = 128	—	—	1032.1	

Symbol (1)		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
δ_{GROUP}	CC	D	Group delay Default filter mode(15)	OSR = 144	—	—	1160.4	Tclk
				OSR = 160	—	—	1288.8	
				OSR = 176	—	—	1417.1	
				OSR = 192	—	—	1545.4	
				OSR = 224	—	—	1802.1	
				OSR = 256	—	—	2058.8	
				OSR = 512	—	—	4112.1	
				OSR = 1024	—	—	8218.7	
δ_{GROUP}	CC	D	Group delay Modified bandwidth mode(15)	Within pass band – Tclk is time period of f_{ADCD_M} /2 freq. = 2/ f_{ADCD_M}	—	—	—	—
				OSR = 24	—	—	217.3	Tclk
				OSR = 28	—	—	252	
				OSR = 32	—	—	286.6	
				OSR = 36	—	—	321.3	
				OSR = 40	—	—	355.9	
				OSR = 44	—	—	390.6	
				OSR = 48	—	—	425.3	
				OSR = 56	—	—	494.6	
				OSR = 64	—	—	563.9	
				OSR = 72	—	—	633.3	
				OSR = 80	—	—	702.6	
				OSR = 88	—	—	771.9	
				OSR = 96	—	—	841.3	
				OSR = 112	—	—	979.9	
				OSR = 128	—	—	1118.6	
				OSR = 144	—	—	1257.3	
				OSR = 160	—	—	1395.9	
				OSR = 176	—	—	1534.6	
				OSR = 192	—	—	1673.2	
				OSR = 224	—	—	1950.6	
				OSR = 256	—	—	2227.9	
				OSR = 512	—	—	4446.5	
				OSR = 1024	—	—	8883.7	
δ_{GROUP}	CC	D	Group delay Bypass FIR mode(15)	Within pass band – Tclk is time period of f_{ADCD_M} /2 freq. = 2/ f_{ADCD_M}	—	—	—	—
				OSR = 24	—	—	73.7	Tclk
				OSR = 28	—	—	85.2	
				OSR = 32	—	—	96.8	
				OSR = 36	—	—	108.4	

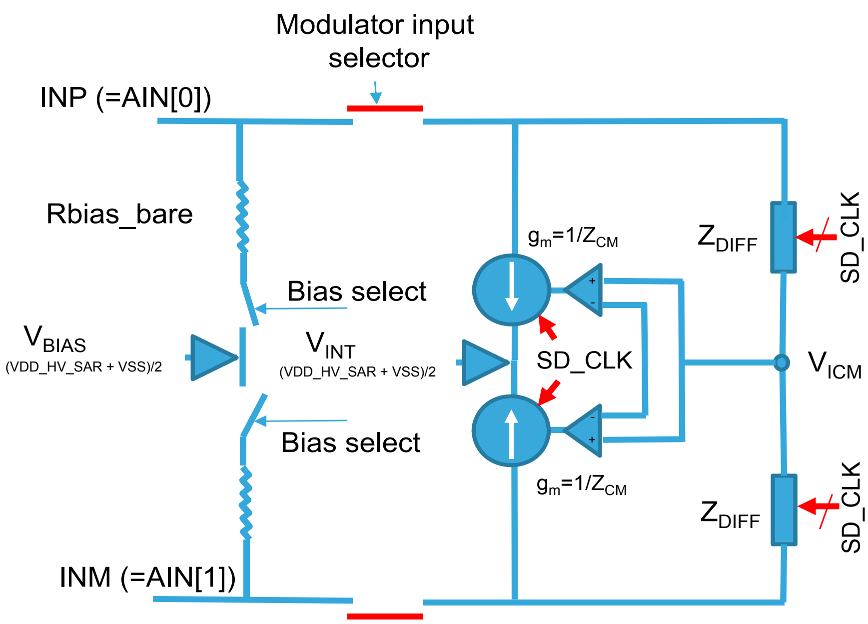
Symbol [1]	C		Parameter	Conditions	Value			Unit
					Min	Typ	Max	
δ_{GROUP}	CC	D	Group delay Bypass FIR mode[15]	OSR = 40	—	—	119.9	Tclk
				OSR = 44	—	—	131.5	
				OSR = 48	—	—	143.1	
				OSR = 56	—	—	166.2	
				OSR = 64	—	—	189.3	
				OSR = 72	—	—	212.4	
				OSR = 80	—	—	235.6	
				OSR = 88	—	—	258.7	
				OSR = 96	—	—	281.8	
				OSR = 112	—	—	328.1	
				OSR = 128	—	—	374.4	
				OSR = 144	—	—	420.6	
				OSR = 160	—	—	466.9	
				OSR = 176	—	—	513.1	
				OSR = 192	—	—	559.4	
				OSR = 224	—	—	651.9	
				OSR = 256	—	—	744.4	
				OSR = 512	—	—	1484.6	
				OSR = 1024	—	—	2964	
δ_{GROUP}	CC	D	Group delay External filter mode[15]	Within pass band – Tclk is time period of f_{ADCD_M} /2 freq. = 2/ f_{ADCD_M}	—	—	—	—
				OSR = 24	—	—	31.25	Tclk
				OSR = 28	—	—	36.25	
				OSR = 32	—	—	41.25	
				OSR = 36	—	—	46.25	
				OSR = 40	—	—	51.25	
				OSR = 44	—	—	56.25	
				OSR = 48	—	—	61.25	
				OSR = 56	—	—	71.25	
				OSR = 64	—	—	81.25	
				OSR = 72	—	—	91.25	
				OSR = 80	—	—	101.25	
				OSR = 88	—	—	111.25	
				OSR = 96	—	—	121.25	
				OSR = 112	—	—	141.25	
				OSR = 128	—	—	161.25	
				OSR = 144	—	—	181.25	
				OSR = 160	—	—	201.25	
				OSR = 176	—	—	221.25	
				OSR = 192	—	—	241.25	

Symbol [1]		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
δ_{GROUP}	CC	D	Group delay External filter mode[15]	OSR = 224	—	—	281.25	Tclk
				OSR = 256	—	—	321.25	
				OSR = 512	—	—	641.25	
				OSR = 1024	—	—	1281.25	
f_{HIGH}	CC	D	High pass filter 3dB frequency	Enabled	—	—	16e-5*f_{ADCD_S}	—
$t_{STARTUP}$	CC	D	Start-up time from power down state	—	—	—	100	µs
$t_{LATENCY}$	CC	D	Latency between input data and converted data (input mux not changed)[16]	HPF = ON	—	—	δ_{GROUP} + 2/ f_{ADCD_S}	—
				HPF = OFF	—	—	δ_{GROUP} + 1/ f_{ADCD_S}	—
$t_{SETTLING}$	CC	D	Settling time after mux change	Analog inputs are muxed HPF = ON	—	—	2*δ_{GROUP} + 3*1/ f_{ADCD_S}	—
				HPF = OFF	—	—	2*δ_{GROUP} + 2*1/ f_{ADCD_S}	—
$t_{ODRECOVERY}$	CC	D	Overdrive recovery time	After input comes within range from saturation HPF = ON	—	—	2*δ_{GROUP} + 2/ f_{ADCD_S}	—
				HPF = OFF	—	—	2*δ_{GROUP} + 2/ f_{ADCD_S}	—
C_{S_D}	CC	D	SDADC sampling capacitance after sampling switch[17]	GAIN = 1, 2, 4, 8	—	—	160*GAIN	fF
		D		GAIN = 16	—	—	1280	fF
I_{ADV_BIAS}	CC	D	Bias consumption	At least 1 SDADC enabled	—	—	1	mA
I_{ADV_D}	CC	C	$V_{DD\_HV\_SD\_DAC\_COMP}$ Power supply current (each ADC)	SDADC enabled	—	—	2.5	mA
I_{ADR_BIAS}	CC	C	BIAS module current[18]	—	—	—	4	µA
I_{ADR_SD}	CC	C	Single SD reference current	—	—	—	2	µA

1. *Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.*
2. *For input voltage above the maximum and below the clamp voltage of the input pad, there is no latch-up concern, and the signal is only 'clipped'.*
3. *V_{INP} is the input voltage applied to the positive terminal of the SDADC.*
4. *V_{INM} is the input voltage applied to the negative terminal of the SDADC.*
5. *Sampling is generated internally $f_{SAMPLING} = f_{ADCD\_M}/2$.*
6. *Maximum input of 166.67 KHz supported with reduced accuracy. See SNR specifications. Tested in production till 20 kHz, covered at bench till 75 kHz (as T parameter).*
7. *Configured oversampling rate: SDADC_MCR[PDR] = 24.*

8. *Calibration of gain is possible when gain = 1. Offset calibration should be done with respect to 0.5*HV_REFH_SD for "differential mode" and "single ended mode with negative input = 0.5*HV_REFH_SD". Offset calibration should be done with respect to 0 for "single ended mode with negative input = 0". Both offset and gain calibration is ensured for ±10% variation of HV_REFH_SD, ±10% variation of $V_{DD\_HV\_SD\_DAC\_COMP}$, on all operating temperature ranges.*
9. *Conversion offset error must be divided by the applied gain factor (1, 2, 4, 8, or 16) to obtain the actual input referred offset error.*
10. *Offset and gain error due to temperature drift can occur in either direction (±) for each of the SDADCs on the device.*
11. *This value is tested in production on each individual device to ensure a correct screening with a tolerance of ~2 dBFS, due to the noise. This value (without tolerance) is however ensured by the measurement carried out on a small number of samples in the analog validation environment. Therefore, the performance is specified by bench, while the screening is specified by tester.*
12. *All channels of all SDADCs are impacted with same degradation, independently from the ADC and the channel subject to current injection.*
13. *SNR value ensured only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of f_{ADCD_M} - f_{ADCD_S} to f_{ADCD_M} + f_{ADCD_S}, where f_{ADCD_M} is the input sampling frequency, and f_{ADCD_S} is the output sample frequency. A proper external input filter must be used to remove any interfering signals in this frequency range.*
14. *The ±1% passband ripple specification is equivalent to 20 * $\log_{10}$ (0.99) = 0.087 dB.*
15. *For details, refer to Section 3.12.4: SDADC filter modes.*
16. *Propagation of the information from the pin to the register CDR[CDATA] and flags SFR[DFEF], SFR[DFFF] is given by the different modules that need to be crossed: delta/sigma filters, high pass filter, fifo module, clock domain synchronizers. The time elapsed between data availability at pin and internal S/D module registers is given by the below formula: REGISTER LATENCY = $t_{LATENCY}$ + 0.5/f_{ADCD_S} + 2 (~+1)/f_{ADCD_M} + 2(~+1)$f_{PBRIDGEx\_CLK}$ where f_{ADCD_S} is the frequency of the sampling clock, f_{ADCD_M} is the frequency of the modulator, and $f_{PBRIDGEx\_CLK}$ is the frequency of the peripheral bridge clock feeds to the SDADC module. The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing. Some further latency may be added by the target module (core, DMA, interrupt) controller to process the data received from the SDADC module.*
17. *This capacitance does not include pin capacitance, that can be considered together with external capacitance, before sampling switch.*
18. *Single bias module providing reference to 2 S/D.*

Figure 11. S/D impedance generic model



$$I_{INP} = \frac{V_{INP} - V_{INM}}{2.Z_{DIFF}} + \frac{V_{ICM} - V_{INT}}{Z_{CM}} = \frac{V_{INP} - V_{ICM}}{Z_{DIFF}} + \frac{V_{ICM} - V_{INT}}{Z_{CM}} \quad (1)$$

$$I_{INM} = \frac{V_{INM} - V_{INP}}{2.Z_{DIFF}} + \frac{V_{ICM} - V_{INT}}{Z_{CM}} = \frac{V_{INM} - V_{ICM}}{Z_{DIFF}} + \frac{V_{ICM} - V_{INT}}{Z_{CM}} \quad (2)$$

Related links

3.12.4 SDADC filter modes on page 47

3.12.4 SDADC filter modes

The following table describes the 4 SDADC filter modes which are controlled by bits BANDSEL, FSEL and EXTFILTER of the module configuration register (MCR).

Gain calibration should be done using the same OSR configuration, FIR filter selection mode and output data rate band selection as the target application, since full-scale values may vary slightly with these settings (normal mode and bypass FIR mode). Refer to Table 31. Digital output codes in full scale for full-scale values (with MCR[GECEN] = 1) with different OSR settings, both for normal and bypass FIR modes.

Table 30. Filter modes

BANDSEL[(1)]	FSEL	EXTFILTER	Filter mode
0	0	0	Normal/default mode
1	0	0	Modified bandwidth mode
X	1	0	Bypass FIR mode
X	X	1	External filter mode

1. *For details, refer to the device reference manual.*

In normal/default mode, modified bandwidth mode and bypass FIR mode, the output values are not normalized by hardware. To apply normalization by software the following table lists the digital output codes in these modes when input signal is full range.

Table 31. Digital output codes in full scale

OSR	MCR[FSEL] = 1 MCR[GECEN] = 1	MCR[FSEL] = 0 MCR[BANDSEL] = 0 MCR[GECEN] = 1	MCR[FSEL] = 0 MCR[BANDSEL] = 1 MCR[GECEN] = 1
24	29160	31081	31095
28	29157	31077	31092
32	29158	31079	31093
36	29155	31075	31090
40	29109	31026	31042
44	29121	31040	31054
48	29160	31081	31095
56	29157	31077	31092
64	29158	31079	31093
72	29155	31075	31090
75	29064	31128	31143
80	29109	31026	31042
88	29121	31040	31054
96	29160	31081	31095
112	29157	31078	31092
128	29158	31079	31093
144	29155	31076	31089
160	29109	31026	31042
176	29121	31040	31054
192	29160	31081	31095
224	29157	31078	31092

OSR	MCR[FSEL] = 1 MCR[GECEN] = 1	MCR[FSEL] = 0 MCR[BANDSEL] = 0 MCR[GECEN] = 1	MCR[FSEL] = 0 MCR[BANDSEL] = 1 MCR[GECEN] = 1
256	29158	31079	31093
512	29158	31079	31093
1024	29158	31079	31093

Related links

3.12.3 SDADC electrical specification on page 38

3.12.5 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

Table 32. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC	—	Temperature monitoring range	—	-40	—	150	°C
ΔT_{ACC}	CC	P	Temperature monitor accuracy	-40°C < T_J < 150°C	-3°C	—	+3°C	°C
I_{TEMP_SENS}	CC	C	Power ($V_{DD\_HV\_SAR}$ power supply current)	—	—	—	900	µA
$T_{flagm40}$	CC	T	-40°C temperature flag threshold	—	-45	—	-37	°C
$T_{flag150}$	CC	T	150°C temperature flag threshold	—	143	—	155	°C

3.12.6 Fast-DAC

This block is a 12-bit digital to analog converter (DAC) and is used to drive internal SoC cells. It can drive capacitive load at high speed. The input digital word is latched at the rising edge of the clock signal.

Table 33. Fast-DAC electrical specification

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
RESOLUTION	CC	D	DAC register resolution	—		12		bit
DAC_{output_rate}	CC	D	Output data rate	—	—	—	15	Msps
DNL	CC	C	Differential non-linearity(1)	—	–2.5	—	2	LSB
INL	CC	C	Integral non-linearity(2)	—	–4	—	4	LSB
TUE	CC	C	Total unadjusted error(3)	—	–6	—	6	LSB
Gain_err	CC	C	Gain error(4)	—	—	—	±0.5	%
Z_{out}	CC	T	DAC output impedance	—	—	1800	—	Ω
$T_{settling}$	CC	D	Settling time (Full scale)(5)	Normal mode (DACMOD_V12=<011>) Capacitive load on DAC output: C_L=500 fF	—	35	45	ns
				Normal mode (DACMOD_V12=<011>) Capacitive load on DAC output: C_L=2 pF	—	55	65	
				Normal mode (DACMOD_V12=<011>) Capacitive load on DAC output: C_L=5 pF	—	100	125	
T_{update}	CC	D	Update rate(6)	Capacitance load: C_L=2 pF	—	40	55	ns
T_{wakeup}	CC	D	Wakeup time(7)	Capacitance load: C_L=2 pF	—	0,6	1	µs
T_{samp}	CC	D	Sampling time in sample and hold mode(8)	DACMOD_V12=<111>	—	—	1,2	µs
V_{drift_hold}	CC	D	Voltage decay rate in sample and hold mode, during hold phase (dV/dt during hold phase)	—	—	—	45	mV/ms
I_{on}	CC	T	Current consumption	Normal mode (DACMOD_V12 = <011>)	—	—	955	µA
I_{off}	CC	D	Current consumption	In power down mode	—	—	0,15	µA

1. *Difference between two consecutive codes - 1 LSB. These values are related to Fast-DAC with 12-bit resolution (for 11-bit resolutions, a /2 factor to be considered). There are no limitations at system level due to these values because of the lower resolution of the comparator modules, which use the output of Fast-DAC modules.*
2. *Difference between measured value at code "i" and the value at code "i" on a line drawn between code 0 and last code 4095. Offset error is included. Parameter specified by design on entire temperature range and measured at cold temperature by design characterization.*
3. *Difference between expected value and measured value at code "i". Parameter specified by design on entire temperature range and measured at cold temperature by design characterization.*
4. *Difference between ideal slope of the transfer function and measured slope computed from code 0 to code 4095.*
5. *Full scale: 12-bit code transition between the lowest and the highest input codes (from code 0 to code 4095) when DAC output reaches final value.*
6. *Time taken for ±0.5 LSB settling (code: 2047 to 2048).*
7. *Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB taken on DAC output.*
8. *Code transition between the lowest input code and the highest input code when DAC output reaches final value ±1 LSB.*

3.12.7 Buffered-DAC

This block is a 12-bit resistive ladder based on digital-to-analog converter (DAC) to drive resistive load up to 5 kΩ and capacitive load up to 50 pF. The input digital word is latched at the rising edge of the clock signal.

Table 34. Buffered-DAC electrical specification

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
RESOLUTION	CC	D	DAC register resolution	—			12	bit
DAC_{output_rate}	CC	T	Output data rate	—	—	—	1	Msps
R_L	SR	D	Resistive load to ground	DAC output buffer ON, with DACMOD_v12=000,001	5	—	—	KΩ
		D	Resistive load to supply	DAC output buffer ON, with DACMOD_v12=000,001	25	—	—	
C_L	SR	D	Capacitive load	Without Sample&Hold: DACMOD_V12<2>=0	—	—	50	pF
		D		With Sample&Hold: For DACMOD_V12<2>=1	—	—	100	nF
DAC_{output_min}	CC	T	Lower DACOUT voltage	With Buffer ON: DACMOD_V12=X00, X01	0.2	—	—	V
		T		With Buffer OFF: DACMOD_V12=X10, X11	0	—	—	
DAC_{output_max}	CC	T	Higher DACOUT voltage	With Buffer ON: DACMOD_V12=X00, X01	—	—	HV_REFH_DAC_COMP - 0.2	V
		T		With Buffer OFF: DACMOD_V12=X10, X11	—	—	HV_REFH_DAC_COMP	
DNL	CC	C	Differential non-linearity(1)	DACMOD_V12 = 000,001	–1	—	2.5	LSB
INL	CC	C	Integral nonlinearity(2)	DACMOD_V12 = 000,001	–4	—	4	LSB
TUE	CC	P	Total unadjusted error(3)	DACMOD_V12 = 000,001	–20	—	+20	LSB
Gain_err	CC	C	Gain error(4)	DACMOD_V12 = 000,001	—	—	±1	%
Offset_err_cal	CC	C	Offset error after calibration	Difference between Vref/2 and actual output at middle code	—	—	5	LSB
$T_{settling\_buff}$	CC	D	Settling time with Buffer ON (Full scale)(5)	DACMOD_V12=<000>, <001> Capacitive load on DAC output: C_L < 50 pF	—	1.7	3	µs
		D		DACMOD_V12=V12=<100>, <101> Capacitive load on DAC output: C_L < 100 nF	—	TBD	—	
$T_{settling\_unbuff}$	CC	D	Settling time with Buffer OFF (Full scale)(5)	DACMOD_V12=<010>, <011> Capacitive load on DAC output: C_L < 10 pF	—	—	2	µs
		D		DACMOD_V12=V12=<110> Capacitive load on DAC output: C_L < 100 nF	—	TBD	—	
T_{update}	CC	D	Update rate(6)	Capacitance load: C_L <50 pF; DACMOD_V12=<000>, <001>	—	1	—	µs
T_{wakeup}	CC	D	Wake-up time(7)	Capacitance load: C_L <50 pF; DACMOD_V12=<000>, <001>	—	—	7.5	µs

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
T_{samp}	—	D	Sampling time in sample and hold mode[8]	DACMOD_V12=<101>	—	—	100	µs
V_{drift_hold}	CC	D	Voltage decay rate in sample and hold mode, during hold phase (dV/dt during hold phase)	—	—	—	12	mV/ms
PSRR	CC	D	Analog supply rejection ratio	@100kHz	—	25	—	dB
SNR	CC	C	Signal to noise ratio[9]	—	—	69	—	dB
THD	CC	C	Total harmonic distortion [9]	—	—	-67	—	db
I_{on}	—	T	Current consumption	In normal operation mode DACMOD_V12=<011>	—	—	1200	µA
I_{off}	—	D	Current consumption	In power down mode	—	—	0.5	µA

1. *Difference between two consecutive codes - 1 LSB.*
2. *Difference between the measured value at code ‘i’ and the value at code ‘i’ on a line drawn between code 0 and last code 4095. Offset error is included.*
3. *Difference between expected value and measured value at code ‘i’.*
4. *Difference between ideal slope of the transfer function and measured slope computed from code 0 to code 4095.*
5. *Full scale: 12-bit code transition between the lowest and the highest input codes (from code 0 to code 4095) when DAC output reaches final value.*
6. *Time taken for ±0.5LSB settling (code: 2047 to 2048).*
7. *Wake-up time from off state (setting the ENx bit in the DAC control register) until final value ±1 LSB taken on DAC output.*
8. *Code transition between the lowest input code and the highest input code when DAC output reaches final value ±1LSB.*
9. *To be measured at 1 kHz.*

3.12.8 Comparator

This block is a reconfigurable rail to rail comparator. This takes input from DAC.

Table 35. Comparator electrical specification

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IN}	SR	D	Comparator input voltage range	Rail to rail	0	—	$V_{DD\_HV\_SD\_DAC\_COMP}$	V
V_{OFF}	CC	C	Comparator offset voltage	Supply voltage = 3.3 V and typical temperature (25 °C) TRIMOFF<3:0> = 1010; 3 sigma	—	—	±10	mV
	CC	C		Full supply voltage range, full temperature range TRIMOFF<3:0> = 1010; 3 sigma	—	—	±12	
I_{DDA}	CC	D	Static current consumption	In power down mode (temperature = 150 °C)	—	—	1	µA
		T		In functional mode (temperature = 150 °C)	—	—	920	
Vhys	CC	C	Comparator hysteresis[1]	HYST[2:0] = 0	–5	0	5	mV
		C		HYST[2:0] = 1	2	10	20	
		C		HYST[2:0] = 2	8	19	40	

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Vhys	CC	C	Comparator hysteresis(1)	HYST[2:0] = 3	12	28	60	mV
		C		HYST[2:0] = 4	16	38	80	
		C		HYST[2:0] = 5	20	47	100	
		C		HYST[2:0] = 6	25	57	120	
		C		HYST[2:0] = 7	30	67	142	
T_P	CC	D	Propagation delay(2)	Step response, with 200 mV step with 100 mV overdrive, rising time for 1 ns slope	—	20	50	ns
Tstart	CC	D	Comparator startup time	Comparator startup time to reach propagation delay specification	—	—	5	µs

1. *Hysteresis voltage defined when COMPOUT goes from high to low state, threshold voltage at INP = INM-VHYST.*
2. *With full supply voltage range ($V_{DD\_HV\_SD\_DAC\_COMP}$ = 3 to 3.45 V).*

3.13 Power management

The power management module monitors the different power supplies as well as it generates the required internal supplies. The regulator is based on an internal switching mode power supply (SMPS) regulator, using external MOSFETs to generate the low voltage supply (V_{DD_LV} for core logic).

3.13.1 Power management integration

Use the integration scheme provided here after to ensure the proper device function.

Place capacitances on the board as near as possible to the associated pins and limit the serial inductance of the board to less than 5 nH.

Figure 12. SMPS regulator mode

Refer to the device pinout IO definition excel file for the list of available PMU control pins for each device and package.

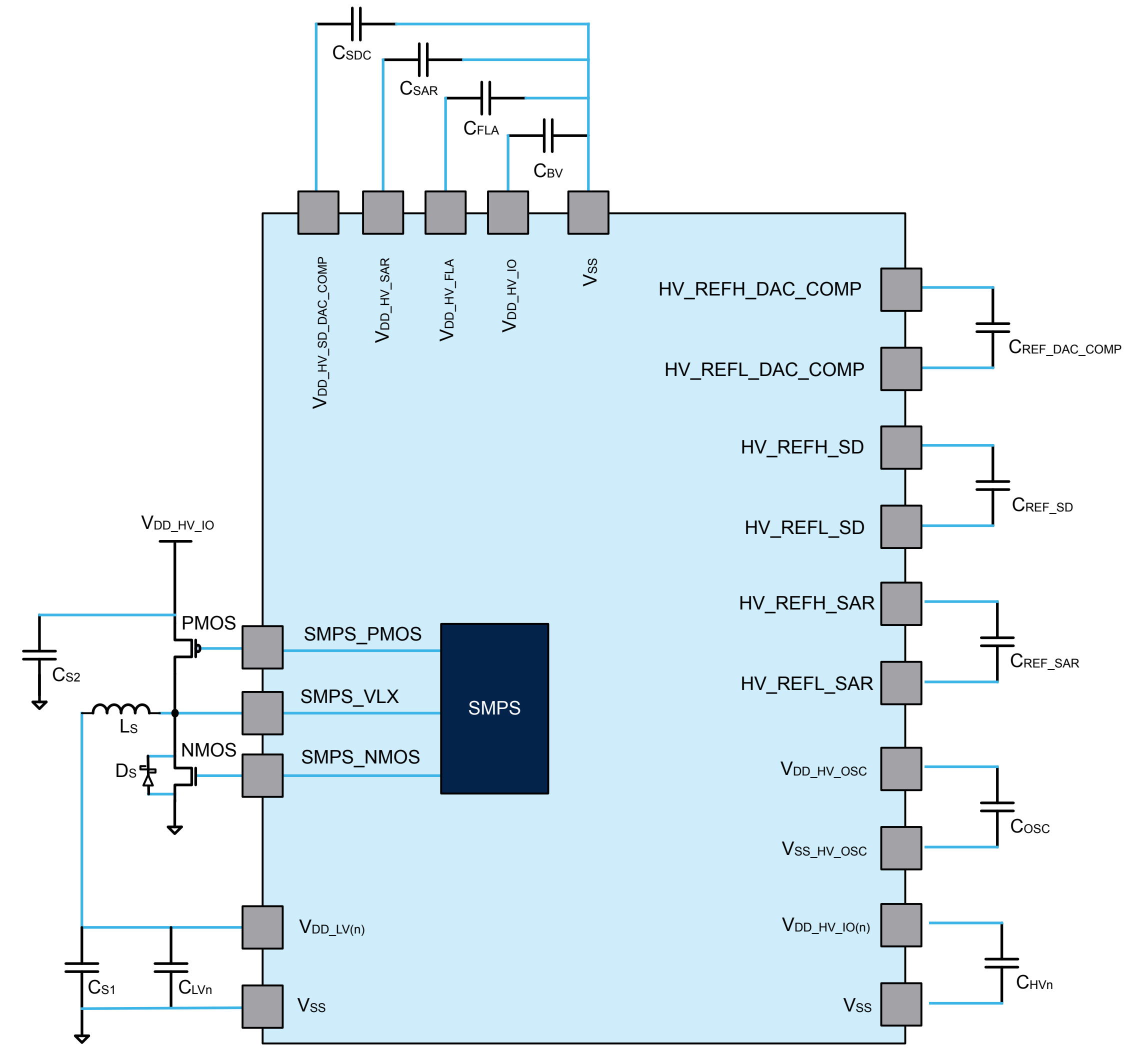


Table 36. External components integration

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Common components								
C_{LVn}	SR	D	Internal voltage regulator decoupling external capacitance(1)(2)	Each V_{DD_LV}/V_{SS} pair	—	47	—	nF
R_{LVn}	SR	D	Stability capacitor equivalent serial resistance	—	—	—	50	mΩ
C_{BV}	SR	D	Bulk capacitance for HV supply(3)	—	—	4.7	—	µF
C_{HVn}	SR	D	Decoupling capacitance for I/Os(3)(4)(5)	Each $V_{DD\_HV\_IO}/V_{SS}$ pair	—	100	—	nF
C_{FLA}	SR	D	Decoupling capacitance for flash supply(3)	—	—	100	—	nF
C_{SAR}	SR	D	ADC_SAR supply external capacitance(2)(7)(8)	—	—	10	—	µF
C_{SDC}	SR	D	ADC_SD, DAC, COMP supply external capacitance(2)(8)	—	—	10	—	µF
$C_{REF\_DAC\_COMP}$	SR	D	DAC, COMP reference external capacitance(2)(8)	—	—	1	—	µF
C_{REF_SD}	SR	D	ADC_SD reference external capacitance(2)(8)	—	—	1	—	µF
C_{REF_SAR}	SR	D	ADC_SAR reference external capacitance(2)(8)	—	—	1	—	µF
C_{OSC}	SR	D	Oscillator supply external capacitance(2)(6)(9)	—	—	10	—	µF
SMPS regulator mode								
PMPB100XPEAX(10)	SR	D	Recommended PMOS transistor for SMPS mode(11)(12)	—	—	—	—	—
PMPB55XNEAX(13)	SR	D	Recommended NMOS transistor for SMPS mode(11)	—	—	—	—	—
C_{S1}	SR	D	SMPS external capacitance on LV supply(4)(7)(8)(9)	—	-50%	20	+30%	µF
C_{S2}(14)(15)	SR	D	SMPS external capacitance on HV supply(4)(7)(8)(9)	—	-50%	47	+35%	µF
L_S	SR	D	SMPS external inductance	—	-30%	10	+30%	µH

1. *$V_{DD\_HV\_IO}$ = 3.3 V ± 5%, T_J = –40 / 150 °C.*
2. *For noise filtering, add a high frequency bypass capacitance of 10 nF, as close as possible to the terminal.*
3. *Recommended X7R capacitors.*
4. *For optimal EMC performance, the addition of a 10 nF has to be considered on every supply rail. The intention is to have a decoupling scheme covering the wider possible frequency range.*
5. *To sustain the HV of the SMPS external Mos, add a 10 µF on $V_{DD\_HV\_IO}$.*
6. *For noise filtering, add a high frequency bypass capacitance of 47 nF as close as possible to the terminal.*
7. *External capacitance is required both in internal and external (test) regulator mode.*
8. *For noise filtering, add a high frequency bypass capacitance of 100 nF as close as possible to the terminal.*
9. *For noise filtering, add a high frequency bypass capacitance of 1 nF as close as possible to the terminal.*
10. *Alternative PMOS transistor for SMPS is BUK4D110-20P.*
11. *Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².*
12. *Recommended Schottky diode PMEG3030EP on NMOS transistor to reduce the emission.*
13. *The alternative NMOS transistor for SMPS is BUK4D60-30.*
14. *Recommended X7R or X5R ceramic –50% / +35% variation across process, temperature, voltage and after aging.*
15. *The value of the capacitance on the HV supply reported in the datasheet is a general recommendation. The application can select a different number, based on the external regulator and EMC requirements.*

Related links

3.12.1 ADC input description on page 35

3.13.2 Voltage regulators

Table 37. SMPS regulator specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD\_HV\_IO}$	SR	P	SMPS regulator supply voltage [(1)]	—	3.13	—	3.47	V
V_{SMPS}	CC	P	SMPS regulator output voltage	After trimming, max load	1.225	1.285	1.35	V
F_{SMPS}	CC	T	SMPS regulator switching frequency	—	-8%	750	+8%	kHz
IDD_{SMPS}	CC	T	SMPS regulator current provided to V_{DD_LV} domain	—	—	—	1000	mA
IDD_{CLAMP}	CC	D	SMPS regulator rush current sinked from $V_{DD\_HV\_IO}$ domain during V_{DD_LV} domain loading	Power-up condition	—	—	TBD	mA
ΔIDD_{SMPS}	CC	T	SMPS regulator current variation	20 µs observation window	-100	—	100	mA

1. *SMPS regulator is functional with an undershoot/overshoot of 40 mV max, but at a reduced efficiency.*

3.13.3 Voltage monitors

The monitors and their associated levels for the device are given in Table 38. Voltage monitor electrical characteristics. The following figure illustrates the workings of voltage monitoring threshold.

Figure 13. Voltage monitor threshold definition

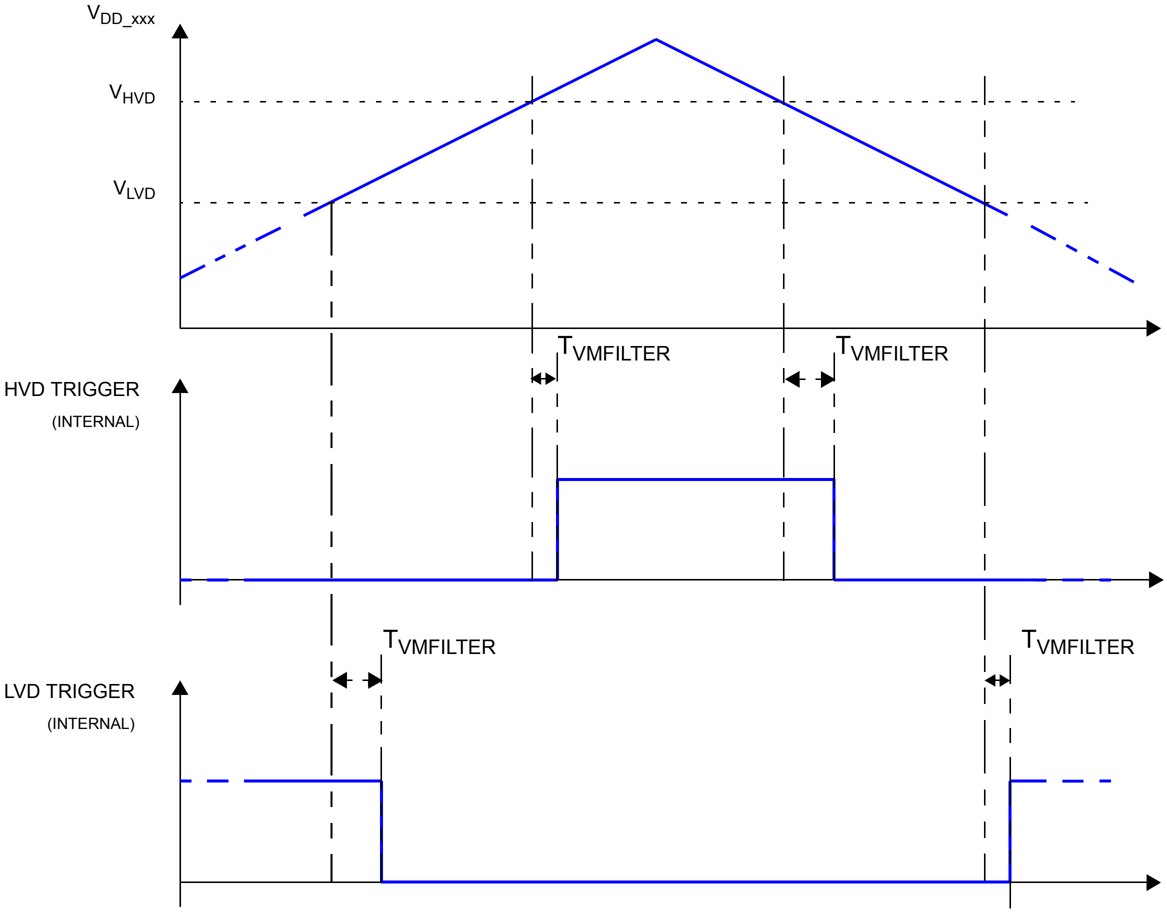


Table 38. Voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions	Value (1)			Unit
					Min	Typ	Max	
Minimum voltage detectors (LV supplies)								
V_{DD_LV}	CC	P	POR031_C Low voltage supply power-on reset voltage monitor V_{DD_LV}	—	0.290	0.600	0.900	V
	CC	P	MVD102T_C LV supply core minimum voltage detector V_{DD_LV}	—	1.005	1.030	1.055	V
	CC	P	MVD114_C LV supply core low range minimum voltage detector V_{DD_LV}	—	1.133	1.150	1.167	V
	CC	P	MVD114_FL LV supply flash minimum voltage detector $V_{DD\_LV\_FLA}$	—	1.133	1.150	1.167	V

Symbol		C	Parameter	Conditions	Value (1)			Unit
					Min	Typ	Max	
Low voltage detectors (LV supplies)								
V_{DD_LV}	CC	P	LVD119_C LV supply core low voltage detector V_{DD_LV}	—	1.188	1.205	1.222	V
	CC	P	LVD119_FL LV supply flash low voltage detector $V_{DD\_LV\_FLA}$	—	1.188	1.205	1.222	V
	CC	P	LVD119_PLL0 LV supply PLL0 low voltage detector $V_{DD\_LV\_PLL0}$	—	1.188	1.205	1.222	V
	CC	P	LVD119_PLL1 LV supply PLL1 low voltage detector $V_{DD\_LV\_PLL1}$	—	1.188	1.205	1.222	V
	CC	P	LVD119_DD LV supply DLL & DelayLanes low voltage detector $V_{DD\_LV\_DD}$	—	1.188	1.205	1.222	V
	CC	P	LVD119_RC LV supply RCOSC low voltage detector V_{DD_LV}	—	1.188	1.205	1.222	V
High and upper voltage detectors (LV supplies)								
V_{DD_LV}	CC	P	HVD140_C LV supply core high voltage detector V_{DD_LV}	—	1.361	1.38	1.399	V
	CC	P	UVD145_C LV supply core upper voltage detector V_{DD_LV}	—	1.411	1.430	1.449	V
	CC	P	UVD145_RC LV supply RCOSC upper voltage detector V_{DD_LV}	—	1.411	1.430	1.449	V
Minimum and low voltage detectors (HV supplies)								
$V_{DD\_HV\_IO}$	CC	P	POR200_C High voltage supply power-on reset voltage monitor $V_{DD\_HV\_PMU}$	—	1.760	1.960	2.160	V
	CC	P	MVD240T_C HV supply core minimum voltage monitor $V_{DD\_HV\_PMU}$	—	2.456	2.525	2.594	V
	CC	P	MVD240_SMPS HV supply core minimum voltage monitor $V_{DD\_HV\_SMPS}$	—	2.456	2.525	2.594	V
	CC	P	MVD270_C HV supply core minimum voltage monitor $V_{DD\_HV\_PMU}$	—	2.794	2.850	2.906	V
	CC	P	LVD290_C HV supply core low voltage monitor $V_{DD\_HV\_PMU}$	—	2.898	2.955	3.012	V
	CC	P	LVD290_IO1 HV supply I/O low voltage monitor $V_{DD\_HV\_IO1}$ segment	—	2.898	2.955	3.012	V
	CC	P	LVD290_IO0	—	2.898	2.955	3.012	V

Symbol		C	Parameter	Conditions	Value [1]			Unit
					Min	Typ	Max	
$V_{DD\_HV\_IO}$			HV supply I/O low voltage monitor $V_{DD\_HV\_IO0}$ segment					
$V_{DD\_HV\_FLA}$	CC	P	MVD270_FL HV supply flash minimum voltage monitor $V_{DD\_HV\_FLA}$	—	2.794	2.850	2.906	V
	CC	P	LVD290_FL HV supply flash low voltage monitor $V_{DD\_HV\_FLA}$	—	2.898	2.955	3.012	V
$V_{DD\_HV\_SD\_DAC\_COMP}$	CC	P	LVD290_AD HV supply SD-ADC low voltage monitor $V_{DD\_HV\_SD}$	—	2.898	2.955	3.012	V
	CC	P	LVD290_DACCMP HV supply DAC & COMP low voltage monitor $V_{DD\_HV\_DAC}$	—	2.898	2.955	3.012	V
$V_{DD\_HV\_SAR}$	CC	P	LVD290_AS HV supply SAR-ADC low voltage monitor $V_{DD\_HV\_SAR}$	—	2.898	2.955	3.012	V
$V_{DD\_HV\_OSC}$	CC	P	LVD290_OSC HV supply OSC low voltage monitor $V_{DD\_HV\_OSC}$	—	2.898	2.955	3.012	V
Upper voltage detectors (HV supplies)								
$V_{DD\_HV\_IO}$	CC	P	UVD380_C HV supply core upper voltage monitor $V_{DD\_HV\_PMU}$	—	3.651	3.725	3.799	V
	CC	P	UVD380_IO0 HV supply I/O upper voltage monitor $V_{DD\_HV\_IO0}$ segment	—	3.651	3.725	3.799	V
$V_{DD\_HV\_FLA}$	CC	P	UVD380_FL HV supply flash upper voltage monitor $V_{DD\_HV\_FLA}$	—	3.651	3.725	3.799	V
$V_{DD\_HV\_SAR}$	CC	P	UVD380_AS HV supply SAR-ADC upper voltage monitor $V_{DD\_HV\_SAR}$	—	3.651	3.725	3.799	V
$V_{DD\_HV\_SD\_DAC\_COMP}$	CC	P	UVD380_DACCMP HV supply DAC & COMP upper voltage monitor $V_{DD\_HV\_DAC}$	—	3.651	3.725	3.799	V
$T_{VMFILTER}$	CC	D	Voltage monitor filter[2]	—	3		20	μs

1. *The values are trimmed during boot process.*
2. *See Figure 13. Voltage monitor threshold definition. Transitions shorter than minimum are filtered. Transitions longer than maximum are not filtered, and are delayed by $T_{VMFILTER}$ time. Transitions between minimum and maximum can be filtered or not filtered, according to temperature, process and voltage variations.*

Related links

3.3 Operating conditions on page 12

3.14 Embedded flash memory

The following table shows the wait state configuration.

Table 39. Wait state configuration

APC	RWSC	Core frequency (MHz)
000[1]	≤1	f ≤ 34
	2	f ≤ 68
	3	f ≤ 136
	4	f ≤ 170
	5	f ≤ 204
	6	f ≤ 238
	7	f ≤ 273
	8	f ≤ 307
100[2]	≤1	f ≤ 34
	2	f ≤ 68
	3	f ≤ 136
	4	f ≤ 170
	5	f ≤ 204
	6	f ≤ 238
	7	f ≤ 273
	8	f ≤ 307
001[3]	3	55 < f ≤ 120
	4	55 < f ≤ 160
	5	55 < f ≤ 200
	6	55 < f ≤ 233
	7	55 < f ≤ 267
	8	55 < f ≤ 307

1. *No pipeline.*
2. *No pipeline with 1 Tclk access delay.*
3. *Pipeline.*

Table 40. Flash memory program and erase specifications

Symbol	Characteristics[1][2]	Value									Unit
		Typ[3]	C	Initial max			Typical end of life[4]	Lifetime max[5]		C	
				25 °C[6]	All temp[7]	C		< 1 K cycles	< 250 K cycles		
$t_{dwprogram}$	Double word (64 bits) program time (partition 0 & 3)	43	C	130	—	—	140	500		C	µs
$t_{pprogram}$	Page (256 bits) program time	72	C	240	—	—	240	1000		C	µs
$t_{pprogrameep}$	Page (256 bits) program time (partition 0 & 3)	83	C	264	—	—	276	1000		C	µs
$t_{qprogram}$	Quad page (1024 bits) program time	220	C	1040	1200	P	850	2000		C	µs
$t_{qprogrameep}$	Quad page (1024 bits) program time (partition 0 & 3)	245	C	1140	1320	P	978	2000		C	µs

Symbol	Characteristics[(1)(2)]	Value									Unit
		Typ[(3)]	C	Initial max			Typical end of life[(4)]	Lifetime max[(5)]		C	
				25 °C[(6)]	All temp[(7)]	C		< 1 K cycles	< 250 K cycles		
$t_{16kpperase0}$	16 KB block pre-program and erase time (partition 0)	230	C	495	550	P	300	600	—	C	ms
$t_{32kpperase0}$	32 KB block pre-program and erase time (partition 0)	345	C	700	825	P	400	1000	—	C	ms
$t_{64kpperase0}$	64 KB block pre-program and erase time (partition 0)	530	C	910	1150	P	600	1600	—	C	ms
$t_{64kpperase}$	64 KB pre-program and erase time	460	C	700	750	P	420	1200	—	C	ms
$t_{256kpperase}$	256 KB block pre-program and erase time	1140	C	2000	2600	P	1300	2800	—	C	ms
$t_{16kprogram0}$	16 KB block program time (partition 0)	30	C	52	58	P	40	100	—	C	ms
$t_{32kprogram0}$	32 KB block program time (partition 0)	60	C	105	120	P	75	200	—	C	ms
$t_{64kprogram0}$	64 KB block program time (partition 0)	120	C	200	250	P	150	400	—	C	ms
$t_{64kprogram}$	64 KB block program time	102	C	175	200	P	150	400	—	C	ms
$t_{256kprogram}$	256 KB block program time	410	C	700	800	P	590	1000	—	C	ms
$t_{16kprogrameep}$	Program 16 KB data flash - EEPROM (partition 3)	30	C	52	58	P	64	200		C	ms
$t_{16keraseeep}$	Erase 16 KB data flash - EEPROM (partition 3)	230	C	495	550	P	400	1000		C	ms
$t_{16kprogramheep}$	Program 16 KB HSM data flash - EEPROM (partition 3)	30	C	52	58	P	64	200		C	ms
$t_{16keraseheep}$	Erase 16 KB HSM data flash - EEPROM (partition 3)	230	C	495	550	P	400	1000		C	ms
t_{tr}	Program rate[(8)]	1.7	C	2.8	3.40	C	2.4	—		C	s/MB
t_{pr}	Erase rate[(8)]	4.8	C	7.2	9.6	C	6.4	—		C	s/MB
t_{tprfm}	Program rate factory mode[(8)]	1.12	C	1.4	1.6	C	—	—		C	s/MB
t_{erfm}	Erase rate factory mode[(8)]	4.0	C	5.2	5.8	C	—	—		C	s/MB
$t_{ffprogram}$	Full flash programming time[(9)]	3.4	C	5.0	6.0	P	3.8	—	—	C	s
$t_{fferase}$	Full flash erasing time[(9)]	9.9	C	17.0	20.0	P	11.0	—	—	C	s
t_{ESRT}	Erase suspend request rate[(10)]	200	T	—	—	—	—	—		—	µs
t_{PSRT}	Program suspend request rate[(10)]	30	T	—	—	—	—	—		—	µs
t_{AMRT}	Array integrity check - margin read suspend request rate	15	T	—	—	—	—	—		—	µs
t_{PSUS}	Program suspend latency[(11)]	—	—	—	—	—	—	15		T	µs
t_{ESUS}	Erase suspend latency[(11)]	—	—	—	—	—	—	30		T	µs
t_{AIC0S}	Array integrity check (1920 KB, sequential)[(12)]	11.3	T	—	—	—	—	—	—	—	ms
$t_{AIC256KS}$	Array integrity check (256 KB, sequential)[(12)]	1.5	T	—	—	—	—	—	—	—	ms
t_{AIC0P}	Array integrity check (1920 KB, proprietary)[(12)]	4.0	T	—	—	—	—	—	—	—	s
t_{MR0S}	Margin read (1920 KB, sequential)[(12)]	30	T	—	—	—	—	—	—	—	ms
$t_{MR256KS}$	Margin read (256 KB, sequential)[(12)]	4.0	T	—	—	—	—	—	—	—	ms

Symbol	Characteristics(1)(2)	Value									Unit
		Typ(3)	C	Initial max			Typical end of life(4)	Lifetime max(5)		C	
				25 °C(6)	All temp(7)	C		< 1 K cycles	< 250 K cycles		
t_{AABT}	Array integrity check abort latency	—	—	—	—	—	—	10		T	µs
t_{MABT}	Margin read abort latency	—	—	—	—	—	—	10		T	µs

1. *Actual hardware operation times; this does not include software overhead.*
2. *Characteristics are valid both for data flash and code flash, unless specified in the characteristics column.*
3. *Typical program and erase times assume nominal supply values and operation at 25 °C.*
4. *Typical end of life program and erase times represent the median performance and assume nominal supply values. Typical end of life program and erase values may be used for throughput calculations. These values are characteristic, but not tested.*
5. *Lifetime maximum program and erase times apply across the voltages and temperatures and occur after the specified number of program/ erase cycles. These maximum values are characterized but not tested or guaranteed.*
6. *Initial factory condition: < 100 program/erase cycles, 25 °C typical junction temperature and nominal (±5%) supply voltages.*
7. *Initial maximum “All temp” program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, –40 °C < T_J < 150 °C junction temperature and nominal (±5%) supply voltages.*
8. *Rate computed based on 256 KB sectors.*
9. *Only code sectors, not including EEPROM, neither UTEST and BAF.*
10. *Time between suspend resume and next suspend. Value stated actually represents min value specification.*
11. *Timings specified by design.*
12. *AIC is done using system clock, thus all timing is dependent on system frequency and number of wait states. Timing in the table is calculated at max frequency.*

All the flash operations require the presence of the system clock for internal synchronization. About 50 synchronization cycles are needed: this means that the timings of the previous table can be longer if a low frequency system clock is used.

Table 41. Flash memory life specification

Symbol	Characteristics(1)(2)	Value				Unit
		Min	C	Typ	C	
N_{CER16K}	16 KB code flash endurance	10	—	100	—	Kcycles
N_{CER32K}	32 KB code flash endurance	10	—	100	—	Kcycles
N_{CER64K}	64 KB code flash endurance	10	—	100	—	Kcycles
$N_{CER256K}$	256 KB code flash endurance	1	—	100	—	Kcycles
	256 KB code flash endurance(3)	10	—	100	—	Kcycles
N_{DER16K}	16 KB data EEPROM flash endurance	250	—	—	—	Kcycles
N_{DER16K}	16 KB HSM data EEPROM flash endurance	100	—	—	—	Kcycles
t_{DR1k}	Minimum data retention blocks with 0 - 1 000 P/E cycles	25	—	—	—	Years
t_{DR10k}	Minimum data retention blocks with 1 001 - 10 000 P/E cycles	20	—	—	—	Years
t_{DR100k}	Minimum data retention blocks with 10 001 - 100 000 P/E cycles	15	—	—	—	Years
t_{DR250k}	Minimum data retention blocks with 100 001 - 250 000 P/E cycles	10	—	—	—	Years

1. *It is recommended that the application enables the core cache memory.*
2. *Program and erase cycles supported across specified temperature specifications.*
3. *10 Kcycles on 4-256 KB blocks are not intended for production. Reduced reliability and degraded erase time are possible.*

3.15 AC specifications

All AC timing specifications are valid up to 150 °C.

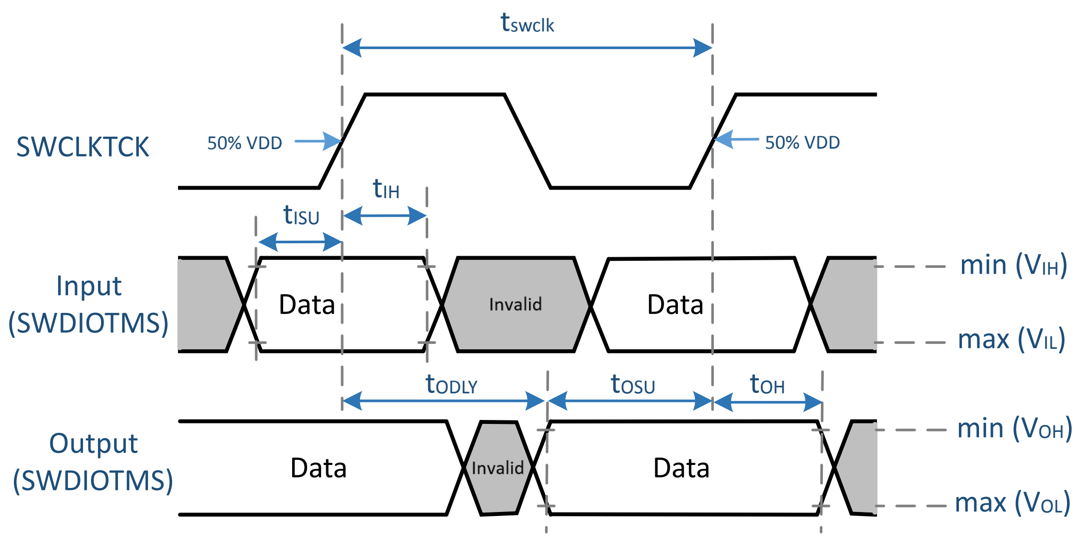
3.15.1 Debug and calibration interface timing

3.15.1.1 SWD interface timing

Table 42. **SWD timings and delay adjustment**

Symbol		C	Characteristics	Condition	Value			Unit	#
					Min	Typ	Max		
Clock (SWCLK)									
$f_{swclktck}$	CC	D	SWCLKTCK frequency	—	—	—	25	MHz	1
$t_{swclktck}$	CC	D	SWCLKTCK period	—	40	—	—	ns	2
Input (SWDIOTMS)									
t_{ISU}	CC	D	SWDIOTMS input setup time	—	15	—	—	ns	3
t_{IH}	CC	D	SWDIOTMS input hold time	—	3	—	—	ns	4
Output (SWDIOTMS)									
t_{ODLY}	CC	D	SWDIOTMS output delay time during data transfer	CL = 25 pF	—	—	30	ns	5
T_{OSU}	CC	D	SWDIOTMS output setup time	CL = 25 pF	5	—	—	ns	6
t_{OH}	CC	D	SWDIOTMS output hold time	CL = 25 pF	1	—	—	ns	7
t_{RISE}	CC	D	SWDIOTMS output rise time	CL = 25 pF	2.2	—	—	ns	8
t_{FALL}	CC	D	SWDIOTMS output fall time	CL = 25 pF	2.2	—	—	ns	9
t_{SKEW_TRAN}	CC	D	SWDIOTMS output SKEW	CL = 25 pF	1	—	—	ns	10

Figure 14. **SWD timings**



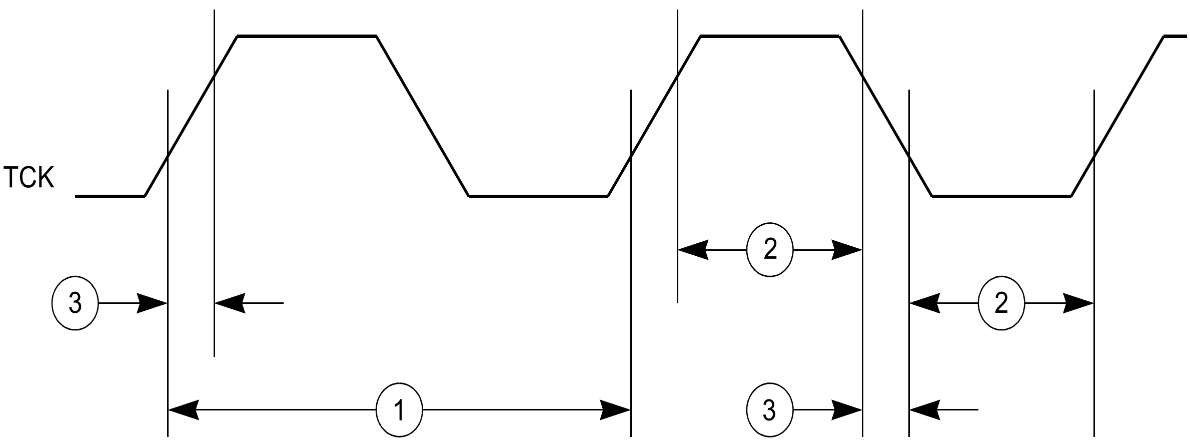
3.15.1.2 JTAG interface timing

Table 43. JTAG pin test and debug timings

Symbol [1][2]		C	Characteristics	Condition	Value			Unit	#
					Min	Typ	Max		
t_{JCYC}	CC	D	TCK cycle time	—	40	—	—	ns	1
t_{JDC}	CC	T	TCK clock pulse width	—	40	—	60	%	2
$t_{TCKRISE}$	CC	D	TCK rise and fall times (40%-70%)	—	—	—	3	ns	3
t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	15	—	—	ns	4
t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	3	—	—	ns	5
t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	—	15 [3]	ns	6
t_{TDOI}	CC	D	TCK low to TDO data invalid	—	1	—	—	ns	7
t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	—	—	15	ns	8
t_{JCMPPW}	CC	D	JCOMP assertion time	—	40	—	—	ns	9
t_{JCMPS}	CC	D	JCOMP setup time to TCK low	—	40	—	—	ns	10
t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	—	600[4]	ns	11
t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	—	600	ns	12
t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	—	600	ns	13
t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	15	—	—	ns	14
t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	15	—	—	ns	15

1. *These specifications apply to JTAG boundary scan only.*
2. *JTAG timing specified at $V_{DD\_HV\_IO}$ = 3.15 to 3.45 V and maximum loading per pad type as specified in the I/O section of the datasheet.*
3. *Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.*
4. *Applies to all pins, limited by pad slew rate. Refer to Section 3.8.2: I/O output DC characteristics and add 20 ns for JTAG delay.*

Figure 15. JTAG test clock input timing



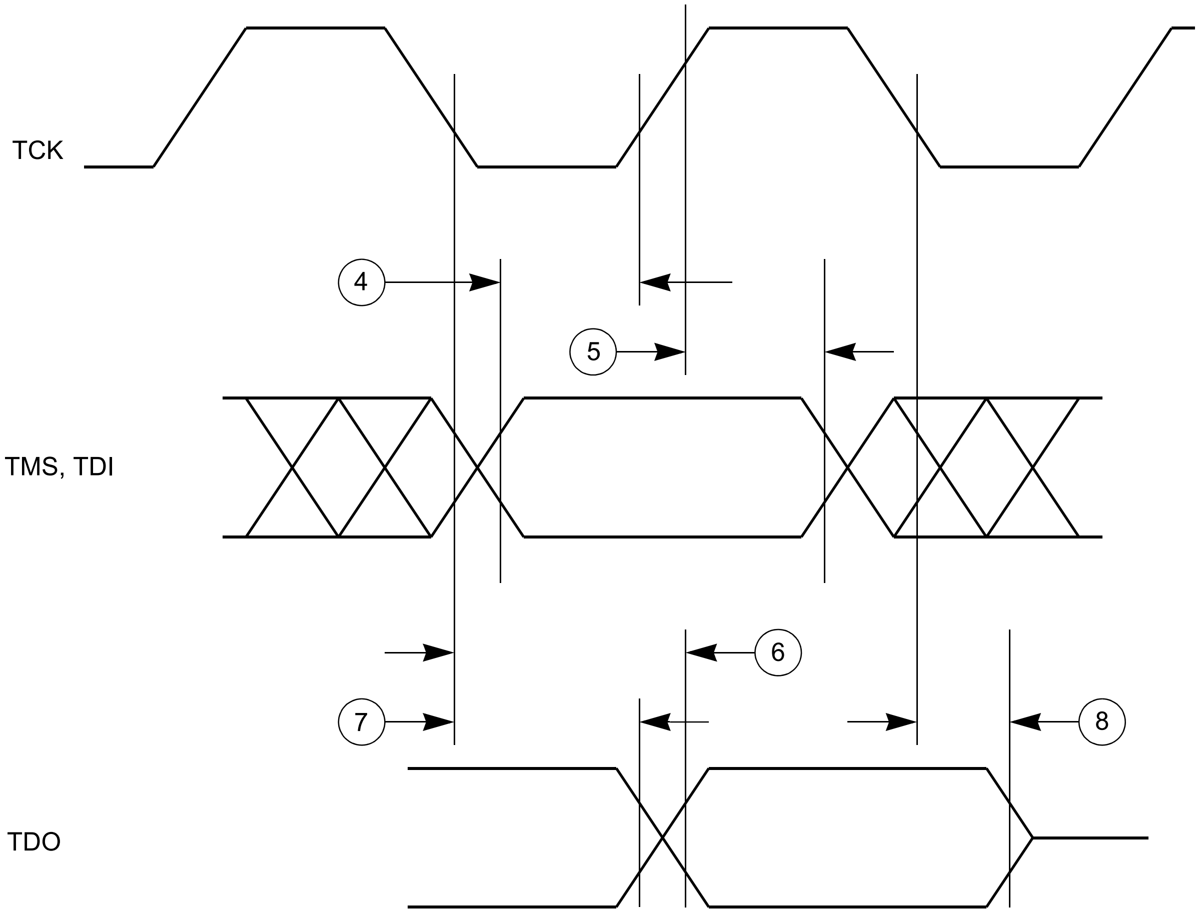


Figure 16. **JTAG test access port timing**

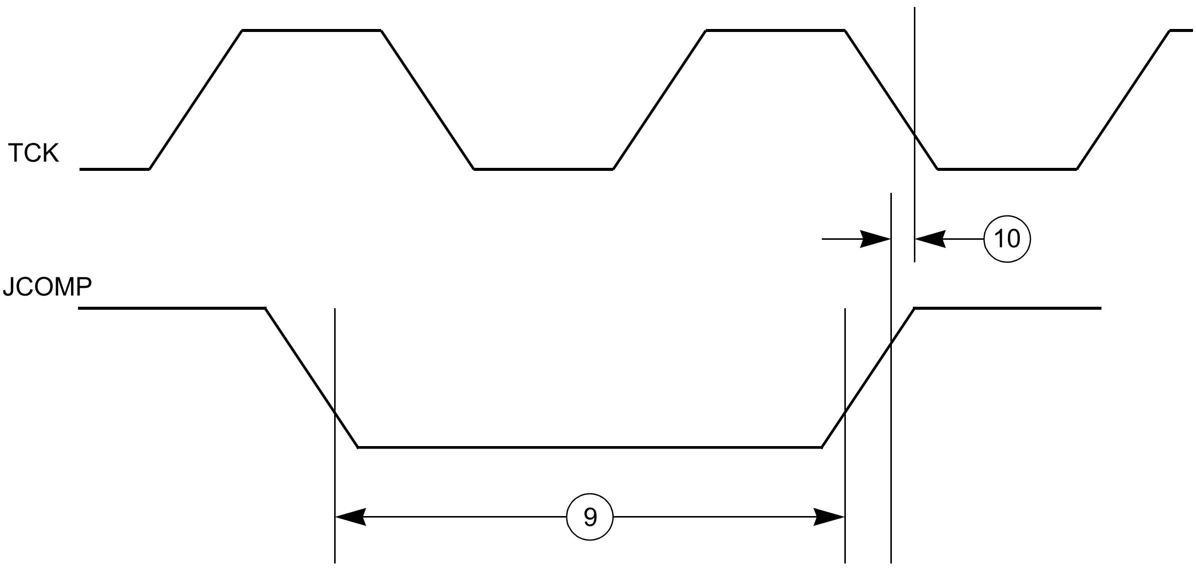
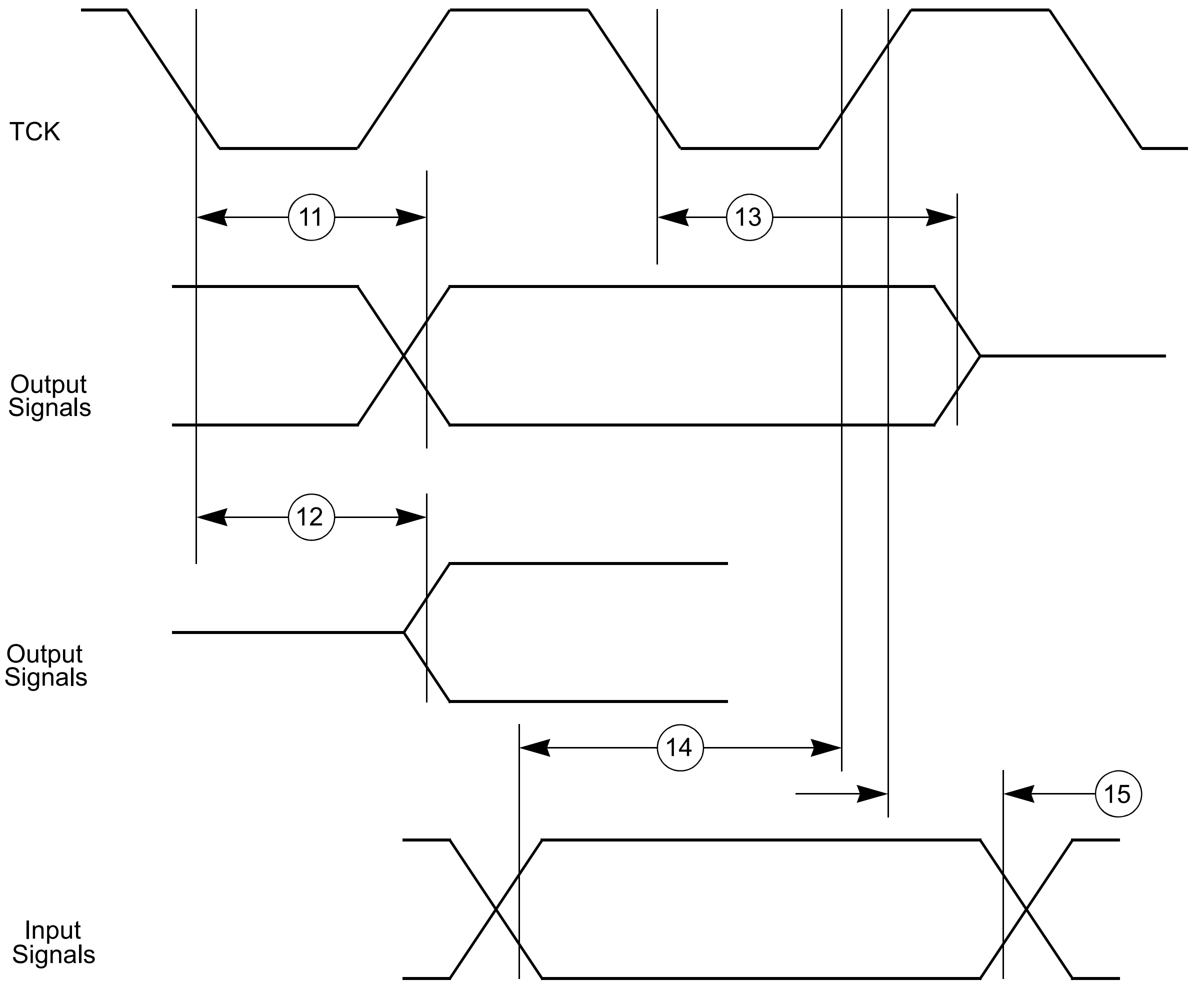


Figure 17. **JTAG JCOMP timing**

Figure 18. JTAG boundary scan timing



Related links

3.8.2 I/O output DC characteristics on page 20

3.15.2 Extended interrupt and event controller input (EXTI)

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 44. External interrupt timing

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
t_{ICYC}	SR	D	IRQ edge to edge time [(1)]	—	10	—	—	ns

1. *Applies when IRQ pins are configured for rising edge or falling edge events, but not both.*

3.15.3 SPI timing

3.15.3.1 SPI — Single ended operation

Table 45. SPI single-ended mode AC specifications — Very Fast IO output characteristics

Symbol		C	Parameter	Conditions [1][2][3][4][5][6]	Value			Unit
					Min	Typ	Max	
f_{SCK}	CC	D	SPI clock frequency[7]	Master mode SPI1, SPI4	—	—	50	MHz
	CC	D		Master mode SPI2, SPI3	—	—	37.5	
	CC	D		Slave receiver mode SPI1, SPI2, SPI3, SPI4	—	—	50	
$t_{su(NSS)}$	CC	D	NSS setup time	Slave mode	2ns+2*T_{PCLK}	—	—	ns
$t_{h(NSS)}$	CC	D	NSS hold time	Slave mode	3	—	—	ns
$t_{w(SCKH)}$,$t_{w(SCKL)}$	CC	D	SCK high and low time	Master mode	T_{PCLK}-2	T_{PCLK}	T_{PCLK}+2	ns
$t_{su(MI)}$	CC	D	Data input setup time	Master mode	2	—	—	ns
$t_{su(SI)}$	CC	D		Slave mode	2	—	—	ns
$t_{h(MI)}$	CC	D	Data input hold time	Master mode	4	—	—	ns
$t_{h(SI)}$	CC	D		Slave mode	3	—	—	ns
$t_{v(SO)}$	CC	D	Data output valid time	Master mode	—	—	15	ns
$t_{v(MO)}$	CC	D		Slave mode	—	—	4	ns
$t_{h(SO)}$	CC	D	Data output hold time	Master mode	4	—	—	ns
$t_{h(MO)}$	CC	D		Slave mode	-2	—	—	ns

1. *All timing values for output signals in this table are measured to 50% of the output voltage.*
2. *All output timing is the worst case and includes the mismatching of rise and fall times of the output pads.*
3. *All timing values are valid for $V_{DD\_HV\_IO}$ = 3.3 V.*
4. *Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / automotive voltage thresholds.*
5. *Very Fast IO output characteristics*
6. *Capacitive Load C_L = 25pF*
7. *Max frequency can be reached under specific device clocks configuration. Refer to the device reference manual, Clocking chapter for details.*

Figure 19. SPI timing diagram — slave mode and CPHA = 1

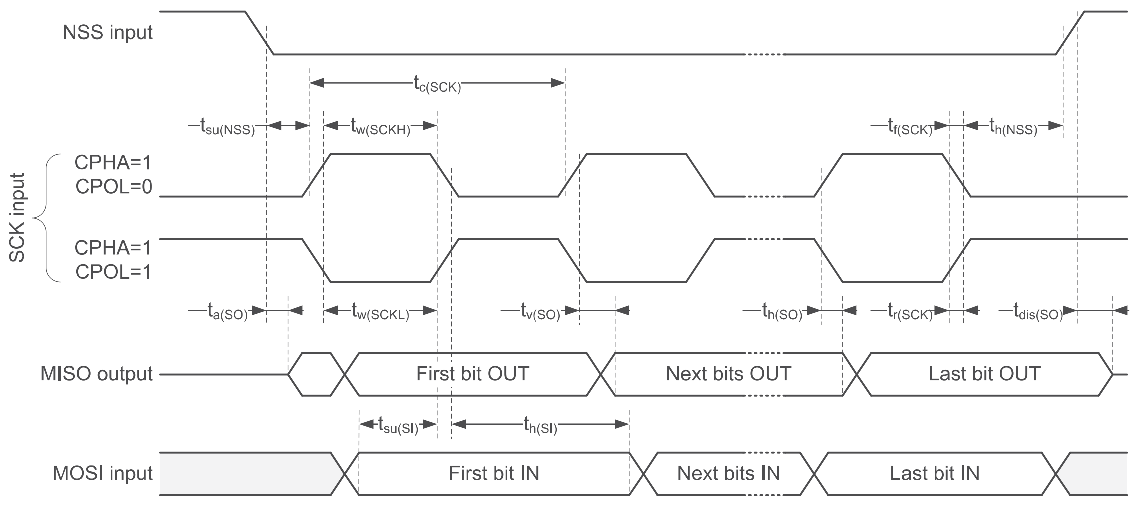
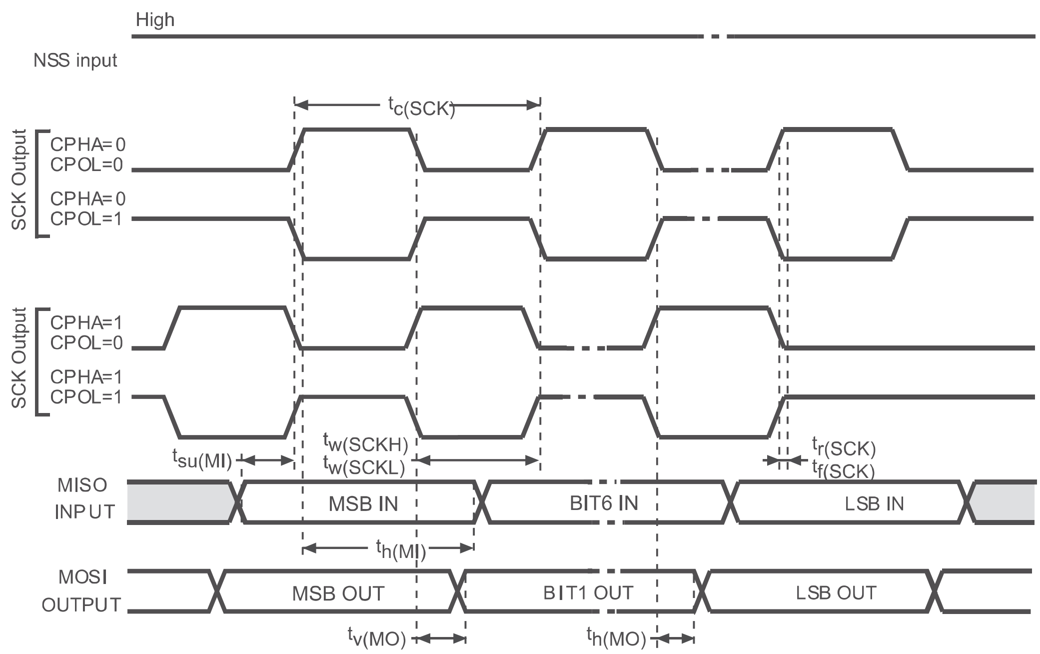


Figure 20. SPI timing diagram — master mode



3.15.4 I^2S timing

The instances SPI2 and SPI3 support the inter-IC sound (I2S) protocol.

Table 46. I^2S dynamic characteristics

Symbol		C	Parameter	Conditions (1)(2)(3)(4)(5)(6)	Value			Unit
					Min	Typ	Max	
f_{MCK}	CC	D	I^2S main clock output	—	256x8K	—	$256F_S$ (7)	MHz
f_{CK}	CC	D	I^2S clock frequency	Master data	—	—	$64F_S$	MHz

Symbol		C	Parameter	Conditions (1)(2)(3)(4)(5)(6)	Value			Unit
					Min	Typ	Max	
f_{CK}	CC	D	I^2S clock frequency	Slave data	—	—	$64F_S$	MHz
$t_{v(WS)}$	CC	D	WS valid time	Master mode	—	—	4	ns
$t_{h(WS)}$	CC	D	WS hold time	Master mode	-3	—	—	ns
$t_{su(WS)}$	CC	D	WS setup time	Slave mode	2	—	—	ns
$t_{h(WS)}$	CC	D	WS hold time	Slave mode	3	—	—	ns
$t_{su(SD\_MR)}$	CC	D	Data input setup time	Master receiver	2	—	—	ns
$t_{su(SD\_SR)}$	CC	D		Slave receiver	3	—	—	ns
$t_{h(SD\_MR)}$	CC	D	Data input hold time	Master receiver	4	—	—	ns
$t_{h(SD\_SR)}$	CC	D		Slave receiver	3	—	—	ns
$t_{v(SD\_ST)}$	CC	D	Data output valid time	Slave transmitter (after enable edge)	—	—	15	ns
$t_{v(SD\_MT)}$	CC	D		Master transmitter (after enable edge)	—	—	4	ns
$t_{h(SD\_ST)}$	CC	D	Data output hold time	Slave transmitter (after enable edge)	4	—	—	ns
$t_{h(SD\_MT)}$	CC	D		Master transmitter (after enable edge)	-2	—	—	ns

1. *All timing values for output signals in this table are measured to 50% of the output voltage.*
2. *All output timing is the worst case and includes the mismatching of rise and fall times of the output pads.*
3. *All timing values are valid for $V_{DD\_HV\_IO}$ = 3.3 V.*
4. *Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / automotive voltage thresholds.*
5. *Very Fast IO output characteristics.*
6. *Capacitive Load C_L = 25 pF.*
7. *Fs is the audio sampling frequency.*

Figure 21. I^2S slave timing diagram

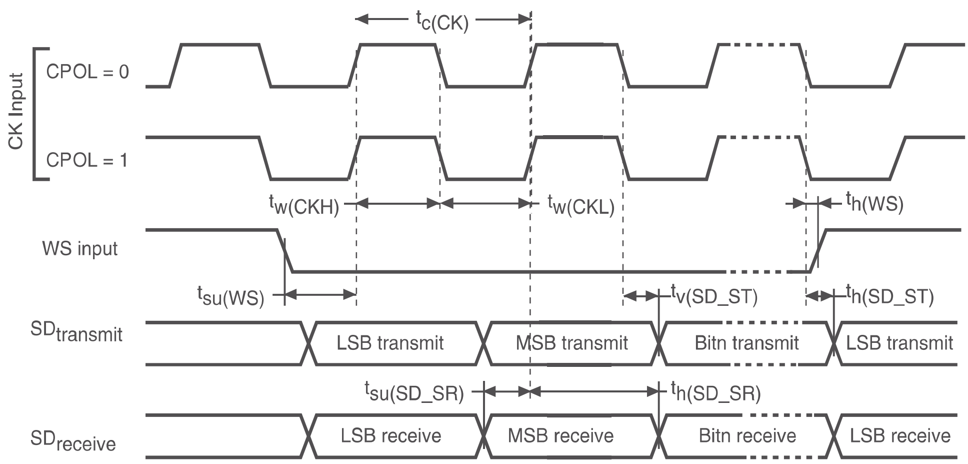
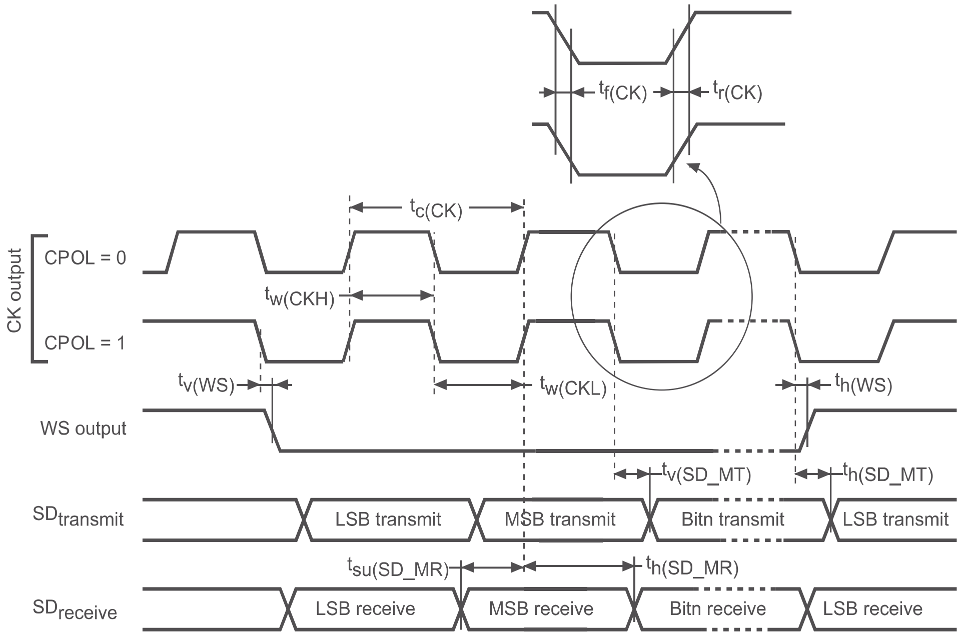


Figure 22. I²S master timing diagram



3.15.5 CAN timing

The following table describes the CAN timing.

Table 47. CAN timing

Symbol		C	Parameter	Condition	Value Min	Value Typ	Value Max	Unit
$t_{P(RX:TX)}$	CC	D	CAN controller propagation delay time standard pads	Fast type pads C_L = 25 pF	—	—	65	ns
	CC	D		Very Fast type pads C_L = 25 pF	—	—	60	

3.15.6 UART timing

UART channel frequency support is shown in the following table.

Table 48. UART frequency support

UART_CLK (MHz)	Oversampling rate	Condition	Max usable frequency (Mbaud)
100	16	—	6.25
	8		12.5

3.15.7 I²C timing

The I²C AC timing specifications are provided in the following tables.

Table 49. I²C input timing specifications — SCL and SDA

Symbol [(1)]		C	Parameter	Condition	Value			Unit	#
					Min	Typ	Max		
t_{SCHT}	CC	D	Start condition hold time	—	2	—	—	PER_CLK Cycle[(2)]	1
t_{CLT}	CC	D	Clock low time	—	8	—	—	PER_CLK Cycle	2
t_{BFT}	CC	D	Bus free time between Start and Stop condition	—	4.7	—	—	μs	3
t_{DHT}	CC	D	Data hold time	—	0.0	—	—	ns	4
t_{CHT}	CC	D	Clock high time	—	4	—	—	PER_CLK Cycle	5
t_{DST}	CC	D	Data setup time	—	0.0	—	—	ns	6
t_{START}	CC	D	Start condition setup time (for repeated start condition only)	—	2	—	—	PER_CLK Cycle	7
t_{STOP}	CC	D	Stop condition setup time	—	2	—	—	PER_CLK Cycle	8

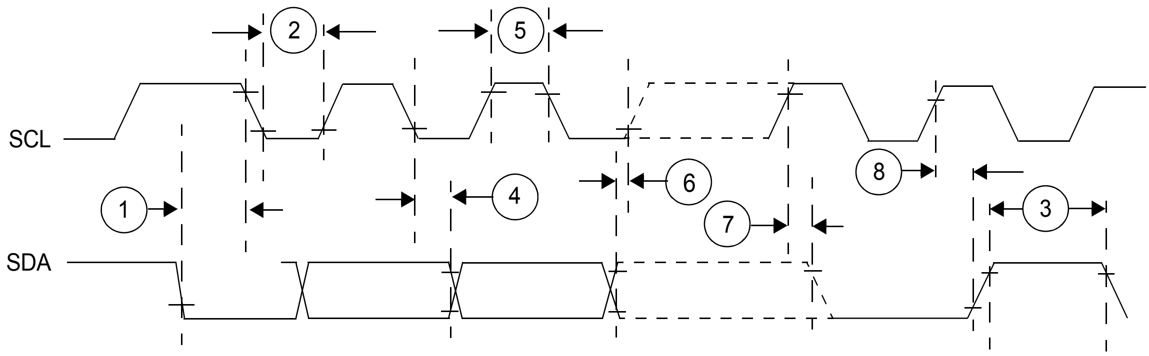
1. *I²C input timing is valid for automotive and TTL inputs levels, hysteresis enabled, and an input edge rate no slower than 1 ns (10% - 90%).*
2. *PER_CLK is the SoC peripheral clock, which drives the I²C BIU and module clock inputs. Refer to the device reference manual, Clocking chapter for more details.*

Table 50. I²C output timing specifications — SCL and SDA

Symbol		C	Parameters [(1)(2)(3)(4)]	Condition	Value			Unit	#
					Min	Typ	Max		
t_{SCHT}	CC	D	Start condition hold time	—	6	—	—	PER_CLK Cycle[(5)]	1
t_{CLT}	CC	D	Clock low time	—	10	—	—	PER_CLK Cycle	2
t_{BFT}	CC	D	Bus free time between start and stop condition	—	4.7	—	—	μs	3
t_{DHT}	CC	D	Data hold time	—	7	—	—	PER_CLK Cycle	4
t_{CHT}	CC	D	Clock high time	—	10	—	—	PER_CLK Cycle	5
t_{DST}	CC	D	Data setup time	—	2	—	—	PER_CLK Cycle	6
t_{START}	CC	D	Start condition setup time (for repeated start condition only)	—	20	—	—	PER_CLK Cycle	7
t_{STOP}	CC	D	Stop condition setup time	—	10	—	—	PER_CLK Cycle	8

1. *Programming the I2C_TIMINGR register (I²C bus frequency divider) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the pre-scale and division values programmed in the I2C_TIMINGR register.*
2. *Timing is specified to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.*
3. *Output parameters are valid for CL = 25 pF, where CL is the external load to the device (lumped). The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.*
4. *All output timing is the worst case and includes the mismatching of rise and fall times of the output pads.*
5. *PER_CLK is the SoC peripheral clock, which drives the I²C BIU and module clock inputs. Refer to the device reference manual, Clocking chapter for more details.*

Figure 23. I2C input/output timing



3.15.8 DLL block

DLL block is used to calibrate digital code for 1 period delay, which will be used by the HRTimer to provide the appropriate code for the required delay from any DELAY block.

Table 51. DLL electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
F_{HRTIM}	CC	D	Input clock frequency (DLL_CK)	—	200	—	306.7	MHz
T_{HRTIM}	CC	D	Input clock frequency (DLL_CK)	—	3.26	—	5	ns
T_{RES}	CC	D	High-resolution step size Tperiod/32	F_{HRTIM} = 306.7MHz	—	102	—	ps
T_{RF}	CC	D	Input clock rise/fall time (DLL_CK)	—	—	—	0.1	ns
Δ_{DLL_CK}	CC	D	Input clock duty cycle (DLL_CK)	—	40	50	60	%
T_{LOCK}	CC	D	Lock time	In term of input clock cycles	—	—	650	Input clock cycles
I_{AVG_CAL}	CC	D	Current consumption during calibration phase	Calibration mode	—	8[1]	10.6	mA
I_{AVG_PDn}	CC	D	Current consumption in power mode	Power down	—	3.8[1]	1100	µA
I_{AVG_TM}[2]	CC	D	Current consumption in test mode	Test mode	—	7.8[1]	12.3	mA

1. *Typical power consumption is at the Typical Process, Typical Temperature (25C) and Typical Voltage (1.26V).*
2. *Test mode power consumption is based on the testing at the mid-code of the calibration delay line (TEST_CMD_IN<10:0> = 111010 0000; Natural code = 704) and assuming that both delay lines are being tested at the same time. TEST_DELAY_EN=H, TEST_MODE_DELAY_0=H and TEST_MODE_DELAY_CMD=H.*

3.15.9 Delay block

Delay block is used to generate the desired pulse width modulation. When the command which allowed to lock the DLL is applied, the global duration of this delay block is 1 clock period. The HRTimer calculates from this value the command to be applied to obtain a delay equal to a fraction (1/32 to 31/32) of the clock period. One delay block is used for one PWM output.

Table 52. Delay electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
T_{RES}	CC	D	High-resolution step size Tperiod/32	F_{HRTIM} = 306.7MHz	—	102	—	ps
I_{AVG}	CC	D	Current consumption	Normal mode	—	940[(1)]	1125	µA
I_{AVG_PDn}[(2)]	CC	D	Current consumption in power mode	Power down	—	0.7[(1)]	130	µA
I_{AVG_TM}[(3)]	CC	D	Current consumption in test mode	Test mode	—	1.1[(1)]	1.9	mA
C_L	CC	D	Capactive load	Output drive for DELAY_OUT.	—	—	20	fF

1. *Typical power consumption is at the Typical Process, Typical Temperature (25C) and Typical Voltage (1.26V).*
2. *Power down mode power consumption mentioned is for DELAY_IN=L, TEST_MODE=L.*
3. *Test mode power consumption is at the mid-code of the delay line (DLL_CMD<10:0> = 111010 0000; Natural code = 704). DELAY_IN=H and TEST_MODE_DELAY=H.*

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

The following table lists the case numbers for SR5E1E3, SR5E1E5, SR5E1E7.

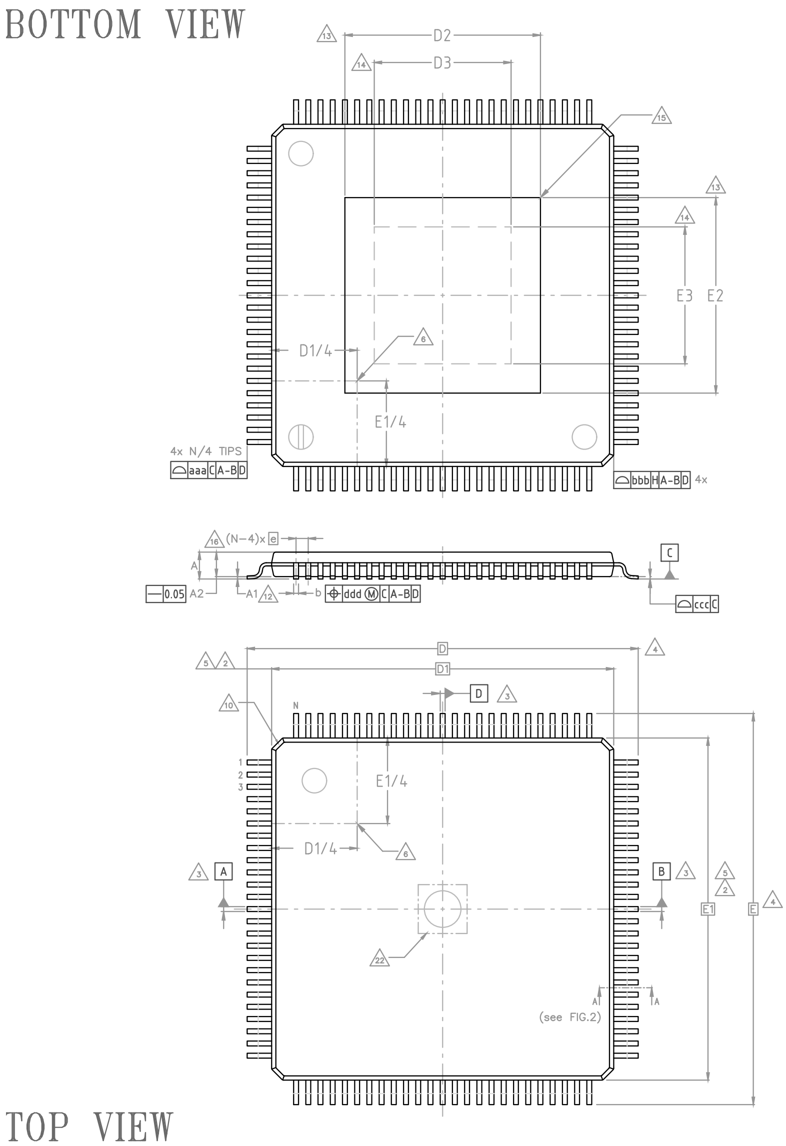
Table 53. Package case numbers

Package type	JEDEC reference specification
eTQFP100	JEDEC standard MS-026-D: MS-026-AED-HD
eTQFP144	JEDEC standard: MS-026-AFB-HD
eLQFP176	JEDEC standard MS-026-D: MS-026-BGA-HD

4.1 eTQPF100 package information

Refer to eTQFP100 package mechanical drawings and data information for the full description of the below figures and table notes.

Figure 24. eTQPF100 package outline



2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "0.25 mm" per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
10. The exact shape of each corner is optional.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from the exposed pad itself. The type of exposed pad is variable depending on leadframe pad design (T1, T2, T3), as shown in the figure below. The end user has to verify D2 and E2 dimensions according to the specific device application.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of the exposed pad, which is guaranteed to be free from resin flashes/bleeds, bordered by an internal edge of the inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. "N" is the number of terminal positions for the specified body size.
22. Notch may be present in this area (max 2.0 mm square) if center top gate molding technology is applied. Resin gate residual not protruding out of package top surface.

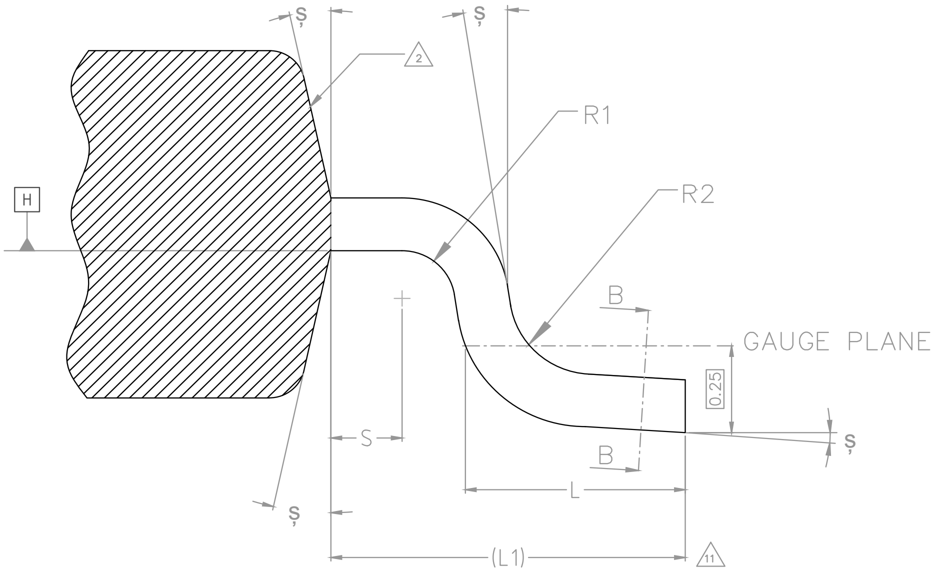


Figure 25. **eTQPF100 section A-A**

2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

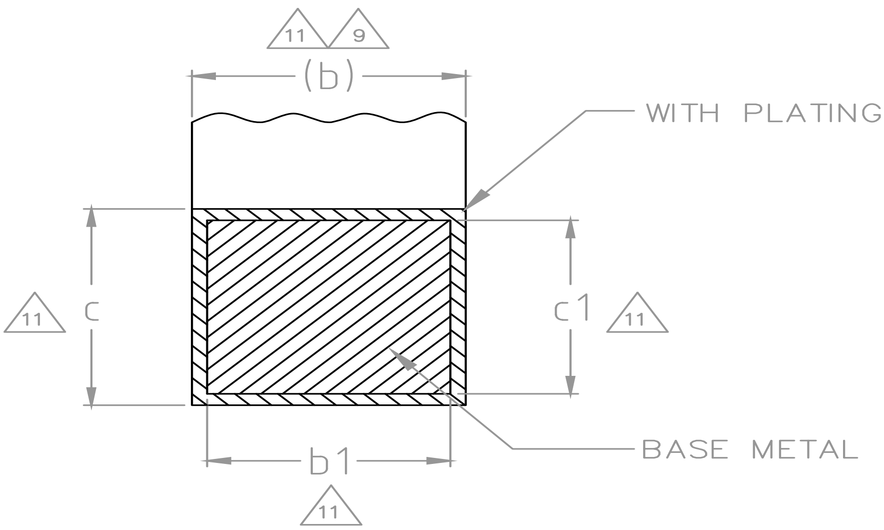


Figure 26. **eTQPF100 section B-B**

9. Dimension “b” does not include a dambar protrusion. Allowable dambar protrusion does not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between the protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

Table 54. eTQPF100 package mechanical data

Symbol	Dimensions[1][2]		
	Min.	Typ.	Max.
Θ	0°	3.5°	7°
Θ1	0°	—	—
Θ2	10°	12°	14°
Θ3	10°	12°	14°
A[3]	—	—	1.20
A1[4]	0.05	—	0.15
A2[3]	0.95	1.00	1.05
b[5][6][7]	0.17	0.22	0.27
b1[7]	0.17	0.20	0.23
c[7]	0.09	—	0.20
c1[7]	0.09	—	0.16
D[8]	16.00 BSC		
D1[9][10]	14.00 BSC		
D2[11]	—	—	6.77
D3[12]	5.10	—	—
e	0.50 BSC		
E[8]	16.00 BSC		
E1[9][10]	14.00 BSC		
E2[11]	—	—	6.77
E3[12]	5.10	—	—
L	0.45	0.60	0.75
L1	1.00 REF		
N[13]	100		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
aaa[14][15]	0.20		
bbb[14][15]	0.20		
ccc[14][15]	0.08		
ddd[14][15]	0.08		

1. *All Dimensions are in millimeters.*
2. *Critical dimensions: a. Stand-off, b. Overall width, c. Lead coplanarity.*
3. *The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.*
4. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
5. *No intrusion is allowed inwards the leads.*
6. *Dimension "b" does not include a dambar protrusion. Allowable dambar protrusion does not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between the protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.*
7. *These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
8. *To be determined at seating datum plane C.*

9. *The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.*
10. *Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.*
11. *Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from the exposed pad itself. The type of exposed pad is variable depending on leadframe pad design (T1, T2, T3), as shown in the figure below. The end user has to verify D2 and E2 dimensions according to the specific device application.*
12. *Dimensions D3 and E3 show the minimum solderable area, defined as the portion of the exposed pad, which is guaranteed to be free from resin flashes/bleeds, bordered by an internal edge of the inner groove.*
13. *“N” is the number of terminal positions for the specified body size.*
14. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*
15. *For Symbols, recommended values and tolerances see "Package symbol definition" table.*

Figure 27. eTQPF100 leadframe pad design

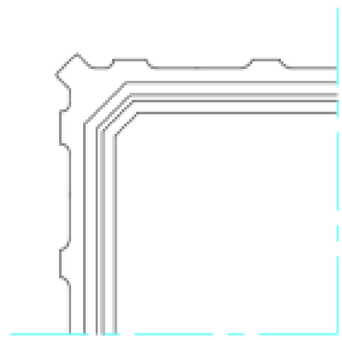
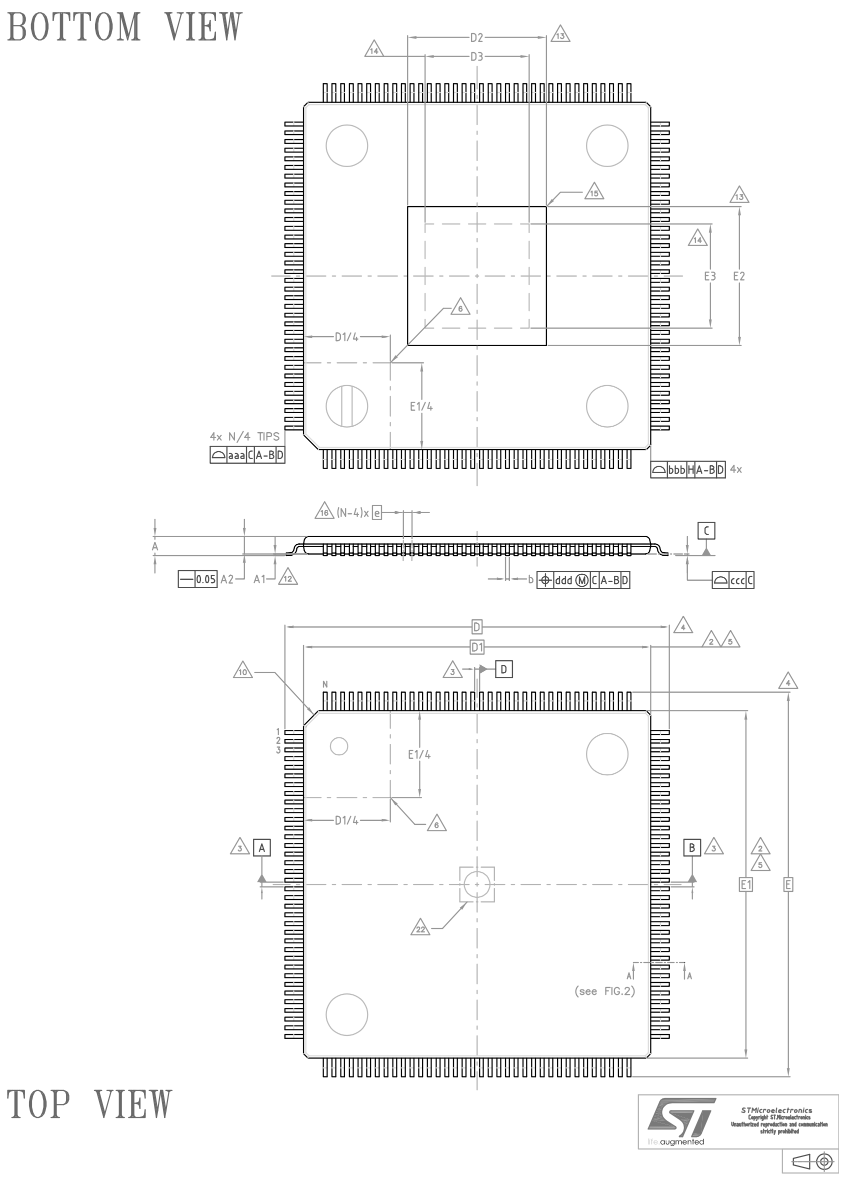


Table 55. eTQPF100 symbol definitions

Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to datum A and B. The center of the tolerance zone for each terminal is defined by a basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	—
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly known as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with a tolerance zone defined by “b”.

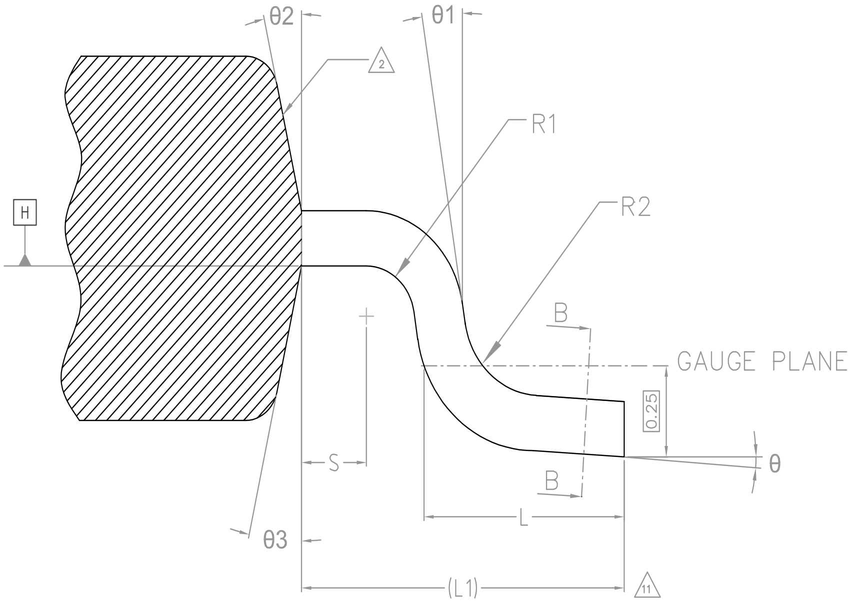
4.2 eTQFP144 package information

Figure 28. eLQFP144 package outline



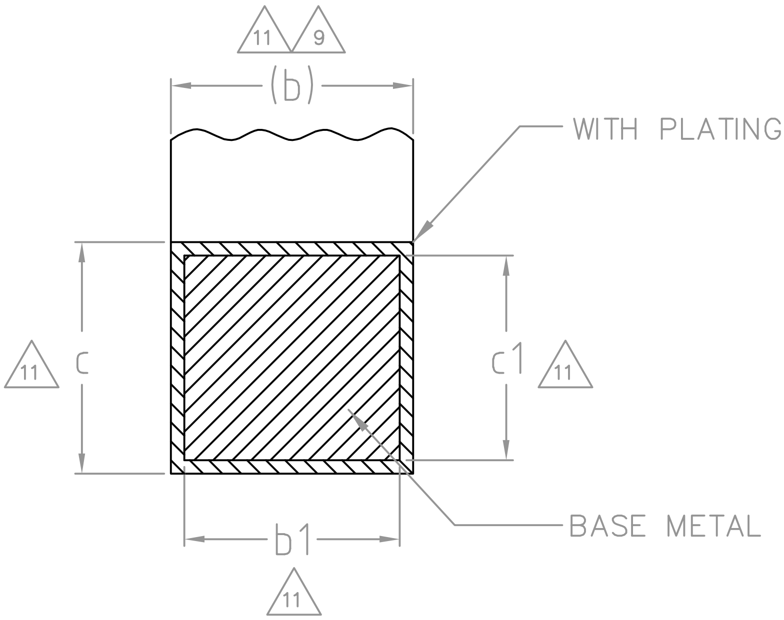
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
10. The exact shape of each corner is optional.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from the exposed pad itself. The type of exposed pad is variable depending on leadframe pad design (T1, T2, T3), as shown in the figure below. The end user has to verify D2 and E2 dimensions according to the specific device application.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of the exposed pad, which is guaranteed to be free from resin flashes/bleeds, bordered by an internal edge of the inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the number of terminal positions for the specified body size.
22. Notch may be present in this area (max 2.0 mm square) if center top gate molding technology is applied. Resin gate residual not protruding out of package top surface.

Figure 29. eLQFP144 section A-A (not to scale)



2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

Figure 30. eLQFP144 section B-B (not to scale)



9. Dimension “b” does not include a dambar protrusion. Allowable dambar protrusion does not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between the protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

Table 56. eLQFP144 package mechanical data

Symbol	Dimensions[1][2]		
	Min.	Typ.	Max.
q	0.0°	3.5°	7.0°
q1	0.0°	—	—
q2	10.0°	12.0°	14.0°
q3	10.0°	12.0°	14.0°
A[3]	—	—	1.20
A1[4]	0.05	—	0.15
A2[3]	0.95	1.00	1.05
b[5][6][7]	0.17	0.22	0.27
b1[7]	0.17	0.20	0.23
c[7]	0.09	—	0.20
c1[7]	0.09	—	0.16
D[8]	22.00 BSC		
D1[9][10]	20.00 BSC		
D2[11]	6.76		
D3[12]	5.1		
e	0.50 BSC		
E[8]	22.00 BSC		
E1[9][10]	20.00 BSC		
E2[11]	6.76		
E3[12]	5.1		
L	0.45	0.60	0.75
L1	—	1.00 REF	—
N[13]	144		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
aaa[14][15]	0.20		
bbb[14][15]	0.20		
ccc[14][15]	0.08		
ddd[14][15]	0.08		

1. *All Dimensions are in millimeters.*
2. *Critical dimensions: a. Stand-off, b. Overall width, c. Lead coplanarity.*
3. *The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.*
4. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
5. *No intrusion is allowed inwards the leads.*
6. *Dimension "b" does not include a dambar protrusion. Allowable dambar protrusion does not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between the protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.*
7. *These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
8. *To be determined at seating datum plane C.*

9. *The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.*
10. *Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.*
11. *Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from the exposed pad itself. The type of exposed pad is variable depending on leadframe pad design (T1, T2, T3), as shown in the figure below. The end user has to verify D2 and E2 dimensions according to the specific device application.*
12. *Dimensions D3 and E3 show the minimum solderable area, defined as the portion of the exposed pad, which is guaranteed to be free from resin flashes/bleeds, bordered by an internal edge of the inner groove.*
13. *“N” is the number of terminal positions for the specified body size.*
14. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*
15. *For Symbols, recommended values and tolerances see "Package symbol definition" table.*

Figure 31. eLQFP144 leadframe pad design

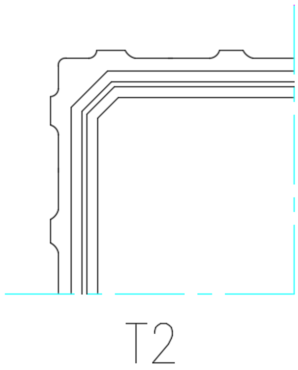
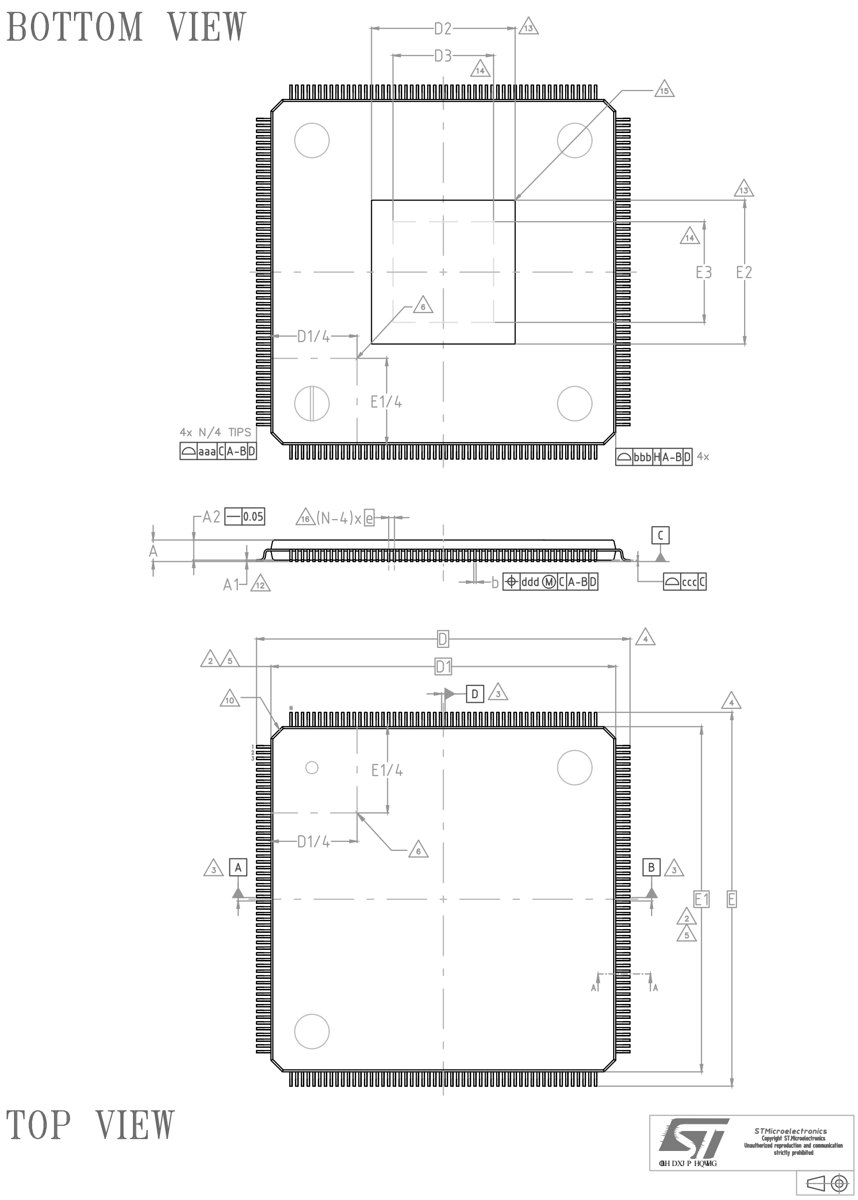


Table 57. eLQFP144 symbol definitions

Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to datum A and B. The center of the tolerance zone for each terminal is defined by a basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	—
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly known as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with a tolerance zone defined by “b”.

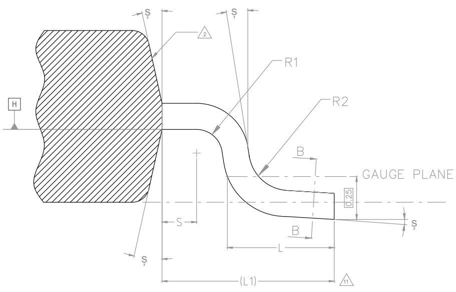
4.3 eLQFP176 package information

Figure 32. eLQFP176 package outline



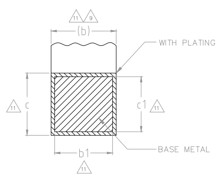
2.The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3.Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
10. The exact shape of each corner is optional.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from the exposed pad itself. The type of exposed pad is variable depending on leadframe pad design (T1, T2, T3), as shown in the figure below. The end user has to verify D2 and E2 dimensions according to the specific device application.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of the exposed pad, which is guaranteed to be free from resin flashes/bleeds, bordered by an internal edge of the inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the number of terminal positions for the specified body size.

Figure 33. eLQFP176 section A-A



2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

Figure 34. eLQFP176 section B-B



9. Dimension “b” does not include a dambar protrusion. Allowable dambar protrusion does not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between the protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

Table 58. **eLQFP176 package mechanical data**

Symbol	Dimensions(1)(2)		
	Min.	Nom.	Max.
Θ	0°	3.5°	7°
Θ1	0°	—	—
Θ2	10°	12°	14°
Θ3	10°	12°	14°
A(3)	—	—	1.60
A1(4)	0.05	—	0.15
A2(3)	1.35	1.40	1.45
b(5)(6)(7)	0.17	0.22	0.27
b1(7)	0.17	0.20	0.23
c(7)	0.09	—	0.20
c1(7)	0.09	—	0.16
D(8)	26.00 BSC		
D1(9)(10)	24.00 BSC		
D2(11)	—	—	7.77
D3(12)	6.10	—	—
e	0.50 BSC		
E(8)	26.00 BSC		
E1(9)(10)	24.00 BSC		
E2(11)	—	—	7.77
E3(12)	6.10	—	—
L	0.45	0.60	0.75
L1	1.00 REF		
N(13)	176		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	
aaa(14)(15)	0.20		
bbb(14)(15)	0.20		
ccc(14)(15)	0.08		
ddd(14)(15)	0.08		

1. *All Dimensions are in millimeters.*
2. *Critical dimensions: a. Stand-off, b. Overall width, c. Lead coplanarity.*
3. *The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.*
4. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
5. *No intrusion is allowed inwards the leads.*
6. *Dimension "b" does not include a dambar protrusion. Allowable dambar protrusion does not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between the protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.*
7. *These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
8. *To be determined at seating datum plane C.*

9. *The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.*
10. *Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.*
11. *Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from the exposed pad itself. The type of exposed pad is variable depending on leadframe pad design (T1, T2, T3), as shown in the figure below. The end user has to verify D2 and E2 dimensions according to the specific device application.*
12. *Dimensions D3 and E3 show the minimum solderable area, defined as the portion of the exposed pad, which is guaranteed to be free from resin flashes/bleeds, bordered by an internal edge of the inner groove.*
13. *“N” is the number of terminal positions for the specified body size.*
14. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*
15. *For Symbols, recommended values and tolerances see "Package symbol definition" table.*

Figure 35. eLQFP176 leadframe pad design

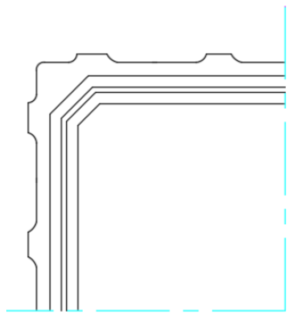


Table 59. eLQFP176 symbol definitions

Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to datum A and B. The center of the tolerance zone for each terminal is defined by a basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	—
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly known as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with a tolerance zone defined by “b”.

4.4 Package thermal characteristics

This section describes the thermal characteristics of the device.

The parameters in this chapter have been evaluated by considering the device consumption configuration reported in the Section 3.7: Device consumption.

4.4.1 eTQFP100 thermal characteristics

Table 60. eTQPF100 thermal characteristics

Symbol		C	Parameter[1]	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board (2s2p)	22.4	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[3]	—	7.5	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case top[4]	—	9.9	°C/W
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom[5]	—	1.6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top[6]	Natural convection	0.4	°C/W

1. *Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, power dissipation of other components on the board, and board thermal resistance.*
2. *Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.*
3. *Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.*
4. *Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).*
5. *Thermal resistance between the die and the exposed pad ground on the bottom of the package based on simulation without any interface resistance.*
6. *Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.*

4.4.2 eTQFP144 thermal characteristics

Table 61. eLQFP144 thermal characteristics

Symbol		C	Parameter[1]	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection[2]	Four layer board (2s2p)	21.9	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[3]	—	8.6	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case top[4]	—	11.5	°C/W
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom[5]	—	1.6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top[6]	Natural convection	0.4	°C/W

1. *Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.*
2. *Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.*
3. *Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.*
4. *Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).*
5. *Thermal resistance between the die and the exposed pad ground on the bottom of the package based on simulation without any interface resistance.*
6. *Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.*

4.4.3 eLQFP176 thermal characteristics

Table 62. eLQFP176 thermal characteristics

Symbol		C	Parameter[1]	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board (2s2p)	20.8	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[3]	—	8.6	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case top[4]	—	12.2	°C/W
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom[5]	—	1.6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top[6]	Natural convection	0.5	°C/W

1. *Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.*
2. *Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.*
3. *Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.*
4. *Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).*
5. *Thermal resistance between the die and the exposed pad ground on the bottom of the package based on simulation without any interface resistance.*
6. *Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.*

4.4.4 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

Where:

- T_A = ambient temperature for the package (°C)
- $R_{\Theta JA}$ = junction-to-ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The differences between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power, and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board, which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leaves the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. Very often, for natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \quad (4)$$

Where:

- T_B = board temperature for the package perimeter (°C)
- $R_{\Theta JB}$= junction-to-board thermal resistance (°C/W) per JESD51-8
- P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition: with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of the junction-to-case thermal resistance plus the case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad (5)$$

Where:

- $R_{\Theta JA}$= junction-to-ambient thermal resistance (°C/W)
- $R_{\Theta JC}$= junction-to-case thermal resistance (°C/W)
- $R_{\Theta CA}$= case-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ is device-related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\Theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to the heat sink to the ambient environment. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + \left(\psi_{JT} \times P_D\right) \tag{6}$$

Where:

- T_T = thermocouple temperature on the top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and on approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When the board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

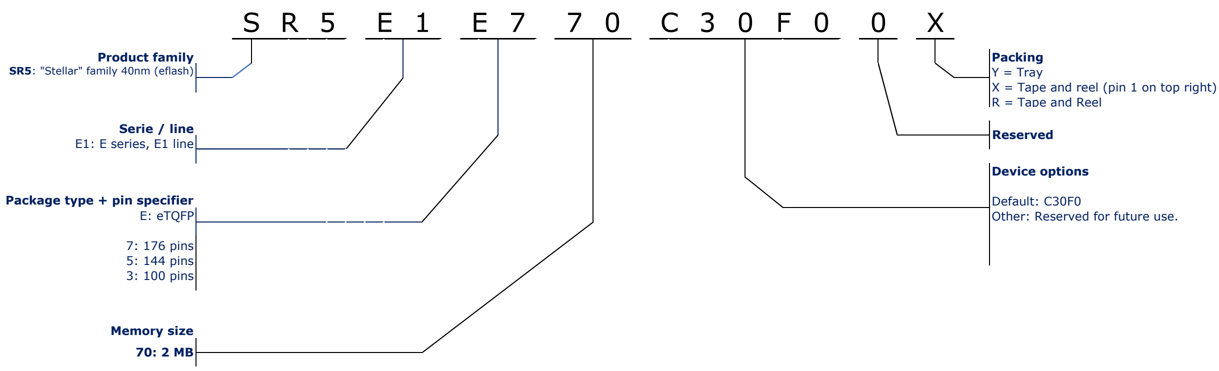
$$T_J = T_B + \left(\psi_{JPB} \times P_D\right) \tag{7}$$

Where:

- T_B = board temperature for the package perimeter (°C)
- Ψ_{JPB} = junction temperature parameter (°C/W)
- P_D = power dissipation in the package (W)

5 Ordering information

Figure 36. Ordering information scheme



Revision history

Table 63. **Document revision history**

Date	Revision	Changes
07-Apr-2022	1	Initial internal release.
02-Jan-2023	2	Second internal release.
02-Feb-2023	3	Third internal release.
24-Oct-2023	4	Fourth internal release.
18-Dec-2023	5	• First public release • Changed the confidentiality level of the document • In the whole document: – replaced SR5E1x with part numbers – minor editorial changes • Table 5. Operating conditions: I_{INJ2}, updated Min, Typ, and Max values • Table 12. I/O input electrical characteristics: – I_{LKG}, updated the Max value of "INPUT-ONLY pads" – C_{P1}, updated the Max value • Table 14. Slow I/O output characteristics: I_{DCMAX_S}, updated Max value • Table 15. Medium I/O output characteristics: I_{DCMAX_M}, updated Max value • Table 16. Fast I/O output characteristics: I_{DCMAX_F}, updated Max value • Table 17. Very fast I/O output characteristics: I_{DCMAX_V}, updated Max value • Table 27. ADC pin specification: C_{P2}, updated Max value • Table 32. Temperature sensor electrical characteristics: – Temperature monitoring range, updated "C" column – $T_{flagm40}$, updated "C" column – $T_{flagm150}$, updated "C" column • Table 34. Buffered-DAC electrical specification: – DNL, updated Max value – TUE, updated Min and Max values. Removed the note – GAIN_err, updated Max value • Table 38. Voltage monitor electrical characteristics: V_{DD_LV}, updated Max value of parameter "POR031_C"
19-Dec-2023	6	• Section 5: Ordering information: pin specifier, added the option “5: 144 pins”

Contents

Glossary

AC Alternating current

ADC Analog-to-digital converter

AEC Automotive Electronics Council. Also known as CDF-AEC for Chrysler-Delco-Ford Automotive Electronics Council. Shortened to AEC.

AHB Advanced high-performance bus

ALC Automatic level control

ANSI American National Standards Institute

APB Advanced peripheral bus

ASIL Automotive safety integrity level

It is a risk classification system defined by the ISO 26262 standard for the functional safety of road vehicles. There are four ASILs identified by ISO 26262—A, B, C, and D. ASIL A represents the lowest degree and ASIL D represents the highest degree of automotive hazard.

AXI Advanced extensible interface

CAN Controller area network

CAN FD® Controller area network flexible data rate

CBC Cipher block chaining

CDM Charged device model

CMAC Cipher-based message authentication code

CMOS Complementary metal-oxide-semiconductor

CPHA Clock phase bit. Selects the clock phase.

CPOL Clock polarity bit. Selects the clock polarity.

CPU Central processing unit

CTI Arm® CoreSight™ cross-trigger interface

CTM Cross-trigger matrix

DAC Digital-to-analog converter

DC Direct current

DCF Device configuration format

DMA Direct memory access

DNL Differential nonlinearity

ECB Electronic code book

ECC Error correction code

ECU Engine control unit

eDMA Enhanced direct memory access

EEPROM Electrically erasable programmable read-only memory

EMC Electromagnetic compatibility

ESD Electrostatic discharge

ESR Equivalent series resistance

EVITA e-safety vehicle intrusion protected applications

EXTAL External oscillator input

FCCU Fault collection and control unit

FIFO First in, first out

FIR Finite-impulse response

FPU Floating-point unit

GCM Galois/counter mode

GPIO General-purpose input/output

HBM Human body model

HSM Hardware security module

I/O Input/output

IEC International Electrotechnical Commission

IEEE Institute of Electrical and Electronics Engineers

IP Intellectual property

IPC Institute of Printed Circuits

IRCOSC Internal RC oscillator

IRQ Interrupt request

ISO International Organization for Standardization

I²C Inter-integrated circuit

I²S Integrated interchip sound

JCOMP JTAG compliance (pin)

JEDEC Joint Electron Device Engineering Council

JTAG Joint Test Action Group

KB Kilobyte

LIN Local interconnect network

LSB Least significant byte

LV Low voltage

LVD Low-voltage detector

MB Mebabyte

MCR Module configuration register

MCU Microcontroller unit

MD Modulation depth

MEMU Memory error management unit

MISO Master input slave output

MOSFET Metal-oxide-semiconductor field-effect transistor

MOSI Master output slave input

NMOS N-type metal–oxide–semiconductor

NVM Nonvolatile memory

OSR Oversampling ratio

OTA Over the air

PC Printed circuit

PCB Printed-circuit board

PHI PLL output clock

PLL Phase-locked loop

PWM Pulse-width modulation

RAM Random access memory

RC Resistor-capacitor

SAR Successive approximation register

SARADC Successive-approximation register analog-to-digital converter

SAR SV SAR supervisor

SCK SPI clock (SPI and other SPI-related specifications such as queued SPI)

SCL Serial clock line (I²C signal)

SD Secure digital

SDADC Sigma-delta analog-to-digital converter

SDIO Secure digital input/output

SoC System on chip

SPI Serial peripheral interface

SRAM Static random-access memory

SSCG Spread-spectrum clock generation

SWD Secondary debug port

TCK Test clock (JTAG standard)

TCM Tightly coupled memory

TMS Test mode select

TRNG True random number generator

TTL Transistor-to-transistor logic

TUE Total unadjusted error

UART Universal asynchronous receiver/transmitter

UTEST User-programmed DCF records.

Some UTEST DCF records are written at the factory during production testing. Others are written by the end user and programmed at the same time as the application code.

UVD Maximum-voltage detector

VCO Voltage-controlled oscillator

WS Wait state

XOSC Crystal oscillator

XTAL External oscillator output

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