

APDS-9253-001

Digital RGB Sensor

Overview

The Broadcom[®] APDS-9253-001 is a digital RGB Sensor in a miniature package that enables the sensor to be designed into space-sensitive applications.

The APDS-9253-001 device uses four individual channels of red, green, blue, and IR (RGB+IR) in a specially designed matrix arrangement. This allows the device to have optimal angular response and accurate RGB spectral response with high Lux accuracy over various light sources. The device detects light intensity under a variety of lighting conditions and through a variety of attenuation materials, including dark glass.

APDS-9253-001 can be configured as an Ambient Light Sensor (ALS) and RGB+IR Sensor.

Ordering Information

| Part Number | Packaging | Quantity |
|---------------|-------------|----------|
| APDS-9253-001 | Tape & Reel | 2,500 |

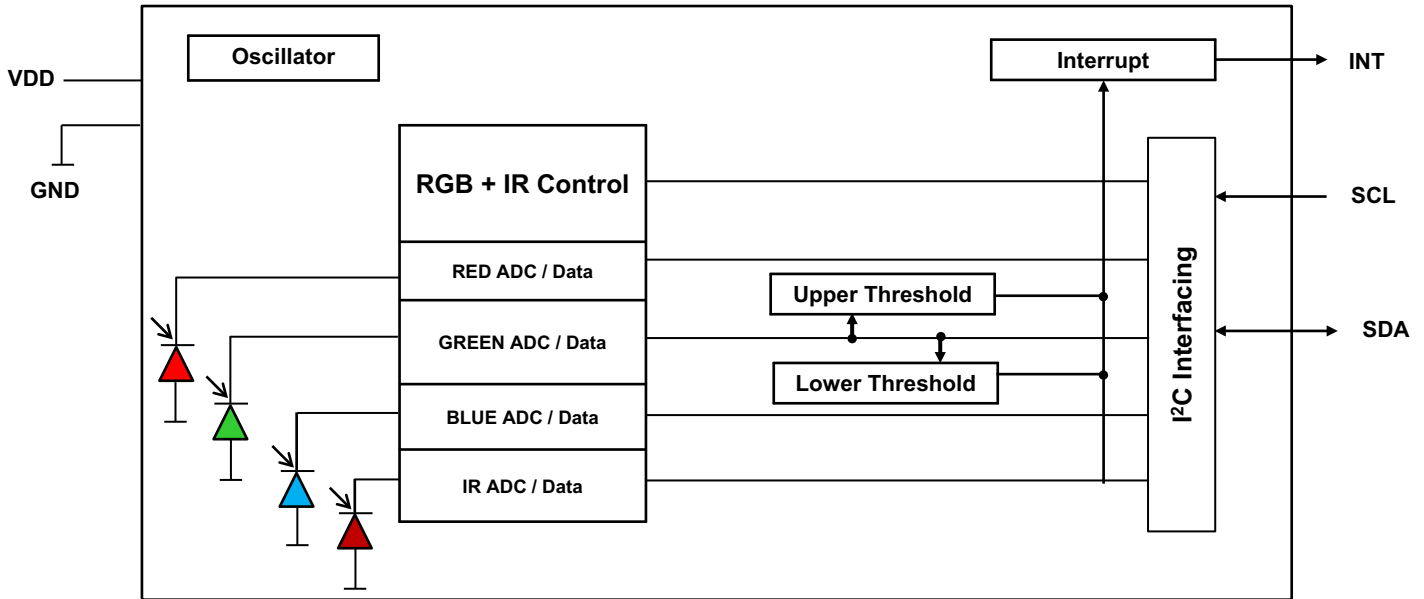
Features

- RGB and ambient light sensing (RGB and ALS)
 - Accuracy of correlated color temperature (CCT)
 - Individual channels for red, green, blue and infrared
 - Approximates human eye response with green channel
 - Light output proportional to light intensity
 - Utilizes optical coating technology to emulate human eye spectral response
 - Works well under different light source conditions
 - Low light sensitivity; operates behind darkened glass
 - 50 Hz/60 Hz light flicker immunity
 - Fluorescent light flicker immunity
 - Programmable interrupt function with upper, lower thresholds and persists function
 - Programmable ALS integration time
 - Programmable ALS gain setting
- Supply voltage 1.7V to 3.6V
- Power management
 - Low active current
 - Low standby current
- I²C interface compatible
 - Up to 400 kHz (I2C fast-mode)
 - Dedicated interrupt pin
- Miniature package
 - L 1.70 mm × W 1.30 mm × H 0.60 mm

Applications

- Cell phone touch-screen disable
- Detection of ambient light to control display backlighting
 - Wearable devices: smart watch
 - Mobile devices: cell phone, PDAs, PMP
 - Computing devices: notebook, tablet PC, keyboard
 - Consumer devices: LCD monitor, TV, video camera, digital still camera
- Automatic residential and commercial lighting management

Functional Block Diagram



I/O Pins Configuration

| Pin | Name | Type | Description |
|-----|-----------------|--------|--|
| 1 | GND | Ground | Power supply ground. All voltages are referenced to GND. |
| 2 | INT | O | Interrupt. Open drain. |
| 3 | NC | | No connect. |
| 4 | V _{DD} | Supply | Power supply voltage. |
| 5 | SDA | I/O | Serial data I/O for I ² C. |
| 6 | SCL | I | I ² C serial clock input terminal. Clock signal for I ² C serial data. |

Absolute Maximum Ratings

Over operating free-air temperature range.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

| Parameter | Symbol | Min | Max | Unit | Conditions |
|-----------------------------------|-----------------|------|------|------|------------|
| Power Supply Voltage ^a | V _{DD} | — | 3.63 | V | |
| Digital Voltage Range | | -0.5 | 3.63 | V | |
| Storage Temperature Range | Tstg | -40 | 100 | °C | |

a. All voltages are with respect to GND.

Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|----------|-----|-----|-----|------|
| Operating Ambient Temperature | T_A | -40 | — | 85 | °C |
| Supply Voltage | V_{DD} | 1.7 | — | 3.6 | V |
| Supply Voltage Accuracy, V_{DD} Total Error Including Transients | | -1 | — | 1 | % |

Operating Characteristics

$V_{DD} = 2.8V$, $T_A = 25^\circ C$ (unless otherwise noted).

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|-------------------------------------|------------|-----|-----|----------|---------|-----------------|
| SCL, SDA Input High Voltage | V_{IH} | 1.5 | — | V_{DD} | V | |
| SCL, SDA Input Low Voltage | V_{IL} | 0 | — | 0.4 | V | |
| INT, SDA Output Low Voltage | V_{OL} | 0 | — | 0.4 | V | |
| Leakage Current, SDA, SCL, INT Pins | I_{LEAK} | -5 | — | 5 | μA | |

RGB Optical Characteristics

$V_{DD} = 2.8V$, $T_A = 25^\circ C$ (unless otherwise noted).

| Parameter | Test Condition | RED Channel | | Green Channel | | Blue Channel | | IR Channel | | Unit |
|---------------------|-----------------|-------------|-----|---------------|-----|--------------|-----|------------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Irradiance Response | $\lambda = 465$ | 0 | 8 | 6 | 22 | 85 | 115 | 0 | 4 | % |
| | $\lambda = 525$ | 2 | 14 | 85 | 115 | 10 | 30 | 0 | 3 | |
| | $\lambda = 625$ | 85 | 115 | 18 | 37 | 0 | 3 | 0 | 3 | |
| | $\lambda = 850$ | 0 | 3 | 0 | 3 | 0 | 3 | 85 | 115 | |

NOTE:

- The percentage shown represents the ratio of the respective red, green, or blue channel value to the IR channel value.
- The 465 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength $\lambda_D = 465$ nm, spectral halfwidth $\Delta\lambda^{1/2} = 22$ nm.
- The 525 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength $\lambda_D = 525$ nm, spectral halfwidth $\Delta\lambda^{1/2} = 35$ nm.
- The 625 nm input irradiance is supplied by an AlInGaP light-emitting diode with the following characteristics: dominant wavelength $\lambda_D = 625$ nm, spectral halfwidth $\Delta\lambda^{1/2} = 15$ nm.
- The 850 nm input irradiance is supplied by an AlInGaP light-emitting diode with the following characteristics: dominant wavelength $\lambda_D = 850$ nm, spectral halfwidth $\Delta\lambda^{1/2} = 40$ nm.

RGB/ALS Characteristics

$V_{DD} = 2.8V$, $T_A = 25^\circ C$ (unless otherwise noted).

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|------------------------------|--------------------------|-------|-------|------|---------|---|
| Supply Current | I_{DD} | — | 118 | 154 | μA | Active mode |
| | | — | 1 | 2 | μA | Standby mode |
| Peak Wavelength | $\lambda_{P_ALS/Green}$ | — | 550 | — | nm | |
| | λ_{P_Red} | — | 610 | — | nm | |
| | λ_{P_Blue} | — | 470 | — | nm | |
| Min. Integration Time | $T_{intmin1}$ | — | 3.125 | — | ms | |
| | $T_{intmin2}$ | — | 50 | — | ms | With 50 Hz/60 Hz rejection |
| Max Integration Time | $T_{intmax1}$ | — | 400 | — | ms | With 50 Hz/60 Hz rejection |
| Output Resolution | RES_{ALS} | 13 | 18 | 20 | bit | Programmable |
| ADC Count Value (ALS/Green) | | 12500 | — | — | counts | White LED 5600 K, 200 lux, 200 ms, Gain = 18x |
| ADC Count Value (ALS/Green) | | 1190 | 1400 | 1610 | counts | $\lambda = 525$ nm, 50 ms, Gain = 3x, $E_e = 72 \mu W/cm^2$ |
| ADC Count Value (Red) | | 1275 | 1500 | 1725 | counts | $\lambda = 625$ nm, 50 ms, Gain = 3x, $E_e = 78 \mu W/cm^2$ |
| ADC Count Value (Blue) | | 1190 | 1400 | 1610 | counts | $\lambda = 465$ nm, 50 ms, Gain = 3x, $E_e = 73 \mu W/cm^2$ |
| Dark Count Value (ALS/Green) | | 0 | — | 4 | counts | Gain = 18x, 400 ms, $E_e = 0$ |
| Dark Count Value (Red) | | 0 | — | 4 | counts | Gain = 18x, 400 ms, $E_e = 0$ |
| Dark Count Value (Blue) | | 0 | — | 4 | counts | Gain = 18x, 400 ms, $E_e = 0$ |

Figure 1: Spectral Response

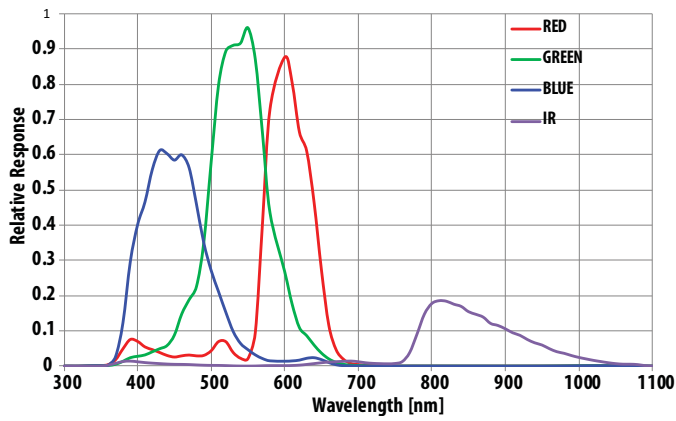


Figure 2: ALS Sensor LUX vs. Meter LUX Using White Light

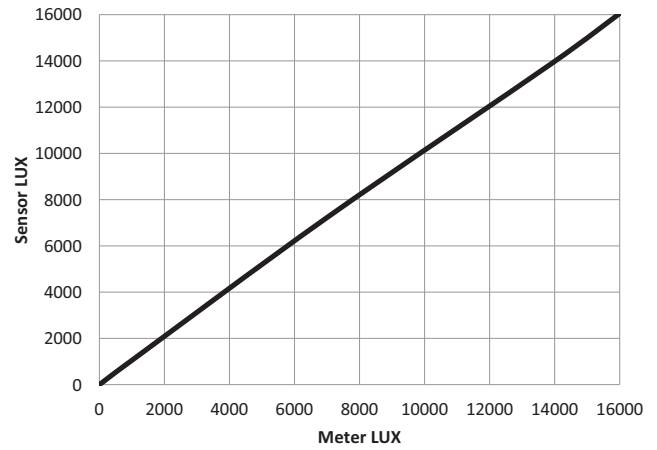


Figure 3: Normalized I_{DD} vs. V_{DD}

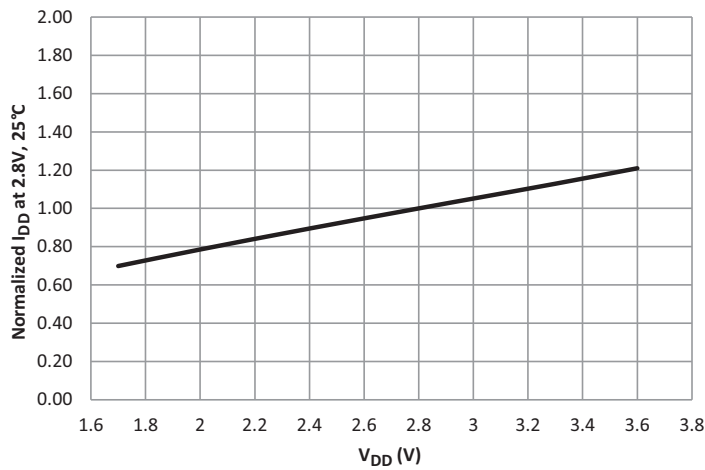


Figure 4: Normalized I_{DD} vs. Temperature

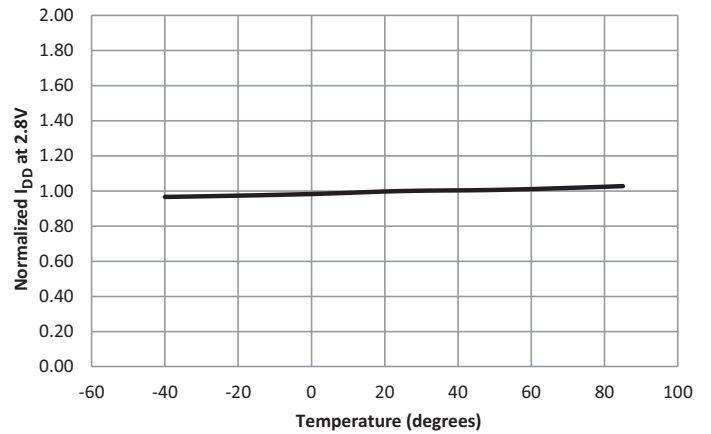


Figure 5: Normalized ALS PD Responsivity vs. Angular Displacement (Perpendicular Axis)

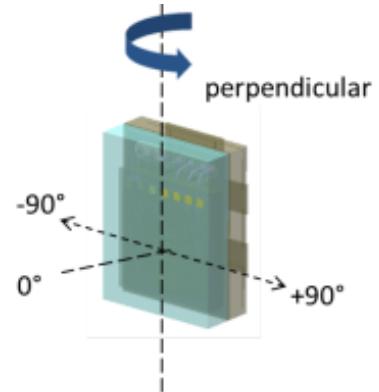
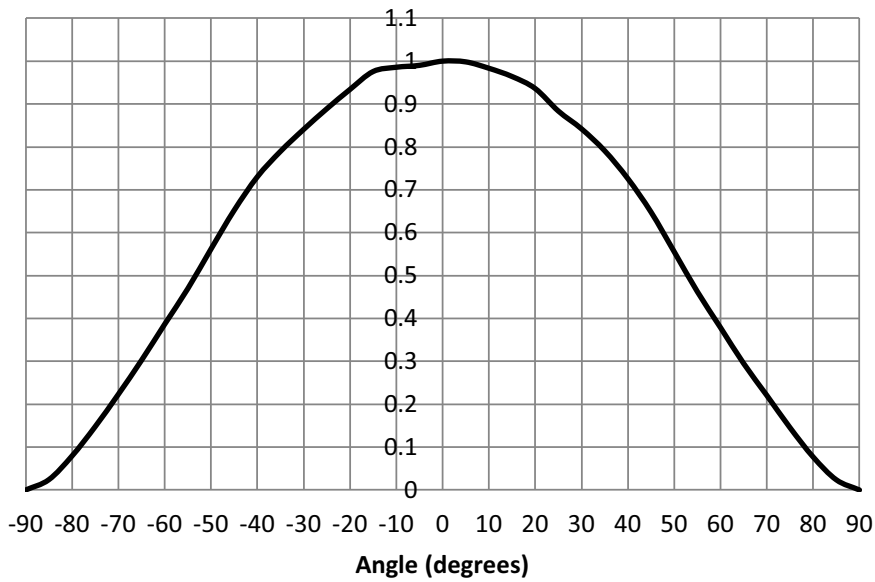
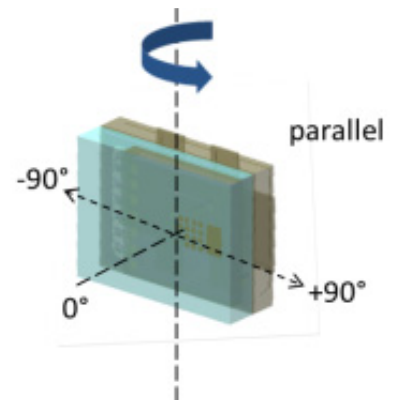
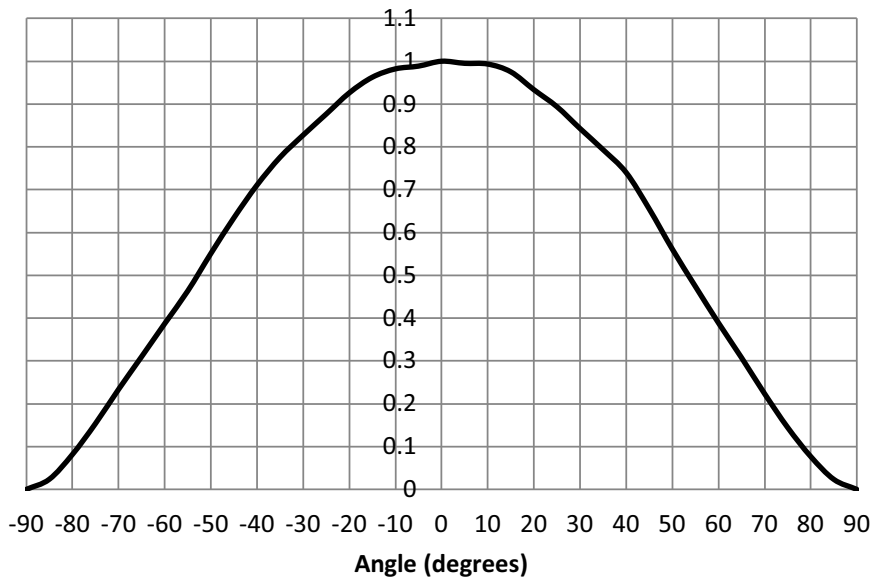


Figure 6: Normalized ALS PD Responsivity vs. Angular Displacement (Parallel Axis)



ALS Gain and Resolution Characteristics

| Gain | Resolution (bits) | Integration Time, itime (ms) | Min Lux | Max Lux | Resolution (lux/count) |
|-------------------------------|-------------------|--------------------------------|--------------|---------------|------------------------|
| 1x | 16 | 25 | 2.193 | 143719 | 2.193 |
| | 17 | 50 | 1.099 | 144035 | 1.099 |
| | 18 | 100 (default) | 0.548 | 143562 | 0.548 |
| | 19 | 200 | 0.273 | 143131 | 0.273 |
| | 20 | 400 | 0.136 | 143092 | 0.136 |
| 3x (default) | 16 | 25 | 0.722 | 47318 | 0.722 |
| | 17 | 50 | 0.359 | 47114 | 0.359 |
| | 18 | 100 (default) | 0.180 | 47182 | 0.180 |
| | 19 | 200 | 0.090 | 47212 | 0.090 |
| | 20 | 400 | 0.045 | 47023 | 0.045 |
| 6x | 16 | 25 | 0.360 | 23608 | 0.360 |
| | 17 | 50 | 0.179 | 23494 | 0.179 |
| | 18 | 100 (default) | 0.090 | 23544 | 0.090 |
| | 19 | 200 | 0.045 | 23531 | 0.045 |
| | 20 | 400 | 0.022 | 23501 | 0.022 |
| 9x | 16 | 25 | 0.239 | 15652 | 0.239 |
| | 17 | 50 | 0.119 | 15619 | 0.119 |
| | 18 | 100 (default) | 0.059 | 15564 | 0.059 |
| | 19 | 200 | 0.030 | 15612 | 0.030 |
| | 20 | 400 | 0.015 | 15630 | 0.015 |
| 18x | 16 | 25 | 0.117 | 7655 | 0.117 |
| | 17 | 50 | 0.059 | 7685 | 0.059 |
| | 18 | 100 (default) | 0.029 | 7680 | 0.029 |
| | 19 | 200 | 0.015 | 7688 | 0.015 |
| | 20 | 400 | 0.007 | 7688 | 0.007 |

Principles of Operation

System State Machine

Start Up after Power-On or Software Reset

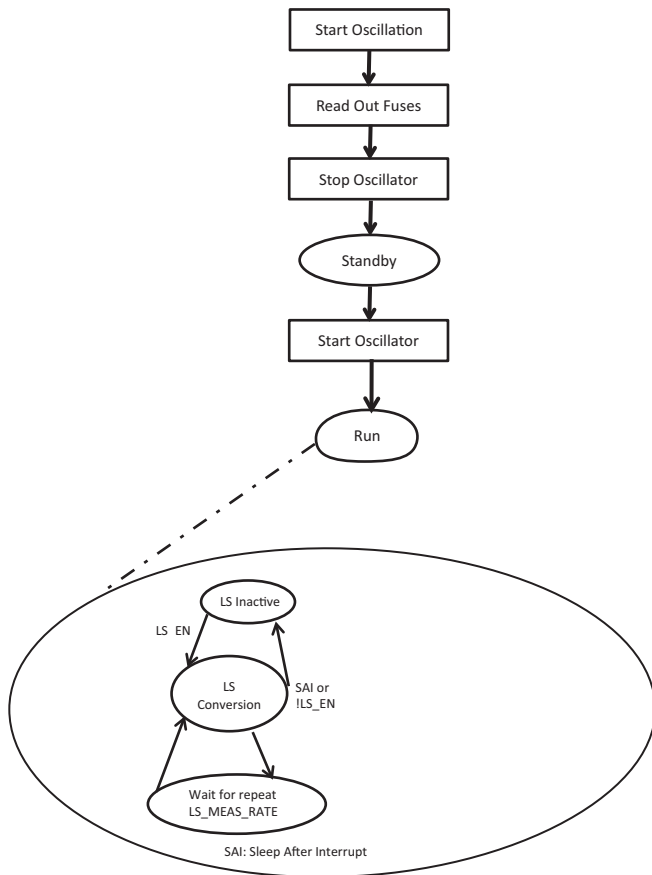
The main state machine is set to Start State during power-on or software reset. As soon as the reset is released, the internal oscillator is started and the programmed I²C address and the trim values are read from the internal non-volatile memory (NVM) trimming data block. The device enters Standby Mode as soon as the Idle State is reached.

If any of the sensor operation modes becomes activated through an I²C command (i.e., the LS_EN bit is set to 1 and the sensor mode is selected with the respective bit in the MAIN_CTRL register), the internal support blocks are immediately powered on. Once the voltages and currents are settled (typical after 500 μs), the state machine checks for trigger events from a measurement scheduler to start conversions according to the selected measurement repeat rates.

When the user resets the LS_EN bit to 0, a running conversion is completed and the relevant ADCs move to Standby Mode thereafter. The support blocks only move to Standby Mode if all sensors are Inactive. If any of the sensors is programmed to sleep after interrupt with the according bit in the MAIN_CTRL register, the relevant ADCs move to Standby Mode after the interrupt condition occurred. Also the sensor's Enable bit LS_EN is reset after following read out of Main Status register.

The deactivation LS in the MAIN_CTRL register does not clear the related status bit in the MAIN_STATUS register. They are always reset upon activation of the respective sensor.

Figure 7: System Main State Machine



Light Sensor Operation

APDS-9253-001 can be configured to run in ALS mode or in RGB mode. The difference between both submodes of the light sensor (LS) is in the activation of the sensor channels. ALS mode is offered for power saving if the full RGB functionality is not needed.

Light Sensor Interrupt

The interrupt is configured by the bit in the INT_CFG register. It can function as either threshold triggered (LS_VAR_MODE = 0) or variance triggered (LS_VAR_MODE = 1).

The threshold interrupt is enabled with LS_INT_EN = 1 and LS_VAR_MODE = 0. The interrupt is set when the respective LS_DATA register of the selected interrupt source channel is above the upper or below the lower threshold configured in the LS_THRES_UP and LS_THRES_LOW registers for a specified number of consecutive measurements as configured in the INT_PST register (1+LS_PERSIST).

The variance interrupt is enabled with LS_INT_EN = 1 and LS_VAR_MODE = 1. It is set when the absolute value difference between the preceding and the current output data of the selected interrupt source channel is above the decoded variance threshold for a specified number of consecutive measurements (1+LS_PERSIST).

For LS, an interrupt can also be triggered if the output variation of consecutive conversions has exceeded a defined limit.

I²C Protocol

Interface and control of the APDS-9253-001 is accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The device supports a single slave address of 0x52 hex using 7-bit addressing protocol. (Contact factory for other addressing options.)

I²C Register Read

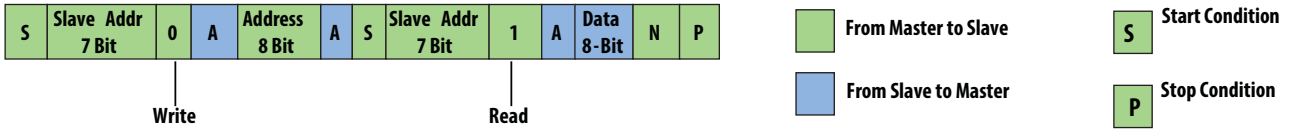
The registers can be read individually or in block read mode. When two or more bytes are read in block read mode, reserved register addresses are skipped and the next valid address is referenced. If the last valid address has been reached, but the master continues with the block read, the address counter in the device does not roll over and the device returns 00HEX for every subsequent byte read.

The block read operation is the only way to ensure correct data read out of multi-byte registers and to avoid splitting of results with HIGH and LOW bytes originating from different conversions. During block read access on ALS result registers, the result update is blocked.

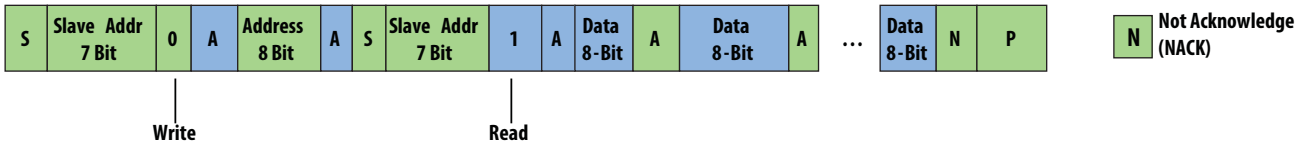
If a read access is started on an address belonging to a non-readable register, the APDS-9253-001 returns NACK until the I²C operation is ended.

Read operations must follow this timing diagram.

Register Read (I²C™ Read)



Register Block Read (I²C™ Read)



I²C Register Write

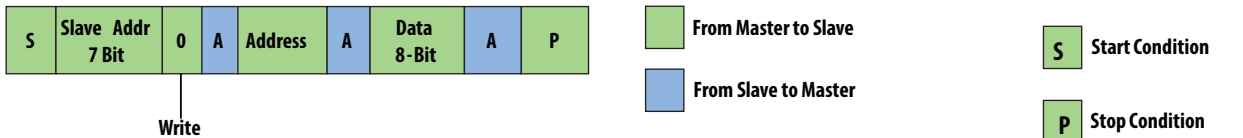
The APDS-9253-001 registers can be written to individually or in block write mode. When two or more bytes are written in block write mode, reserved registers and read-only registers are skipped. The transmitted data is automatically applied to the next writable register. If a register includes read (R) and read/write (RW) bit, the register is not skipped. Data written to read-only bit is ignored.

If the last valid address of the APDS-9253-001 address range is reached but the master attempts to continue the block write operation, the address counter of the APDS-9253-001 does not roll over. The APDS-9253-001 returns NACK for every following byte sent by the master until the I²C operation is ended.

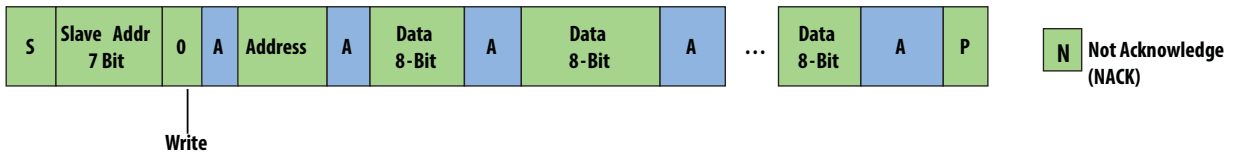
If a write access is started on an address belonging to a non-writeable register, the APDS-9253-001 returns NACK until the I²C operation is ended.

Write operations must follow this timing.

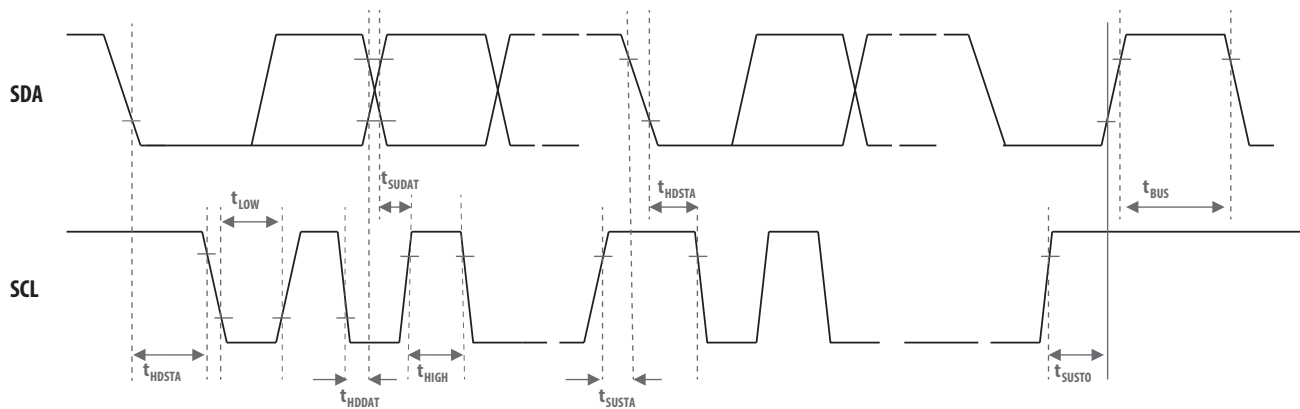
Register Write (I²C™ Write)



Register Block Write (I²C™ Write)



I²C Interface - Bus Timing



Bus Timing Characteristics

| Parameter | Symbol | Standard Mode | Fast Mode | Unit |
|--|-------------|---------------|-----------|---------|
| Maximum SCL Clock Frequency | f_{SCL} | 100 | 400 | kHz |
| Minimum START Condition Hold Time Relative to SCL Edge | t_{DSTA} | 4 | — | μs |
| Minimum SCL Clock Low Width | t_{LOW} | 4.7 | — | μs |
| Minimum SCL Clock High Width | t_{HIGH} | 4 | — | μs |
| Minimum START Condition Setup Time Relative to SCL Edge | t_{SUSTA} | 4.7 | — | μs |
| Minimum Data Hold Time on SDA Relative to SCL Edge | t_{HDDAT} | 0 | — | μs |
| Minimum Data Setup Time on SDA Relative to SCL Edge | t_{SUDAT} | 0.1 | 0.1 | μs |
| Minimum STOP Condition Setup Time on SCL | t_{SUSTO} | 4 | — | μs |
| Minimum Bus Free Time Between Stop Condition and Start Condition | t_{BUS} | 4.7 | — | μs |

Register Set

The APDS-9253-001 is controlled and monitored by data registers and a command registers accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions.

| Address | Type | Name | Description | Reset Value |
|---------|------|--|--|-------------|
| 00HEX | RW | MAIN_CTRL | Operation mode control, SW reset | 00HEX |
| 04HEX | RW | LS_MEAS_RATE | LS measurement rate and resolution | 22HEX |
| 05HEX | RW | LS_GAIN | LS analog gain range | 01HEX |
| 06HEX | R | PART_ID | Part number ID and revision ID | C2HEX |
| 07HEX | R | MAIN_STATUS | Power-on status, interrupt status, data status | 20HEX |
| 0AHEX | R | LS_DATA_IR_0 | IR ADC measurement data, LSB | 00HEX |
| 0BHEX | R | LS_DATA_IR_1 | IR ADC measurement data | 00HEX |
| 0CHEX | R | LS_DATA_IR_2 | IR ADC measurement data, MSB | 00HEX |
| 0DHEX | R | LS_DATA_GREEN_0 | ALS/Green ADC measurement data, LSB | 00HEX |
| 0EHEX | R | LS_DATA_GREEN_1 | ALS/Green ADC measurement data | 00HEX |
| 0FHEX | R | LS_DATA_GREEN_2 | ALS/Green ADC measurement data, MSB | 00HEX |
| 10HEX | R | LS_DATA_BLUE_0 | Blue ADC measurement data, LSB | 00HEX |
| 11HEX | R | LS_DATA_BLUE_1 | Blue ADC measurement data | 00HEX |
| 12HEX | R | LS_DATA_BLUE_2 | Blue ADC measurement data, MSB | 00HEX |
| 13HEX | R | LS_DATA_RED_0 | RED ADC measurement data, LSB | 00HEX |
| 14HEX | R | LS_DATA_RED_1 | RED ADC measurement data | 00HEX |
| 15HEX | R | LS_DATA_RED_2 | RED ADC measurement data, MSB | 00HEX |
| 19HEX | RW | INT_CFG | Interrupt configuration | 10HEX |
| 1AHEX | RW | INT_PST | Interrupt persist setting | 00HEX |
| 21HEX | RW | LS_THRES_UP_0 | LS Interrupt upper threshold, LSB | FFHEX |
| 22HEX | RW | LS_THRES_UP_1 | LS Interrupt upper threshold | FFHEX |
| 23HEX | RW | LS_THRES_UP_2 | LS Interrupt upper threshold, MSB | 0FHEX |
| 24HEX | RW | LS_THRES_LOW_0 | LS Interrupt lower threshold, LSB | 00HEX |
| 25HEX | RW | LS_THRES_LOW_1 | LS Interrupt lower threshold | 00HEX |
| 26HEX | RW | LS_THRES_LOW_2 | LS Interrupt lower threshold, MSB | 00HEX |
| 27HEX | RW | LS_THRES_VAR | LS Interrupt variance threshold | 00HEX |
| 29HEX | RW | DK_COUNT_STORAGE_GREEN/ALS | Dark Count Storage for GREEN/ALS | — |

MAIN_CTRL

Default Value: 00HEX

Address: Address: 00HEX

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----|----|--------|----------|----|----------|-------|----|
| 0 | 0 | SAI_LS | SW RESET | 0 | RGB_MODE | LS_EN | 0 |

| Field | Bit | Description |
|----------|-----|---|
| SAI_LS | 5 | Sleep after Interrupt for LS: When this bit is set, the light sensor returns to standby (LS_EN is cleared when the measurement is finished and the MAIN_STATUS register is read), once an interrupt occurs. This bit reacts on LS interrupt status bit in the MAIN_STATUS register. |
| SW RESET | 4 | 1: If bit is set to 1, a software reset will be triggered immediately and therefore the I ² C bus command is NOT answered with ACK. |
| RGB_MODE | 2 | 0: ALS and IR channels activated (default). 1: All Light Sensor (RGB and IR) channels activated. |
| LS_EN | 1 | 0: Ambient light sensor standby (default). 1: Light Sensor active. |

LS_MEAS_RATE

Default Value: 22HEX

Address: 04HEX

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----|---------------|----|----|----|---------------------|----|----|
| 0 | LS RESOLUTION | | | 0 | LS MEASUREMENT RATE | | |

| Field | Bit | Description |
|---------------------|-----|---|
| LS RESOLUTION | 6:4 | 000: 20 bit – 400 ms 001: 19 bit – 200 ms 010: 18 bit – 100 ms (default) 011: 17 bit – 50 ms 100: 16 bit – 25 ms 101: 13 bit – 3.125 ms 110: Reserved 111: Reserved |
| LS MEASUREMENT RATE | 2:0 | 000: 25 ms 001: 50 ms 010: 100 ms (default) 011: 200 ms 100: 500 ms 101: 1000 ms 110: 2000 ms 111: 2000 ms |

Bit 2:0 register controls the timing of the periodic measurements of the LS in active mode.

When the measurement repeat rate is programmed to be faster than possible for the programmed ADC measurement time, the repeat rate will be lower than programmed (maximum speed).

Writing to this register resets LS state machine and starts new measurements.

LS_GAIN

Default Value: 01HEX

Address: 05HEX

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----|----|----|----|----|---------------|----|----|
| 0 | 0 | 0 | 0 | 0 | LS GAIN RANGE | | |

| Field | Bit | Description |
|---------------|-----|--|
| LS GAIN RANGE | 2:0 | 000: Gain 1. 001: Gain 3 (default). 010: Gain 6. 011: Gain 9. 100: Gain 18. |

Writing to this register resets LS state machine and starts new measurements.

PART_ID

Default Value: C2HEX

Address: 06HEX

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------|----|----|----|-------------|----|----|----|
| PART ID | | | | REVISION ID | | | |

| Field | Bit | Description |
|-------------|-----|-------------------------------|
| PART ID | 7:4 | Part number ID. |
| REVISION ID | 3:0 | Revision ID of the component. |

MAIN_STATUS

Default Value: 20HEX

Address: 07HEX

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----|----|-----------------|---------------------|----------------|----|----|----|
| 0 | 0 | POWER ON STATUS | LS INTERRUPT STATUS | LS DATA STATUS | 0 | 0 | 0 |

| Field | Bit | Description |
|---------------------|-----|--|
| POWER ON STATUS | 5 | 1: Part went through a power-up event, either because the part was turned on or because there was power supply disturbance. (default at first register read). All interrupt threshold settings in the registers have been reset to power-on default states and should be examined if necessary. The flag is cleared after the register is read. |
| LS INTERRUPT STATUS | 4 | 0: Interrupt condition not fulfilled (default). 1: Interrupt condition fulfilled (cleared after read). |
| LS DATA STATUS | 3 | 0: Old data, already read (default). 1: New data, not yet read (cleared after read). |

LS_DATA_IR

Default Value: 00HEX, 00HEX, 00HEX

Address: 0AHEX, 0BHEX, 0CHEX

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--------------|----|----|----|--------------|----|----|----|
| LS_DATA_IR_0 | | | | | | | |
| LS_DATA_IR_1 | | | | | | | |
| 0 | 0 | 0 | 0 | LS_DATA_IR_2 | | | |

IR channel output data (unsigned integer, 13 to 20 bit, LSB aligned).

When an I²C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I²C read operation is completed or this address range is left.

This ensures that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual LS_DATA registers are updated as soon as there is no ongoing I²C read operation to the address range 07HEX to 18HEX.

| | | |
|-----------|-----------|--|
| Reg 0AHEX | Bit [7:0] | IR diode data least significant data byte. |
| Reg 0BHEX | Bit [7:0] | IR diode data intervening data byte. |
| Reg 0CHEX | Bit [3:0] | IR diode data most significant data byte. |

LS_DATA_GREEN

Default Value: 00HEX, 00HEX, 00HEX

Address: 0DHEX, 0EHEX, 0FHEX

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----------------|----|----|----|-----------------|----|----|----|
| LS_DATA_GREEN_0 | | | | | | | |
| LS_DATA_GREEN_1 | | | | | | | |
| 0 | 0 | 0 | 0 | LS_DATA_GREEN_2 | | | |

ALS/Green channel digital output data (unsigned integer, 13 to 20 bit, LSB aligned).

When an I²C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I²C read operation is completed or this address range is left.

This ensures that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual LS_DATA registers are updated as soon as there is no on-going I²C read operation to the address range 07HEX to 18HEX.

| | | |
|-----------|-----------|---|
| Reg 0DHEX | Bit [7:0] | ALS/Green diode data least significant data byte. |
| Reg 0EHEX | Bit [7:0] | ALS/Green diode data intervening data byte. |
| Reg 0FHEX | Bit [3:0] | ALS/Green diode data most significant data byte. |

LS_DATA_BLUE

Default Value: 00HEX, 00HEX, 00HEX

Address: 10HEX, 11HEX, 12HEX

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----------------|----|----|----|----------------|----|----|----|
| LS_DATA_BLUE_0 | | | | | | | |
| LS_DATA_BLUE_1 | | | | | | | |
| 0 | 0 | 0 | 0 | LS_DATA_BLUE_2 | | | |

Blue channel digital output data (unsigned integer, 13 to 20 bit, LSB aligned).

When an I²C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I²C read operation is completed or this address range is left.

This ensures that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual LS_DATA registers are updated as soon as there is no on-going I²C read operation to the address range 07HEX to 18HEX.

| | | |
|-----------|-----------|--|
| Reg 10HEX | Bit [7:0] | Blue diode data least significant data byte. |
| Reg 11HEX | Bit [7:0] | Blue diode data intervening data byte. |
| Reg 12HEX | Bit [3:0] | Blue diode data most significant data byte. |

LS_DATA_RED

Default Value: 00HEX, 00HEX, 00HEX

Address: 13HEX, 14HEX, 15HEX

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------------|----|----|----|---------------|----|----|----|
| LS_DATA_RED_0 | | | | | | | |
| LS_DATA_RED_1 | | | | | | | |
| 0 | 0 | 0 | 0 | LS_DATA_RED_2 | | | |

Red channel digital output data (unsigned integer, 13 to 20 bit, LSB aligned).

When an I²C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I²C read operation is completed or this address range is left.

This ensures that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual LS_DATA registers are updated as soon as there is no on-going I²C read operation to the address range 07HEX to 18HEX.

| | | |
|-----------|-----------|---|
| Reg 13HEX | Bit [7:0] | Red diode data least significant data byte. |
| Reg 14HEX | Bit [7:0] | Red diode data intervening data byte. |
| Reg 15HEX | Bit [3:0] | Red diode data most significant data byte. |

INT_CFG

Default Value: 10HEX

Address: 19HEX

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----|----|------------|-------------|-----------|----|----|----|
| 0 | 0 | LS_INT_SEL | LS_VAR_MODE | LS_INT_EN | 0 | 0 | |

| Field | Bit | Description |
|-------------|-----|---|
| LS_INT_SEL | 5:4 | 00: IR channel. 01: ALS channel/Green channel (default). 10: Red channel. 11: Blue channel. |
| LS_VAR_MODE | 3 | 0: LS threshold interrupt mode (default). 1: LS variation interrupt mode. |
| LS_INT_EN | 2 | 0: LS Interrupt disabled (default). 1: LS Interrupt enabled. |

INT_PST

Default Value: 00HEX

Address: 1AHEX

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----|------------|----|----|----|----|----|----|
| 0 | LS_PERSIST | | | 0 | | | |

| Field | Bit | Description |
|------------|-----|--|
| LS_PERSIST | 6:4 | 0000: Every LS value out of threshold range (default) asserts an interrupt. 0001: 2 consecutive LS values out of threshold range assert an interrupt. ... 1111: 16 consecutive LS values out of threshold range assert an interrupt. |

These register sets the number of similar consecutive LS interrupt events that must occur before the interrupt is asserted.

LS_THRES_UP

Default Value: FFHEX, FFHEX, 0FHEX

Address: 21HEX, 22HEX, 23HEX

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------------|----|----|----|---------------|----|----|----|
| LS_THRES_UP_0 | | | | | | | |
| LS_THRES_UP_1 | | | | | | | |
| 0 | 0 | 0 | 0 | LS_THRES_UP_2 | | | |

LS_THRES_UP sets the upper threshold value for the LS interrupt. The interrupt controller compares the value in LS_THRES_UP against measured data in the LS_DATA registers of the selected LS interrupt channel. It generates an interrupt event if DATA exceeds the threshold level.

The data format for LS_THRES_UP must match that of the LS_DATA registers.

Writing to these registers resets the LS state machine and starts new measurements.

| | | |
|-----------|-----------|---|
| Reg 21HEX | Bit [7:0] | LS upper interrupt threshold value, LSB. |
| Reg 22HEX | Bit [7:0] | LS upper interrupt threshold value, intervening byte. |
| Reg 23HEX | Bit [3:0] | LS upper interrupt threshold value, MSB. |

LS_THRES_LOW

Default Value: 00HEX, 00HEX, 00HEX

Address: 24HEX, 25HEX, 26HEX

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----------------|----|----|----|----------------|----|----|----|
| LS_THRES_LOW_0 | | | | | | | |
| LS_THRES_LOW_1 | | | | | | | |
| 0 | 0 | 0 | 0 | LS_THRES_LOW_2 | | | |

LS_THRES_LOW sets the lower threshold value for the LS interrupt. The interrupt controller compares the value in LS_THRES_LOW against measured data in the LS_DATA registers of the selected LS interrupt channel. It generates an interrupt event if DATA is below the threshold level.

The data format for LS_THRES_LOW must match that of the LS_DATA registers.

Writing to these registers resets the LS state machine and starts new measurements.

| | | |
|-----------|-----------|---|
| Reg 24HEX | Bit [7:0] | LS lower interrupt threshold value, LSB. |
| Reg 25HEX | Bit [7:0] | LS lower interrupt threshold value, intervening byte. |
| Reg 26HEX | Bit [3:0] | LS lower interrupt threshold value, MSB. |

LS_THRES_VAR

Default Value: 00HEX

Address: 27HEX

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----|----|----|----|----|--------------|----|----|
| 0 | 0 | 0 | 0 | 0 | LS_THRES_VAR | | |

| Field | Bit | Description |
|--------------|-----|--|
| LS_THRES_VAR | 2:0 | 000: LS result varies by 8 counts compared to previous result (default). 001: LS result varies by 16 counts compared to previous result. 010: LS result varies by 32 counts compared to previous result. 011: LS result varies by 64 counts compared to previous result. ... 111: LS result varies by 1024 counts compared to previous result. |

DK_COUNT_STORAGE_GREEN/ALS

Default Value: —

Address: 29HEX

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----|----|----|----|------------|------------------|----|----|
| 0 | 0 | 0 | 0 | DARK_VALID | DARK_COUNT_GREEN | | |

| Field | Bit | Description |
|------------------|-----|--|
| DARK_VALID | 3 | 0: DARK_COUNT_GREEN is not valid. 1: DARK_COUNT_GREEN is valid. |
| DARK_COUNT_GREEN | 2:0 | Dark count of green channel is tested at 400 ms and 18x gain. |

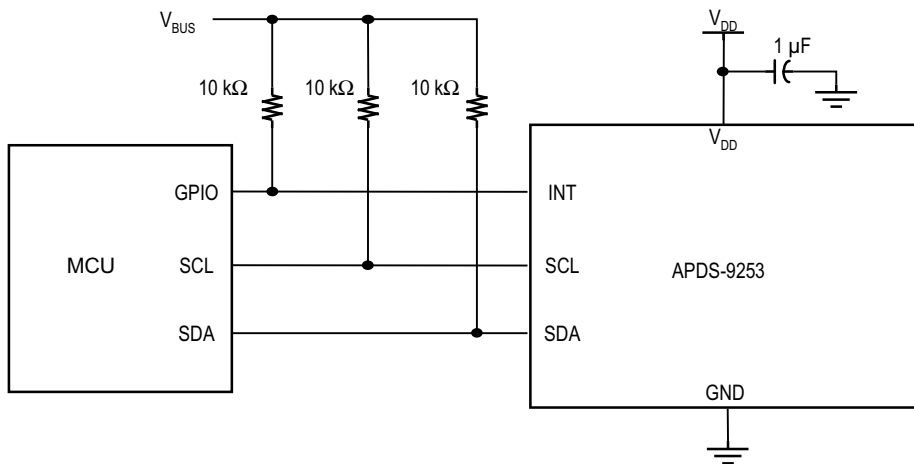
Application Information: Hardware

The application hardware circuit for implementing APDS-9253-001 is shown in following figure. The bypass capacitor is placed as close to the device package as possible and is connected directly to the power source and to the ground, as shown in the following figure. It allows the AC component of the V_{DD} to pass through to ground. It is suggested that you use a bypass capacitor that has a low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents caused by internal logic switching.

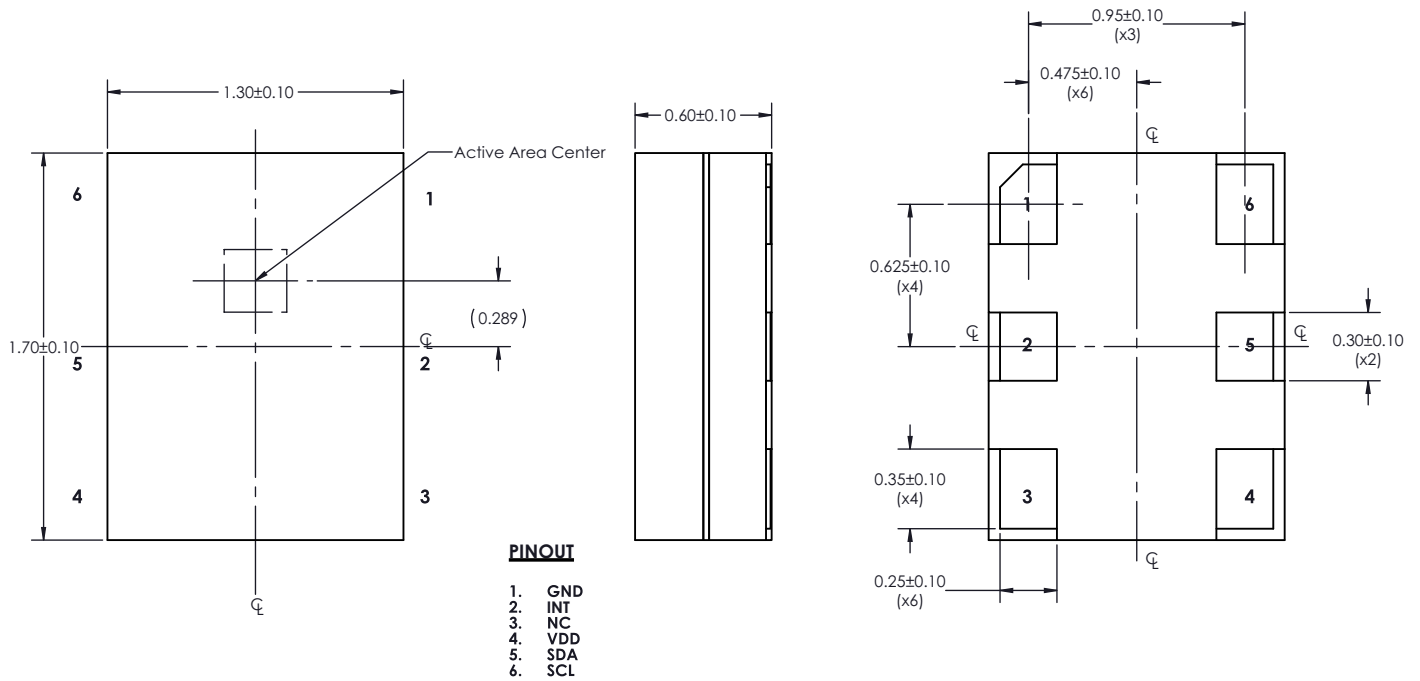
Pull-up resistors, RSDA and RSCL, maintain the SDA and SCL lines at a high level when the bus is free and ensure the signals are pulled up from a low to a high level within the required rise time. A pull-up resistor, RINT, is also required for the interrupt (INT), which functions as a wired-AND signal, similar to the SCL and SDA lines. A typical impedance value of 10 k Ω can be used.

For a complete description of I²C maximum and minimum R1 and R2 values, review the I²C Specification at <http://www.semiconductors.philips.com>.

Figure 8: Application Hardware Circuit

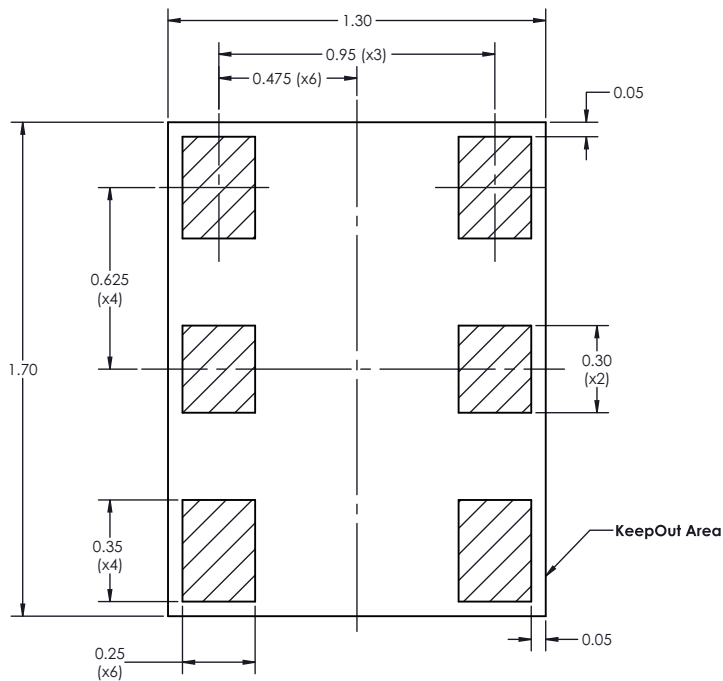


Package Outline Dimensions



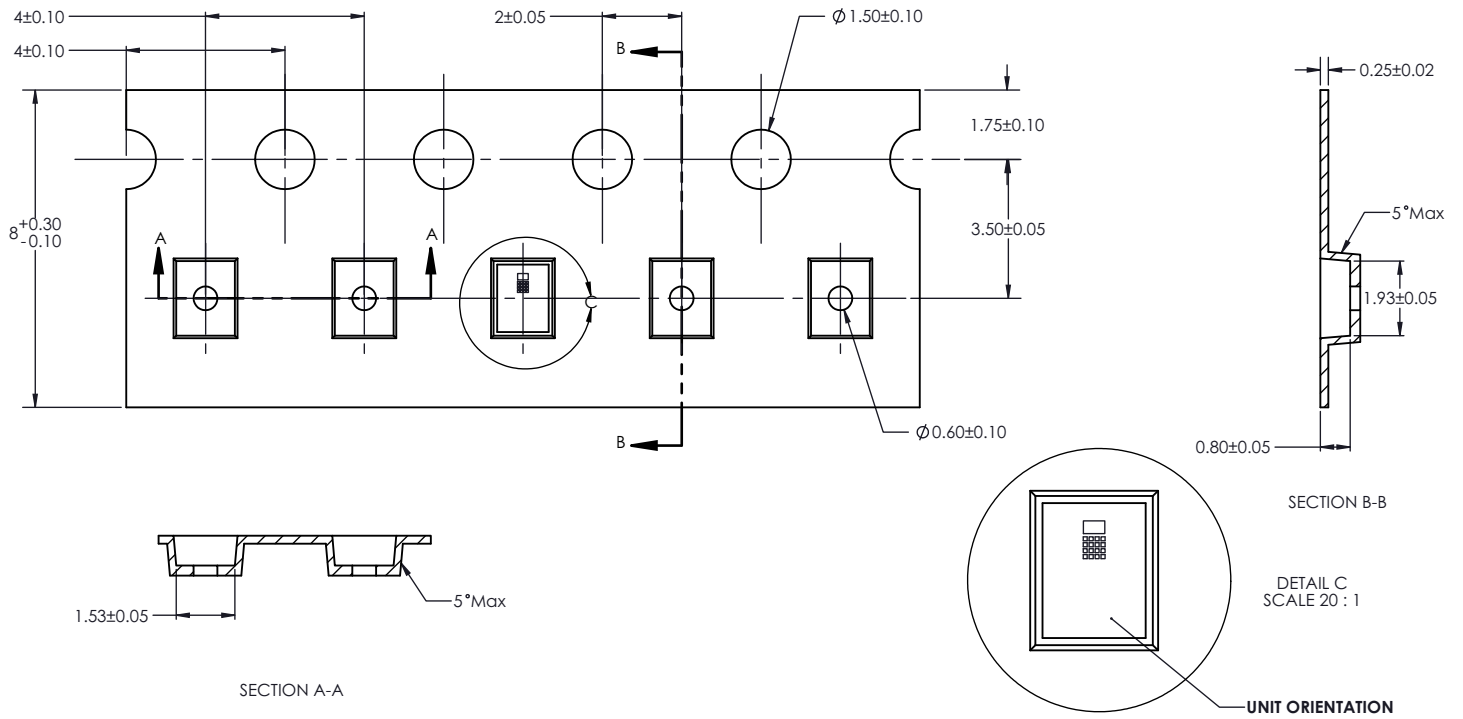
NOTE: All dimensions are in mm.

PCB Pad Layout



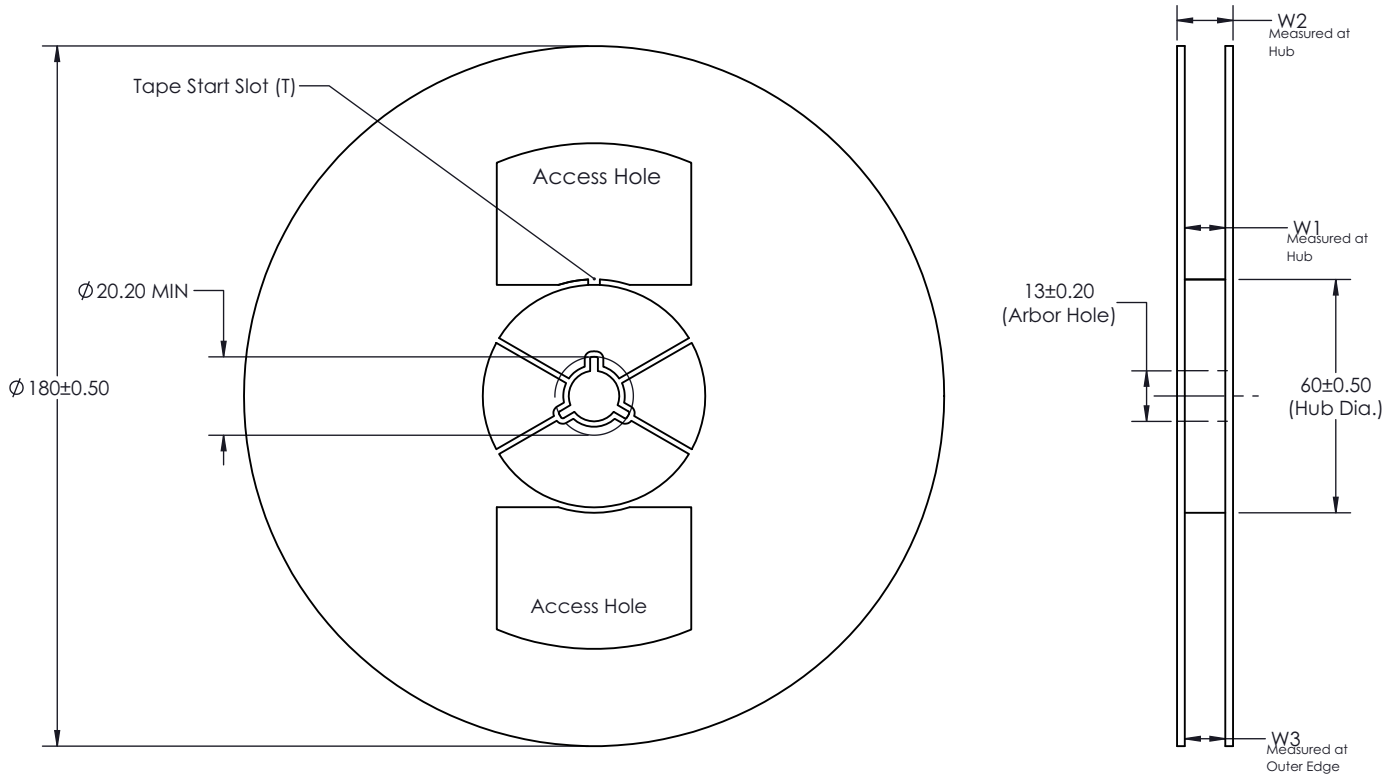
NOTE: All dimensions are in mm.

Tape Dimensions



NOTE: All dimensions are in mm.

Reel Dimensions

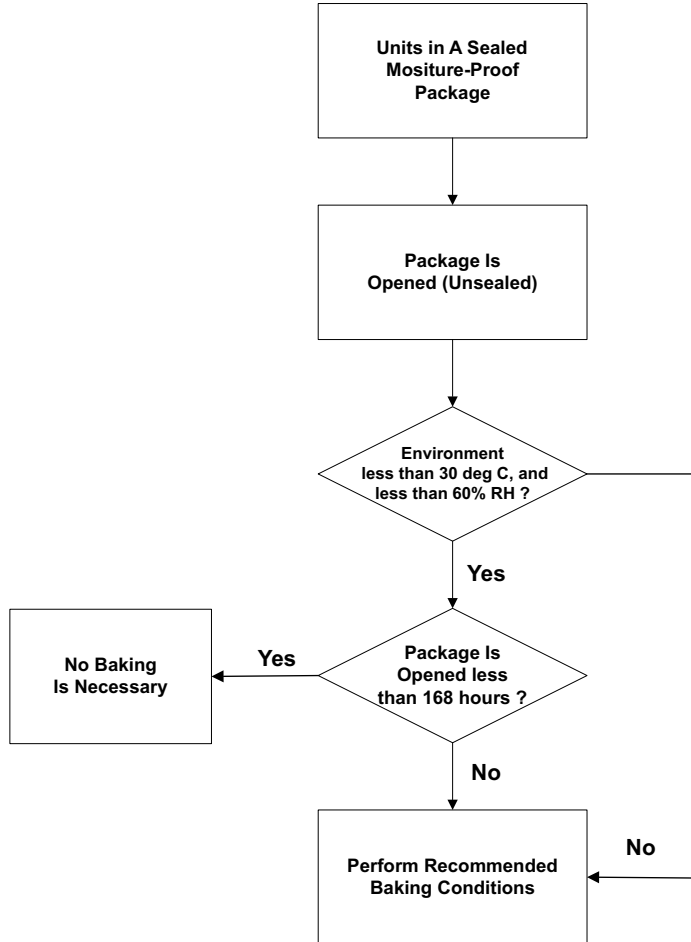


| Tape Width | T | W1 | W2 | W3 |
|------------|---------|--------------------|-----------|-----------------------|
| 8 mm | 3 ± 0.5 | 8.4 + 1.5 - 0.0 | 14.4 Max. | 7.9 Min. 10.9 Max. |

NOTE: All dimensions are in mm.

Moisture Proof Packaging

All APDS-9253-001 options are shipped in moisture proof package. Once opened, moisture absorption begins. This part is compliant to JEDEC MSL 3.



Baking Conditions

| Package | Temperature | Time |
|---------|-------------|----------|
| In Reel | 60°C | 48 hours |
| In Bulk | 100°C | 4 hours |

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Baking should only be done once.

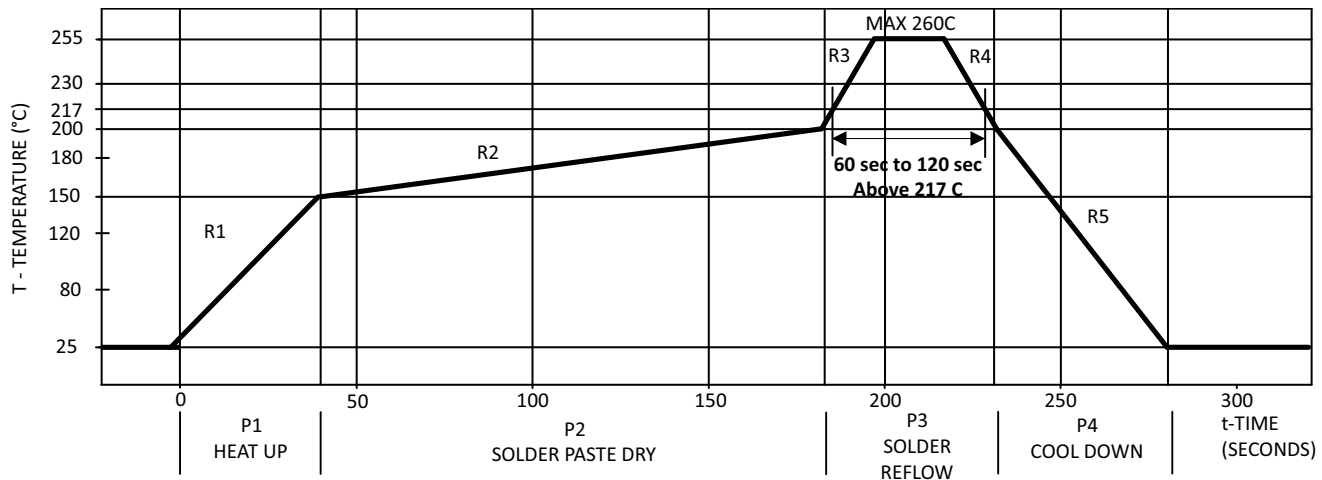
Recommended Storage Conditions

| | |
|---------------------|--------------|
| Storage Temperature | 10°C to 30°C |
| Relative Humidity | below 60% RH |

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within 168 hours if stored at the recommended storage conditions. If times longer than 168 hours are needed, the parts must be stored in a dry box.

Recommended Reflow Profile



| Process Zone | Symbol | ΔT | Maximum $\Delta T/\Delta$ time or Duration |
|---|--------|----------------|--|
| Heat Up | P1, R1 | 25°C to 150°C | 3°C/s |
| Solder Paste Dry | P2, R2 | 150°C to 200°C | 100s to 180s |
| Solder Reflow | P3, R3 | 200°C to 260°C | 3°C/s |
| | P3, R4 | 260°C to 200°C | -6°C/s |
| Cool Down | P4, R5 | 200°C to 25°C | -6°C/s |
| Time Maintained above Liquidus Point, 217°C | | >217°C | 60s to 120s |
| Peak Temperature | | 260°C | — |
| Time within 5°C of Actual Peak Temperature | | >255°C | 20s to 40s |
| Time 25°C to Peak Temperature | | 25°C to 260°C | 8 mins |

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different $\Delta T/\Delta$ time temperature change rates or duration. The $\Delta T/\Delta$ time rates or duration are detailed in the previous table. The temperatures are measured at the component to printed circuit board connections.

In **process zone P1**, the PC board and component pins are heated to a temperature of 150°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the PC board and component pins.

Process zone P2 should be of sufficient time duration (100s to 180s) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder.

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 260°C (500°F) for optimum results. The dwell time above the liquidus point of solder should be between 60s and 120s. This is to ensure proper coalescing of the solder paste into liquid solder and the formation of good solder connections. Beyond the recommended dwell time, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and component pins to change dimensions evenly, putting minimal stresses on the component.

It is recommended to perform reflow soldering no more than twice.

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