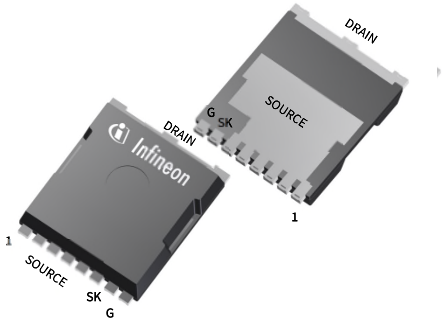
IGT60R190D1S

600V CoolGaN™ enhancement-mode Power Transistor

Features

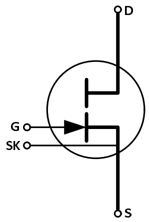
- Enhancement mode transistor – Normally OFF switch
- Ultra fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate charge, low output charge
- Superior commutation ruggedness
- Qualified for standard grade applications according to JEDEC



Standards Benefits

- Improves system efficiency
- Improves power density
- Enables higher operating frequency
- System cost reduction savings
- Reduces EMI

Gate	8
Drain	drain contact
Kelvin Source	7
Source	1,2,3,4,5,6



Applications

Consumer SMPS and high density chargers based on the half-bridge topology (half-bridge topologies for hard and soft switching such as Totem pole PFC, high frequency LLC and flyback).
For other applications: review CoolGaN™ reliability white paper and contact Infineon regional support

Table 1 Key Performance Parameters at $T_J = 25$ °C

Parameter	Value	Unit
$V_{DS,max}$	600	V
$R_{DS(on),max}$	190	mΩ
$Q_{G,typ}$	3.2	nC
$I_{D,pulse}$	23	A
Q_{oss} @ 400 V	16	nC
Q_{rr}	0	nC

Table 2 Ordering Information

Type / Ordering Code	Package	Marking	Related links
IGT60R190D1S	PG-HSOF-8-3	60S190D1	see Appendix A

Table of Contents

1 Maximum ratings

at $T_j = 25$ °C, unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact your local Infineon sales office.

Table 3 Maximum ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain Source Voltage [1]	$V_{DS,max}$	-	-	600	V	$V_{GS} = 0$ V
Continuous current, drain source	I_D	- - -	- - -	12.5 8.0 5.5	A	$T_C = 25$ °C; $T_j = T_{j,\,max}$ $T_C = 100$ °C; $T_j = T_{j,\,max}$ $T_C = 125$ °C; $T_j = T_{j,\,max}$
Pulsed current, drain source [2,3]	$I_{D,pulse}$	-	-	23	A	$T_C = 25$ °C; $I_G = 9.6$ mA; See Figure 3; Figure 5;
Pulsed current, drain source [3,4]	$I_{D,pulse}$	-	-	13.5	A	$T_C = 125$ °C; $I_G = 9.6$ mA; See Figure 4; Figure 6;
Gate current, continuous [3,4,5]	$I_{G,avg}$	-	-	7.7	mA	$T_j = -55$ °C to 150 °C;
Gate current, pulsed [3,5]	$I_{G,pulse}$	-	-	770	mA	$T_j = -55$ °C to 150 °C; $t_{PULSE} = 50$ ns, f=100 kHz
Gate source voltage, continuous [5]	V_{GS}	-10	-	-	V	$T_j = -55$ °C to 150 °C;
Gate source voltage, pulsed [5]	$V_{GS,pulse}$	-25	-	-	V	$T_j = -55$ °C to 150 °C; $t_{PULSE} = 50$ ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	-	-	55.5	W	$T_C = 25$ °C
Operating temperature	T_j	-55	-	150	°C	
Storage temperature	T_{stg}	-55	-	150	°C	Max shelf life depends on storage conditions.
Drain-source voltage slew-rate	dV/dt			200	V/ns	

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[1] All devices are 100% tested at $I_{DS} = 4.3$ mA to assure $V_{DS} \geq 800$ V

[2] Limits derived from product characterization, parameter not measured during production

[3] Ensure that average gate drive current, $I_{G,avg}$ is ≤ 7.7 mA. Please see figure 27 for $I_{G,avg}$, $I_{G,pulse}$ and I_G details

[4] Parameter is influenced by rel-requirements. Please contact the local Infineon Sales Office to get an assessment of your application.

[5] We recommend using an advanced driving technique to optimize the device performance. Please see gate drive application note for details.

2 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-	2.25	°C/W	
Thermal resistance, junction-ambient	R_{thJA}	-	-	62	°C/W	Device on PCB, minimum footprint
Thermal resistance, junction-ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm* 1.5mm epoxy PCB FR4 with 6cm^2 (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Reflow soldering temperature	T_{sold}	-	-	245	°C	MSL3

3 Electrical characteristics

at $T_j = 25$ °C, unless specified otherwise

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9 0.7	1.2 1.0	1.6 1.4	V	$I_{DS} = 0.96$ mA; $V_{DS} = 10$ V; $T_j = 25$ °C $I_{DS} = 0.96$ mA; $V_{DS} = 10$ V; $T_j = 125$ °C
Drain-Source leakage current	I_{DSS}	- -	0.4 8	40 -	µA	$V_{DS} = 600$ V; $V_{GS} = 0$ V; $T_j = 25$ °C $V_{DS} = 600$ V; $V_{GS} = 0$ V; $T_j = 150$ °C
Drain-Source leakage current at application conditions[1]	I_{DSSapp}	-	0.3	-	µA	$V_{DS} = 400$ V; $V_{GS} = 0$ V; $T_j = 125$ °C
Gate-Source leakage current	I_{GSS}	-1 -1	- -	- -	mA	$V_{DS} = 0$ V; $V_{GS} = -10$ V; $T_j = 25$ °C $V_{DS} = 0$ V; $V_{GS} = -10$ V; $T_j = 125$ °C
Drain-Source on-state resistance	$R_{DS(on)}$	- -	0.14 0.26	0.19 -	Ω	$I_G = 9.6$ mA; $I_D = 5$ A; $T_j = 25$ °C $I_G = 9.6$ mA; $I_D = 5$ A; $T_j = 150$ °C
Gate resistance	$R_{G,int}$	-	0.27	-	Ω	LCR impedance measurement; $f = f_{res}$

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	157	-	pF	$V_{GS} = 0$ V; $V_{DS} = 400$ V; $f = 1$ MHz
Output capacitance	C_{oss}	-	28	-	pF	$V_{GS} = 0$ V; $V_{DS} = 400$ V; $f = 1$ MHz
Reverse Transfer capacitance	C_{rss}	-	0.15	-	pF	$V_{GS} = 0$ V; $V_{DS} = 400$ V; $f = 1$ MHz
Effective output capacitance, energy related [2]	$C_{o(er)}$	-	32.5	-	pF	$V_{DS} = 0$ to 400 V
Effective output capacitance, time related [3]	$C_{o(tr)}$	-	40	-	pF	$V_{GS} = 0$ V; $V_{DS} = 0$ to 400 V; Id = const
Output charge	Q_{oss}	-	16	-	nC	$V_{DS} = 0$ to 400 V
Turn- on delay time	$t_{d(on)}$	-	11	-	ns	see Figure 23
Turn- off delay time	$t_{d(off)}$	-	12	-	ns	see Figure 23
Rise time	t_r	-	5	-	ns	see Figure 23
Fall time	t_f	-	12	-	ns	see Figure 23

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[1] Parameter represents end of use leakage in applications

[2] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as Coss while VDS is rising from 0 to 400 V

[3] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as Coss while VDS is rising from 0 to 400 V

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	3.2	-	nC	I_{GS} = 0 to 3.8 mA; V_{DS}= 400 V; I_D= 5 A

Table 8 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.5	3	V	V_{GS} = 0V; I_{SD} = 5 A
Pulsed current, reverse	$I_{S,pulse}$	-	-	23	A	I_G = 9.6 mA
Reverse recovery charge	Q_{rr}[1]	-	0	-	nC	I_{SD} = 5 A, V_{DS} = 400V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

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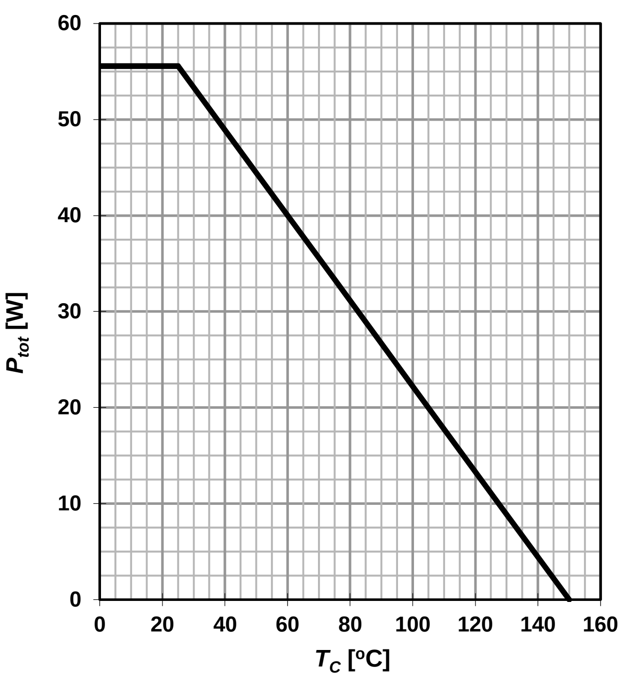
[1] Excluding Qoss

4 Electrical characteristics diagrams

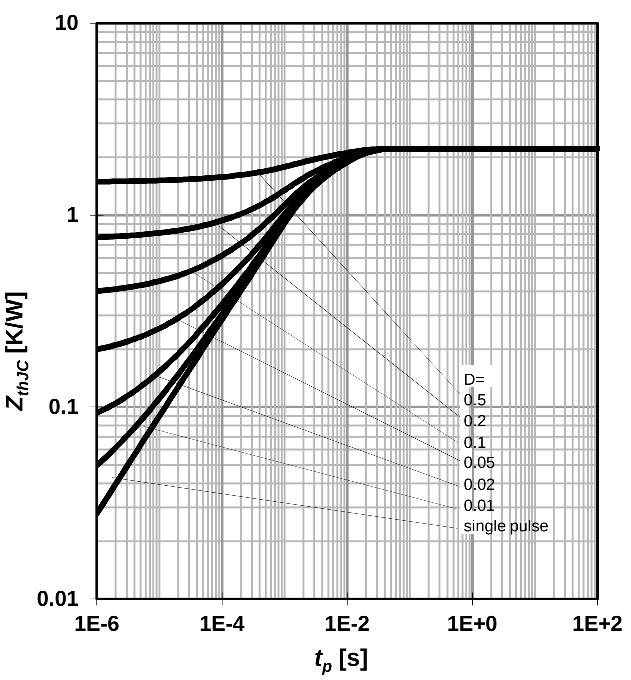
at T_j = 25 °C, unless specified otherwise

Figure 1 Power dissipation



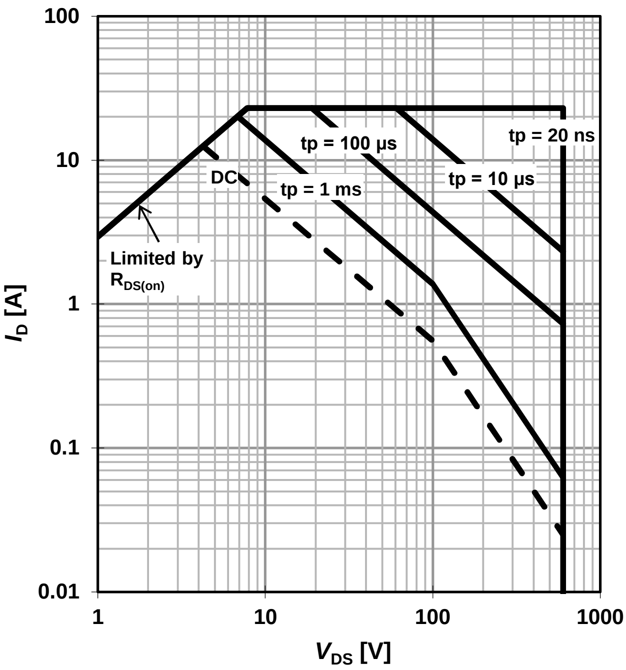
$P_{tot}=f(T_c)$

Figure 2 Max. transient thermal impedance



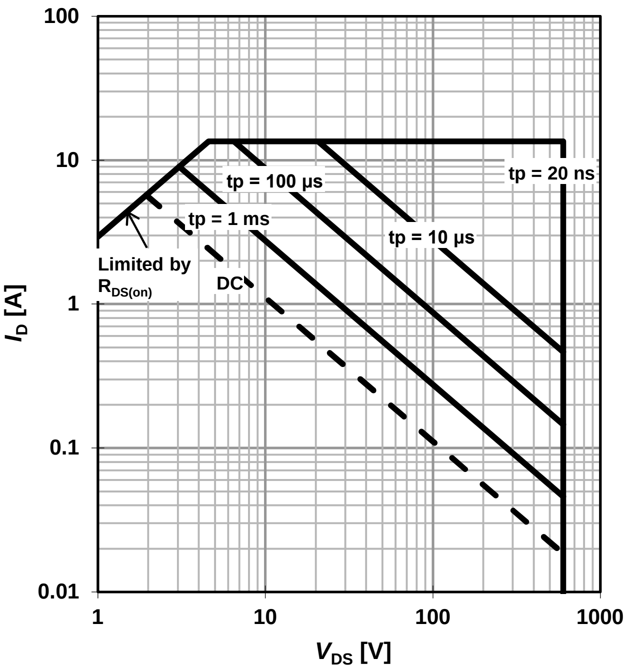
$Z_{thJC}=f(t_p, D)$

Figure 3 Safe operating area



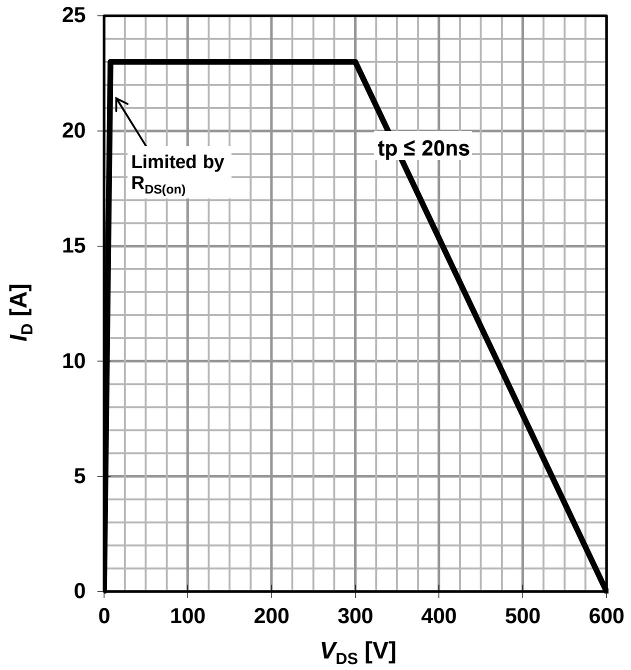
$I_D=f(V_{DS})$; T_C = 25 °C

Figure 4 Safe operating area



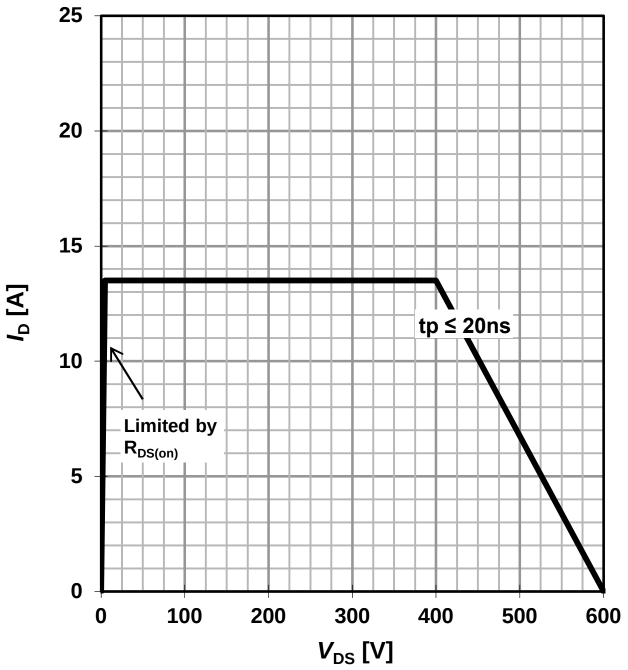
$I_D=f(V_{DS})$; T_C = 125 °C

Figure 5 Repetitive safe operating area[1]



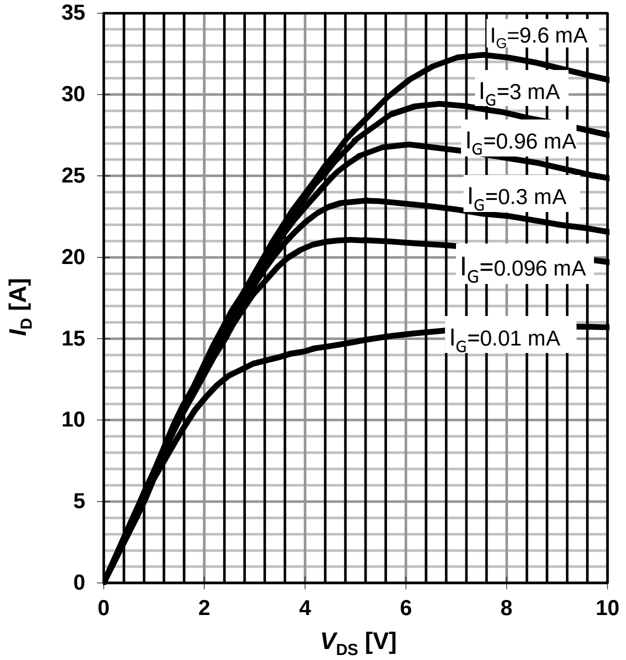
Tc = 25 °C; $T_j \leq 150$ °C

Figure 6 Repetitive safe operating area[1]



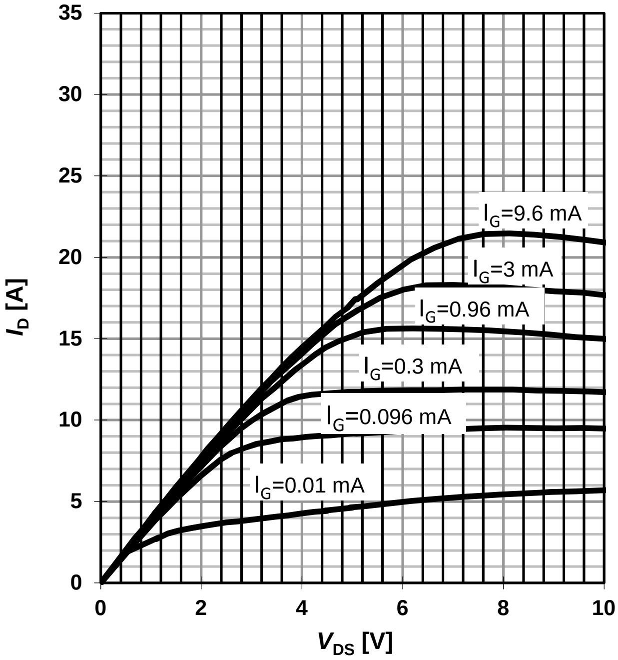
Tc = 125 °C; $T_j \leq 150$ °C

Figure 7 Typ. output characteristics



$I_D=f(V_{DS},I_{GS})$; T_J = 25 °C

Figure 8 Typ. output characteristics



$I_D=f(V_{DS},I_{GS})$; T_J = 125 °C

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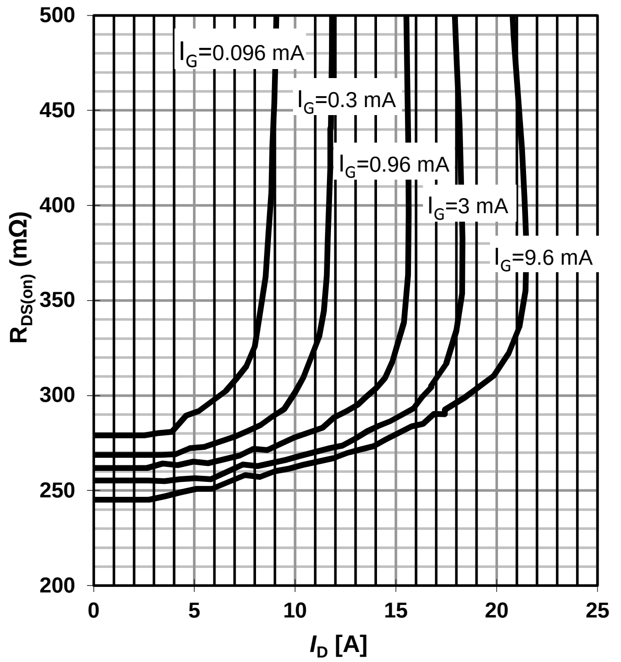
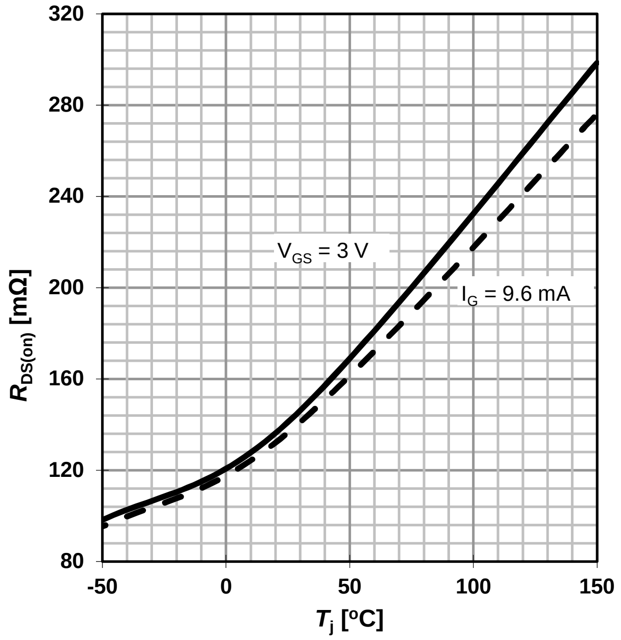
[1] Parameter is influenced by rel-requirements. This value is determined by a typical lifetime-model for consumer applications. Please contact the local Infineon Sales Office to get an assessment of your application.

Figure 9 Typ. Drain-source on-state resistance



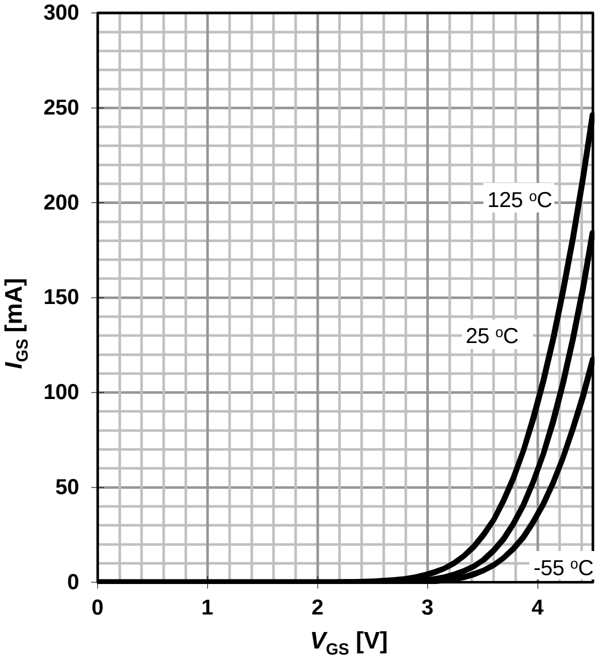
$R_{DS(on)}=f(I_D,I_G)$; T_j = 125 °C

Figure 10 Drain-source on-state resistance



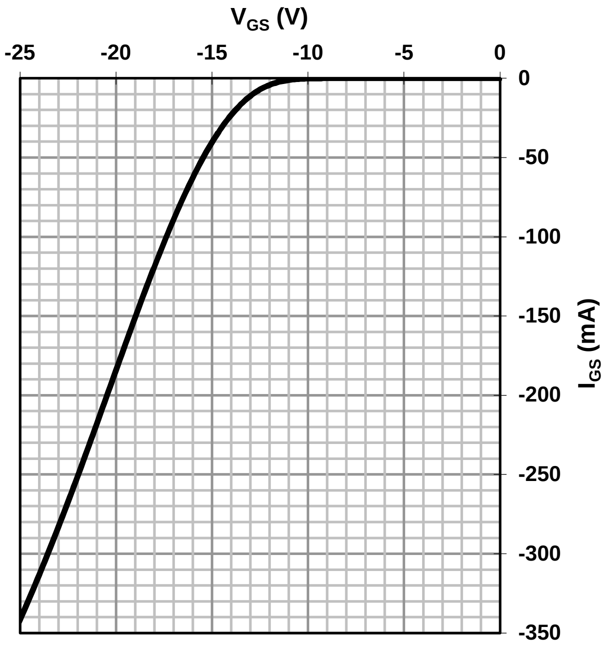
$R_{DS(on)}=f(T_j)$; I_D = 5 A

Figure 11 Typ. gate characteristics forward



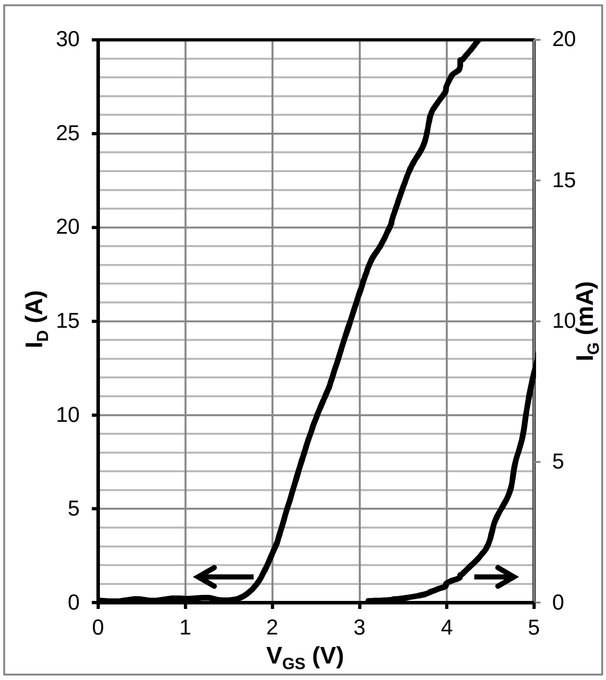
$I_{GS}=f(V_{GS},T_j)$; open drain

Figure 12 Typ. gate characteristics reverse



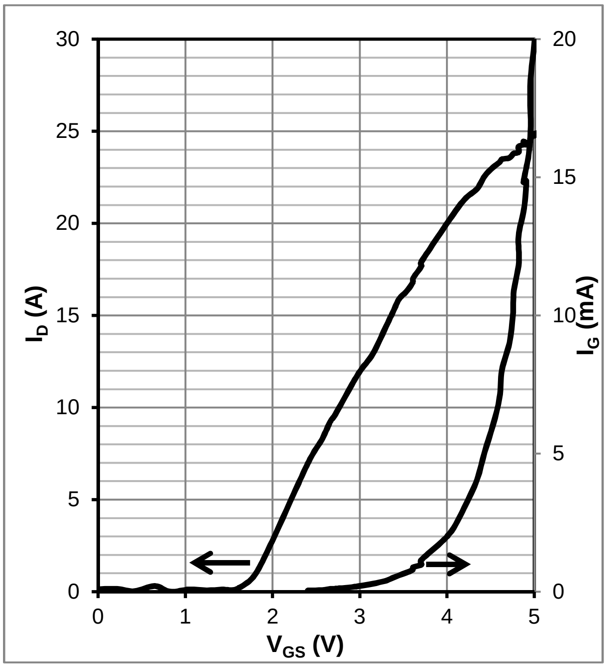
$I_{GS}=f(V_{GS})$; T_j = 25 °C

Figure 13 Typ. transfer characteristics



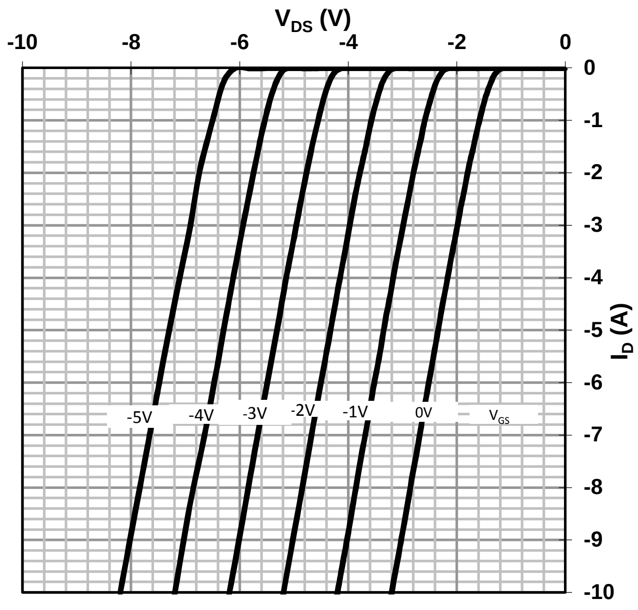
I_D, I_G =f(V_{GS}); V_{DS} = 8 V; T_j = 25 °C

Figure 14 Typ. transfer characteristics



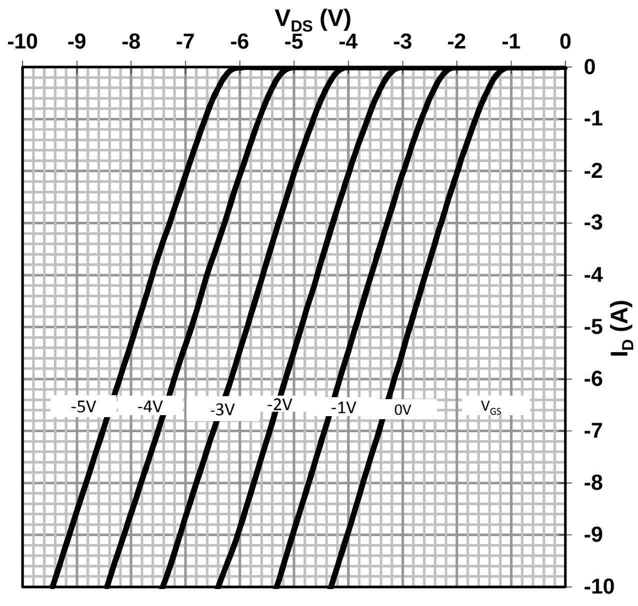
I_D, I_G =f(V_{GS}); V_{DS} = 8 V ; T_j = 125 °C

Figure 15 Typ. channel reverse characteristics



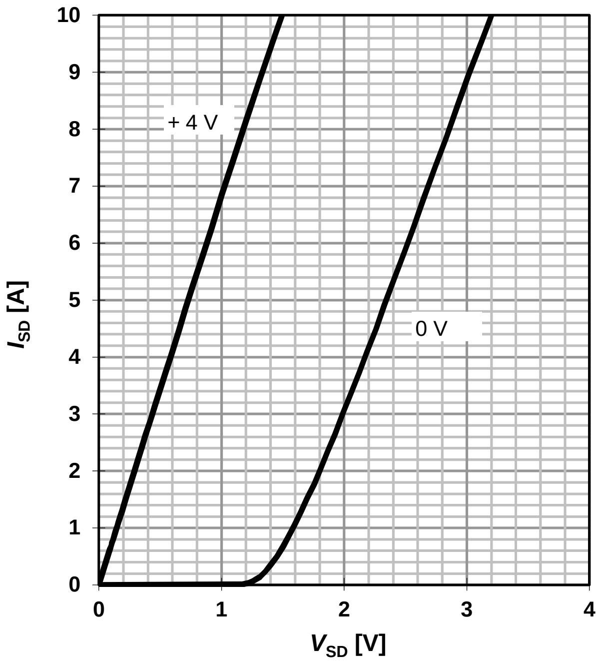
V_{DS}=f(I_D, V_{GS}); T_j = 25 °C

Figure 16 Typ. channel reverse characteristics



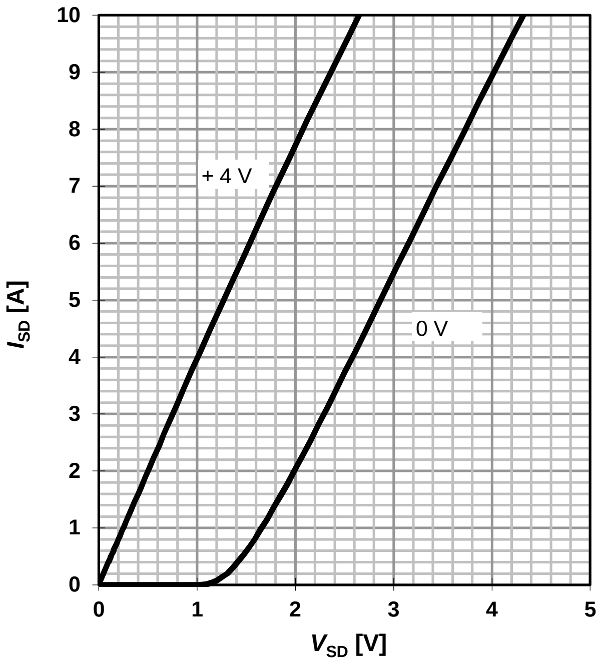
V_{DS}=f(I_D, V_{GS}); T_j = 125 °C

Figure 17 Typ. channel reverse characteristics



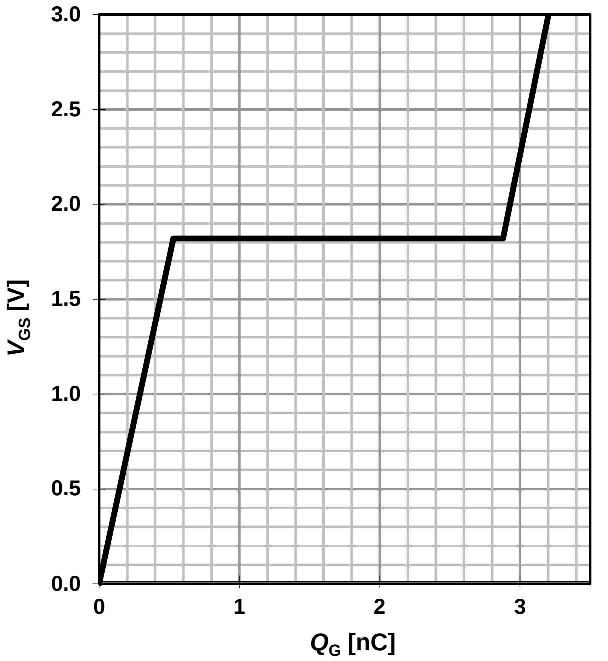
$I_D=f(V_{DS}, V_{GS})$; $T_j = 25$ °C

Figure 18 Typ. channel reverse characteristics



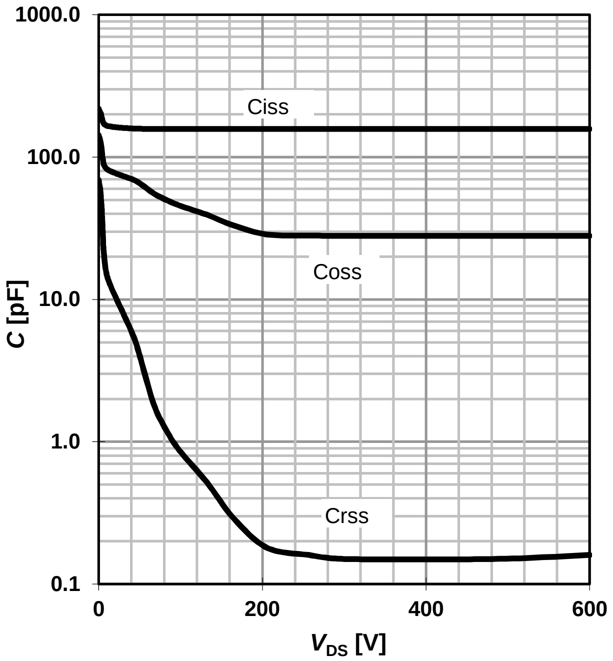
$I_D=f(V_{DS}, V_{GS})$; $T_j = 125$ °C

Figure 19 Typ. gate charge



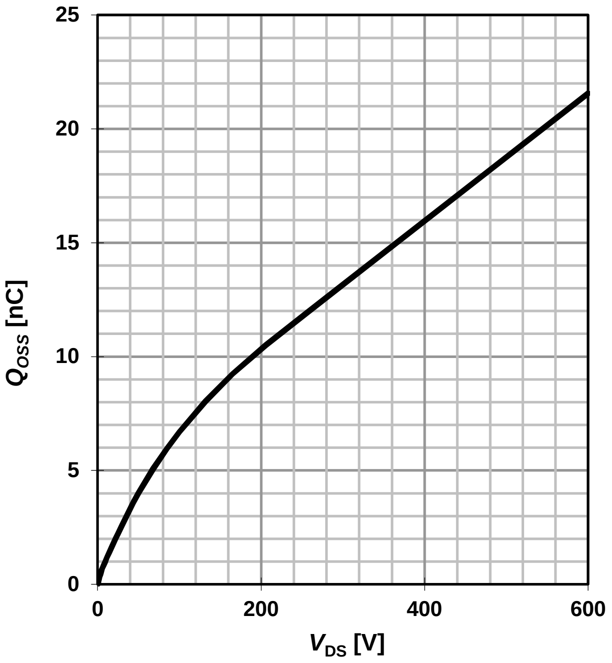
$V_{GS} = f(Q_G)$; $V_{DCLINK} = 400$ V; $I_D = 5$ A

Figure 20 Typ. capacitances



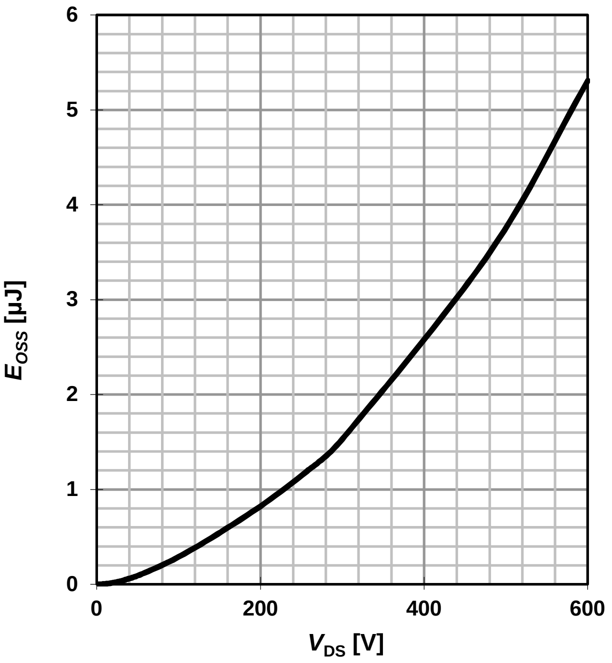
$C_{xss} = f(V_{DS})$

Figure 21 Typ. output charge



$Q_{OSS} = f(V_{DS})$

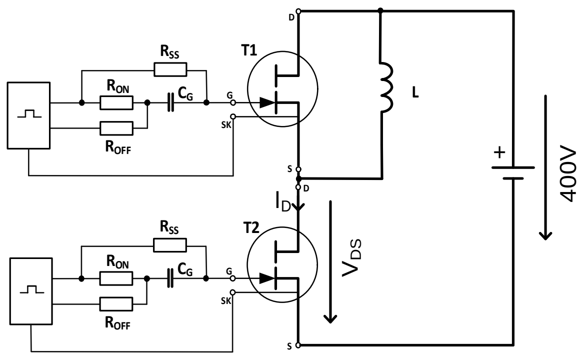
Figure 22 Typ. Coss stored Energy



$E_{OSS} = f(V_{DS})$

5 Test Circuits

Figure 23 Switching times with inductive load



I_D=5 A, R_{ON}=15 Ω; R_{OFF}=4.7 Ω; R_{SS}=1500 Ω;
C_G=0.68 nF; V_{DRV} = 12 V

Figure 24 Switching times waveform

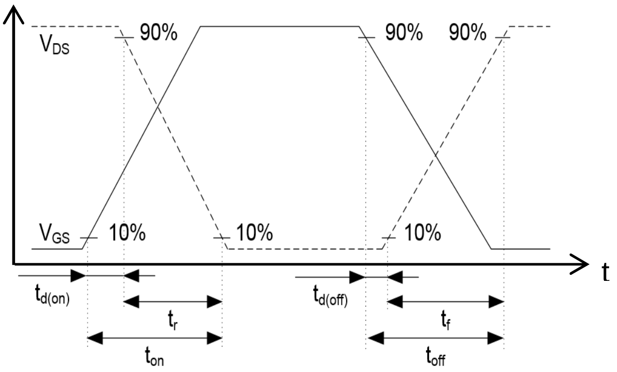
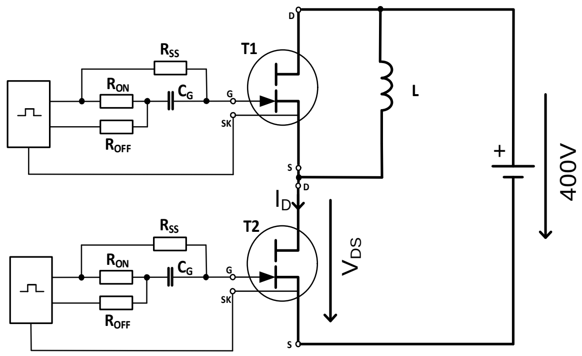
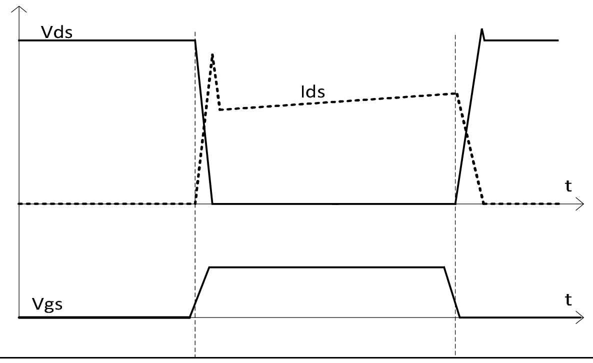


Figure 25 Reverse Channel Characteristics Test



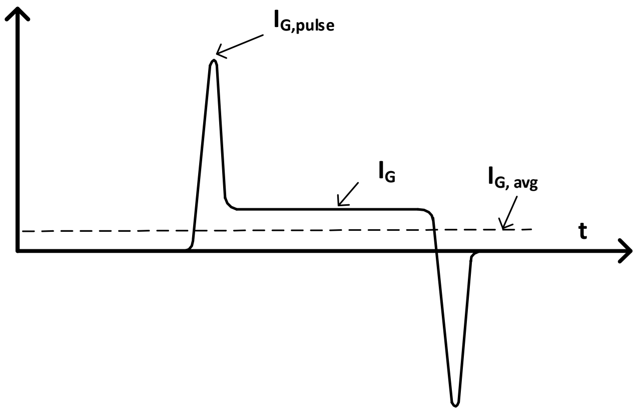
I_D=5 A, R_{ON}=15 Ω; R_{OFF}=4.7 Ω; R_{SS}=1500 Ω;
C_G=0.68 nF; V_{DRV} = 12 V

Figure 26 Typical Reverse Channel Recovery

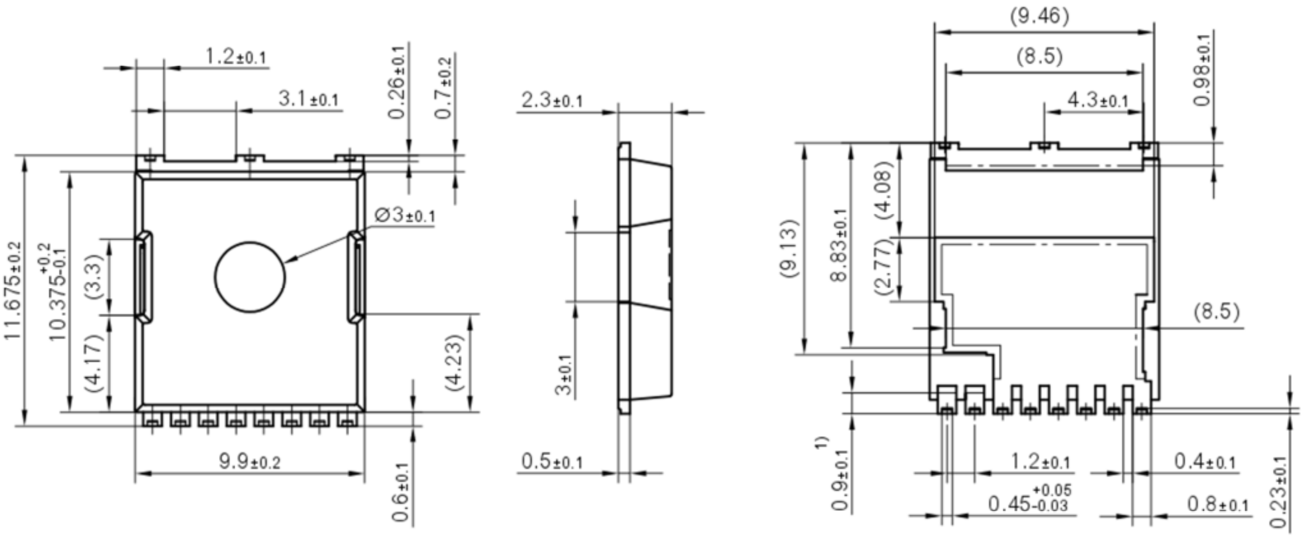


The recovery charge is Q_{OSS} only, no additional Q_{rr}

Figure 27 Gate current switching waveform



6 Package Outlines



1) LEAD LENGTH UP TO ANTI FLASH PROFILE, MOLD FLASHES EXCLUDED.
ALL DIMENSIONS ARE IN UNITS MM
THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 [⊲⊕]

Figure 28 PG-HSOF-8-3 Package Outline, dimensions (mm)

7 Appendix A

Table 9 Related links

- IFX CoolGaN™ webpage: www.infineon.com/why-coolgan
- IFX CoolGaN™ reliability white paper: www.infineon.com/gan-reliability
- IFX CoolGaN™ gate drive application note: www.infineon.com/driving-coolgan
- IFX CoolGaN™ applications information:
  - www.infineon.com/gan-in-server-telecom
  - www.infineon.com/gan-in-wirelesscharging
  - www.infineon.com/gan-in-audio
  - www.infineon.com/gan-in-adapter-charger

8 Revision History

Major changes since the last revision

Revision	Date	Description of change
3.0	2017-04-25	Release of final version
3.1	2018-10-12	Updated application section; added Appendix A and Fig. 27; updated maximum rating table footnotes, switching times and figures.

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