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MCOT128032BX-WM	128 x 32	White	OLED Module
Specification			
Version: 1		Date: 13/07/2012	
Revision			
1	11/07/2012	First issue.	

Display Features			
Resolution	128 x 32		
Appearance	White on Black		
Logic Voltage	2.8V		
Interface	Multi		
Module Size	62.00 x 24.00 x 2.00mm		
Operating Temperature	-40°C ~ +85°C	Box Quantity	Weight / Display
Construction	TAB	---	---

*- For full design functionality, please use this specification in conjunction with the SSD1309 specification.(Provided Separately)

Display Accessories	
Part Number	**Description**
MPBV-7	Interface board compatible with up to 30way, 0.5mm pitch FFC. Driven from any board that can be wired to a 1mm pitch SHDR-30V-S-B receptacle.

Optional Variants	
Appearance	**Voltage**

Basic Specifications

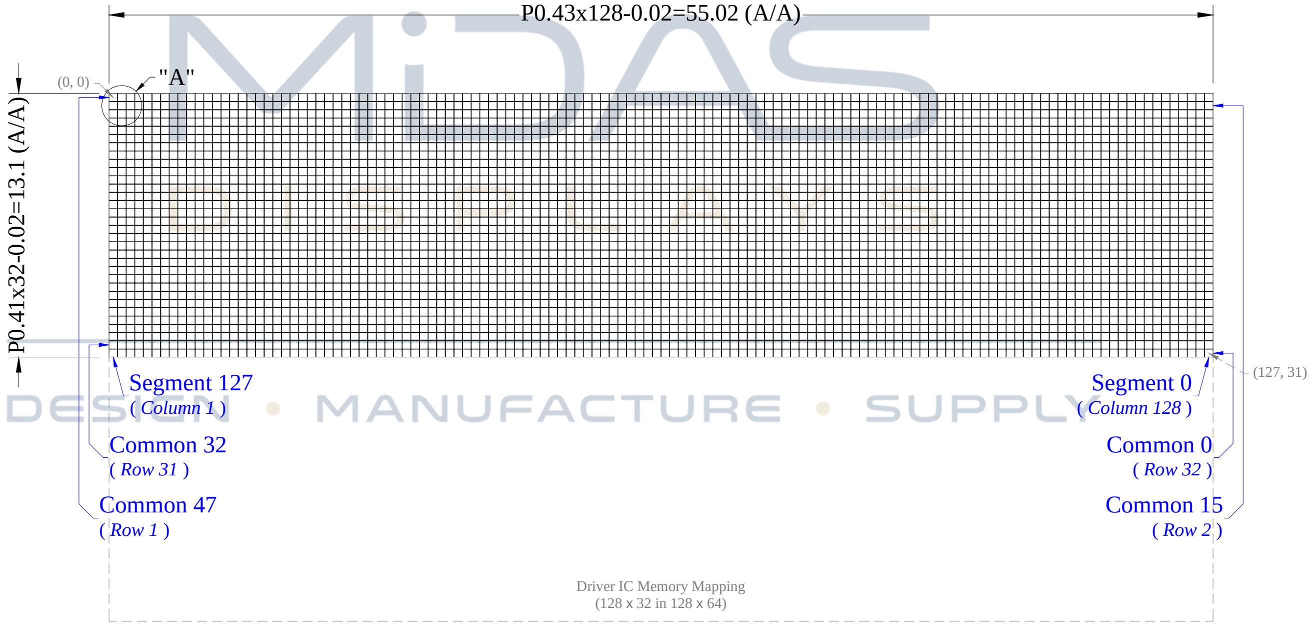
Display Specifications

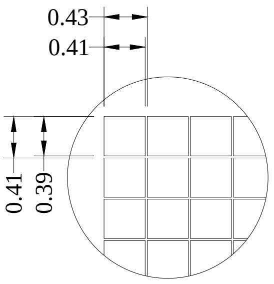
1) Display Mode: Passive Matrix
2) Display Color: Monochrome (White)
3) Drive Duty: 1/32 Duty

Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing
2) Number of Pixels: 128 × 32
3) Module Size: 62.00 × 60.00 × 2.00 (mm)
4) Panel Size: 62.00 × 24.00 × 2.00 (mm) including “Anti-Glare Polarizer”
5) Active Area: 55.02 × 13.10 (mm)
6) Pixel Pitch: 0.43 × 0.41 (mm)
7) Pixel Size: 0.41 × 0.39 (mm)
8) Weight: 5.82 (g) ±10%

Active Area / Memory Mapping & Pixel Construction

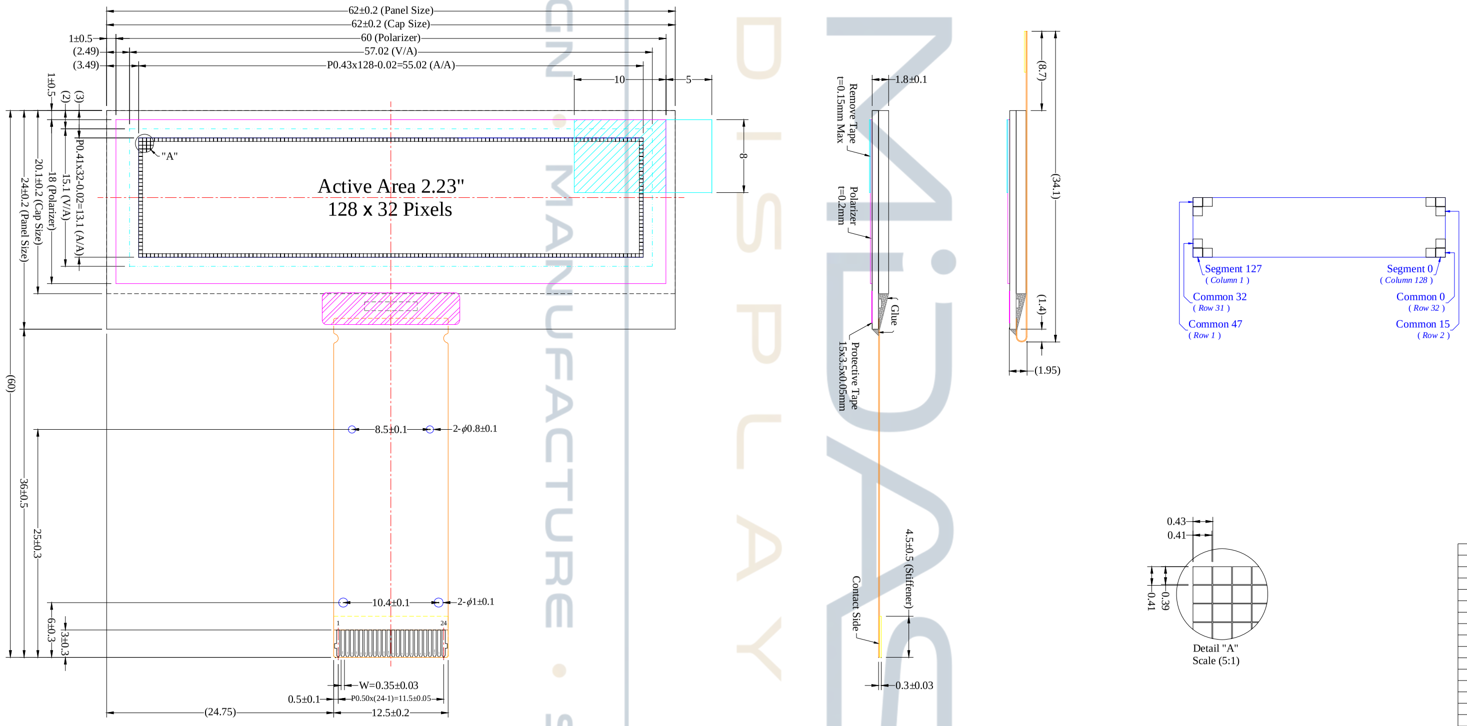




Detail "A"
Scale (5:1)

Mechanical Drawing

Item	Date	Remark
A	20120711	Original Drawing



Pin	Symbol
1	N.C. (GND)
2	VLSS
3	VSS
4	N.C.
5	VDD
6	BS1
7	BS2
8	CS#
9	RES#
10	D/C#
11	R/W#
12	E/RD#
13	D0
14	D1
15	D2
16	D3
17	D4
18	D5
19	D6
20	D7
21	IREF
22	VCOMH
23	VCC
24	N.C. (GND)

Notes:

1. Color: White
2. Driver IC: SSD1309
3. FPC Number: UT-0209-P05
4. Interface:
   8-bit 68XX/80XX Parallel, 4-wire SPI, I2C
5. General Tolerance: ±0.30
6. The total thickness (1.90 Max) is without protective film.
   The actual assembled total thickness with above materials should be 2.00 Max.

Customer Approval
Signature

Unless Otherwise Specified		Title					Drawing Number		Rev.
Unit	mm						MCOT128032BX-WM		A
General Roughness	⌖ ◁						Material		
Tolerance			Drawn	E.E.	Panel / E.	P.M.	Soda Lime / Polyimide		
Dimension	±0.3	By	Dora Yang	Ting-Kuo Hu	Ivy Lo	Tiffany Hsu	Scale	Sheet	Size
Angle	±1	Date	20120711	20120711	20120711	20120711	1:1	1 of 1	A3

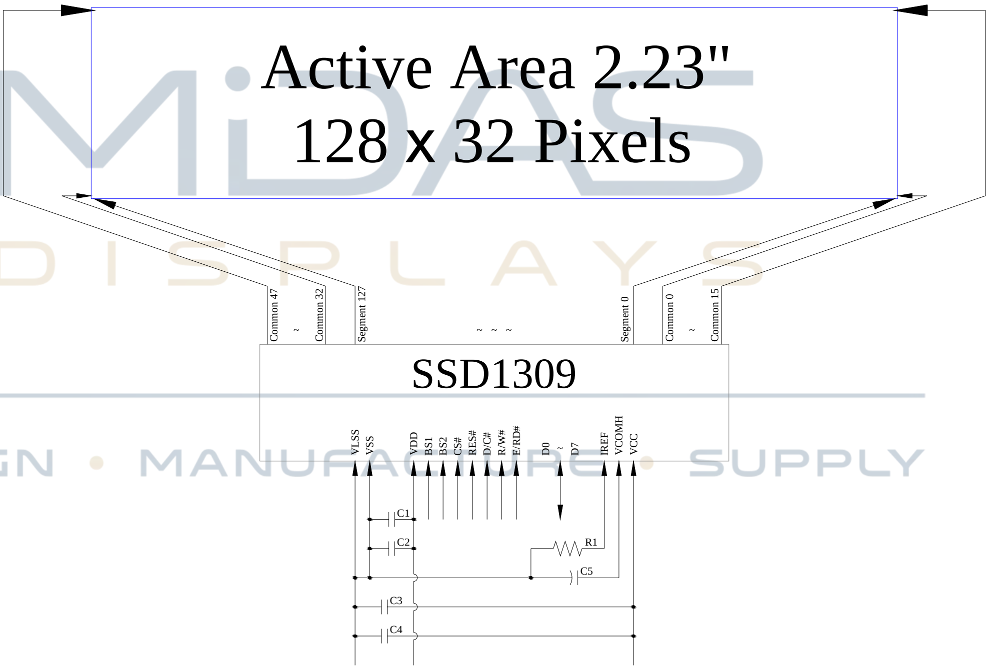
Pin Definition

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4"><i>Power Supply</i></td></tr>
<tr><td>5</td><td>VDD</td><td>P</td><td>Power Supply for Logic Circuit
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>3</td><td>VSS</td><td>P</td><td>Ground of Logic Circuit
This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>23</td><td>VCC</td><td>P</td><td>Power Supply for OEL Panel
This is the most positive voltage supply pin of the chip. It must be supplied externally.</td></tr>
<tr><td>2</td><td>VLSS</td><td>P</td><td>Ground of Analog Circuit
This is an analog ground pin. It should be connected to V_{SS} externally.</td></tr>
<tr><td colspan="4"><i>Driver</i></td></tr>
<tr><td>21</td><td>IREF</td><td>I</td><td>Current Reference for Brightness Adjustment
This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 10μA.</td></tr>
<tr><td>22</td><td>VCOMH</td><td>O</td><td>Voltage Output High Level for COM Signal
This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V_{SS}.</td></tr>
<tr><td colspan="4"><i>Interface</i></td></tr>
<tr><td>6
7</td><td>BS1
BS2</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS1</th><th>BS2</th></tr>
<tr><td>I^2C</td><td>1</td><td>0</td></tr>
<tr><td>4-wire Serial</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>0</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>9</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>8</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>10</td><td>D/C#</td><td>I</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register.
When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I^2C mode, this pin acts as SA0 for slave address selection.
For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>12</td><td>E/RD#</td><td>I</td><td>Read/Write Enable or Read
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.
When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
When serial or I^2C mode is selected, this pin must be connected to V_{SS}.</td></tr>
<tr><td>11</td><td>R/W#</td><td>I</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode.
When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
When serial or I^2C mode is selected, this pin must be connected to V_{SS}.</td></tr>
</table>

Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
Interface (Continued)			
13~20	D0~D7	I/O	**Host Data Input/Output Bus** These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I^{2}C mode is selected, D2, D1 should be tired together and serve as SDA$_{OUT}$, SDA$_{IN}$ in application and D0 is the serial clock input, SCL. Unused pins must be connected to V$_{SS}$ except for D2 in serial mode.
Reserve			
4	N.C.	-	**Reserved Pin** The N.C. pin between function pins is reserved for compatible and flexible design.
1, 24	N.C. (GND)	-	**Reserved Pin (Supporting Pin)** The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.

Block Diagram



MCU Interface Selection: BS1 and BS2
Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7

C1, C3: 0.1μF
C2: 4.7μF
C4: 10μF
C5: 4.7μF / 25V Tantalum Capacitor
R1: 910kΩ, R1 = (Voltage at IREF - BGGND) / IREF

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	0	15	V	1, 2
Operating Temperature	T_{OP}	-40	85	°C	3
Storage Temperature	T_{STG}	-40	90	°C	3

Lifetime 55 cd/m^2 , 70,000 hours (TYP) Notes 4.

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 12.5V, T_a = 25°C, 50% Checkerboard.
Software configuration follows Section 4.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

Optics & Electrical Characteristics

Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 5	100	120	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.27	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 12.5V.
Software configuration follows Section 4.4 Initialization.

DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for Display	V_{CC}	Note 5	12.0	12.5	13.0	V
High Level Input	V_{IH}	I_{OUT} = 100µA, 3.3MHz	0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}	I_{OUT} = 100µA, 3.3MHz	0	-	0.2×V_{DD}	V
High Level Output	V_{OH}	I_{OUT} = 100µA, 3.3MHz	0.9×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT} = 100µA, 3.3MHz	0	-	0.1×V_{DD}	V
Operating Current for V_{DD}	I_{DD}		-	180	300	µA
Operating Current for V_{CC}	I_{CC}	Note 6	-	12.0	15.0	mA
		Note 7	-	19.9	24.9	mA
		Note 8	-	37.9	47.4	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	1	5	µA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	2	10	µA

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 6: V_{DD} = 2.8V, V_{CC} = 12.5V, 30% Display Area Turn on.
Note 7: V_{DD} = 2.8V, V_{CC} = 12.5V, 50% Display Area Turn on.
Note 8: V_{DD} = 2.8V, V_{CC} = 12.5V, 100% Display Area Turn on.

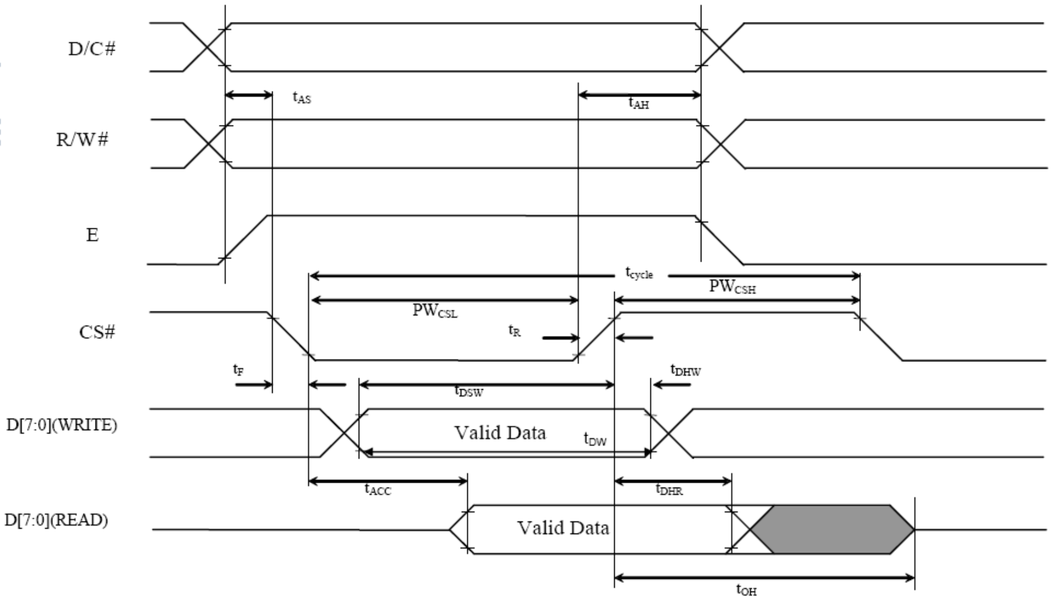
* Software configuration follows Section 4.4 Initialization.

AC Characteristics

68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	**Description**	**Min**	**Max**	**Unit**
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	20	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DW}	Data Write Time	80	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

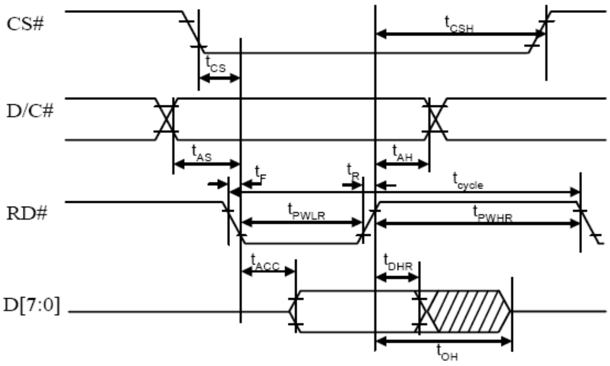
* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



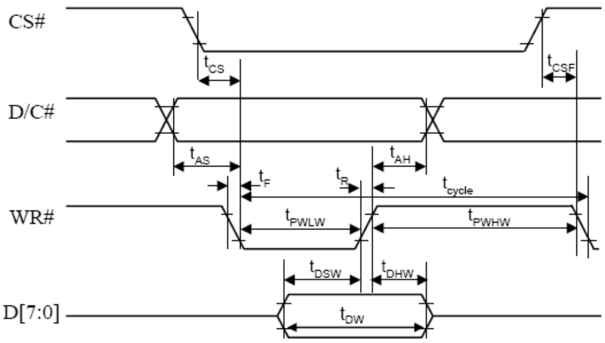
80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	**Description**	**Min**	**Max**	**Unit**
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	20	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DW}	Data Write Time	70	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



(Read Timing)

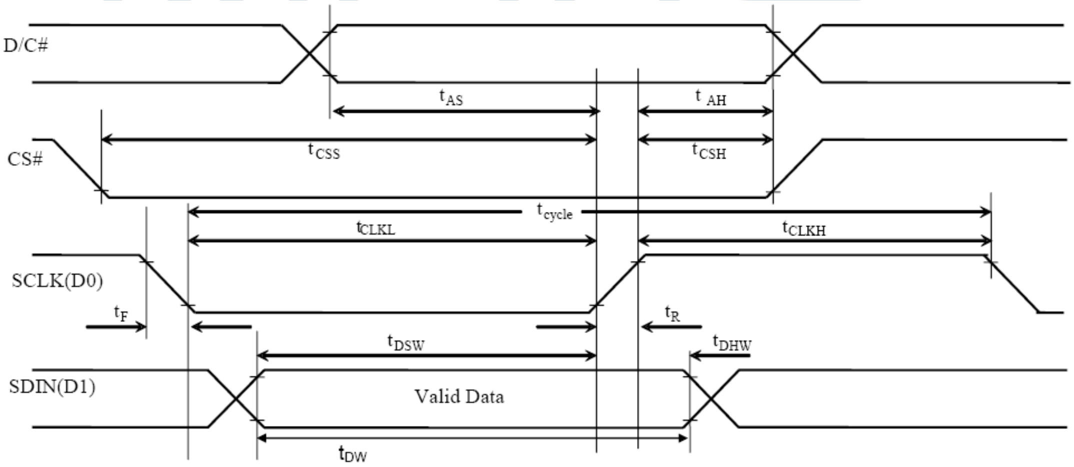


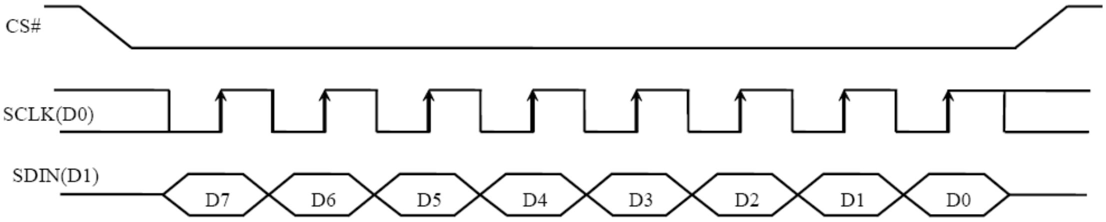
(Write Timing)

Serial Interface Timing Characteristics:

Symbol	**Description**	**Min**	**Max**	**Unit**
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	50	-	ns
t_{DW}	Data Write Time	55	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	50	-	ns
t_{CLKH}	Clock High Time	50	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)

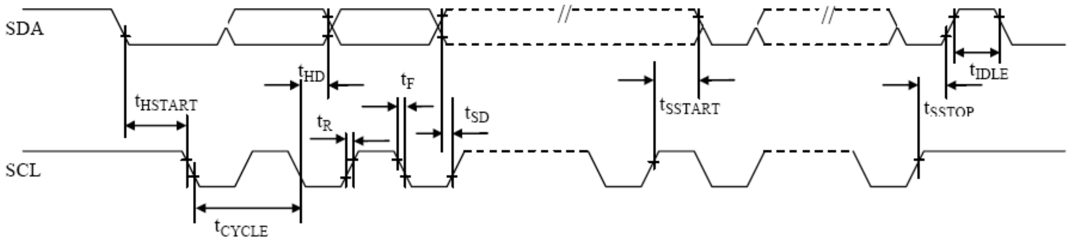




I^{2}C Interface Timing Characteristics:

Symbol	**Description**	**Min**	**Max**	**Unit**
t_{cycle}	Clock Cycle Time	2.5	-	µs
t_{HSTART}	Start Condition Hold Time	0.6	-	µs
t_{HD}	Data Hold Time (for "SDA$_{OUT}$" Pin)	0	-	ns
	Data Hold Time (for "SDA$_{IN}$" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	µs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	µs
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	µs

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



Functional Specification

Commands

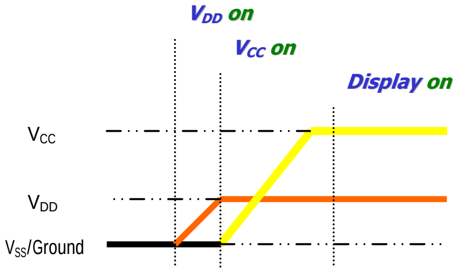
Refer to the Technical Manual for the SSD1309

Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

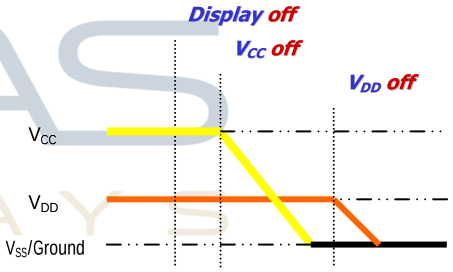
Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 9:

1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} power down.

Reset Circuit

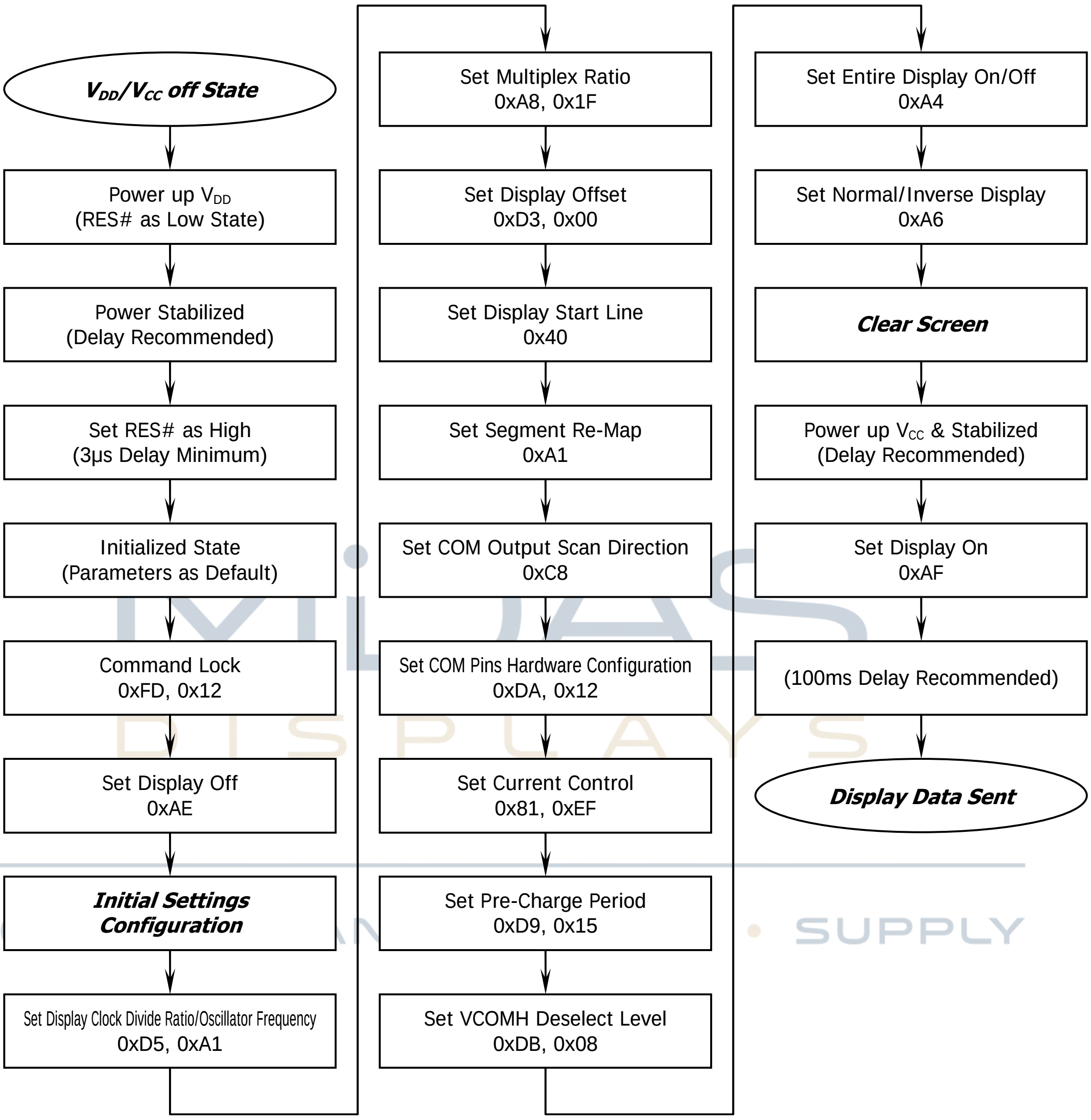
When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

Actual Application Example

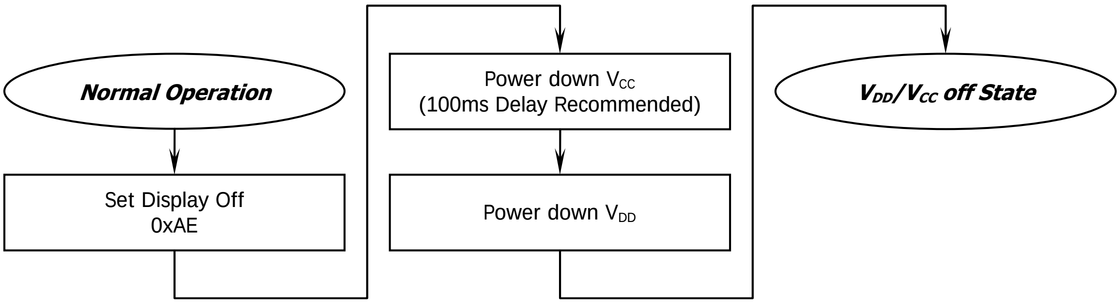
Command usage and explanation of an actual example

<Power up Sequence>

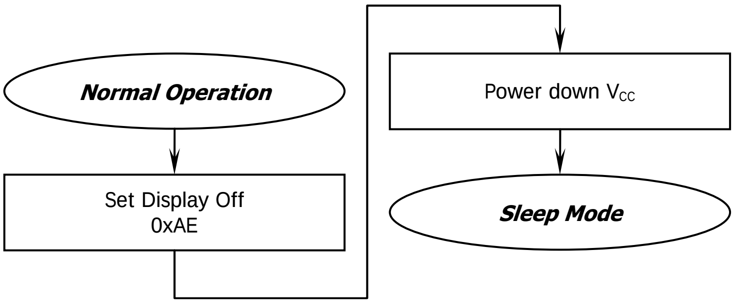


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

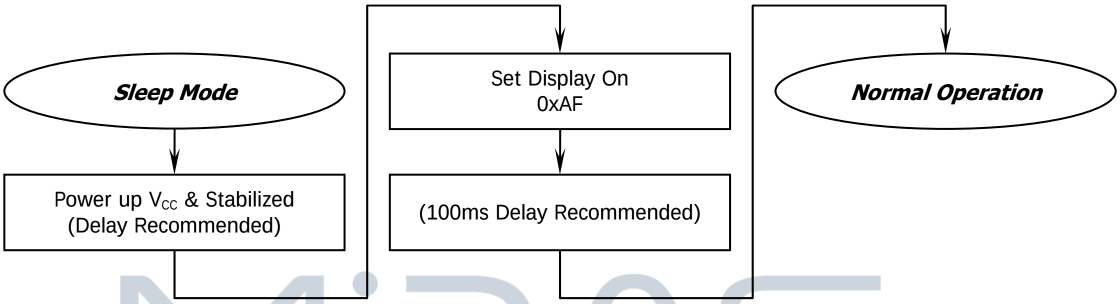
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



Reliability

Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	85°C, 500 hrs	The operational functions work.
Low Temperature Operation	-40°C, 500 hrs	
High Temperature Storage	90°C, 500 hrs	
Low Temperature Storage	-40°C, 500 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 240 hrs	
Thermal Shock	-40°C ⇔ 85°C, 100 cycles 30 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

Outgoing Quality Control Specifications

Environment Required

Customer’s test & measurement are required to be conducted under the following conditions:

Temperature: 23 ± 5°C
Humidity: 55 ± 15% RH
Fluorescent Lamp: 30W
Distance between the Panel & Lamp: ≥ 50cm
Distance between the Panel & Eyes of the Inspector: ≥ 30cm
Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

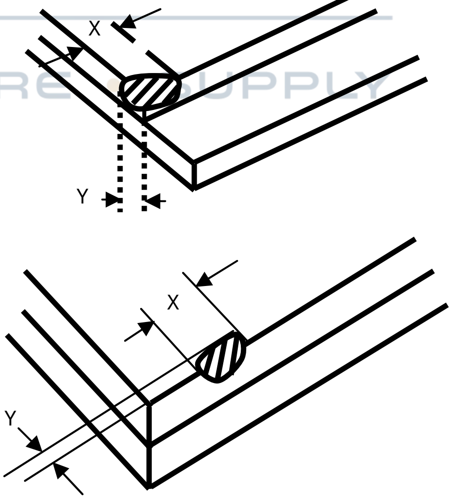
Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

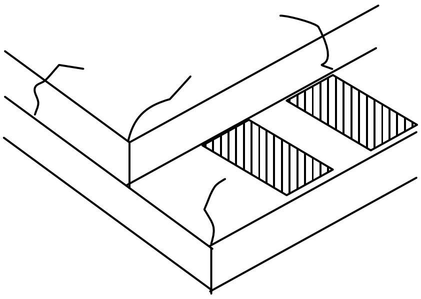
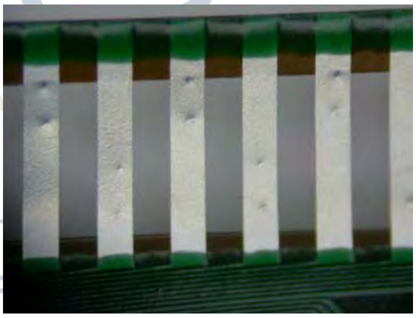
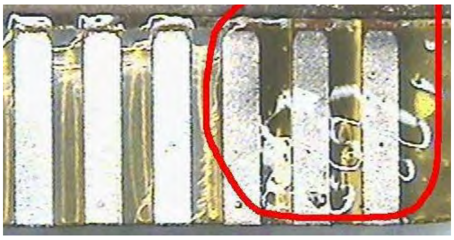
Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

Cosmetic Check (Display Off) in Non-Active Area

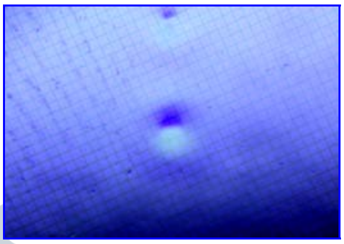
Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

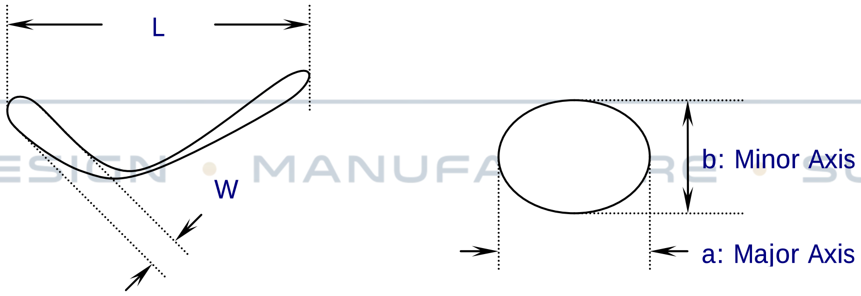
Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

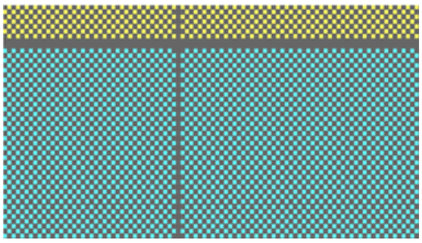
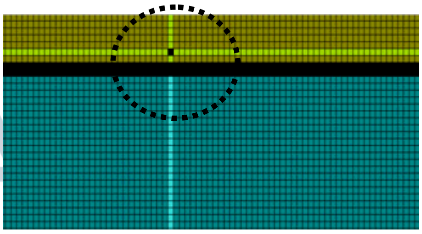
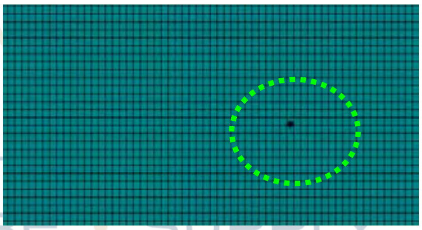
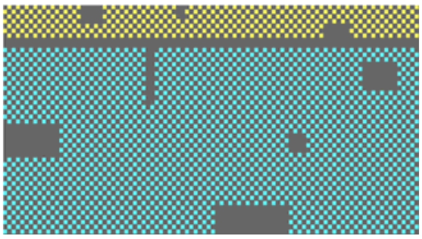
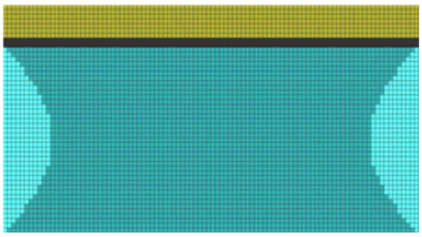
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \le 0.1$ Ignore $W > 0.1$ $L \le 2$ $n \le 1$ $L > 2$ $n = 0$
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	$\Phi \le 0.1$ Ignore $0.1 < \Phi \le 0.25$ $n \le 1$ $0.25 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \le 0.5$ ➔ Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$



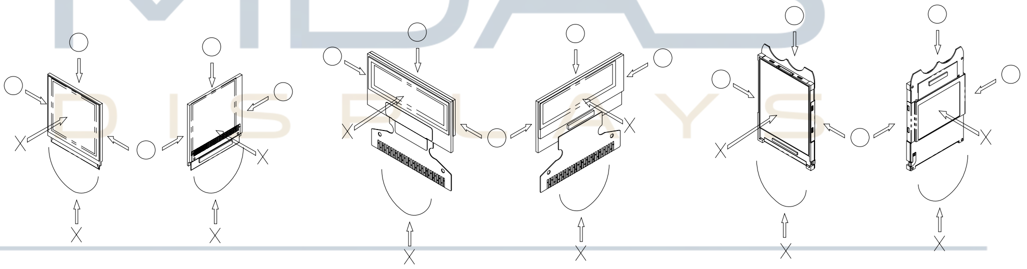
Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

Precautions When Using These OEL Display Modules

Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent
   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the driver IC and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high

humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Midas Displays.)
At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the V_{IL} and V_{IH} specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (V_{DD}). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1309
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.