Sauls Wharf House
Crittens Road
Great Yarmouth
Norfolk
NR31 0AG

Telephone +44 (0)1493 602602
Email:sales@midasdisplays.com
Email:tech@midasdisplays.com
www.midasdisplays.com

MCOT256064DY-WM	256 x 64	White	OLED Module
Specification			
Version: 1		Date: 18/05/2016	
Revision			
1	18/05/2016	First Release.	

Display Features			
Resolution	256 x 64	RoHS compliant	
Appearance	White on Black		
Logic Voltage	3V		
Interface	Parallel / SPI / I²C		
Module Size	60.50 x 19.00 x 1.60mm		
Operating Temperature	-40°C ~ +80°C	Box Quantity	Weight / Display
Construction	COT	---	---

* - For full design functionality, please use this specification in conjunction with the SH1122 specification.(Provided Separately)

Display Accessories	
Part Number	**Description**

Optional Variants	
Appearance	**Voltage**

1. Basic Specifications

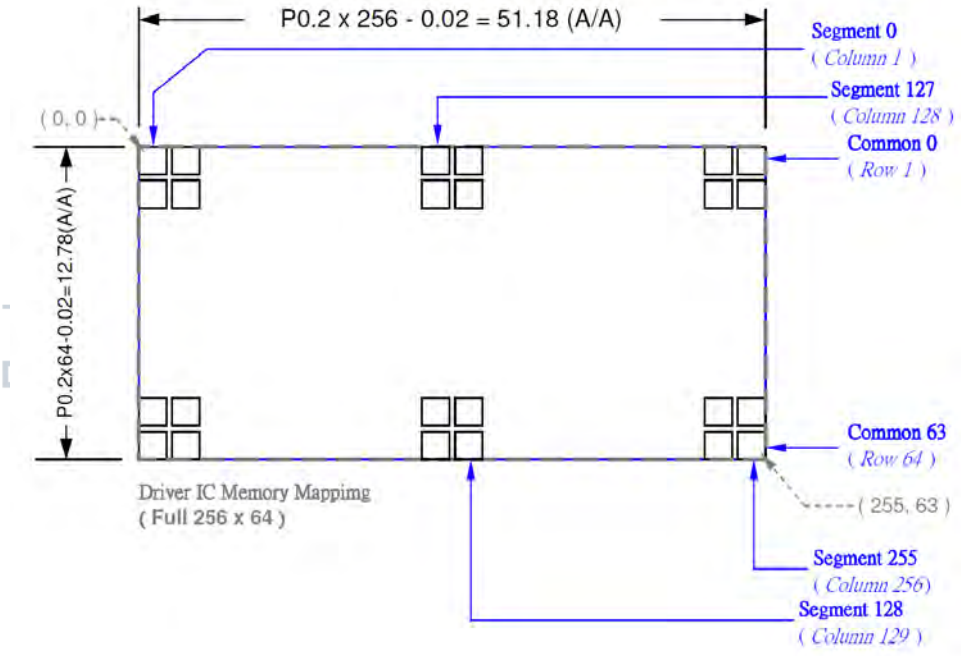
1.1 Display Specifications

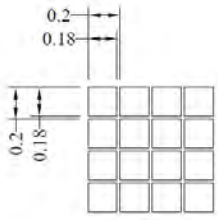
1) Display Mode : Passive Matrix
2) Display Color : Monochrome with 16 Gray Scales (White)
3) Drive Duty : 1/64 Duty

1.2 Mechanical Specifications

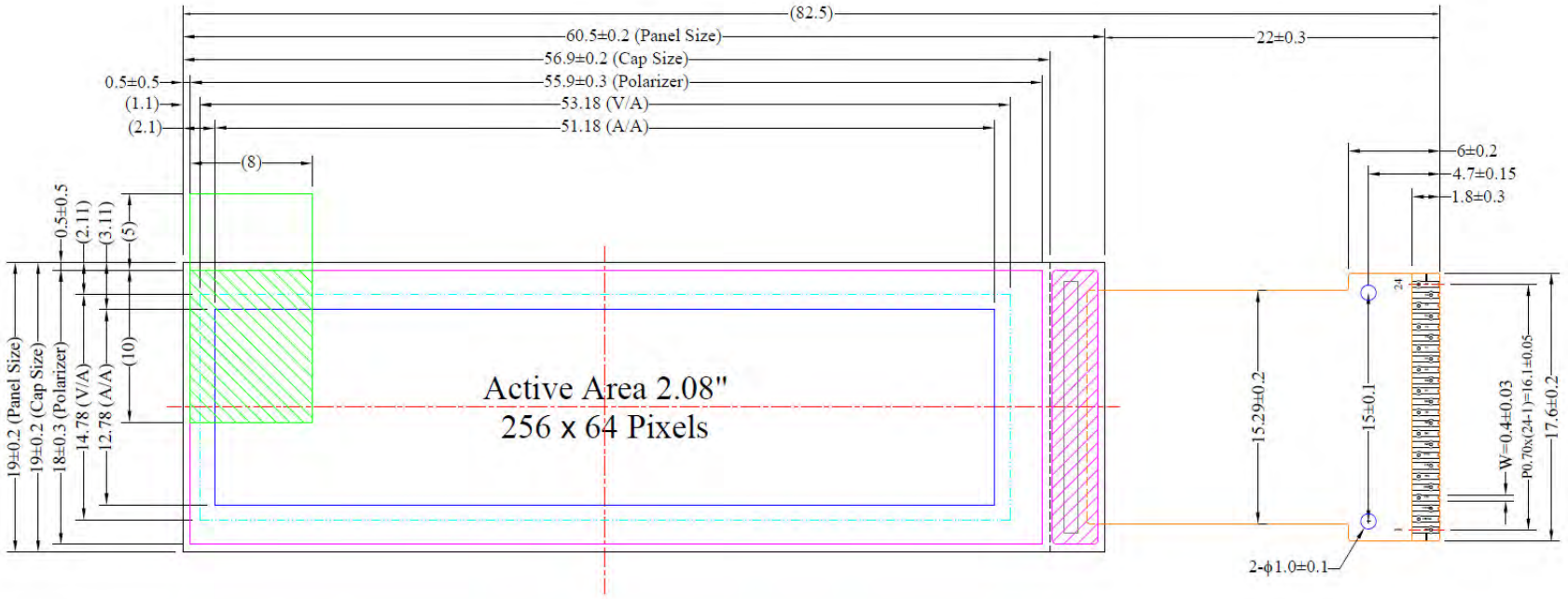
1) Outline Drawing : According to the annexed outline drawing
2) Number of Pixels : 256 × 64
3) Module Size : 82.50 × 19.00 × 1.60 (mm)
4) Panel Size : 60.50 × 19.00 × 1.60 (mm) including "Anti-Glare Polarizer"
5) Active Area : 51.18 × 12.78 (mm)
6) Pixel Pitch : 0.20 × 0.20 (mm)
7) Pixel Size : 0.18 × 0.18 (mm)
8) Weight : T.B.D. (g) ± 10%

1.3 Active Area / Memory Mapping & Pixel Construction

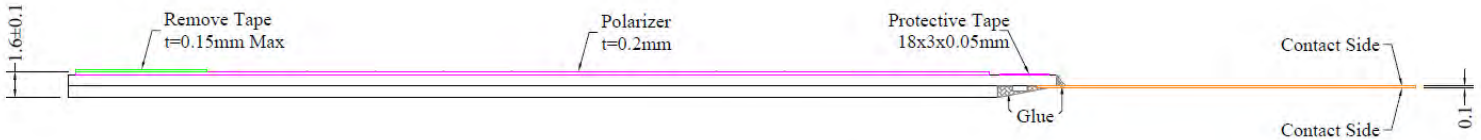


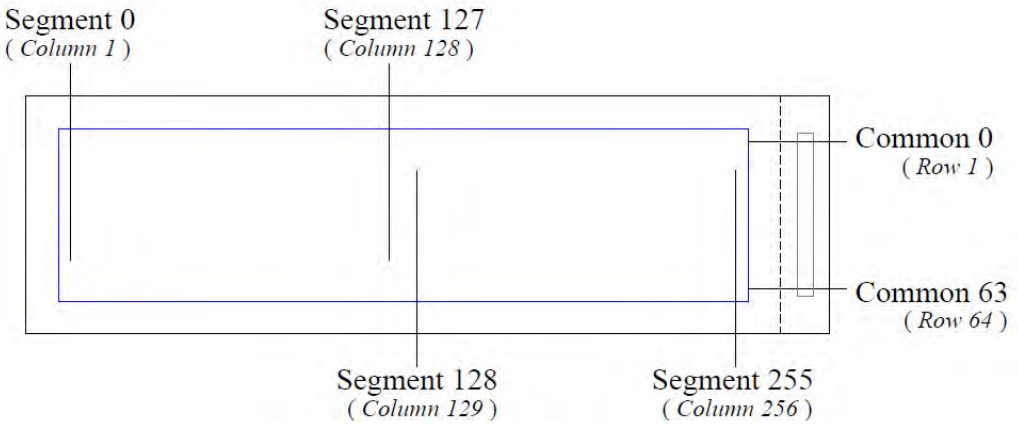


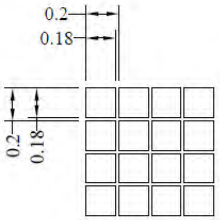
Pixel Detail
Scale (10:1)



Pin	Symbol
1	VPP
2	VSEGM
3	VCOMH
4	VSL
5	IREF
6	VSS
7	VCL
8	VDD
9	IM0
10	IM1
11	IM2
12	CS
13	RES
14	A0
15	WR
16	RD
17	D0
18	D1
19	D2
20	D3
21	D4
22	D5
23	D6
24	D7







Pixel Detail
Scale (10:1)

Notes:

1. Color: White
2. Driver IC: SH1122
3. FPC Number:
4. Interface: 8-bit 68xx/80xx Parallel,3/4-wire SPI, I²C
5. General Tolerance: ±0.30
6. The total thickness (1.7 Max) is without Protective Film.
   The actual assembled total thickness with above materials should be 1.95 Max.

1.5 Pin Definition

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Power Supply</td></tr>
<tr><td>1</td><td>VPP</td><td>P</td><td>Power Supply for OEL Panel
These are the most positive voltage supply pin of the chip. They must be connected to external source.</td></tr>
<tr><td>6</td><td>VSS</td><td>P</td><td>Ground of Logic Circuit
This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>8</td><td>VDD</td><td>P</td><td>Power Supply for Operation
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td colspan="4">Driver</td></tr>
<tr><td>2</td><td>VSEGM</td><td>O</td><td>Voltage Output High Level for Segment Pre-Charge
This pin is for the voltage output high level for SEG pre-charge. A capacitor should be connected between this pin and GND.</td></tr>
<tr><td>3</td><td>VCOMH</td><td>O</td><td>Voltage Output High Level for COM Signal
This pin is for the voltage output high level for COM signals. A capacitor should be connected between this pin and GND.</td></tr>
<tr><td>4</td><td>VSL</td><td>P</td><td>Voltage Reference of Segment
This pin is segment voltage reference pin. A capacitor should be connected between this pin and GND.</td></tr>
<tr><td>5</td><td>IREF</td><td>O</td><td>Current Reference for Brightness Adjustment
This pin is segment current reference pin. A resistor should be connected between this pin and GND. Set the current at 15.625μA maximum.</td></tr>
<tr><td>7</td><td>VCL</td><td>P</td><td>Voltage Reference of Common
This pin is Common voltage reference pin. This pad should be connected VSS externally.</td></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>9
10
11</td><td>IM0
IM1
IM2</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><th>Interface mode</th><th>IM0</th><th>IM1</th><th>IM2</th></tr>
<tr><td>3-wire Serial</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>4-wire Serial</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>I^2C</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>12</td><td>CS</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>13</td><td>RES</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>14</td><td>A0</td><td>I</td><td>Data/Command Control
This pin is Data/Command control pin.
When the pin is pulled high, the input at D7~D0 is treated as display data.
When the pin is pulled low, the input at D7~D0 will be transferred to the command register.
In I^2C interface, this pad serves as SA0 to distinguish the different address.
For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>15</td><td>WR
(R/W)</td><td>I</td><td>Read/Write Select or Write
This pin is MCU interface input.
When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode.
When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
When serial mode is selected, this pin must be connected to V_{SS}.</td></tr>
</table>

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
Interface (Continued)			
16	RD	I	**Read/Write Enable or Read** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to V_{SS}.
17~24	D7~D0	I/O	**Host Data Input/Output Bus** These pins are 8-bit bi-directional data bus to be connected to 8-bit standard MPU data bus. When serial mode is selected, D1 will be the serial data input pad (SI) and D0 will be the serial clock input pad (SCL). At this time, D2 to D7 are set to high impedance. When I^2C interface is selected, D1 will be the serial data input pad (SDA) and D0 will be the serial clock input pad (SCL). At this time, D2 to D7 are set to high impedance.

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Core Operation	V_{DD}	-0.3	3.6	V	1, 2
Supply Voltage for Display	V_{PP}	-0.3	14.5	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	3
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (50 cd/m2)	**Typ(30K)**			**hour**	**4**

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 12.0V, T_a = 25°C, 50% Checkerboard.
Software configuration follows Section 4.5 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 5	120	150	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.27 0.29	0.31 0.33	0.35 0.37	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 3.0V, V_{CC} = 12.0V.
Software configuration follows Section 4.5 Initialization.

3.2 DC Characteristics

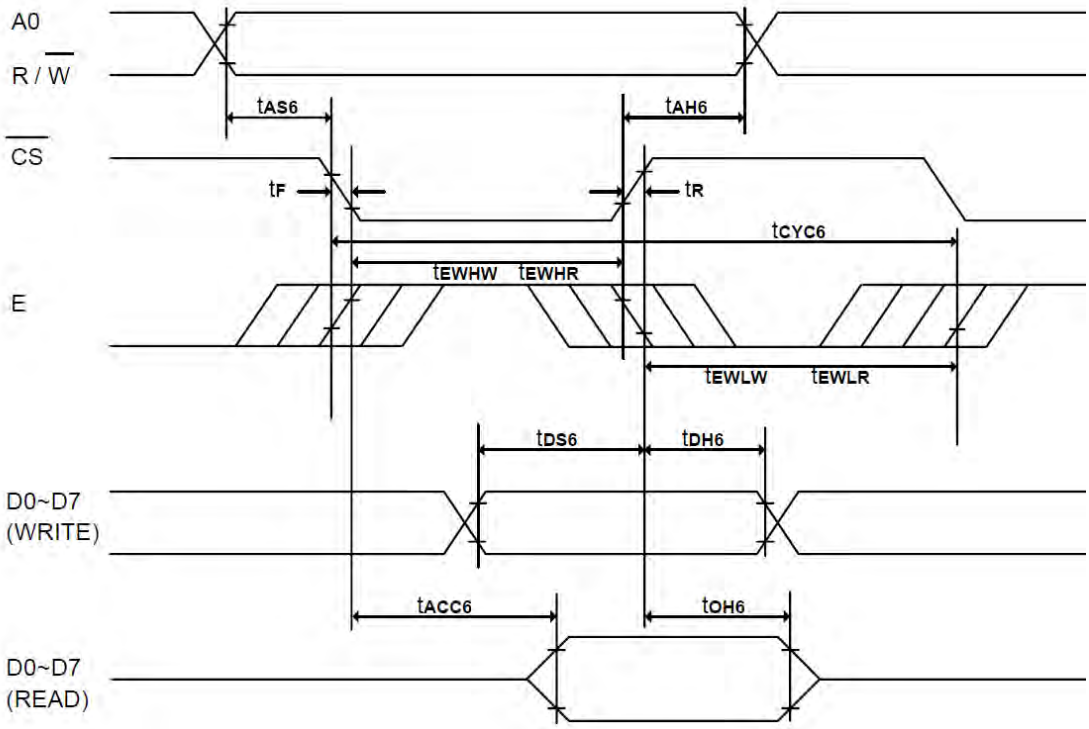
Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{DD}		1.65	3.0	3.5	V
Supply Voltage for Display	V_{CC}	Note 5	11.5	12.0	12.5	
High Level Input	V_{IHC}			-	V_{DD}	V
Low Level Input	V_{ILC}		V_{SS}	-	$0.2\times V_{DD}$	V
High Level Output	V_{OHC}	I_{OH} = -0.5mA	$0.8\times V_{DD}$	-	V_{DD}	V
Low Level Output	V_{OLC}	I_{OL} = 0.5mA	V_{SS}	-	$0.2\times V_{DD}$	V
SDA low-level output voltage	V_{OLCS}	V_{DD} < 2V, I_{OL} = 0.3mA	V_{SS}	-	$0.2\times V_{DD}$	V
		V_{DD} > 2V, I_{OL} = 0.3mA		-	0.4	V
Operating Current for V_{DD}	I_{DD}		-	110	160	μA
Operating Current for V_{PP}	I_{PP}	Note 6		12.0	15.0	mA
		Note 7	-	19.3	24.1	mA
		Note 8	-	37.2	46.5	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	-	5	μA
Sleep Mode Current for V_{PP}	$I_{PP, SLEEP}$		-	-	5	μA

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{PP}) are subject to the change of the panel characteristics and the customer's request.
Note 6: V_{DD} = 2.8V, V_{PP} = 12.0V, 30% Display Area Turn on.
Note 7: V_{DD} = 2.8V, V_{PP} = 12.0V, 50% Display Area Turn on.
Note 8: V_{DD} = 2.8V, V_{PP} = 12.0V, 100% Display Area Turn on.

* Software configuration follows Section 4.5 Initialization.

3.3 AC Characteristics

3.3.1 6800-Series MPU Parallel Interface Timing Characteristics:



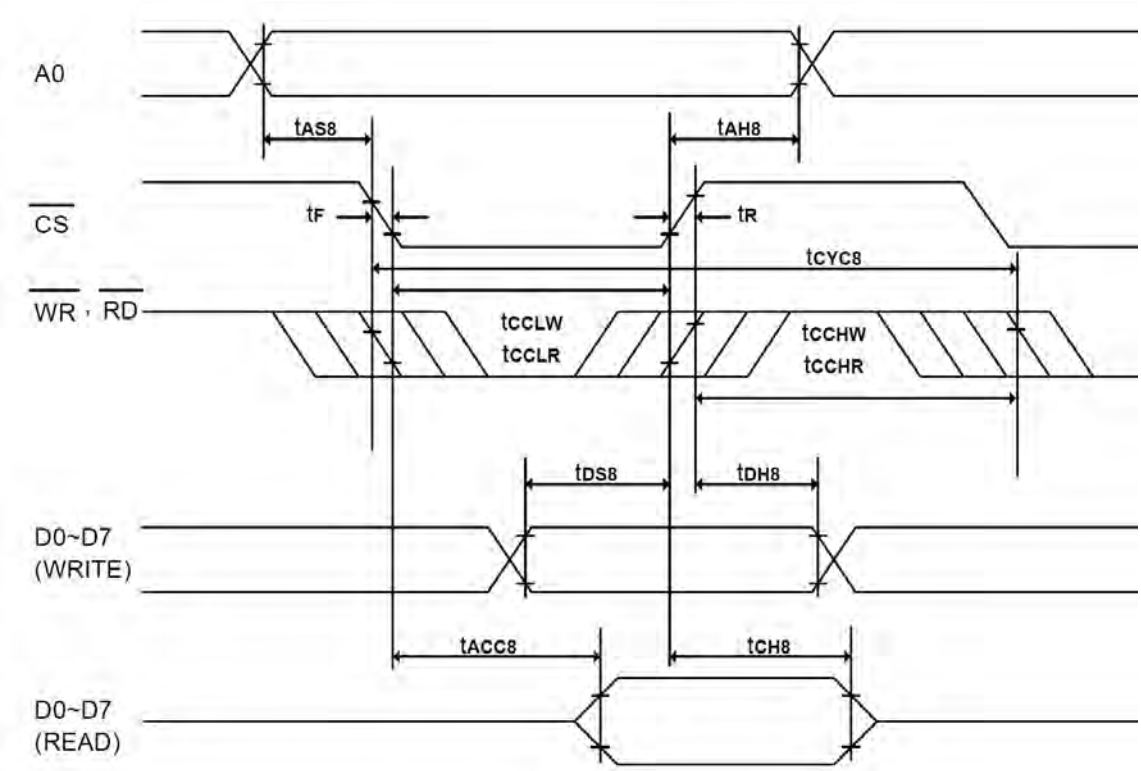
Symbol	Description	Min	Max	Unit
t_{cyc6}	System cycle time	600	-	ns
t_{AS6}	Address Setup Time	0	-	ns
t_{AH6}	Address Hold Time	0	-	ns
t_{DS6}	Data Setup Time	80	-	ns
t_{DH6}	Data Hold Time	30	-	ns
t_{CH6}	Output Disable Time (C_L=100pF)	20	140	ns
t_{ACC6}	Access Time (C_L=100pF)	-	280	ns
t_{EWHW}	Enable H pulse width(Write)	200	-	ns
t_{EWHR}	Enable H pulse width(Read)	240	-	ns
t_{EWLW}	Enable L pulse width(Writw)	200	-	ns
t_{EWLR}	Enable L pulse width(Read)	200	-	ns
t_R	Rise Time	-	30	ns
t_F	Fall Time	-	30	ns

* (VDD -VSS = 1.65V-3.5V, TA = +25°C)

Symbol	Description	Min	Max	Unit
t_{cyc6}	System cycle time	300	-	ns
t_{AS6}	Address Setup Time	0	-	ns
t_{AH6}	Address Hold Time	0	-	ns
t_{DS6}	Data Setup Time	40	-	ns
t_{DH6}	Data Hold Time	15	-	ns
t_{CH6}	Output Disable Time (C_L=100pF)	10	70	ns
t_{ACC6}	Access Time (C_L=100pF)	-	140	ns
t_{EWHW}	Enable H pulse width(Write)	100	-	ns
t_{EWHR}	Enable H pulse width(Read)	120	-	ns
t_{EWLW}	Enable L pulse width(Writw)	100	-	ns
t_{EWLR}	Enable L pulse width(Read)	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (VDD -VSS = 2.4V-3.5V, TA = +25°C)

3.3.2 8080-Series MPU Parallel Interface Timing Characteristics:



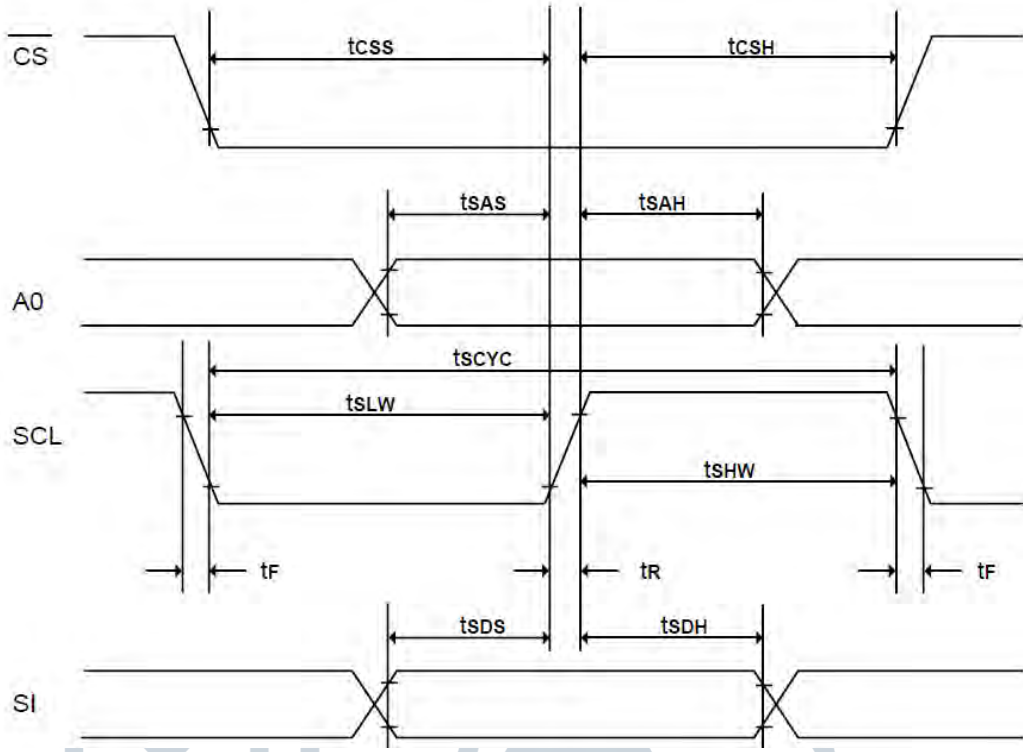
Symbol	Description	Min	Max	Unit
t_{cyc8}	System cycle time	600	-	ns
t_{AS8}	Address Setup Time	0	-	ns
t_{AH8}	Address Hold Time	0	-	ns
t_{DS8}	Data Setup Time	80	-	ns
t_{DH8}	Data Hold Time	30	-	ns
t_{CH8}	Output Disable Time (C_L=100pF)	20	140	ns
t_{ACC8}	Access Time (C_L=100pF)	-	280	ns
t_{CCLW}	Control L pulse width(WR)	200	-	ns
t_{CCLR}	Control L pulse width(RD)	240	-	ns
t_{CCHW}	Control H pulse width(WR)	200	-	ns
t_{CCHR}	Control H pulse width(RD)	200	-	ns
t_R	Rise Time	-	30	ns
t_F	Fall Time	-	30	ns

* (VDD -VSS = 1.65V-3.5V, TA = +25°C)

Symbol	Description	Min	Max	Unit
t_{cyc8}	System cycle time	300	-	ns
t_{AS8}	Address Setup Time	0	-	ns
t_{AH8}	Address Hold Time	0	-	ns
t_{DS8}	Data Setup Time	40	-	ns
t_{DH8}	Data Hold Time	15	-	ns
t_{CH8}	Output Disable Time (C_L=100pF)	10	70	ns
t_{ACC8}	Access Time (C_L=100pF)	-	140	ns
t_{CCLW}	Control L pulse width(WR)	100	-	ns
t_{CCLR}	Control L pulse width(RD)	120	-	ns
t_{CCHW}	Control H pulse width(WR)	100	-	ns
t_{CCHR}	Control H pulse width(RD)	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (VDD -VSS = 2.4V-3.5V, TA = +25°C)

3.3.3 Serial Interface Timing Characteristics: (4-wire SPI)



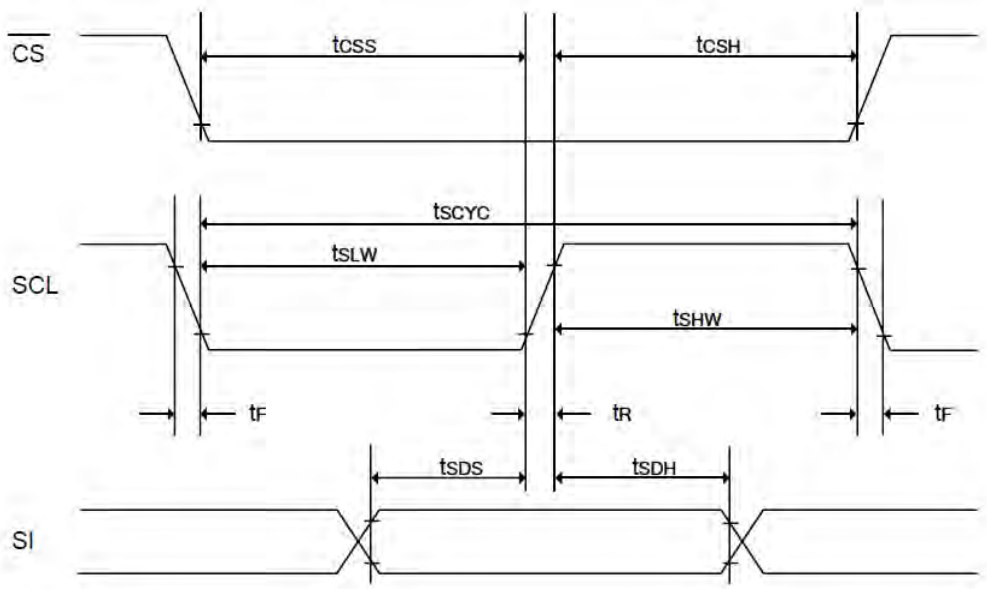
Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	500	-	ns
t_{SAS}	Address Setup Time	300	-	ns
t_{SAH}	Address Hold Time	300	-	ns
t_{SDS}	Write Data Setup Time	200	-	ns
t_{SDH}	Write Data Hold Time	200	-	ns
t_{CSS}	CS Setup Time	240	-	ns
t_{CSH}	CS Hold Time	120	-	ns
t_{SHW}	Serial Clock H pulse Time	200	-	ns
t_{SLW}	Serial Clock L pulse Time	200	-	ns
t_R	Rise Time	-	30	ns
t_F	Fall Time	-	30	ns

* (VDD -VSS = 1.65V ~ 3.5V, TA = 25°C)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	ns
t_{SAS}	Address Setup Time	150	-	ns
t_{SAH}	Address Hold Time	150	-	ns
t_{SDS}	Write Data Setup Time	100	-	ns
t_{SDH}	Write Data Hold Time	100	-	ns
t_{CSS}	CS Setup Time	120	-	ns
t_{CSH}	CS Hold Time	60	-	ns
t_{SHW}	Serial Clock H pulse Time	100	-	ns
t_{SLW}	Serial Clock L pulse Time	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (VDD -VSS = 2.4V ~ 3.5V, TA = 25°C)

3.3.4 Serial Interface Timing Characteristics: (3-wire SPI)



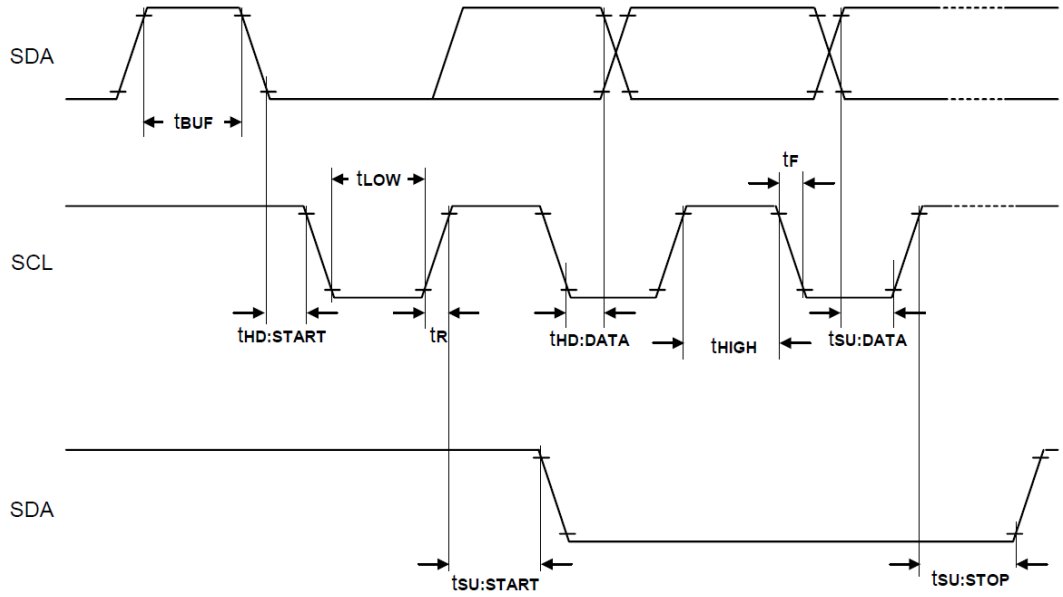
Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	500	-	ns
t_{SDS}	Write Data Setup Time	200	-	ns
t_{SDH}	Write Data Hold Time	200	-	ns
t_{CSS}	CS Setup Time	240	-	ns
t_{CSH}	CS Hold Time	120	-	ns
t_{SHW}	Serial Clock H pulse Time	200	-	ns
t_{SLW}	Serial Clock L pulse Time	200	-	ns
t_R	Rise Time	-	30	ns
t_F	Fall Time	-	30	ns

* (VDD -VSS = 1.65V ~ 3.5V, TA = 25°C)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	ns
t_{SDS}	Write Data Setup Time	100	-	ns
t_{SDH}	Write Data Hold Time	100	-	ns
t_{CSS}	CS Setup Time	120	-	ns
t_{CSH}	CS Hold Time	60	-	ns
t_{SHW}	Serial Clock H pulse Time	100	-	ns
t_{SLW}	Serial Clock L pulse Time	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (VDD -VSS = 2.4V ~ 3.5V, TA = 25°C)

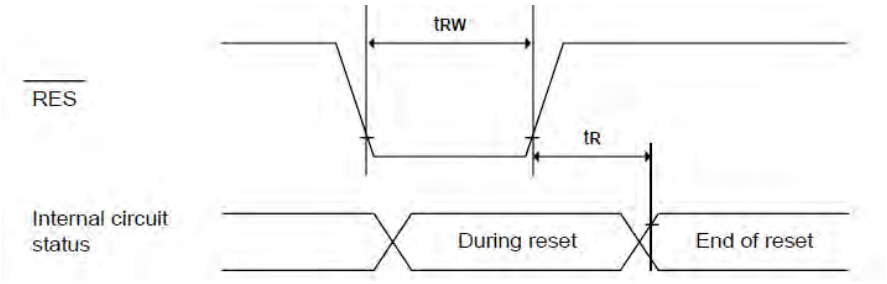
3.3.5 I^2C Interface Timing Characteristics:



Symbol	Description	Min	Max	Unit
f_{SCL}	SCL clock frequency	DC	400	kHz
T_{LOW}	SCL Clock L pulse Time	1.3	-	μs
T_{HIGH}	SCL Clock H pulse Time	0.6		μs
$T_{SU:\ DATA}$	Data Setup Time	100	-	ns
$T_{HU:\ DATA}$	Data Hold Time	0	0.9	μs
T_R	SCL、SDA rise Time	20+0.1Cb	300	ns
T_F	SCL、SDA fall Time	20+0.1Cb	300	ns
Cb	Capacity load on each bus line	-	400	pF
$T_{SU:\ START}$	Setup Time for re-START	0.6	-	μs
$T_{HU:\ START}$	START Hold Time	0.6	-	μs
$T_{SU:\ STOP}$	Setup Time for STOP	0.6	-	μs
T_{BUF}	Bus free time between STOP and START condition	1.3	-	μs

* (VDD -VSS = 1.65V ~ 3.5V, TA = 25°C)

3.3.6 Reset Timing Characteristics:



Symbol	Description	Min	Max	Unit
t_R	Reset Time	-	2	µs
t_{RW}	Reset low pulse Time	10	-	µs

* (VDD -VSS = 1.65V ~ 3.5V, TA = 25°C)

Symbol	Description	Min	Max	Unit
t_R	Reset Time	-	1	µs
t_{RW}	Reset low pulse Time	5	-	µs

* (VDD -VSS = 2.4V ~ 3.5V, TA = 25°C)

4. Functional Specification

4.1 Commands

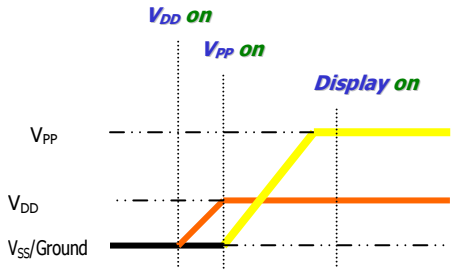
Refer to the Technical Manual for the SH1122

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

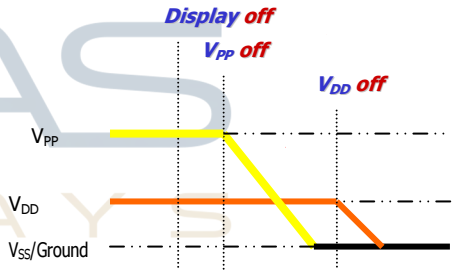
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{PP}
6. Delay 200ms
   (When V_{PP} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{PP}
3. Delay 100ms
   (When V_{PP} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 9:

1) Since an ESD protection circuit is connected between V_{DD} and V_{PP} inside the driver IC, V_{PP} becomes lower than V_{DD} whenever V_{PP} is OFF.
2) V_{PP} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{PP}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{PP} power down.

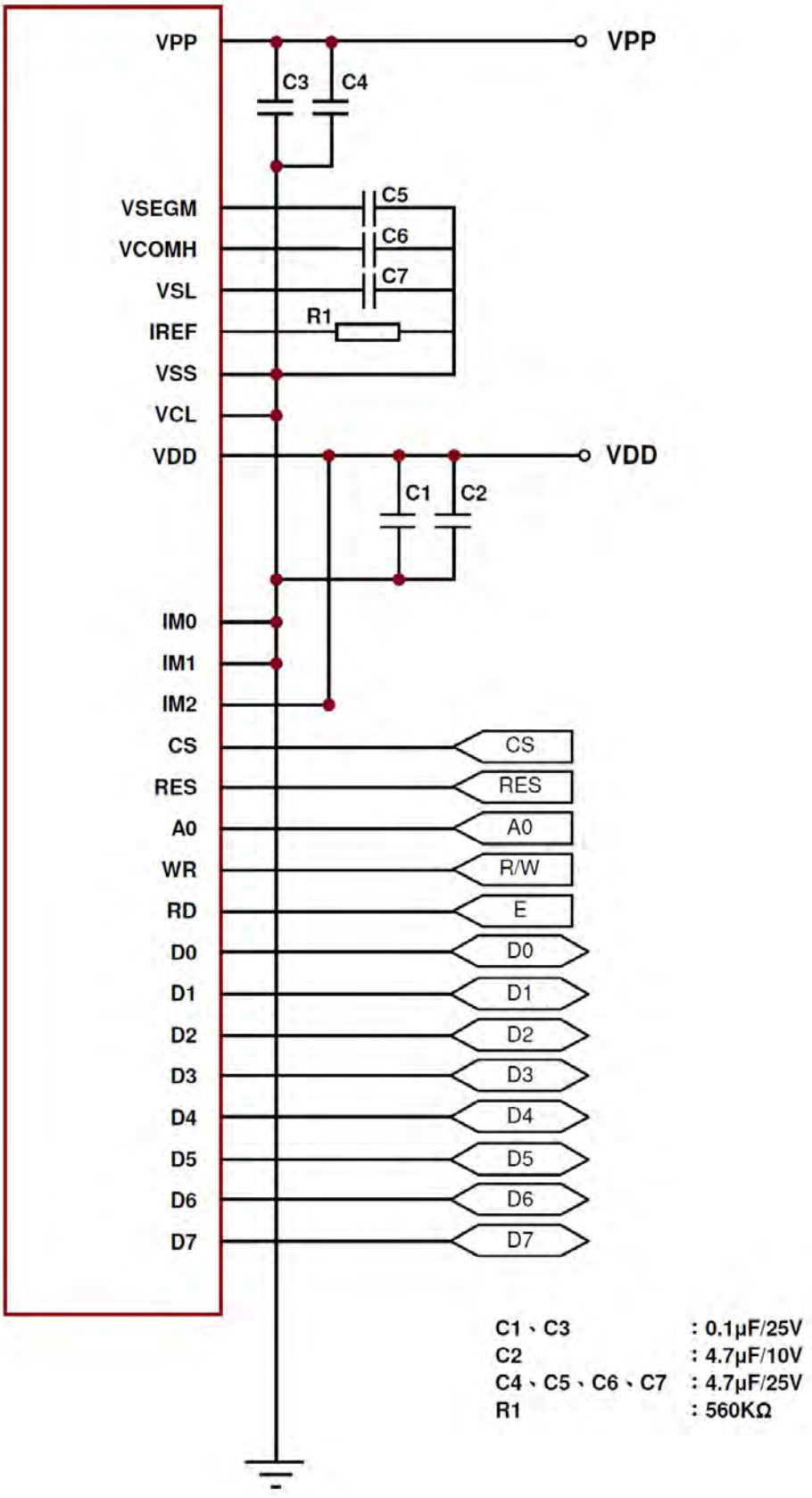
4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

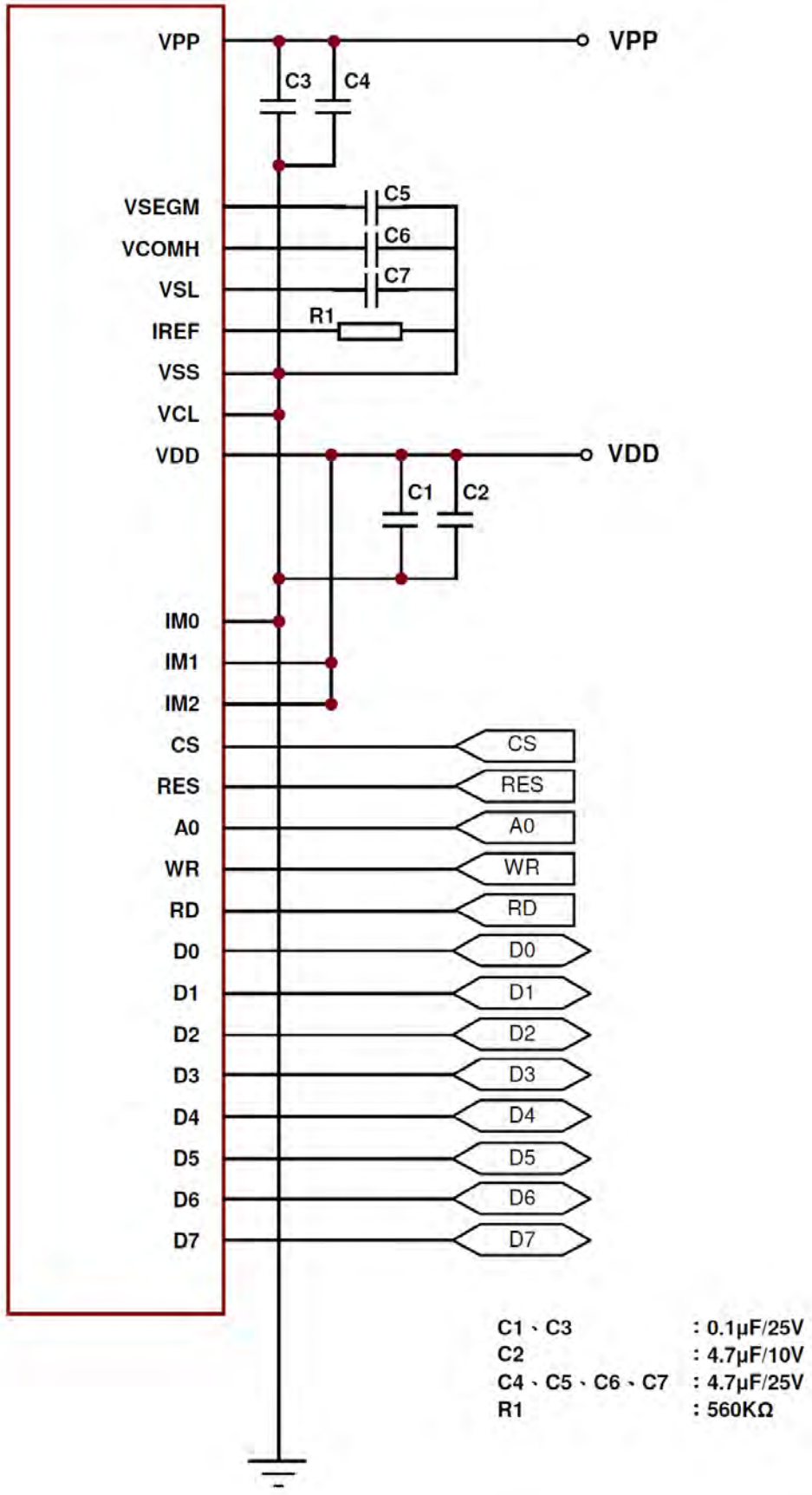
1. Display is OFF. Common and Segment are in high impedance state.
2. 256 × 64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface.
5. Display start line is set at display RAM address 00H
6. Column address counter is set at 0
7. Normal scanning direction of the Common outputs
8. Contrast control register is set at 80H
9. Internal DC-DC is selected.

4.4 Application circuit

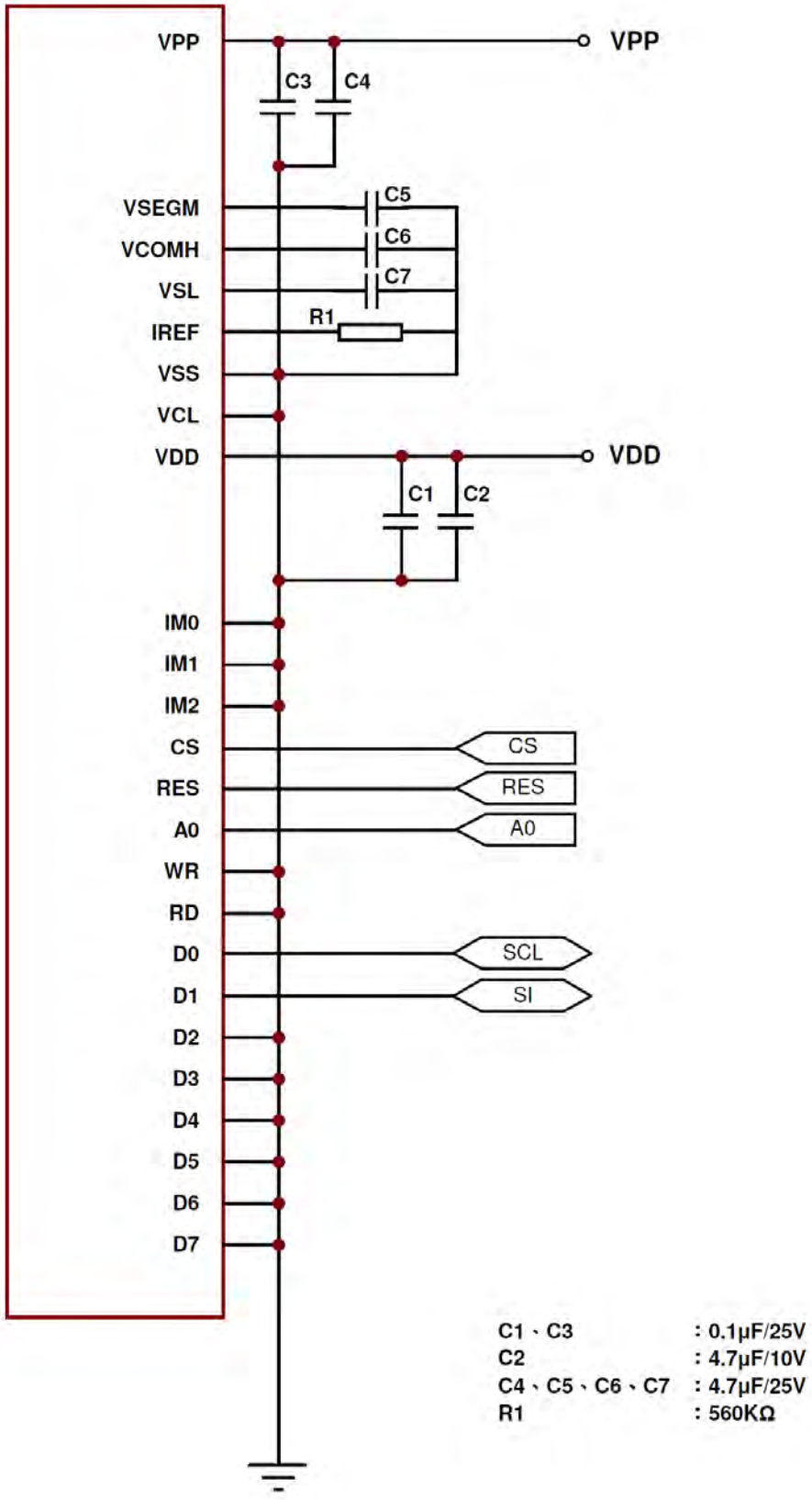
4.4.1 6800-Series MPU Parallel Interface



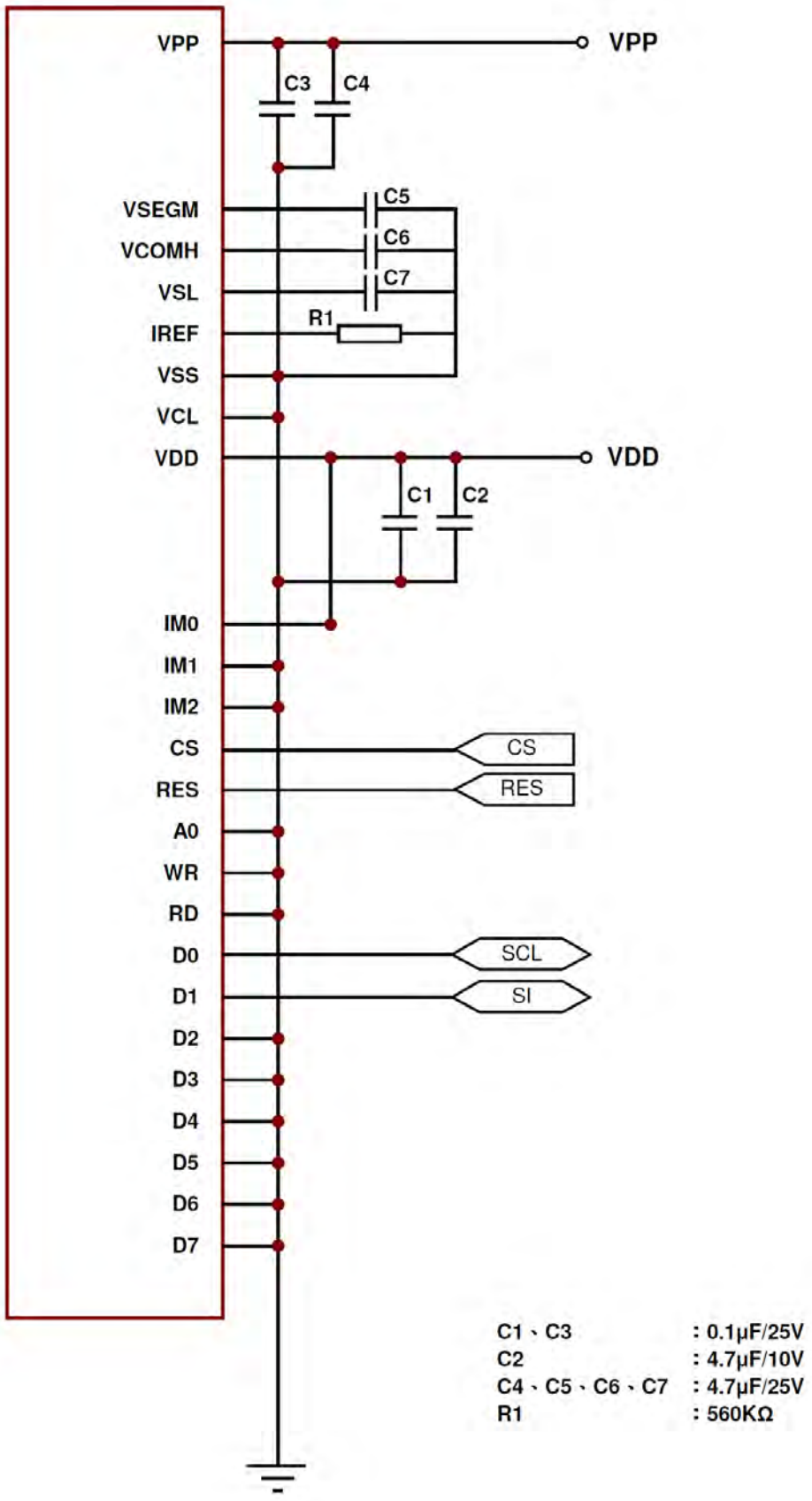
4.4.2 8080-Series MPU Parallel Interface



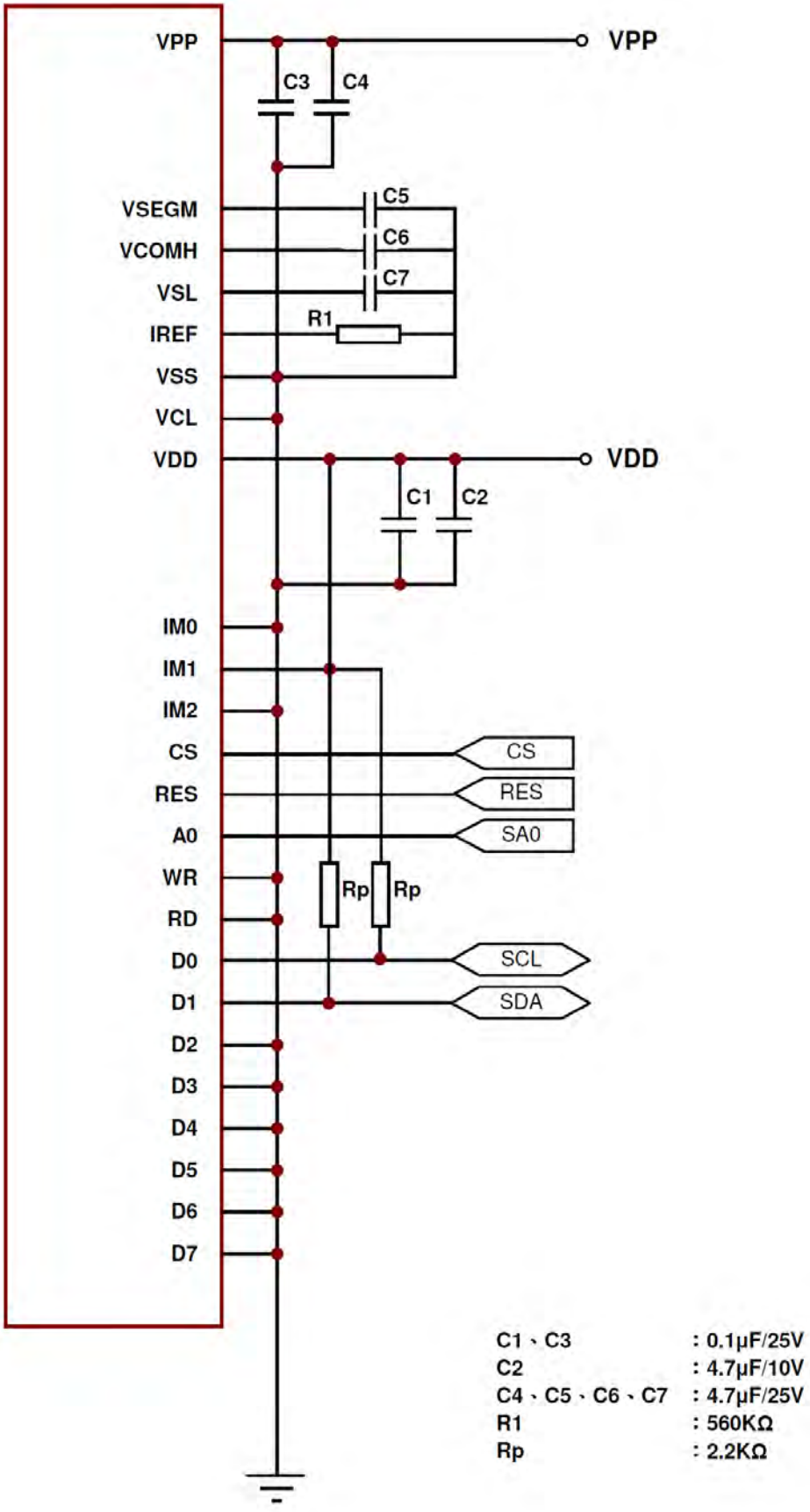
4.4.3 4wire SPI



4.4.4 3wire SPI



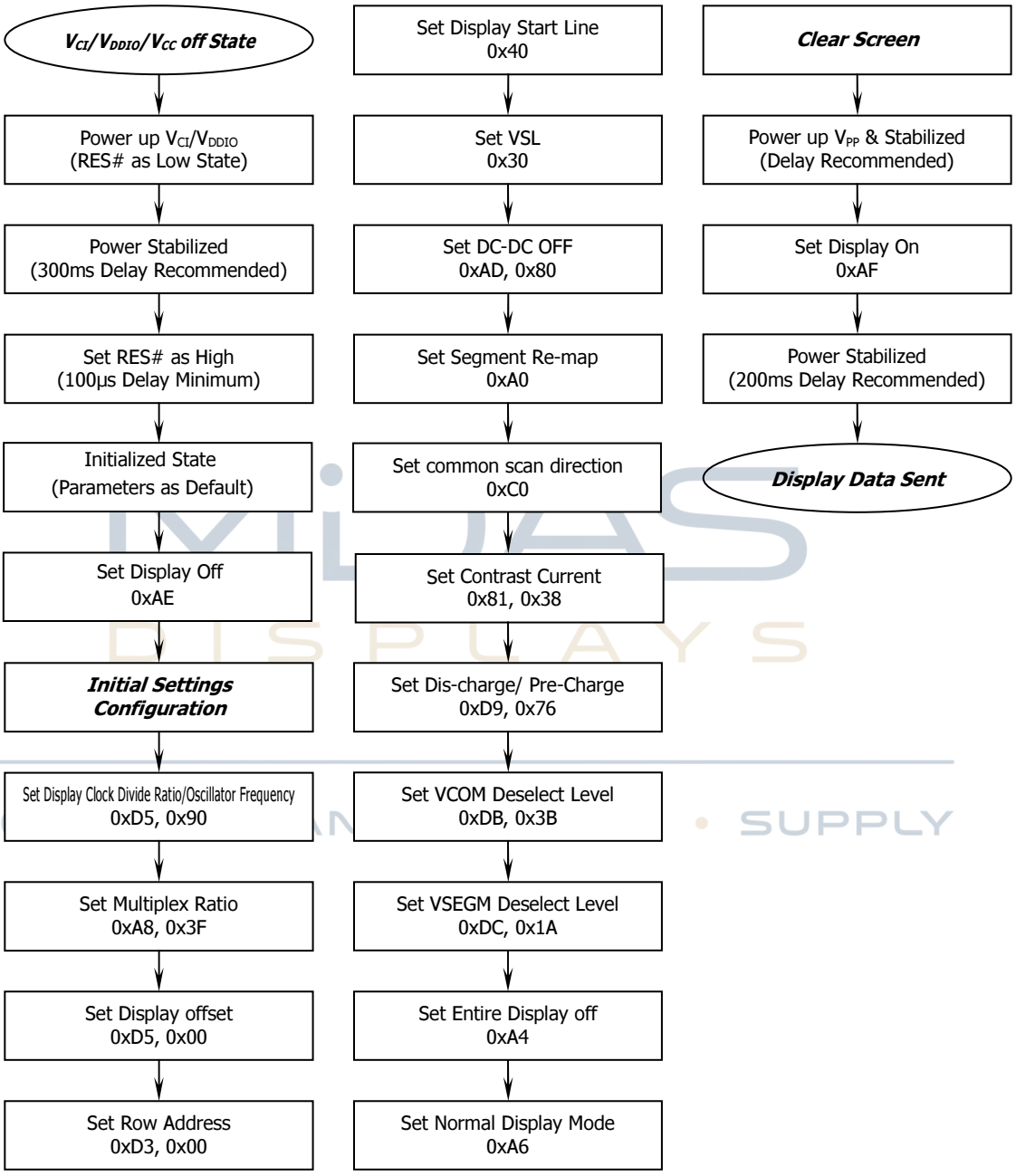
4.4.5 I^2C interface



4.5 Actual Application Example

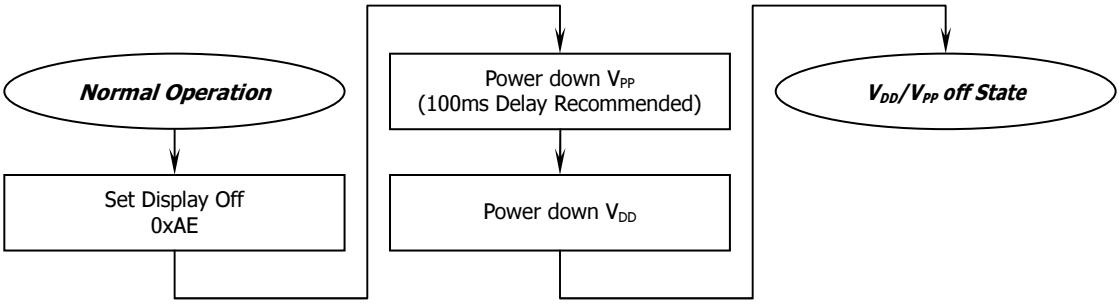
Command usage and explanation of an actual example

<Power up Sequence>

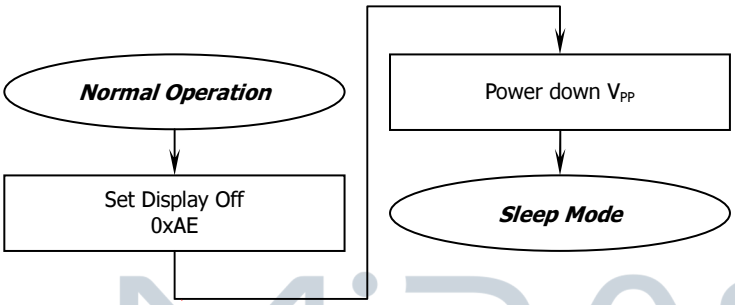


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>