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MCOT128032CY-WS	128 x 32	OLED Module
Specification		
Version: 1	Date: 10/12/2016	
Revision		
1	07/12/2016	First Issue

Display Features			
Resolution	128 x 32		
Appearance	White on Black		
Logic Voltage	2.8V		
Interface	SPI		
Module Size	48.00 x 11.50 x 1.40mm		
Operating Temperature	-40°C ~ +80°C	Box Quantity	Weight / Display
Construction	COT	---	---

RoHS compliant

* - For full design functionality, please use this specification in conjunction with the SSD1306 specification. (Provided Separately)

Display Accessories	
Part Number	**Description**

Optional Variants	
Appearance	**Voltage**

Basic Specifications

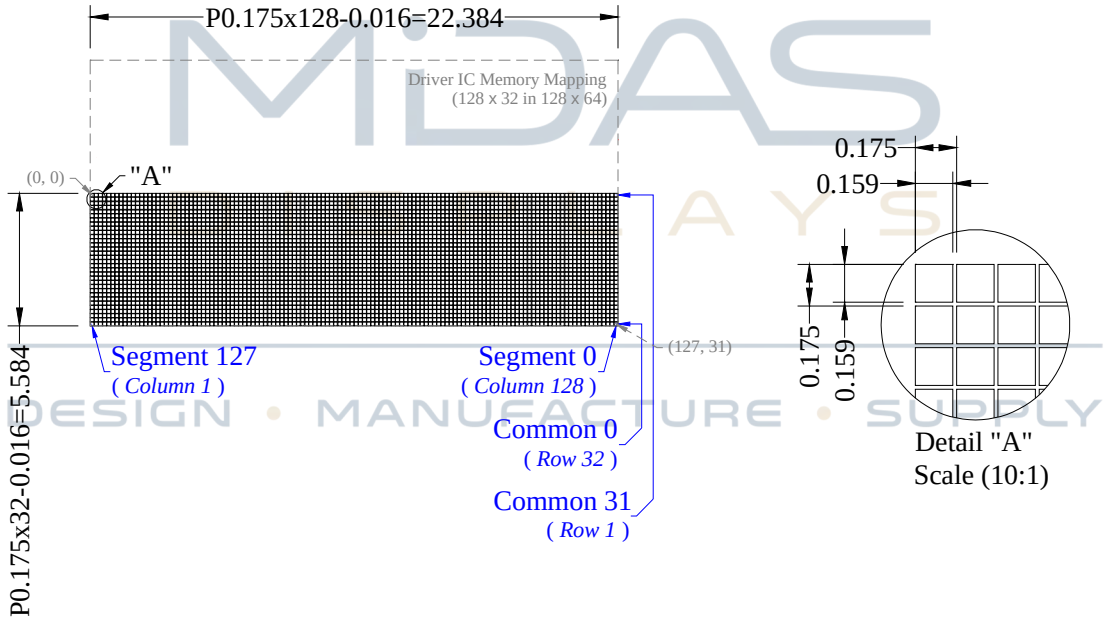
Display Specifications

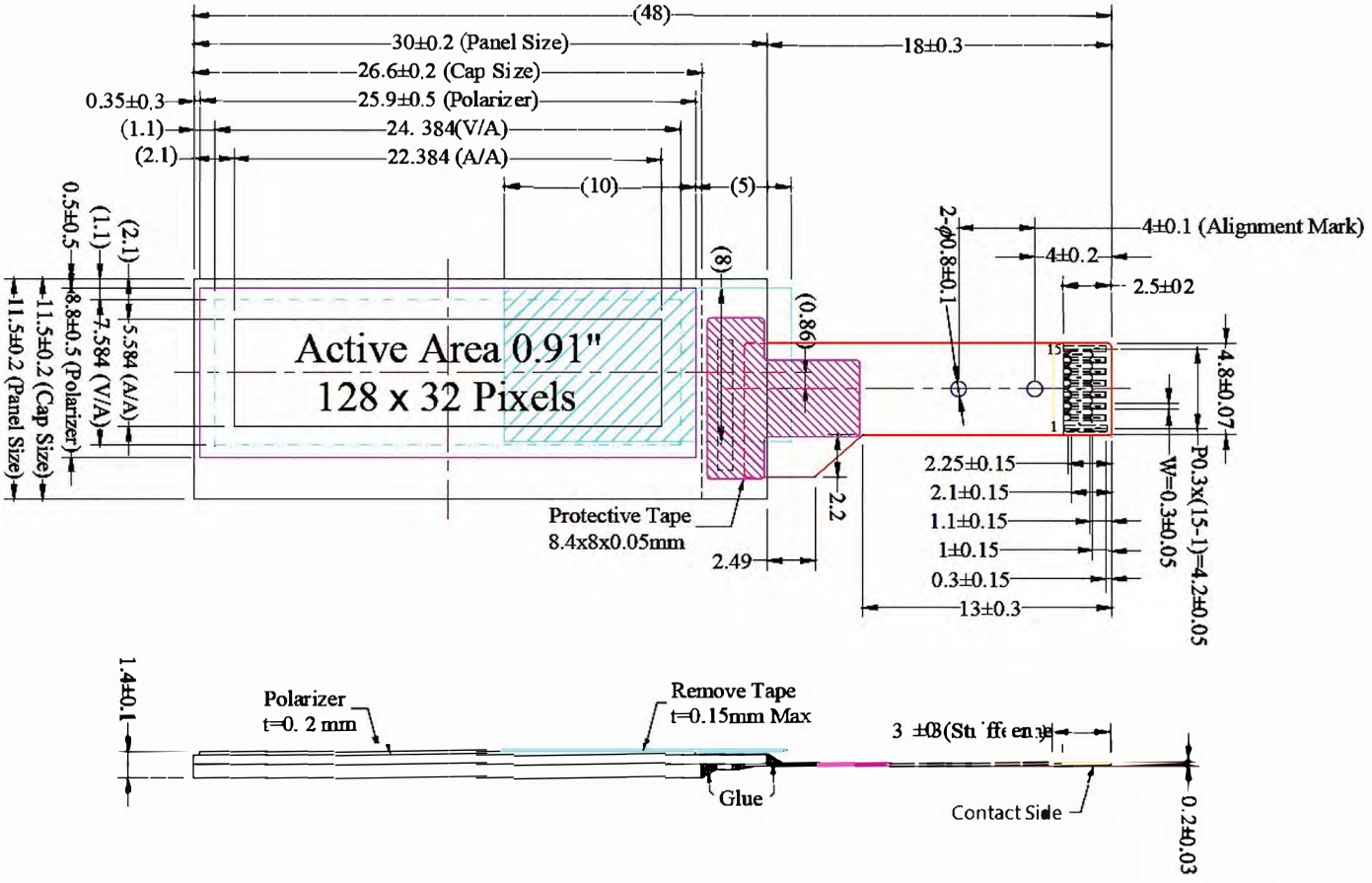
1) Display Mode : Passive Matrix
2) Display Color : Monochrome (white)
3) Drive Duty : 1/32 Duty

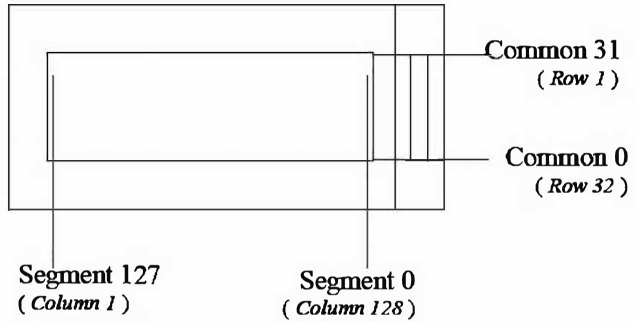
Mechanical Specifications

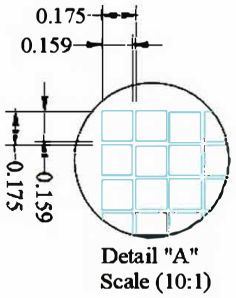
1) Outline Drawing : According to the annexed outline drawing
2) Number of Pixels : 128 × 32
3) Module Size : 48.00 × 11.50 × 1.40 (mm)
4) Panel Size : 30.00 × 11.50 × 1.40 (mm) including "Anti-Glare polarizer"
5) Active Area : 22.384 × 5.584 (mm)
6) Pixel Pitch : 0.175 × 0.175 (mm)
7) Pixel Size : 0.159 × 0.159 (mm)
8) Weight : TBD (g) ± 10%

Active Area / Memory Mapping & Pixel Construction









Pin	Symbol
1	C2P
2	C2N
3	C1P
4	C1N
5	VDDB
6	VSS
7	VDD
8	CS#
9	RES#
10	D/C#
11	D0(SCLK)
12	D1(SDIN)
13	IREF
14	VCOMH
15	VCC

Notes:

1. Color:
2. Driver IC: SSD1306
3. Connector : HIROSE(HRS) FH26-15S-0.3SHW(05) Farnell : 2427760 or Equivalent)
4. Interface: 4-wire SPI
5. General Tolerance: ±0.30
6. The total thickness (1.5 Max) is without polarizer protective film & remove tape.
   The actual assembled total thickness with above materials should be 1.75 Max.

Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
6	VSS	P	**Ground of OEL System** This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.
7	VDD	P	**Power Supply for Logic** This is a voltage supply pin. It must be connected to external source.
15	VCC	P	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and V_{SS} when the converter is used. It must be connected to external source when the converter is not used.
Driver			
13	IREF	I	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 12.5μA maximum.
14	VCOMH	O	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V_{SS}.
DC/DC Converter			
1 / 2 3 / 4	C2P / C2N C1P / C1N	I	**Positive Terminal of the Flying Inverting Capacitor** **Negative Terminal of the Flying Boost Capacitor** The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.
5	VDDB	P	**Power Supply for DC/DC Converter Circuit** This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to V_{DD} when the converter is not used.
Interface			
8	CS#	I	**Chip Select** This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
9	RES#	I	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed.
10	D/C#	I	**Data/Command Control** This pin is Data/Command control pin. When the pin is pulled high, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
11	SCLK	I	**Serial Clock Input Signal** The transmission of information in the bus is following a clock signal. Each transmission of data bit is taken place during a single clock period of this pin.
12	SDIN	I	**Serial Data Input Signal** This pin acts as a communication channel. The input data through SDIN are latched at the rising edge of SCLK in the sequence of MSB first and converted to 8-bit parallel data and handled at the rising edge of last serial clock. SDIN is identified to display data or command by D/C# bit data at the rising of first SCLK.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	0	11	V	1, 2
Supply Voltage for DC/DC	V_{DDB}	-0.3	5	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	
Storage Temperature	T_{STG}	-40	85	°C	3
Lifetime (70 nits) (Typ)	30K			hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: End of lifetime is specified as 50% of initial brightness reached. The reference average operation life time at room temperature is estimated by the accelerated at high temperature conditions.

Optics & Electrical Characteristics

Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 5	120	150	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.27	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 7.5V.
Software configuration follows Section 4.5 Initialization.

DC Characteristics

V_{CC} Supplied Externally

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	V_{CC}	Note 5 (Internal DC/DC Disable)	7.0	7.5	8.0	V
High Level Input	V_{IH}		$0.8\times V_{DD}$	-	V_{DD}	V
Low Level Input	V_{IL}		0	-	$0.2\times V_{DD}$	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	$0.9\times V_{DD}$	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	$0.1\times V_{DD}$	V
Operating Current for V_{DD}	I_{DD}		-	180	300	μA
Operating Current for V_{CC} (V_{CC} Supplied Externally)	I_{CC}	Note 6	-	2.8	3.5	mA
		Note 7	-	4.4	5.5	mA
		Note 8	-	8.2	10.3	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	2	10	μA

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 6: V_{DD} = 2.8V, V_{CC} = 7.5V, 30% Display Area Turn on.
Note 7: V_{DD} = 2.8V, V_{CC} = 7.5V, 50% Display Area Turn on.
Note 8: V_{DD} = 2.8V, V_{CC} = 7.5V, 100% Display Area Turn on.

* Software configuration follows Section 4.5.1 Initialization.

3.2.2 V_{CC} Generated by Internal DC/DC Circuit

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for DC/DC	V_{DDB}	Internal DC/DC Enable	3.0	-	4.2	V
Supply Voltage for Display (Generated by Internal DC/DC)	V_{CC}	Note 9 (Internal DC/DC Enable)	7.0	7.5	8.0	V
High Level Input	V_{IH}		0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}		0	-	0.2×V_{DD}	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	0.9×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.1×V_{DD}	V
Operating Current for V_{DD}	I_{DD}		-	180	300	μA
Operating Current for V_{DDB} (V_{CC} Generated by Internal DC/DC)	I_{DDB}	Note 10	-	7.8	9.8	mA
		Note 11	-	12.2	15.3	mA
		Note 12	-	22.1	27.6	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	2	10	μA

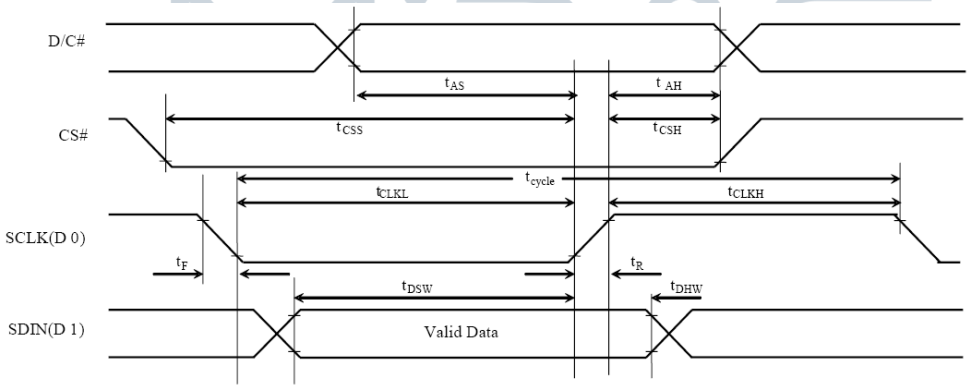
Note 9: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 10: V_{DD} = 2.8V, V_{DDB} = 3.5V, V_{CC} Generated by Internal DC/DC Circuit, 30% Display Area Turn on.
Note 11: V_{DD} = 2.8V, V_{DDB} = 3.5V, V_{CC} Generated by Internal DC/DC Circuit, 50% Display Area Turn on.
Note 12: V_{DD} = 2.8V, V_{DDB} = 3.5V, V_{CC} Generated by Internal DC/DC Circuit, 100% Display Area Turn on.

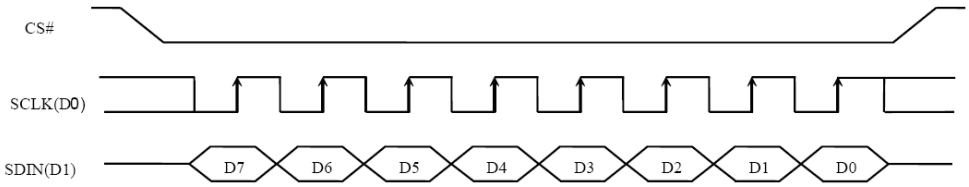
* Software configuration follows Section 4.5.2 Initialization.

AC Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)





Commands

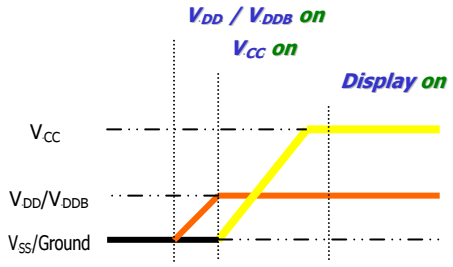
Refer to the Technical Manual for the SSD1306

Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

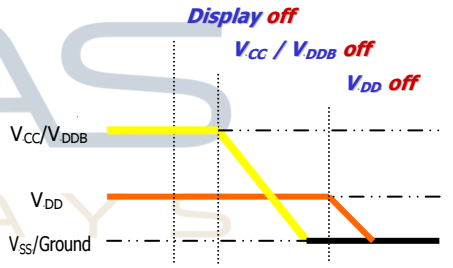
4.2.1 Power up Sequence:

1. Power up V_{DD} / V_{DDB}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC} / V_{DDB}
3. Delay 100ms
   (When V_{CC} / V_{DDB} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 9:

1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} / V_{DDB} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}, V_{DDB}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} / V_{DDB} power down.

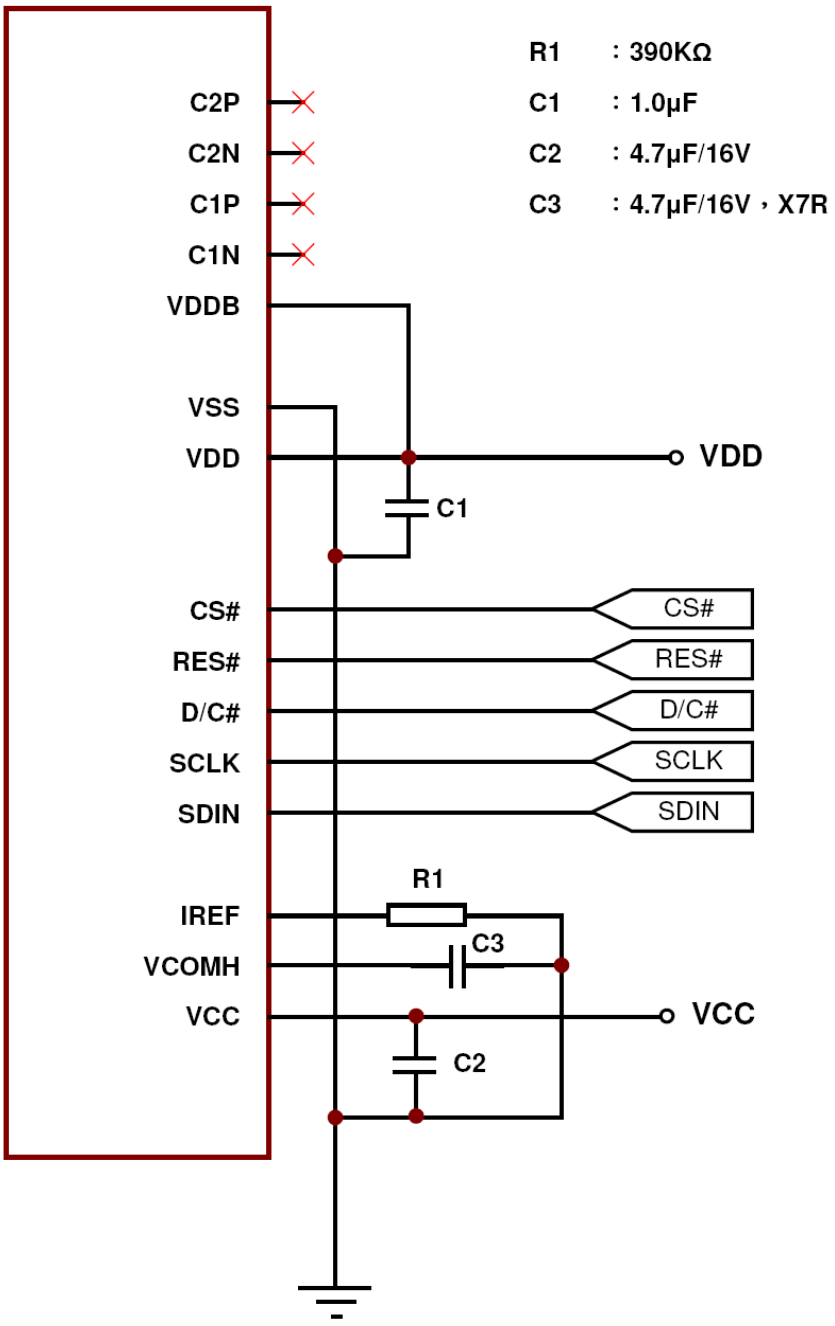
Reset Circuit

When RES# input is low, the chip is initialized with the following status:

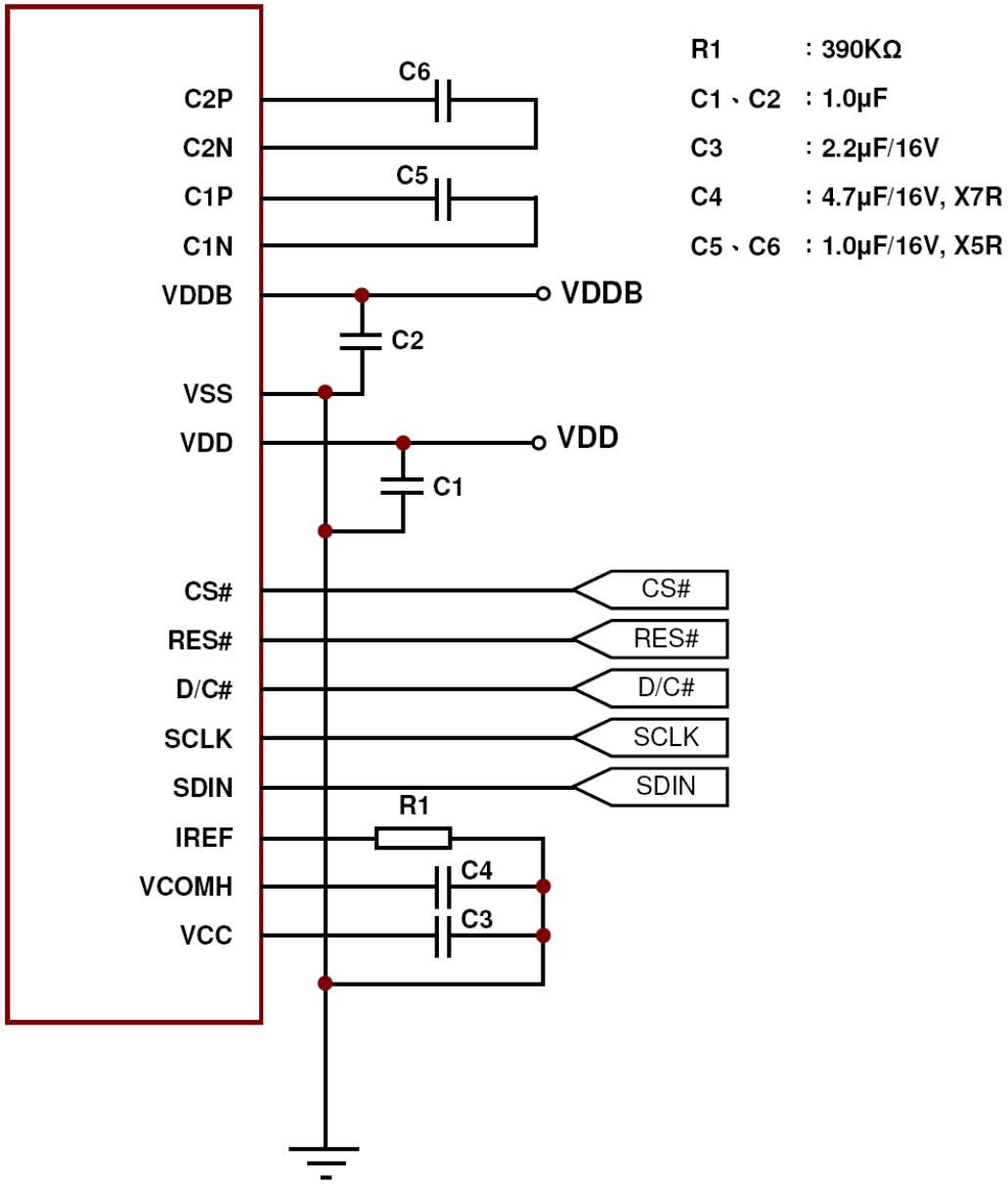
1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

Application Circuit

V_{CC} Supplied Externally



V_{CC} Generated by Internal DC/DC Circuit

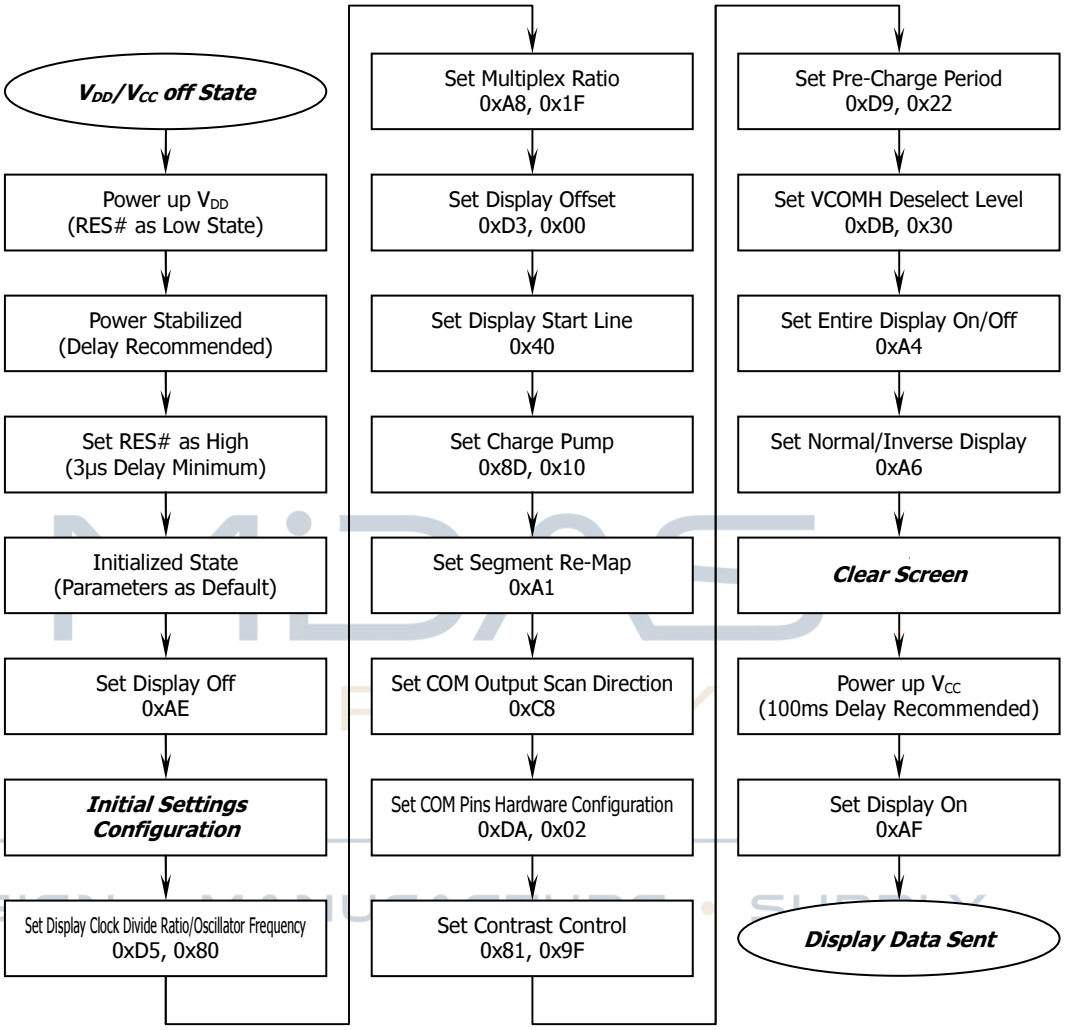


Actual Application Example

Command usage and explanation of an actual example

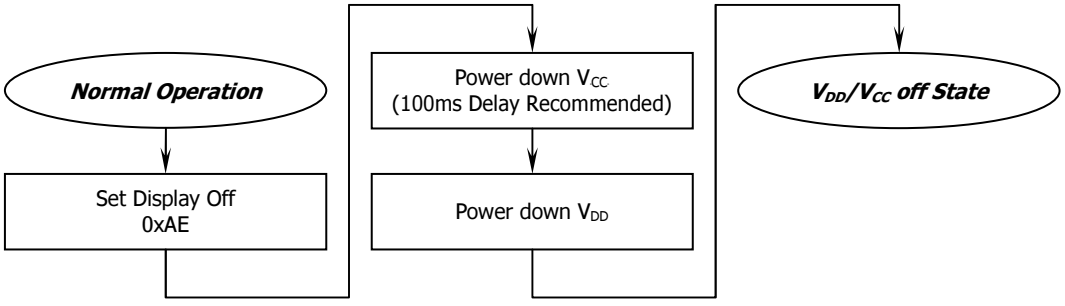
4.5.1 V_{CC} Supplied Externally

<Power up Sequence>

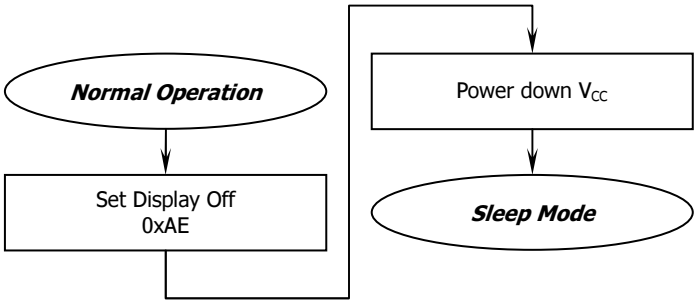


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence>



<Entering Sleep Mode>



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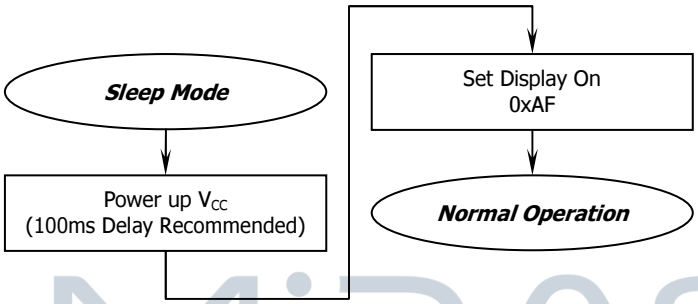
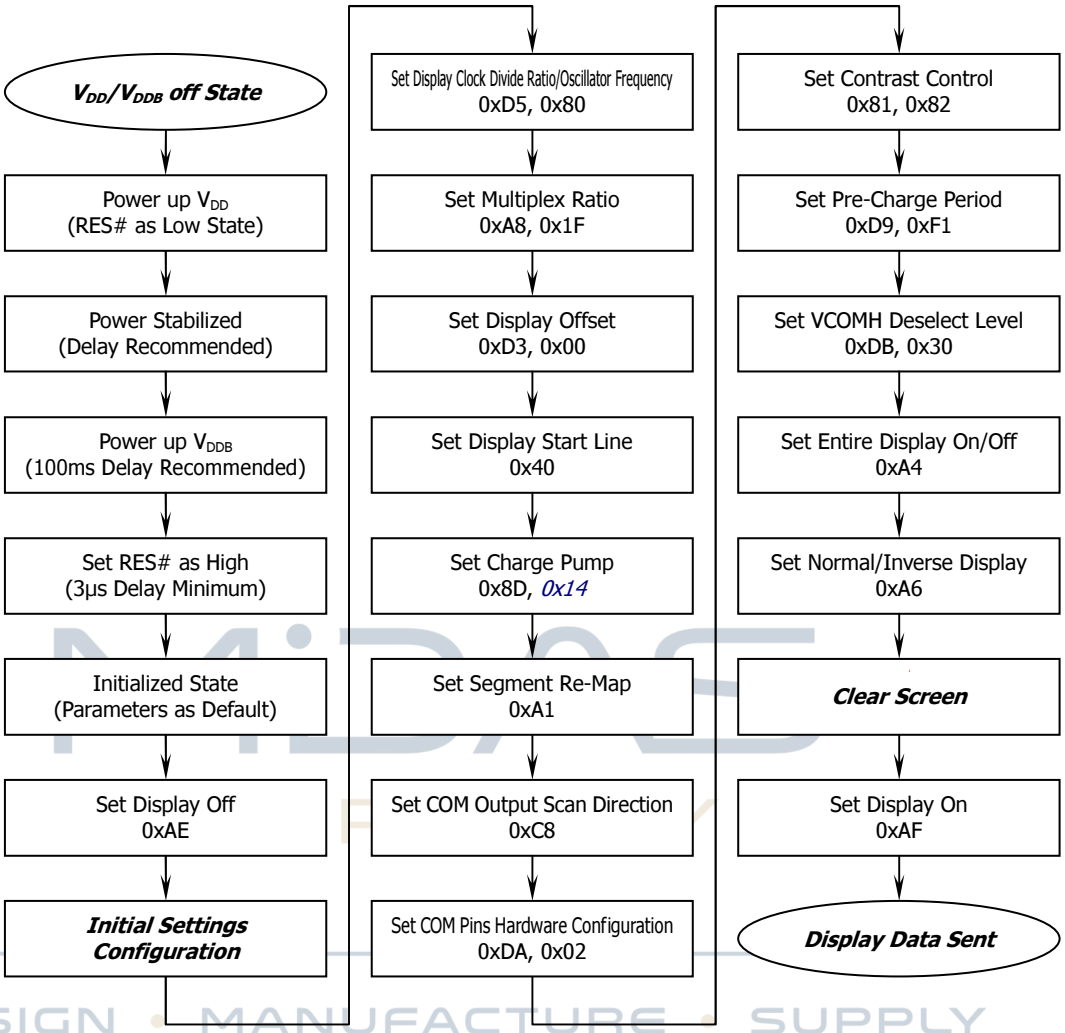


4.5.2 V_{CC} Generated by Internal DC/DC Circuit

<Power up Sequence>



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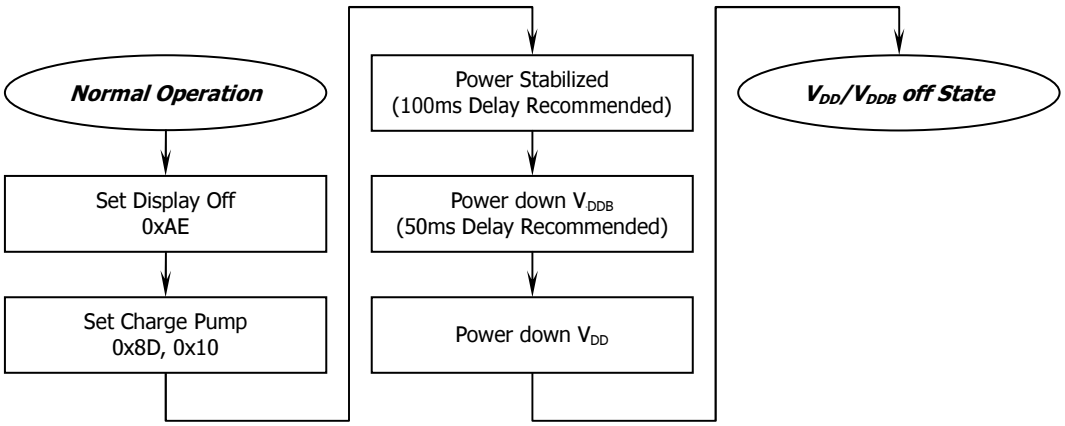
<Power down Sequence>



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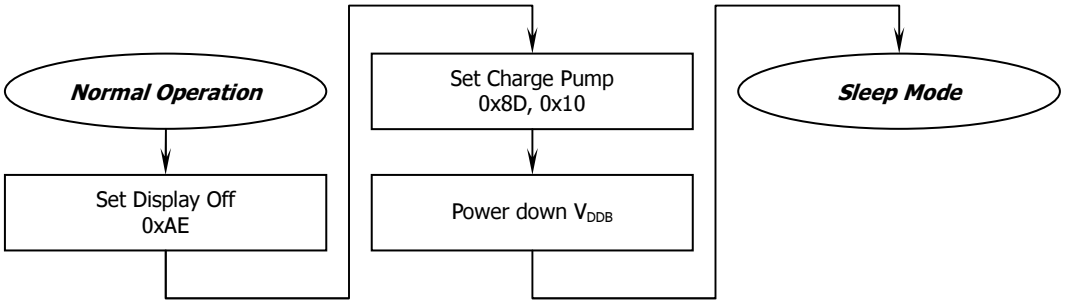

<Exiting Sleep Mode>