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MDOB256064CX-GM	256 x 64	OLED Module
Specification		
Version: 1	Date: 22/04/2016	
Revision		
1	21/04/2016	First Issue

Display Features			
Resolution	256 x 64		
Appearance	Green on Black		
Logic Voltage	3.3V		
Interface	Parallel, SPI		
Module Size	159.33 x 49.80 x 6.30mm		
Operating Temperature	-40°C ~ +80°C	Box Quantity	Weight / Display
Construction	COB	---	---

* - For full design functionality, please use this specification in conjunction with the SSD1322 specification. (Provided Separately)

Display Accessories	
Part Number	**Description**

Optional Variants	
Appearance	**Voltage**

FUNCTIONS & FEATURES

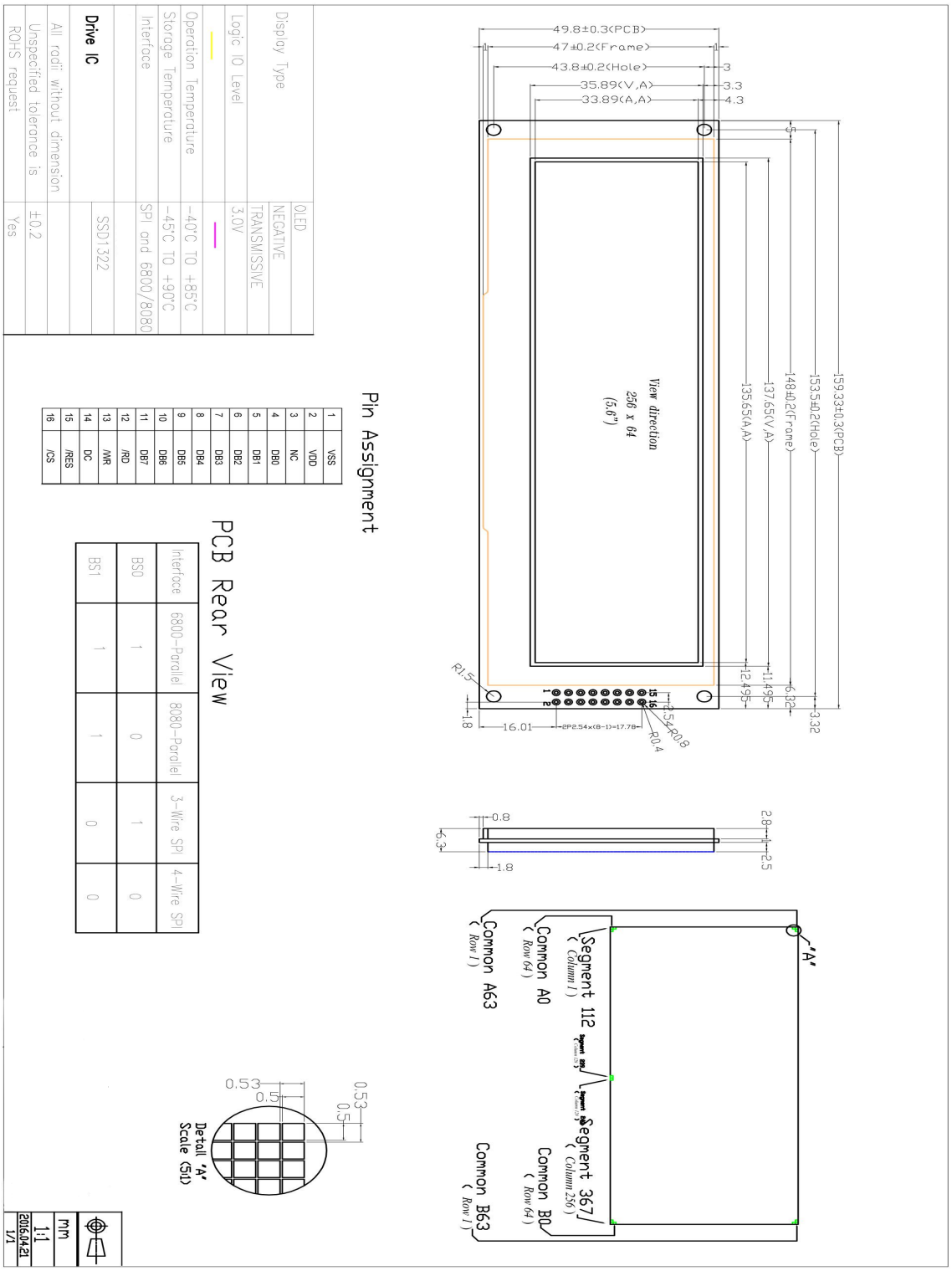
Features

Item	Specs
Display Mode/Colour	Passive Matrix OLED. YELLOW/GREEN
Interface	8-Bit 68XX/80XX Parallel、 SPI
Drive Duty	1/64
Driver IC	SSD1322
Shell	0.5T
Other	- 256X64 dots

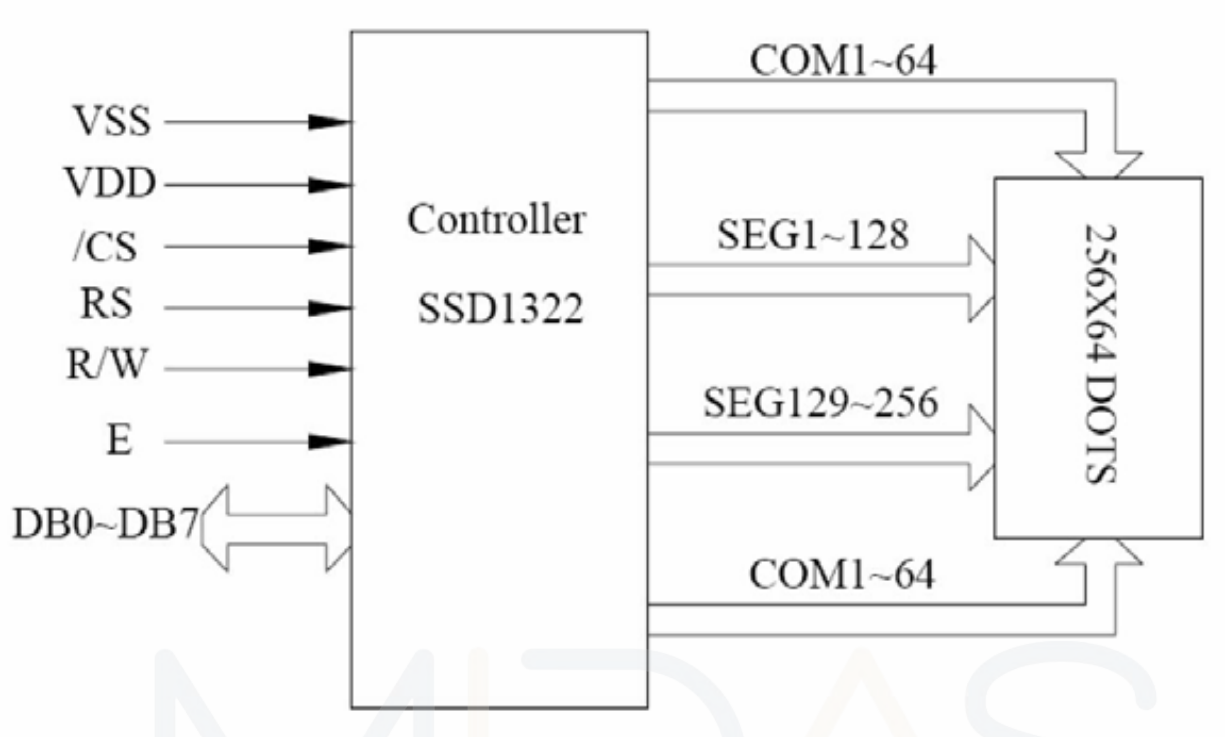
MECHANICAL SPECIFICATIONS

ITEM	SPECIFICATIONS	UNIT
Module Size	159.33L×49. 8W×6. 3H	mm
View Area	137. 65×35. 89	mm
Effective Area	256×64	dots
Pixel Size	0.28×0.28	mm
Pixel Pitch	0.30×0.30	mm

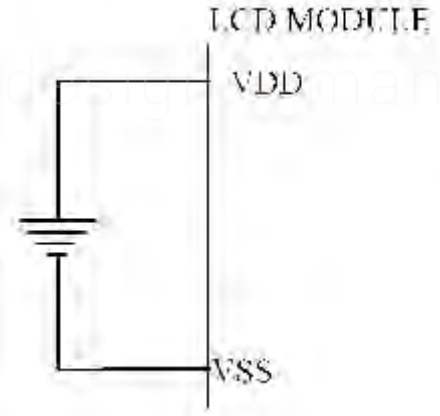
EXTERNAL DIMENSIONS



BLOCK DIAGRAM



5. POWER SUPPLY



6. PIN DESCRIPTION

Parallel Interface(8080): (R18,R21 USE; R19,R20 NO USE)

ITEM	SYMBOL	LEVEL	FUNCTION
1	GND	0V	Power Ground
2	VDD	+3.3~+5.0V	Power Supply For Logic
3	NC	-	No connect
4~11	D0～D7	H/L	Data Bus

12	RD	H/L	8080: Active LOW Read signal
13	WR	H/L	8080:Active LOW Write signal
14	D/C(RS)	H/L	H：Data　L：Command
15	/RST	H/L	Active LOW Reset signal
16	/CS	L	Chip Select

Parallel Interface(6800): (R18,R20 USE; R19,R21 NO USE)

ITEM	SYMBOL	LEVEL	FUNCTION
1	GND	0V	Power Ground
2	VDD	+3.3~+5.0V	Power Supply For Logic
3	NC	-	No connect
4~11	D0～D7	H/L	Data Bus
12	RD	H/L	6800:Operation enable signal. Falling edge triggered.
13	WR	H/L	6800:Read/Write select signal, R/W=1: Read R/W: =0: Write
14	D/C(RS)	H/L	H：Data　L：Command
15	/RST	H/L	Active LOW Reset signal
16	/CS	L	Chip Select

4-SPI: (R19,R21 USE; R18,R20 NO USE)

ITEM	SYMBOL	LEVEL	FUNCTION
1	GND	0V	Power Ground
2	VDD	+3.3~+5.0V	Power Supply For Logic
3	NC	-	No connect
4	SCLK(D0)	H/L	Serial Clock signal
5	SDIN(D1)	H/L	Serial Data input signal
6	NC(D2)	-	No connect
7~11	D3~D7	0V	Power Ground
12	RD	0V	Power Ground
13	WR	0V	Power Ground
14	D/C(RS)	H/L	H：Data　L：Command
15	/RST	H/L	Active LOW Reset signal
16	/CS	L	Chip Select

3-SPI : (R19,R20 USE; R18,R21 NO USE)

ITEM	SYMBOL	LEVEL	FUNCTION
1	GND	0V	Power Ground
2	VDD	+3.3~+5.0V	Power Supply For Logic
3	NC	-	No connect

4	SCLK(D0)	H/L	Serial Clock signal
5	SDIN(D1)	H/L	Serial Data input signal
6	NC(D2)	-	No connect
7~11	D3~D7	0V	Power Ground
12	RD	0V	Power Ground
13	WR	0V	Power Ground
14	D/C(RS)	0V	Power Ground
15	/RST	H/L	Active LOW Reset signal
16	/CS	L	Chip Select

MCU Interface assignment under different bus interface mode:

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	Tie LOW	RES#
4-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#

7 . Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	Vdd	3.3	5	V	1, 2
Supply Voltage for Display	Vcc	0	15	V	1, 2
Operating Temperature	Top	-40	85	℃	-
Storage Temperature	Tst	-45	90	℃	-

Note 1: All the above voltages are on the basis of "VSS = 0V".
Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

8 . ELECTRICAL CHARACTERISTICS

Items	Symbol	Condition	Min	TY	Max	Unit

				P		
Operating Temperature Range	Top	Absolute Max	-40	—	+85	C
Storage Temperature Range	Tst	Absolute Max	-45	—	+90	C
Supply Voltage	Vdd		2.8	3.0	3.3	V
Supply Current (logic)	Idd	Ta=25°C, VDD=3.3V	—	180	300	µA
Supply Current (display)	ICC	50% ON, VDD=3.3V	—	62	70	mA
		100% ON, VDD=3.3V	—	113	120	mA
Sleep Mode Current	IDD+ICCS LEEP		—	3	15	µA
“H” Level input	Vih		0.8*VDD	—	VDD	V
“L” Level input	Vil		VSS	—	0.2*VDD	V
“H” Level output	Voh		0.9*VDD	—	VDD	V
“L” Level output	Vol		VSS	—	0.1*VDD	V

9 . Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing Angle – Top	AV		—	80	—	
Viewing Angle – Bottom	AV		—	80	—	
Viewing Angle – Left	AH		—	80	—	
Viewing Angle – Right	AH		—	80	—	
Contrast Ratio	Cr		2000:1	—	—	—
Response Time (rise)	Tr	—	—	10	—	us
Response Time (fall)	Tf	—	—	10	—	us
Brightness		50% checkerboard	100	120	—	cd/m2
Lifetime		Ta=25°C, 50% checkerboard	10,000	—	—	Hrs

Note: Lifetime at typical temperature is based on accelerated high‐temperature operation. Lifetime is tested at average 50% pixels on and is rated as Hours until Half‐Brightness. The Display OFF command can be used to extend the lifetime of the display.

Luminance of active pixels will degrade faster than inactive pixels. Residual (burn‐in) images may occur. To avoid this, every pixel should be illuminated uniformly.

10. COMMAND TABLE

Built - in SSD1322 controller.

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	00	0	0	0	0	0	0	0	0	Enable Gray Scale table	This command is sent to enable the Gray Scale table setting (command B8h)
0 1 1	15 A[6:0] B[6:0]	0 * *	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Set Column start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=119] Range from 0 to 119
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	75 A[6:0] B[6:0]	0 * *	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	Set Row start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0 1 1	A0 A[7:0] B[4]	1 0 *	0 0 *	1 A_5 0	0 A_4 B_4	0 0 0	0 A_2 0	0 A_1 0	0 A_0 1	Set Re-map and Dual COM Line mode	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Disable Column Address Re-map [reset] A[1]=1b, Enable Column Address Re-map A[2]=0b, Disable Nibble Re-map [reset] A[2]=1b, Enable Nibble Re-map A[4]=0b, Scan from COM0 to COM[N –1] [reset] A[4]=1b, Scan from COM[N-1] to COM0, where N is the Multiplex ratio A[5]=0b, Disable COM Split Odd Even [reset] A[5]=1b, Enable COM Split Odd Even B[4], Enable / disable Dual COM Line mode 0b, Disable Dual COM mode [reset] 1b, Enable Dual COM mode (MUX ≤ 63) **Note** (1) COM Split Odd Even mode must be disabled (A[5]=0b) when enabling the Dual COM mode (B[4]=1b) Details refer to Section 10.1.6
0 1	A1 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set display RAM display start line register from 0-127 Display start line register is reset to 00h after RESET

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 1	A2 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical scroll by COM from 0-127 The value is reset to 00H after RESET
0	A4~A7	1	0	1	0	0	X_2	X_1	X_0	Set Display Mode	A4h = Entire Display OFF, all pixels turns OFF in GS level 0 A5h = Entire Display ON, all pixels turns ON in GS level 15 A6h = Normal Display [reset] A7h = Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13, …)
0 1 1	A8 A[6:0] B[6:0]	1 0 0	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	1 A_3 B_3	0 A_2 B_2	0 A_1 B_1	0 A_0 B_0	Enable Partial Display	This command turns ON partial mode. The partial mode display area is defined by the following two parameters, A[6:0]: Address of start row in the display area B[6:0]: Address of end row in the display area, where B[6:0] must be ≥ A[6:0]
0	A9	1	0	1	0	1	0	0	1	Exit Partial Display	This command is sent to exit the Partial Display mode
0 1	AB A[0]	1 0	0 0	1 0	0 0	1 0	0 0	1 0	1 A_0	Function Selection	A[0]=0b, Select external V_{DD} A[0]=1b, Enable internal V_{DD} regulator [reset]
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Sleep mode ON/OFF	AEh = Sleep mode ON (Display OFF) AFh = Sleep mode OFF (Display ON)
0 1	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Phase Length	A[3:0] Phase 1 period (reset phase length) of 5~31 DCLK(s) clocks as follow: A[3:0] / Phase 1 period 0000 / invalid 0001 / invalid 0010 / 5 DCLKs 0011 / 7 DCLKs 0100 / 9 DCLKs [reset] : / : 1111 / 31 DCLKs A[7:4] Phase 2 period (first pre-charge phase length) of 3~15 DCLK(s) clocks as follow: A[7:4] / Phase 2 period 0000 / invalid 0001 / invalid 0010 / invalid 0011 / 3 DCLKs : / : 0111 / 7 DCLKs [reset] : / : 1111 / 15 DCLKs

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D2</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
1</td><td>B3
A[7:0]</td><td>1
A_7</td><td>0
A_6</td><td>1
A_5</td><td>1
A_4</td><td>0
A_3</td><td>0
A_2</td><td>1
A_1</td><td>1
A_0</td><td>Set Front Clock Divider / Oscillator Frequency</td><td>A[3:0] [reset=0], divide by DIVSET where
<table><tr><th>A[3:0]</th><th>DIVSET</th></tr><tr><td>0000</td><td>divide by 1</td></tr><tr><td>0001</td><td>divide by 2</td></tr><tr><td>0010</td><td>divide by 4</td></tr><tr><td>0011</td><td>divide by 8</td></tr><tr><td>0100</td><td>divide by 16</td></tr><tr><td>0101</td><td>divide by 32</td></tr><tr><td>0110</td><td>divide by 64</td></tr><tr><td>0111</td><td>divide by 128</td></tr><tr><td>1000</td><td>divide by 256</td></tr><tr><td>1001</td><td>divide by 512</td></tr><tr><td>1010</td><td>divide by 1024</td></tr><tr><td>>=1011</td><td>invalid</td></tr></table>
A[7:4] Oscillator frequency, frequency increases as level increases [reset=0101b]</td></tr>
<tr><td>0
1
1</td><td>B4
A[1:0]
B[7:3]</td><td>1
1
B_7</td><td>0
0
B_6</td><td>1
1
B_5</td><td>1
0
B_4</td><td>0
0
B_3</td><td>1
0
1</td><td>0
A_1
0</td><td>0
A_0
1</td><td>Display Enhancement A</td><td>A[1:0] = 00b: Enable external VSL
A[1:0] = 10b: Internal VSL [reset]

B[7:3] = 11111b: Enhanced low GS display quality
B[7:3] = 10110b: Normal [reset]</td></tr>
<tr><td>0
1</td><td>B5
A[3:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>0
A_3</td><td>1
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set GPIO</td><td>A[1:0] GPIO0: 00 pin HiZ, Input disabled
01 pin HiZ, Input enabled
10 pin output LOW [reset]
11 pin output HIGH

A[3:2] GPIO1: 00 pin HiZ, Input disabled
01 pin HiZ, Input enabled
10 pin output LOW [reset]
11 pin output HIGH</td></tr>
<tr><td>0
1</td><td>B6
A[3:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>0
A_3</td><td>1
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set Second Precharge Period</td><td>A[3:0] Second Pre-charge period
0000b 0 dclk
0001b 1 dclk
.....
1000b 8 dclks [reset]
.....
1111b 15 dclks</td></tr>
</table>

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next 15 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d) A1[7:0]: Gamma Setting for GS1, A2[7:0]: Gamma Setting for GS2, : A14[7:0]: Gamma Setting for GS14, A15[7:0]: Gamma Setting for GS15 **Note** (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS14 < Setting of GS15 Refer to Section 8.8 for details (2) The setting must be followed by the Enable Gray Scale Table command (00h)
1	A1[7:0]	$A1_7$	$A1_6$	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
1	A2[7:0]	$A2_7$	$A2_6$	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	A14[7:0]	$A14_7$	$A14_6$	$A14_5$	$A14_4$	$A14_3$	$A14_2$	$A14_1$	$A14_0$		
1	A15[7:0]	$A15_7$	$A15_6$	$A15_5$	$A15_4$	$A15_3$	$A15_2$	$A15_1$	$A15_0$		
0	B9	1	0	1	1	1	0	0	1	Select Default Linear Gray Scale table	The default Linear Gray Scale table is set in unit of DCLK's as follow GS0 level pulse width = 0; GS1 level pulse width = 0; GS2 level pulse width = 8; GS3 level pulse width = 16; : : GS14 level pulse width = 104; GS15 level pulse width = 112 Refer to Section 8.8 for details
0	BB	1	0	1	1	1	0	1	1	Set Pre-charge voltage	Set pre-charge voltage level.[reset = 17h]
1	A[4:0]	*	*	*	A_4	A_3	A_2	A_1	A_0		
0	BE	1	0	1	1	1	1	1	0	Set V_{COMH}	Set COM deselect voltage level [reset = 04h]
1	A[2:0]	*	*	*	*	0	A_2	A_1	A_0		
0	C1	1	1	0	0	0	0	0	1	Set Contrast Current	A[7:0]: Contrast current value, range:00h~FFh, i.e. 256 steps for I_{SEG} current [reset = 7Fh]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

A[4:0]	Hex code	pre-charge voltage
00000	00h	0.20 x V_{CC}
:	:	:
11111	1Fh	0.60 x V_{CC}

A[2:0]	Hex code	V_{COMH}
000	00h	0.72 x V_{CC}
:	:	:
100	04h	0.80 x V_{CC} [reset]
:	:	:
111	07h	0.86 x V_{CC}

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	C7	1	1	0	0	0	1	1	1	Master Contrast Current Control	A[3:0] = 0000b, reduce output currents for all colors to 1/16 0001b, reduce output currents for all colors to 2/16 : 1110b, reduce output currents for all colors to 15/16 1111b, no change [reset]
1	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		
0	CA	1	1	0	0	1	0	1	0	Set MUX Ratio	A[6:0]: Set MUX ratio from 16MUX ~ 128MUX A[6:0] = 15d represents 16MUX : A[6:0] = 127d represents 128MUX [reset]
1	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	D1	1	1	0	1	0	0	0	1	Display Enhancement B	A[5:4] = 00b: Reserved A[5:4] = 10b: Normal [reset]
1	A[5:4]	1	0	A_5	A_4	0	0	1	0		
1	20	0	0	1	0	0	0	0	0		
0	FD	1	1	1	1	1	1	0	1	Set Command Lock	A[2]: MCU protection status [reset = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset] A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command
1	A[2]	0	0	0	1	0	A_2	1	0		

Note
(1) "*" stands for "Don't care".

For detailed instruction information, see SSD1322 datasheet .

11 . MPU Interface

Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-1 : 6800-series MCU parallel interface characteristics

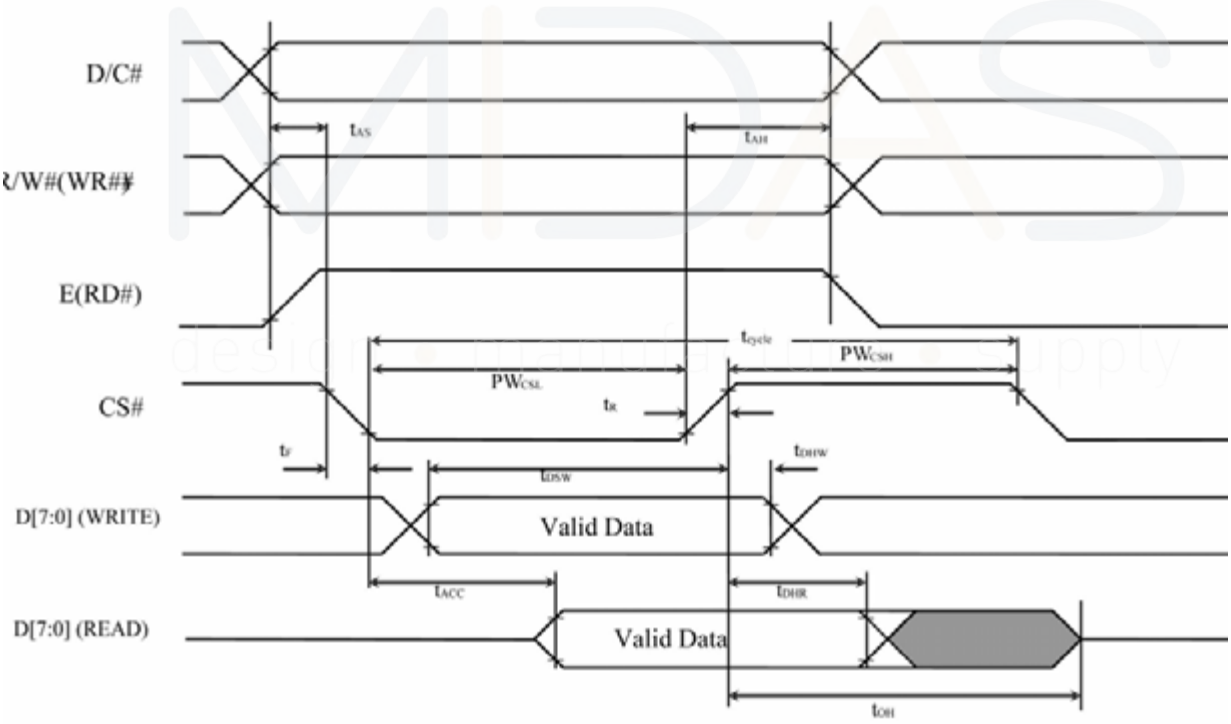


Table 13-3 : 8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 13-2 : 8080-series MCU parallel interface characteristics

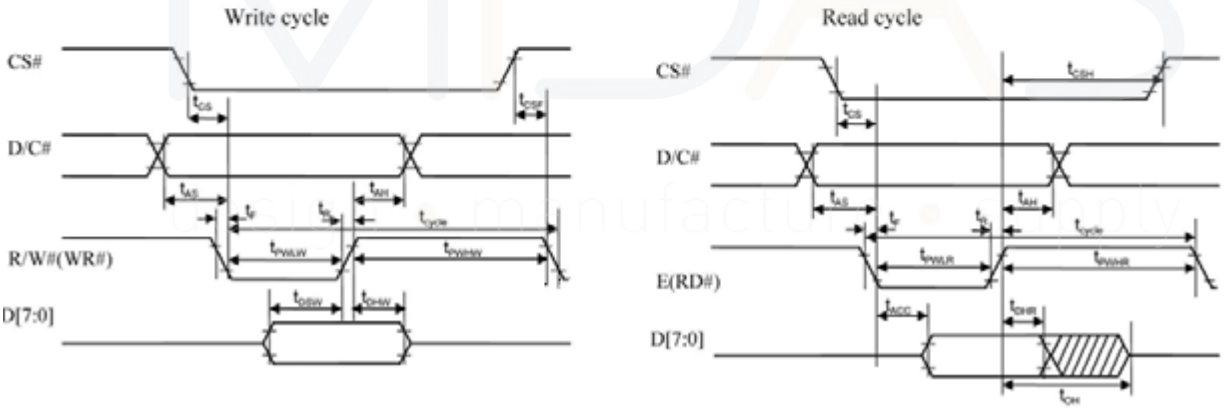


Table 13-4 : Serial Interface Timing Characteristics (4-wire SPI)

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-3 : Serial interface characteristics (4-wire SPI)

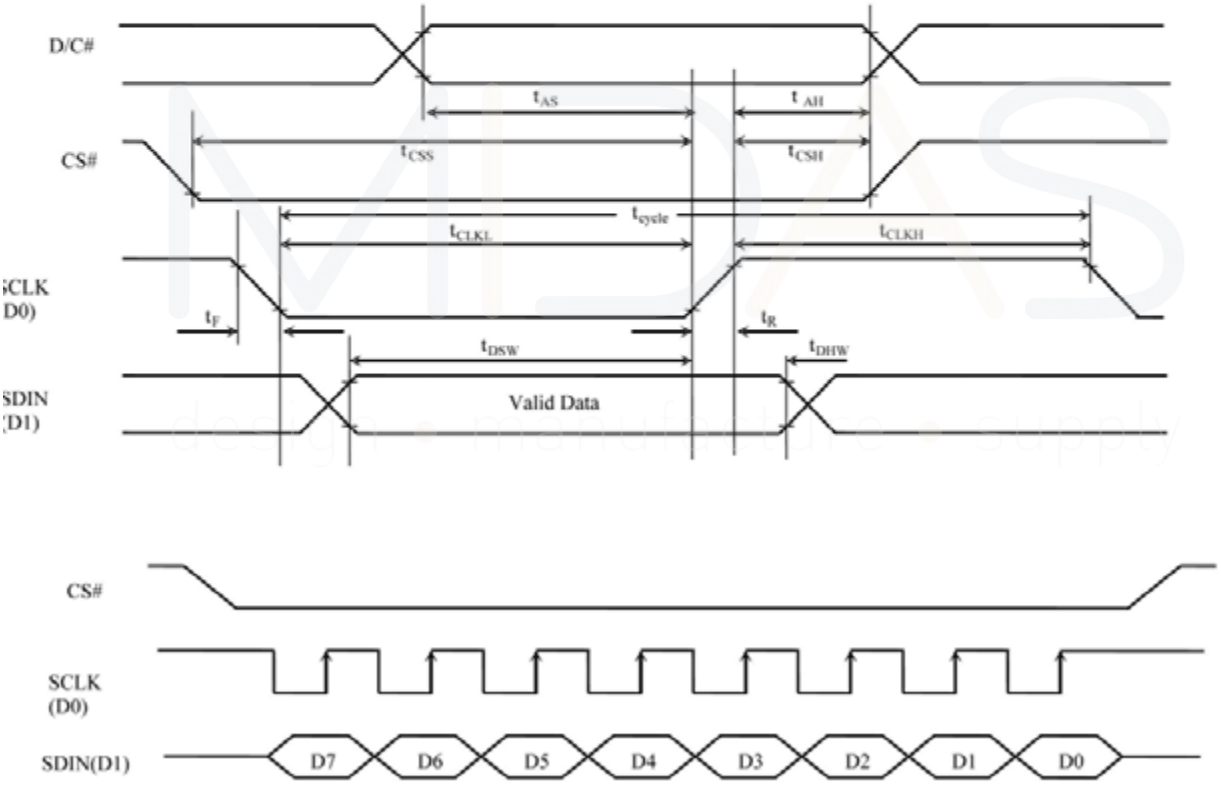
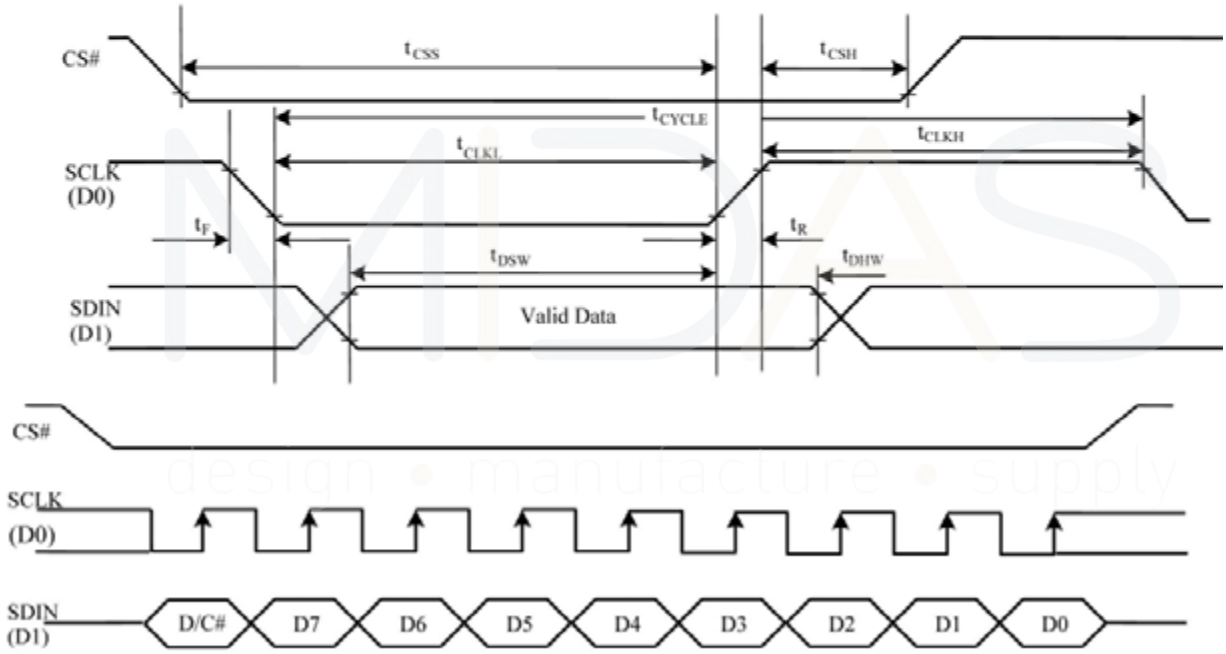


Table 13-5: Serial Interface Timing Characteristics (3-wire SPI)

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-4: Serial interface characteristics (3-wire SPI)



12. GDDRAM

12.1 GDDRAM structure in Gray Scale mode

The GDDRAM address map in Table 8-6 shows the GDDRAM in Gray Scale mode. Since in Gray

Scale mode, there are 16 gray levels. Therefore four bits (one nibble) are allocated for each pixel. For example D30480[3:0] in Table 8-6 corresponds to the pixel located in (COM127, SEG2). So the lower nibble and higher nibble of D0, D1, D2, …, D30717, D30718, D30719 in Table 8-6 represent the 480x128 data nibbles in the GDDRAM.

Table 8-6 : GDDRAM in Gray Scale mode (RESET)

		SEG0	SEG1	SEG2	SEG3		SEG476	SEG477	SEG478	SEG479	SEG Outputs
		00		00			77		77		RAM Column address (HEX)
COM0	00	D1[3:0]	D1[7:4]	D0[3:0]	D0[7:4]		D239[3:0]	D239[7:4]	D238[3:0]	D238[7:4]	
COM1	01	D241[3:0]	D241[7:4]	D240[3:0]	D240[7:4]		D479[3:0]	D479[7:4]	D478[3:0]	D478[7:4]	
|	|									
COM126	7E	D30241[3:0]	D30241[7:4]	D30240[3:0]	D30240[7:4]		D30479[3:0]	D30479[7:4]	D30478[3:0]	D30478[7:4]	
COM127	7F	D30481[3:0]	D30481[7:4]	D30480[3:0]	D30480[7:4]		D30719[3:0]	D30719[7:4]	D30718[3:0]	D30718[7:4]	
COM Outputs	RAM Row Address (HEX)										

Corresponding to one pixel

12.2 Data bus to RAM mapping

Table 8-7 : Data bus usage

Read / Write Data		Data bus D[7:0]							
Bus width	**Input order**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
8 bits	1st	3	3	3	3	2	2	2	2
	2nd	1	1	1	1	0	0	0	0

Corresponding to one pixel

14 . DESIGN AND HANDING PRECAUTION

14.1 The LCD panel is made by glass. Any mechanical shock (eg. Dropping form high place) will damage the LCD module. Do not add excessive force on the surface of the

display, which may cause the Display color change abnormally.

14.2 The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.

14.3 Never attempt to disassemble or rework the LCD module.
14.4 Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
14.5 When mounting the LCD module, make sure that it is free form twisting, warping and distortion.
14.6 Ensure to provide enough space(with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result
14.7 Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
14.8 Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
14.9 LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
14.10 When peeling of the protective film form LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
14.11 Take care and prevent get hurt by the LCD panel edge.
14.12 Never operate the LCD module exceed the absolute maximum ratings.
14.13 Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
14.14 Never apply signal to the LCD module without power supply.
14.15 IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
14.16 LCD module reliability may be reduced by temperature shock.
14.17 When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module