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MDT0240A9IS-MULTI	240 x 320	MULTI Interface	TFT Module

Specification

Version: 1	Date: 30/03/2019

Revision

1	27/03/2019	First issue

Display Features	
Display Size	2.4”
Resolution	240 x 320
Orientation	Portrait
Appearance	RGB
Logic Voltage	2.8V
Interface	MULTI
Brightness	350 cd/m^2
Touchscreen	---
Module Size	42.72 x 60.26 x 2.20mm
Operating Temperature	-20°C ~ +60°C
Pinout	45 way FFC
Pitch	0.3mm

RoHS compliant

Box Quantity	Weight / Display
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* - For full design functionality, please use this specification in conjunction with the ILI9340X specification.(Provided Separately)

Display Accessories

Part Number	Description

Optional Variants

Appearances	Voltage

General Specifications

Feature		Spec
Characteristics	Size	2.4 inch
	Resolution	240(horizontal)*320(Vertical)
	Interface	MCU8/16 bit OR RGB 18bit
	Connect type	Connector
	Display Colors	262K
	Technology type	a-Si
	Pixel pitch (mm)	0.153*0.153
	Pixel Configuration	R.G.B.-Stripe
	Display Mode	Normally Black
	Driver IC	ILI9340X
	Viewing Direction	Full view
Mechanical	LCM (W x H x D) (mm)	42.72*60.26*2.20
	Active Area(mm)	36.72*48.96
	Weight (g)	TBD
	LED Numbers	4 LEDs

Note 1: Requirements on Environmental Protection: RoHs
Note 2: LCM weight tolerance: +/- 5%

Input/Output Terminals

LCD PIN-MAP

PIN NO.	PIN NAME	DESCRIPTION
1	VCI	Power supply.
2	IOVCC	Digital power supply.
3	IM0	<table><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>80 MCU 16-bit bus interface II</td><td>D[8:1]</td><td>D[17:10], D[8:1]</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>80 MCU 8-bit bus interface II</td><td>D[17:10]</td><td>D[17:10]</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 MCU 18-bit bus interface II</td><td>D[8:1]</td><td>D[17:0]</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80 MCU 9-bit bus interface II</td><td>D[17:10]</td><td>D[17:9]</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface II</td><td colspan="2">SDI: In SDO: Out</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface II</td><td colspan="2">SDI: In SDO: Out</td></tr></table>
4	IM3	
5	IM2	
6	IM1	
7	RESET	Reset signal input terminal
8	VSYNC	Vertical Sync signal
9	HSYNC	Horizontal Sync signal
10	DOTCLK	Dot clock signal.
11	ENABLE	Data Enable
12~29	DB17~DB0	DATA BUS.
30	SDO	Serial output data
31	SDI	Serial Input Data.
32	RD	Read signal
33	WR/(D/CX)	8080-I system :Write signal Serial interface: Data or command select.
34	RS/(SCL)	8081-I system :Data or command select. Serial interface:Serial clock signal.
35	CS	Chip select
36	GND	System Ground
37	LEDA	LED Anode.
38	LEDK	LED Cathode.
39	LEDK	LED Cathode.
40	NC	No connection
41	NC	No connection
42	NC	No connection
43	NC	No connection
44	NC	No connection
45	NC	No connection

Absolute Maximum Rating

Driving TFT LCD Panel

Item	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	V_{CC}	2.5	4.6	V	
Input Voltage	IOVCC	1.65	4.6	V	
Operating Temperature	T_{OPR}	-20	60	℃	
Storage Temperature	T_{STG}	-30	70	℃	

Timing characteristics

ELECTRICAL CHARACTERISTICS

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Analog Supply Voltage		V_{CC}	2.5	2.8	3.3	V	
Logic Signal Input /Output Voltage		IOVCC	1.65	1.8	3.3	V	
Input Signal Voltage	Low Level	V_{IL}	VSS	-	0.3x IOVCC	V	
	High Level	V_{IH}	0.7x IOVCC	-	IOVCC	V	
TFT Common Electrode		V_{COMH}	2.5	-	5	V	
TFT Gate ON Voltage		V_{GH}	10	-	16	V	
TFT Gate ON Voltage		V_{GL}	-10	-	-5	V	

LED Driving Conditions

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	20	-	mA	
Forward Voltage	V_F	11.2	12	12.8	V	
Backlight Power consumption	W_{BL}	-	0.24	-	W	
LED Lifetime		-	30000	-	Hrs	

Note 1: Each LED: IF =20 mA, VF =3.2+/0.2V.
Note 2: Optical performance should be evaluated at Ta=25℃ only.
Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life Time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

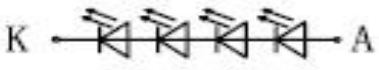
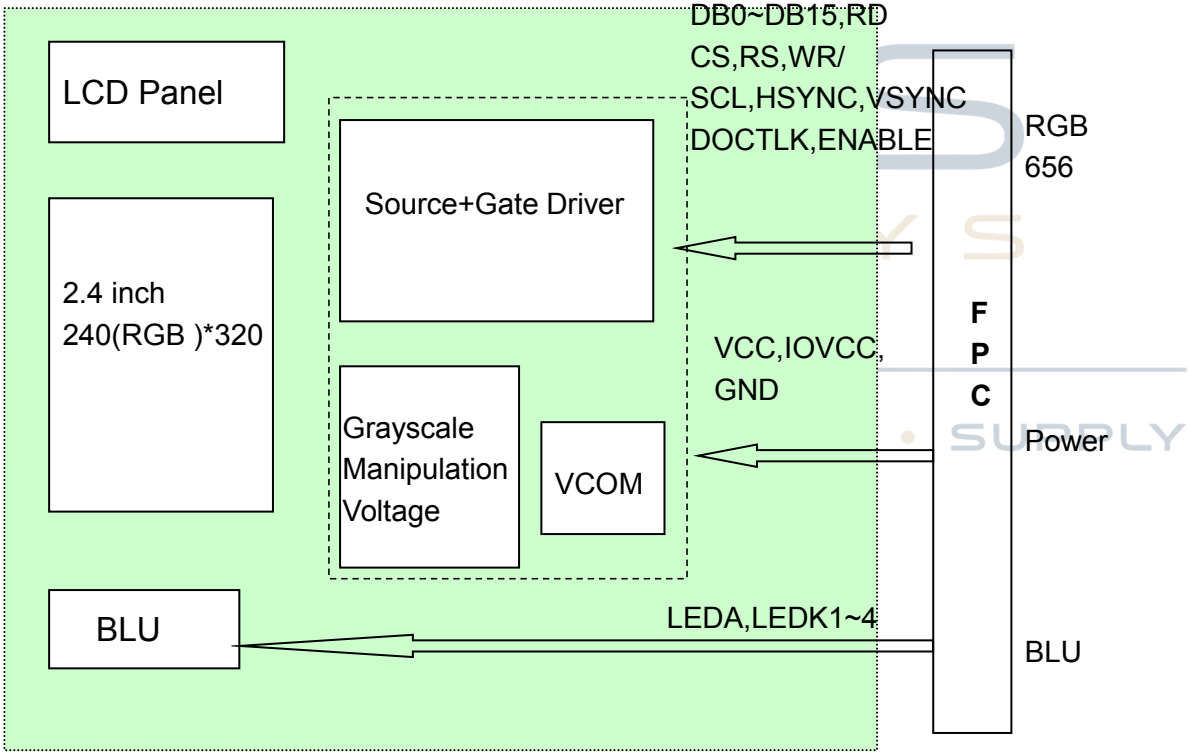


Figure: LED connection of backlight(Constant Current)

Block Diagram



Interface Timing

DC Electrical Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	IOVCC	V	I/O supply voltage	1.65	1.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	15.0	Note3
Gate Driver Low Voltage	VGL	V	-	-12.6	-	-7.0	Note3
Driver Supply Voltage	-	V	|VGH-VGL|	19	-	27.6	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	GND	-	0.3*IOVCC	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	GND	-	0.2*IOVCC	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=IOVCC or GND	-0.1	-	+0.1	Note1,2,3
VCOM Operation							
VCOM Amplitude	VCOMA	V			GND		Note3
Source Driver							
Source Output Range	Vsout	V	-	VREG2OUT	-	VREG1OUT	Note4

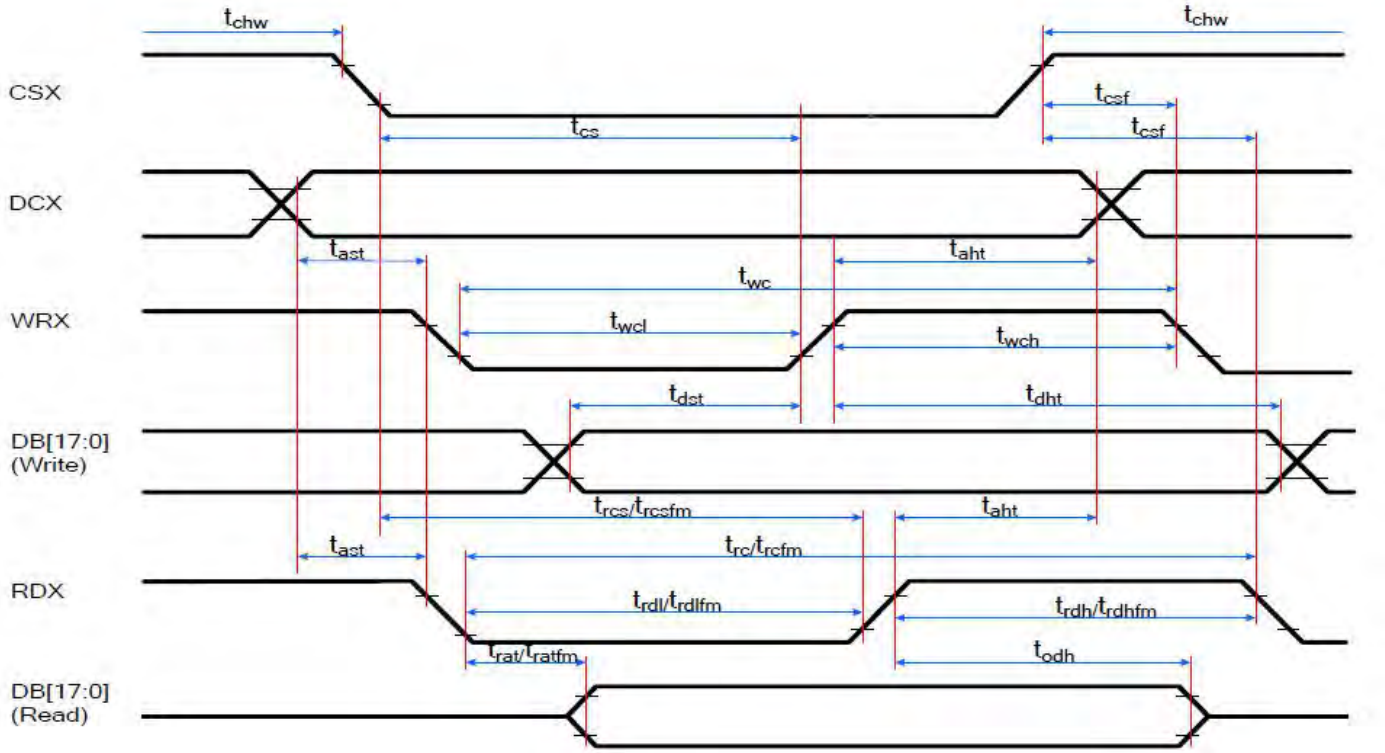
Note 1: IOVCC=1.65 to 3.3V, VCI=2.5 to 3.3V, AGND=GND=0V, Ta=-30 to 80 ℃.

Note2: Please supply digital IOVCC voltage equal or less than analog VCI voltage.

Note3: CSX, RDX, WRX, DB[17:0], DCX, RESX, TE, DOTCLK, VSYNC, HSYNC, ENABLE, SDA, SCL, IM3, IM2, IM1, IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

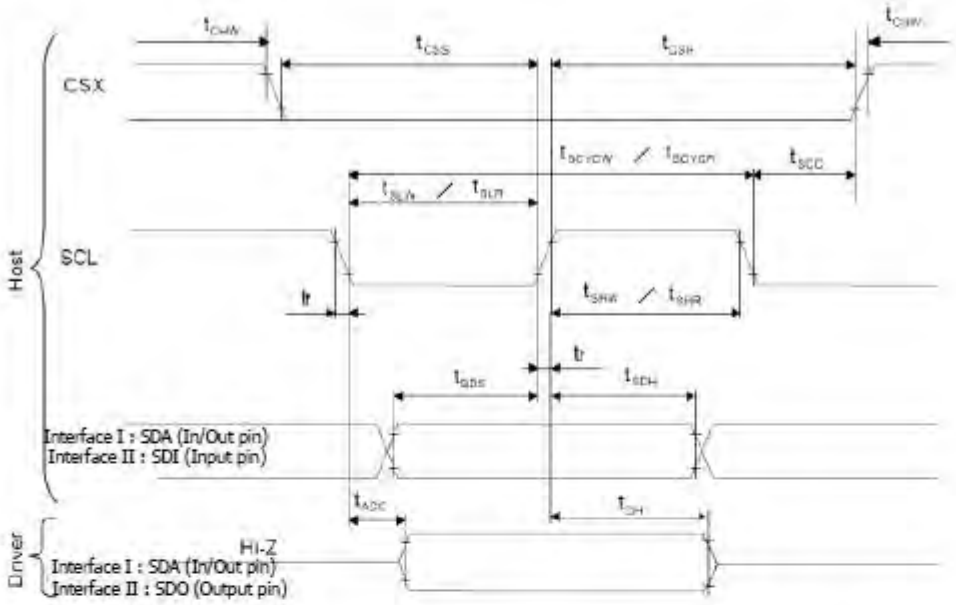
Timing



Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB[17:0],DB[15:0], DB[8:0], DB[7:0] DB[17:10],DB[8:1] DB[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	todh	Read output disable time	20	80	ns	

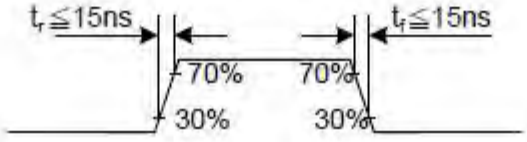
Note: Ta = -30 to 80 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, GND=0V

Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- Ⅰ /Ⅱ system)

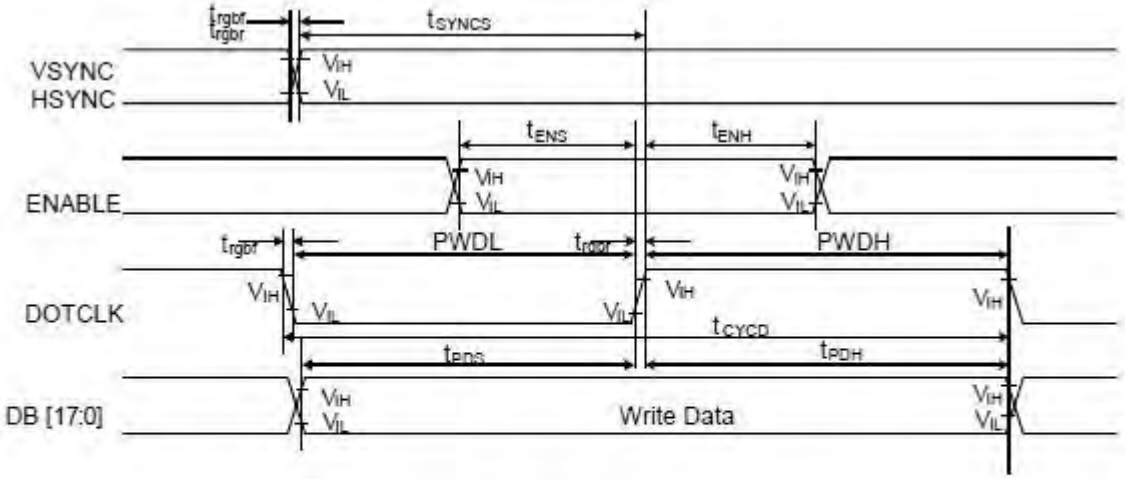


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	t_{SCYCW}	Serial Clock Cycle (Write)	66	-	ns	
	t_{SHW}	SCL "H" Pulse Width (Write)	33	-	ns	
	t_{SLW}	SCL "L" Pulse Width (Write)	33	-	ns	
	t_{SCYCW}	Serial Clock Cycle (Write RGB data)	15	-	ns	MTK-2 lane mode only
	t_{SHW}	SCL "H" Pulse Width (Write RGB data)	4	-	ns	MTK-2 lane mode only
	t_{SLW}	SCL "L" Pulse Width (Write RGB data)	4	-	ns	MTK-2 lane mode only
	t_{SCYCR}	Serial Clock Cycle (Read)	150	-	ns	
	t_{SHR}	SCL "H" Pulse Width (Read)	75	-	ns	
	t_{SLR}	SCL "L" Pulse Width (Read)	75	-	ns	
SDA / SDI (Input)	t_{SDS}	Data setup time (Write)	30	-	ns	
	t_{SDH}	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	t_{ACC}	Access time (Read)	10	-	ns	
	t_{OH}	Output disable time (Read)	10	70	ns	
CSX	t_{SCC}	SCL-CSX	20	-	ns	
	t_{CHW}	CSX "H" Pulse Width	40	-	ns	
	t_{CSS}	CSX-SCL Time(write)	15	-	ns	
	t_{CSH}		15	-	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=GND=0V



Display Serial Interface Timing Characteristics (3-line SPI system)



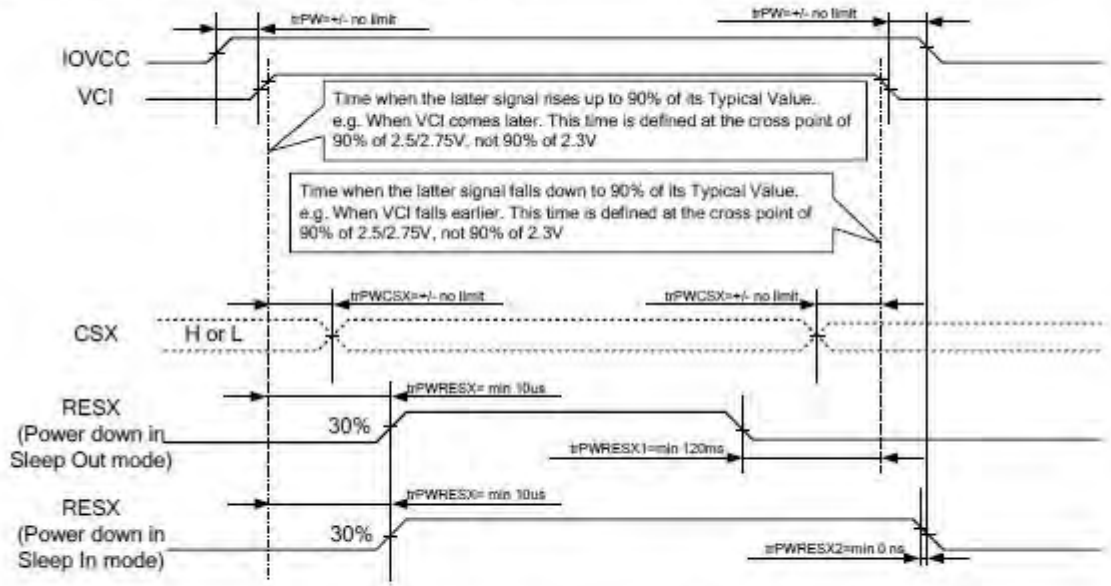
Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB[17:0]	t_{PDS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	33	-	ns	
	PWDL	DOTCLK low-level period	33	-	ns	
	t_{CYCD}	DOTCLK cycle time(18 bit)	66	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB[17:0]	t_{PDS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	25	-	ns	
	PWDL	DOTCLK low-level pulse period	25	-	ns	
	t_{CYCD}	DOTCLK cycle time (6 bit)	50	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time		15	ns	

Note: Ta = -30 to 80 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=GND=0V

Parallel 18/16/6-bit RGB Interface Timing Characteristics

Power ON/OFF Sequence

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and IOVCC have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

Optical Characteristics

Items		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	Note
Response time		Tr+Tf	-	-	45	65	ms	FIG.1	Note4
Contrast Ratio		CR		300	350	-	-	FIG.2	Note1
Surface luminance		LV	θ =0°	-	350	-	cd/m2	FIG.2	Note2
Luminance uniformity		Yu	θ =0°	80	-	-	%	FIG.2	Note3
NTSC		-	θ =0°	-	60	-	%	FIG.2	Note5
Viewing angle		θ Cr>10	θ_T	-	80	-	deg	FIG.3	Note6
			θ_B	-	80	-	deg	FIG.3	
			θ_L	-	80	-	deg	FIG.3	
			θ_R	-	80	-	deg	FIG.3	
Chromaticity	Red	R_X	θ =0° ∅=0° Ta=25°	TBD	TBD	TBD	-	FIG.2 CIE1931	Note5
		R_Y		TBD	TBD	TBD	-		
	Green	G_X		TBD	TBD	TBD	-		
		G_Y		TBD	TBD	TBD	-		
	Blue	B_X		TBD	TBD	TBD	-		
		B_Y		TBD	TBD	TBD	-		
	White	W_X		TBD	TBD	TBD	-		
		W_Y		TBD	TBD	TBD	-		

Note1. Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula. For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON’s BM-5 or BM-7 photo detector or compatible.

Note2. Definition of surface luminance.

Surface luminance is the luminance with all pixels displaying white. For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note3. Definition of luminance uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$YU = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note4. Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and

"Black"state.Rise time (Tr) is the time between photo detector output intensity changed from 90% to 10%. And fall time (Tf) is the time between photo detector output intensity changed from 10% to 90%.
For additional information see FIG1.

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity,The x,y value is determined by screen active area center position P5.For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. Angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers' s ConoScope or DMS series Instruments or compatible.

FIG.1.The definition of response Time

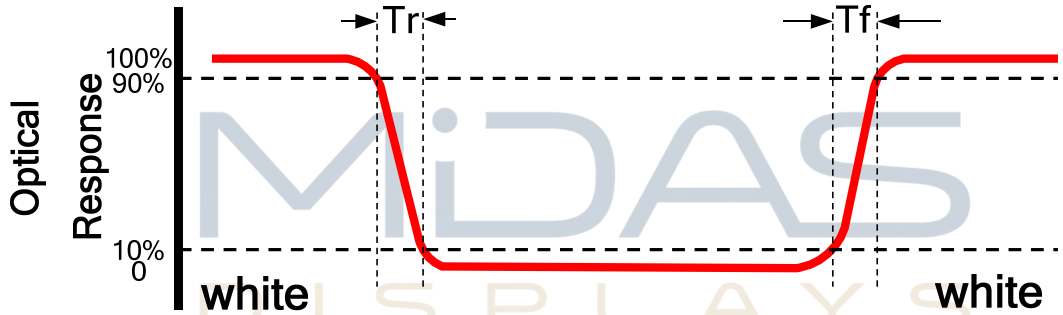


FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

Size : S≤5"(see Figure a) A : 5 mm B : 5 mm
H,V : Active area
Light spot size ∅=5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens.
test spot position : see Figure a.
measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

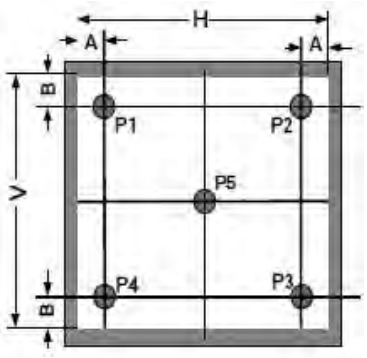


Figure a

Size : 5"＜S≤12.3"(see Figure b) H,V : Active area

Light spot size ∅=5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens.

test spot position : see Figure b.

measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

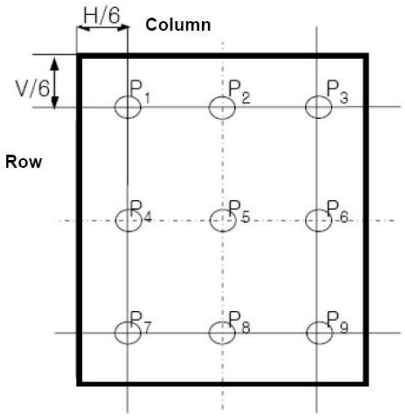


Figure b

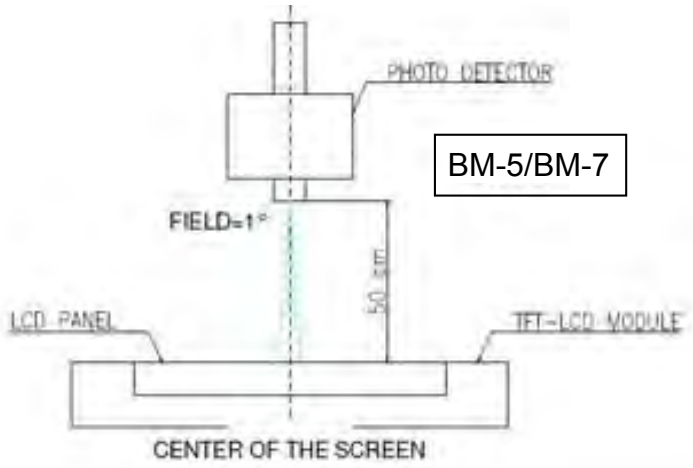
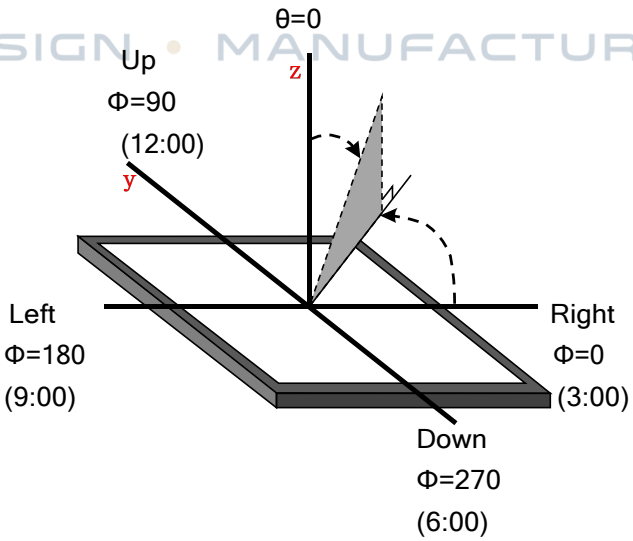


Figure c

FIG.3.The definition of viewing angle

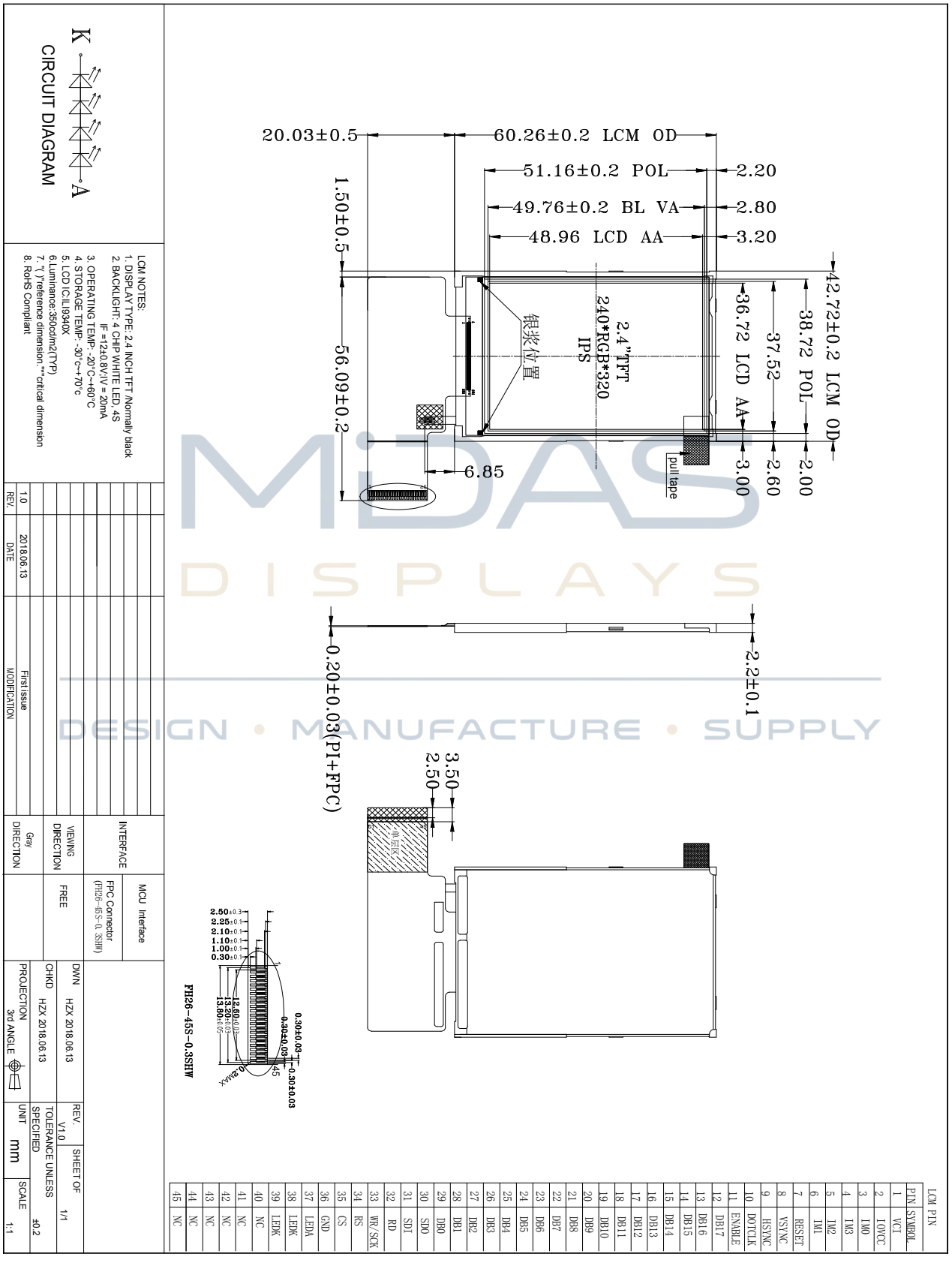


Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +60℃, 96hrs	Note 1 IEC60068-2-2, GB2423. 2-89
2	Low Temperature Operation	Ta= -20℃, 96hrs	Note 2 IEC60068-2-1 GB2423.1-89
3	High Temperature Storage	Ta= +70℃, 120hrs	IEC60068-2-2 GB2423. 2-89
4	Low Temperature Storage	Ta= -30℃, 120hrs	IEC60068-2-1 GB/T2423.1-89
5	High Temperature & Humidity Storage	Ta= +60℃, 90% RH max,120 hours	IEC60068-2-3 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-20℃ 30 min ~ +60℃ 30 min Change time: 5min, 30 Cycle	Start with cold temperature, end with high temperature IEC60068-2-14, GB2423.22-87
7	Electro Static Discharge (Operation)	C=150pF, R=330 Ω, 5 points/panel Air:±8KV, 5 times; Contact: ±4KV, 5 times; (Environment: 15℃ ~ 35℃, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2 GB/T17626.2-1998
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition)	IEC60068-2-6 GB/T2423.5-1995
9	Shock (Non-operation)	60G 6ms, ± X, ±Y , ± Z 3 times for each direction	IEC60068-2-27 GB/T2423.5-1995
10	Package Drop Test	Height: 80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8-1995

Note:1. Ts is the temperature of panel's surface.
2. Ta is the ambient temperature of sample.
3. The size of sample is 5pcs.

Mechanical Drawing



TFT-LCD Module Inspection Criteria

Scope

The incoming inspection standards shall be applied to TFT －LCD Modules (hereinafter Called "Modules") that supplied by Midas Displays.

Incoming Inspection

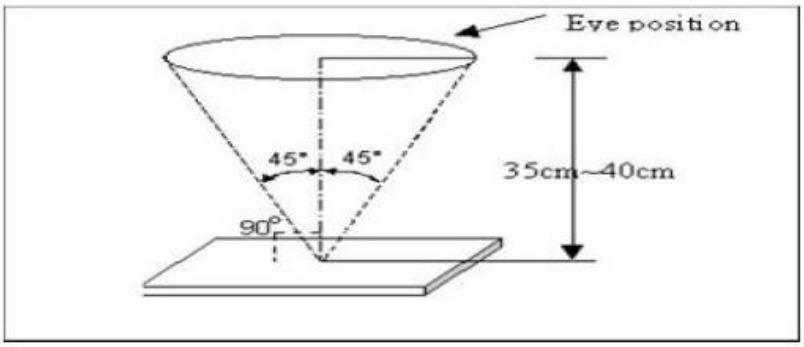
The customer shall inspect the modules within twenty calendar days of the delivery date（the “inspection period）at its own cost. The result of the inspection（acceptance or rejection）shall be recorded in writing, and a copy of this writing will be promptly sent to The seller, If the results of the inspecting from buyer does not send to the seller within twenty Calendar days of the delivery date. The modules shall be regards as acceptance. Should the customer fail to notify the seller within the inspection period, the buyers Right to reject the modules shall be lapsed and the modules shall be deemed to have Been accepted by the buyer

Inspection Sampling

3.1. Lot size: Quantity per shipment lot per model
3.2. Sampling type: Normal inspection, Single sampling
3.3. Inspection level: II
3.4. Sampling table: MIL-STD-105E
3.5. Acceptable quality level （AQL ）
Major defect: AQL=0.65 Minor defect: AQL=1.00

Inspection Conditions

4.1 Ambient conditions:
a. Temperature: Room temperature 25±5℃
b. Humidity: (60±10) ％RH
c. Illumination: Single fluorescent lamp non-directive (300 to 700 Lux)
4.2 Viewing distance
The distance between the LCD and the inspector’s eyes shall be at least 35±5 ㎝.
4.3 Viewing Angle
U/D: 45 ° /45°, L/R: 45° /45°



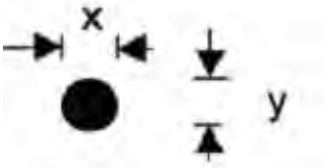
Inspection Criteria

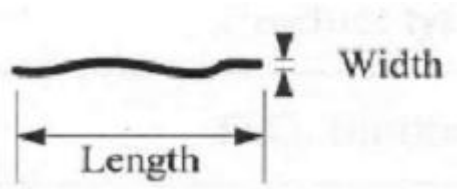
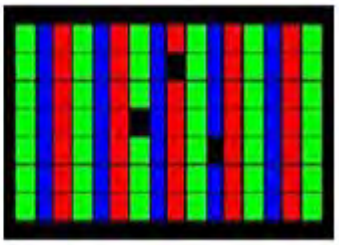
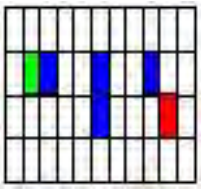
Defects are classified as major defects and minor defects according to the degree of Defectiveness defined herein.

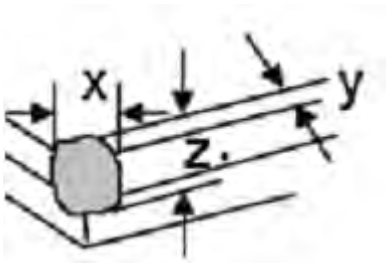
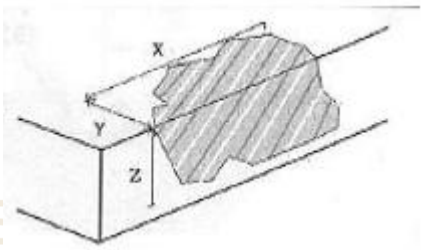
Major defect

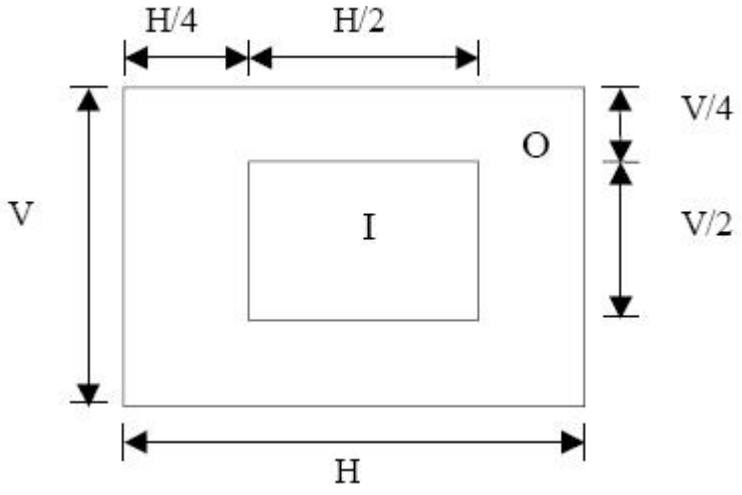
Item No	Items to be inspected	Inspection Standard
5.1.1	All functional defects	1) No display 2) Display abnormally 3) Short circuit 4) line defect
`5.1.2	Missing	Missing function component
5.1.3	Crack	Glass Crack

Minor defect

Item No	Items to be inspected	Inspection standard	
5.2.1	Spot Defect Including Black spot White spot Pinhole Foreign particle Polarizer dirt	For dark/white spot is defined $\varphi = (x+y)/2$ 	
		Size φ(mm)	Acceptable Quantity
		φ≤0.05	Ignore
		0.05 < φ ≤0.15	2
		0.15< φ	Not allowed
5.2.2	Polarizer dirt,	Size φ(mm)	Acceptable Quantity

<table>
<tr><td rowspan="2"></td><td rowspan="2">particle</td><td>Φ≤0.15</td><td>1</td></tr>
<tr><td>Φ>0.15</td><td>Not allowed</td></tr>
<tr><td rowspan="5">5.2.3</td><td rowspan="5">Line Defect
Including Black line
White line Scratch</td><td colspan="2">Define:
 
</td></tr>
<tr><td>Width(mm) Length(mm)</td><td>Acceptable Quantity</td></tr>
<tr><td>W≤0.05</td><td>Ignore</td></tr>
<tr><td>0.05 < W≤0.1
L≤1.5</td><td>1</td></tr>
<tr><td>0.1 < W，or L>1.5</td><td>Not allowed</td></tr>
<tr><td>5.2.4</td><td>Polarizer
Dent/Bubble</td><td colspan="2">Not allowed</td></tr>
<tr><td>5.2.5</td><td>Electrical Dot
Defect</td><td colspan="2">Bright and Black dot define:
 
and


Two Adjacent Dot</td></tr>
<tr><td colspan="3">Inspection pattern: Full white、Full black、Red、green and blue screens</td></tr>
<tr><td colspan="3"><table>
<tr><td rowspan="2">Item</td><td colspan="2">Acceptable Quantity</td></tr>
<tr><td>I</td><td>O</td><td>Note</td></tr>
<tr><td>Black dot defect</td><td colspan="2">1</td><td rowspan="2">(5mm≤Distance)</td></tr>
<tr><td>Bright dot defect</td><td colspan="2">1</td></tr>
<tr><td>Two Adjacent Dot</td><td colspan="2">Not allow</td><td></td></tr>
</table></td></tr>
</table>

<table>
<tr><td rowspan="5">5.2.6</td><td rowspan="5">Glass defect</td><td colspan="2">1.Corner Fragment:
  </td></tr>
<tr><td>Size(mm)</td><td>Acceptable Quantity</td></tr>
<tr><td>X≤2mm
Y≤1mm
Z≤T</td><td>Ignore
T： Glass thickness
X: Length
Y: Width
Z: thickness</td></tr>
<tr><td colspan="2">2. Side Fragment:
  </td></tr>
<tr><td>Size(mm)</td><td>Acceptable Quantity</td></tr>
<tr><td>X≤5.0mm
Y ≤1mm
Z≤T</td><td>T： Glass thickness
X: Length
Y: Width
Z: thickness</td></tr>
</table>



I area & O area

Note: 1). Dot defect is defined as the defective area of the dot area is larger than 50% of the dot area.

2). The distance between two bright dot defects (red, green, blue, and white) should be larger than 15mm.

3). The distance between black dot defects or black and bright dot defects should be more than 5mm apart.

4). Polarizer bubble is defined as the bubble appears on active display area. The defect of polarizer bubble shall be ignored if the polarizer bubble appears on the outside of active display area.

Mechanics specification

As for the outside dimension, weight of the modules, please refer to product specification For more details

Precautions for Use of LCD modules

1. Handling Precautions

1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

1.6. Do not attempt to disassemble the LCD Module.

1.7. If the logic circuit power is off, do not apply the input signals.

1.8. To prevent destruction of the elements by static electricity, be careful to maintain an

optimum work environment.

1.8.1. Be sure to ground the body when handling the LCD Modules.

1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

Storage Precautions

2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

2.2. The LCD modules should be stored under the storage temperature range If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.