


MDT0500D6IH-LVDS	800 x 480	LVDS Interface	TFT Module
Specification			
Version: 1		Date: 24/06/2020	
Revision			
1	22/06/2020	First issue	

Display Features			
Display Size	5.0"		
Resolution	800 x 480		
Orientation	Landscape		
Appearance	RGB		
Logic Voltage	3.3V		
Interface	LVDS		
Brightness	500 cd/m ²		
Touchscreen	---		
Module Size	120.70 x 75.80 x 2.80mm		
Operating Temperature	-30°C ~ +80°C		
Pinout	40 way FFC		Box Quantity
Pitch	0.5mm		Weight / Display
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* - For full design functionality, please use this specification in conjunction with the ST7262 specification.(Provided Separately)

Display Accessories	
Part Number	Description
MPBV6	40 Way FFC to cable and wires. Driven by any driver board that can be wired to a 1mm pitch SHDR-40V-S-B receptacle.
MCIB14/16	HDMI-to-LVDS interface board, with voltage generation.

Optional Variants	
Appearances	Voltage



Summary

TFT 5.0" is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This TFT LCD has a 5.0 inch diagonally measured active display area with 800 x 480 (800 horizontal by 480 vertical pixel) resolution.

General Specifications

- Size: 5.0 inch
- Dot Matrix: 800 × 3(RGB) × 480 dots
- Module dimension: 120.7(W) × 75.8(H) × 2.8mm
- Active area: 108(W) × 64.8 (H) mm
- Dot pitch: 0.135(W) × 0.135(H) mm
- LCD type: TFT, Normally Black, Transmissive
- View Direction: 80/80/80/80
- Aspect Ratio: 16:9
- Driver IC: ST7262 or equivalent
- Interface: LVDS
- Backlight Type: LED ,Normally White
- With /Without TP: Without TP
- Surface: Anti-Glare

*Color tone slight changed by temperature and driving voltage.



Interface

1. LCM PIN Definition

FPC Connector is used for the module electronics interface.

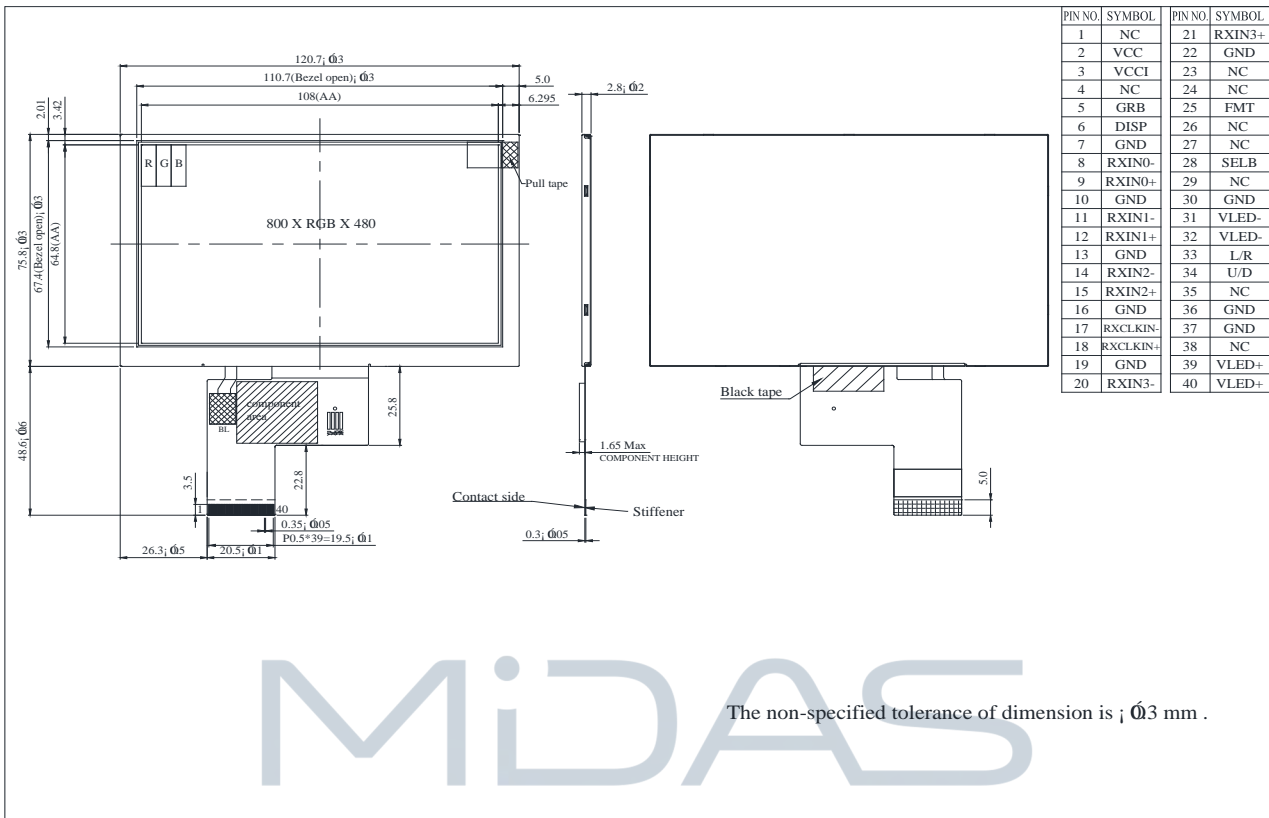
Pin	Symbol	Function	Remark						
1	NC	No connection							
2	VCC	Power voltage							
3	VCCI	Power supply for digital I/O pins.							
4	NC	No connection							
5	GRB	Global reset pin. When GRB is “L” , internal initialization procedure is executed							
6	DISP	Display on/off							
7	GND	Power Ground							
8	RXIN0-	LVDS input lane: RX0-/ RX0+							
9	RXIN0+								
10	GND	Power Ground							
11	RXIN1-	LVDS input lane: RX1-/ RX1+							
12	RXIN1+								
13	GND	Power Ground							
14	RXIN2-	LVDS input lane: RX2-/ RX2+							
15	RXIN2+								
16	GND	Power Ground							
17	RXCLKIN-	LVDS input lane, detail pin define please refer to LVDS Input Pin Mapping Table.							
18	RXCLKIN+								
19	GND	Power Ground							
20	RXIN3-	LVDS input lane: RX3-/ RX3+							
21	RXIN3+								
22	GND	Power Ground							
23-24	NC	No connection							
25	FMT	<p>LVDS_FMT sets LVDS data format.</p> <table border="1"> <thead> <tr> <th>LVDS_FMT</th> <th>Function Description</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>VESA Mode(Default)</td> </tr> <tr> <td>H</td> <td>JEIDA Mode</td> </tr> </tbody> </table> <p>LVDS_FMT is not used in RGB interface and should be connected to “L” .</p>	LVDS_FMT	Function Description	L	VESA Mode(Default)	H	JEIDA Mode	
LVDS_FMT	Function Description								
L	VESA Mode(Default)								
H	JEIDA Mode								
26-27	NC	No connection							
28	SELB	SELB sets VSYNC polarity in RGB interface and sets LVDS							



		3- / 4- lane in LVDS interface.														
		<table border="1"> <thead> <tr> <th>MCU Type</th> <th>VDPOL</th> <th>Function Description</th> </tr> </thead> <tbody> <tr> <td rowspan="2">RGB interface</td> <td>L</td> <td>VSYNC polarity: positive</td> </tr> <tr> <td>H</td> <td>VSYNC polarity: negative(Default)</td> </tr> <tr> <td rowspan="2">LVDS interface</td> <td>L</td> <td>LVDS 3 lane</td> </tr> <tr> <td>H</td> <td>LVDS 4 lane(Default)</td> </tr> </tbody> </table>	MCU Type	VDPOL	Function Description	RGB interface	L	VSYNC polarity: positive	H	VSYNC polarity: negative(Default)	LVDS interface	L	LVDS 3 lane	H	LVDS 4 lane(Default)	
MCU Type	VDPOL	Function Description														
RGB interface	L	VSYNC polarity: positive														
	H	VSYNC polarity: negative(Default)														
LVDS interface	L	LVDS 3 lane														
	H	LVDS 4 lane(Default)														
29	NC	No connection														
30	GND	Power Ground														
31-32	VLED-	Power for LED backlight (Cathode)														
33	L/R	Horizontal scan direction control pin. This pin must be connected to "H" or "L" according to system application														
		<table border="1"> <thead> <tr> <th>HDIR</th> <th>Function Description</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>From right to left</td> </tr> <tr> <td>H</td> <td>From left to right(Default)</td> </tr> </tbody> </table>	HDIR	Function Description	L	From right to left	H	From left to right(Default)								
HDIR	Function Description															
L	From right to left															
H	From left to right(Default)															
34	U/D	Vertical scan direction control pin. This pin must be connected to "H" or "L" according to system application.														
		<table border="1"> <thead> <tr> <th>VDIR</th> <th>Function Description</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>From down to up.</td> </tr> <tr> <td>H</td> <td>From up to down. (Default)</td> </tr> </tbody> </table>	VDIR	Function Description	L	From down to up.	H	From up to down. (Default)								
VDIR	Function Description															
L	From down to up.															
H	From up to down. (Default)															
35	NC	No connection														
36-37	GND	Power Ground														
38	NC	No connection														
39-40	VLED+	Power for LED backlight (Anode)														



Contour Drawing



Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-30	—	+80	°C
Storage Temperature	TST	-30	—	+80	°C

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

- Temp. $\leq 60^\circ\text{C}$, 90% RH MAX. Temp. $> 60^\circ\text{C}$, Absolute humidity shall be less than 90% RH at 60°C

Electrical Characteristics

7.1. Typical Operation Conditions

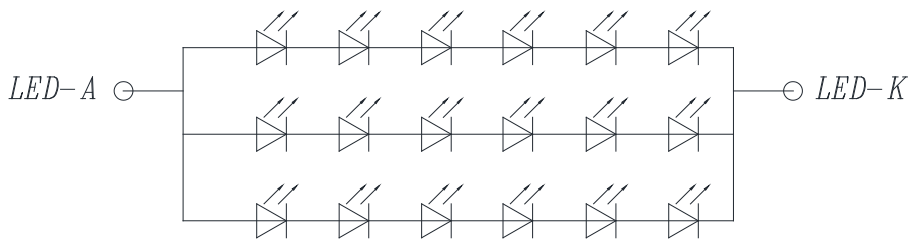
Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	VCC	3.1	3.3	3.6	V	
Power voltage	VCCI	3.1	3.3	3.6	V	
Current for Driver(Black)	ICC	-	67.6	102	mA	Vcc=3.3V

7.2. Backlight Driving Conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Voltage for LED backlight	VL	16.8	19.2	20.4	V	Note 1
Current for LED backlight	IL	--	60	--	mA	
LED life time	-	--	50,000	-	Hr	Note 2

Note 1: The LED Supply Voltage is defined by the number of LED at Ta=25°C and IL=20mA/pcs.

Note 2: The "LED life time" is defined as the module brightness decrease to 50% Original brightness at Ta=25°C and IL=20mA/pcs. The LED lifetime could be decreased if operating IL is larger than 25mA/pcs.

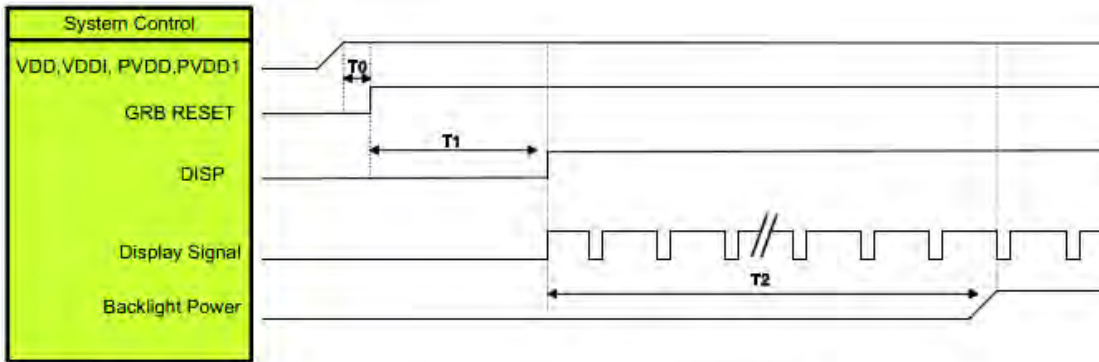


CIRCUIT DIAGRAM(LED 3*6=18 DIES)



Power ON/OFF Sequence

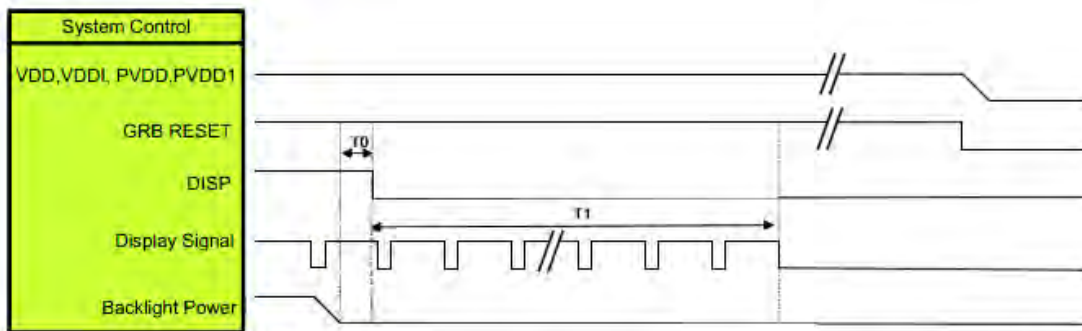
1. Power On Sequence



Symbol	Description	Min. Time	Unit
T0	System power stability to GRB RESET signal	0	ms
T1	GRB RESET="High" to DISP="High"	10	ms
T2	Display Signal output to Backlight Power on	250	ms

Note: LVDS interface Display signal: DCLK P/N; RX[3:0]P/N

2. Power Off Sequence



Symbol	Description	Min. Time	Unit
T0	Backlight Power off to DISP="Low"	5	ms
T1	DISP="Low" to IC internal voltage discharge complete	100	ms

Note: LVDS interface Display signal: DCLK P/N; RX[3:0]P/N



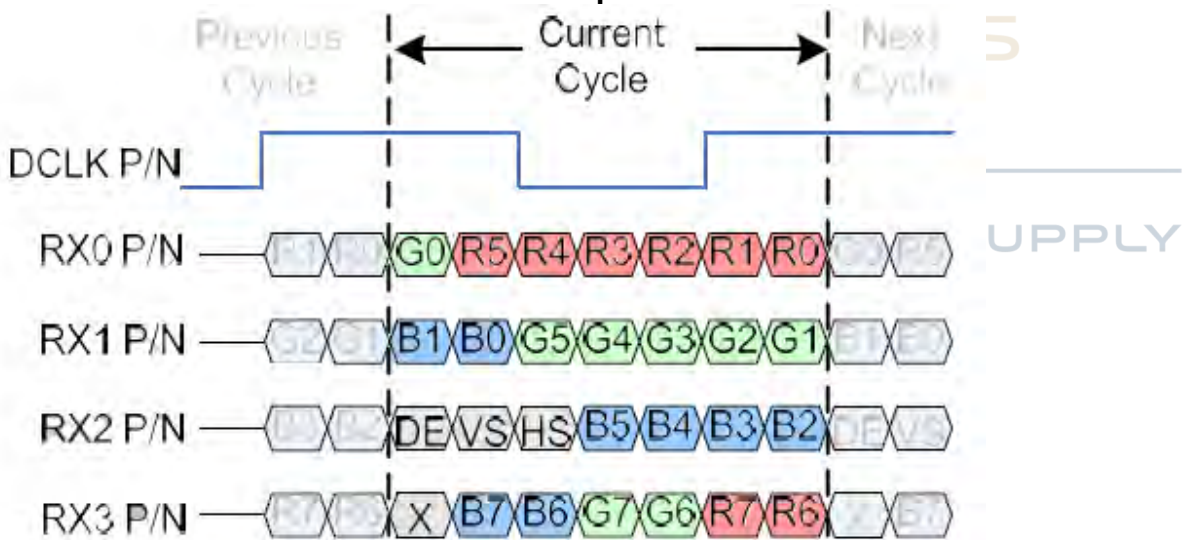
LVDS Interface

1. LVDS Input Pin Mapping Table

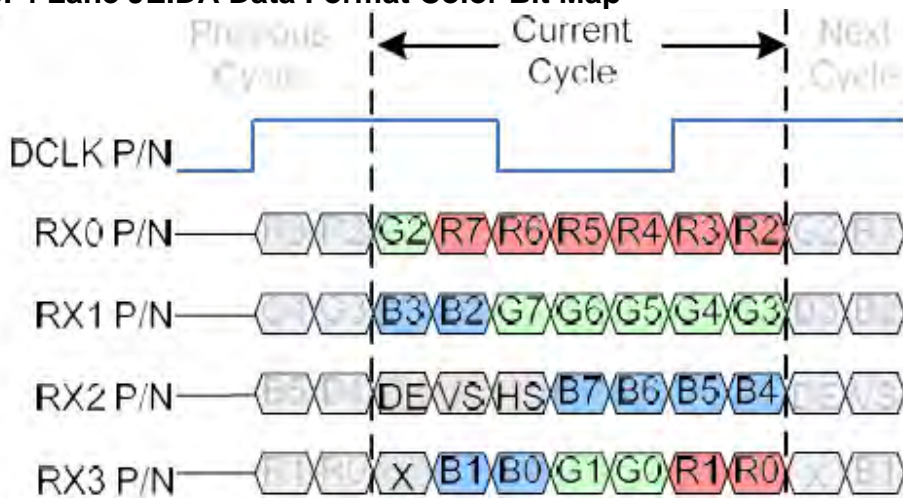
Pin Name RGB (LVDS)	LVDS 3 lane	LVDS 4 Lane
DCLKN	DCLKN	DCLKN
DCLKP	DCLKP	DCLKP
DB0	RX0P	RX0P
DB1	RX0N	RX0N
DB2	RX1P	RX1P
DB3	RX1N	RX1N
DB4	RX2P	RX2P
DB5	RX2N	RX2N
DB6	-	RX3P
DB7	-	RX3N

Note: Symbol "-" means reserve pin and should fix to "L" by DGND.

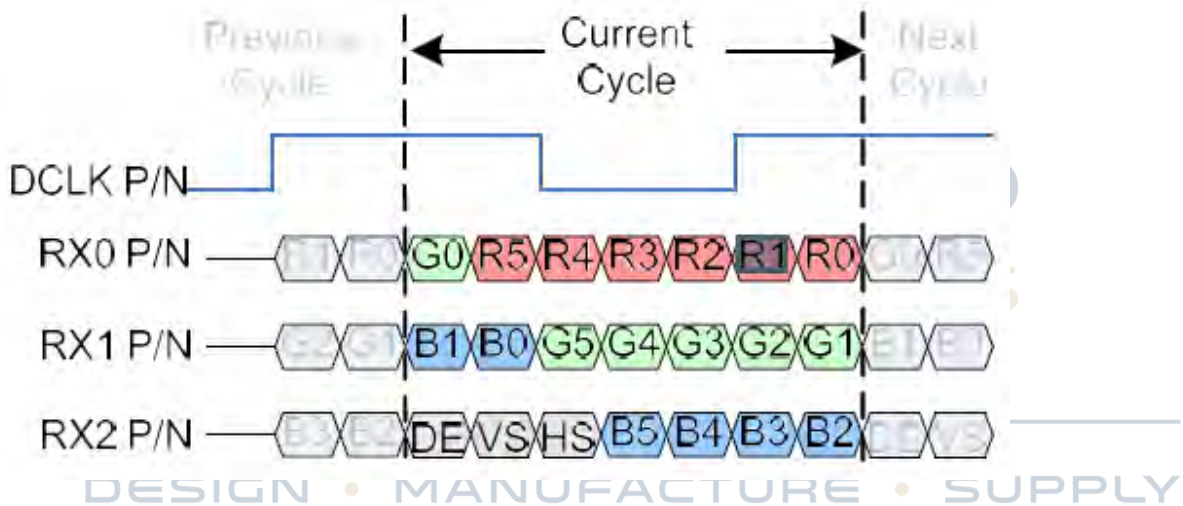
2. 4 Lane VESA Data Format Color Bit Map



3. 4 Lane JEIDA Data Format Color Bit Map

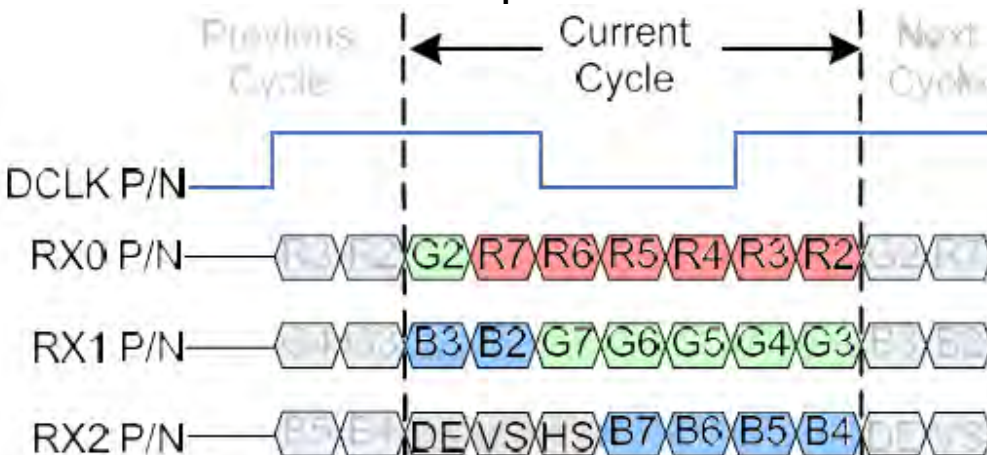


4. 3 Lane VESA Mode Color Bit Map

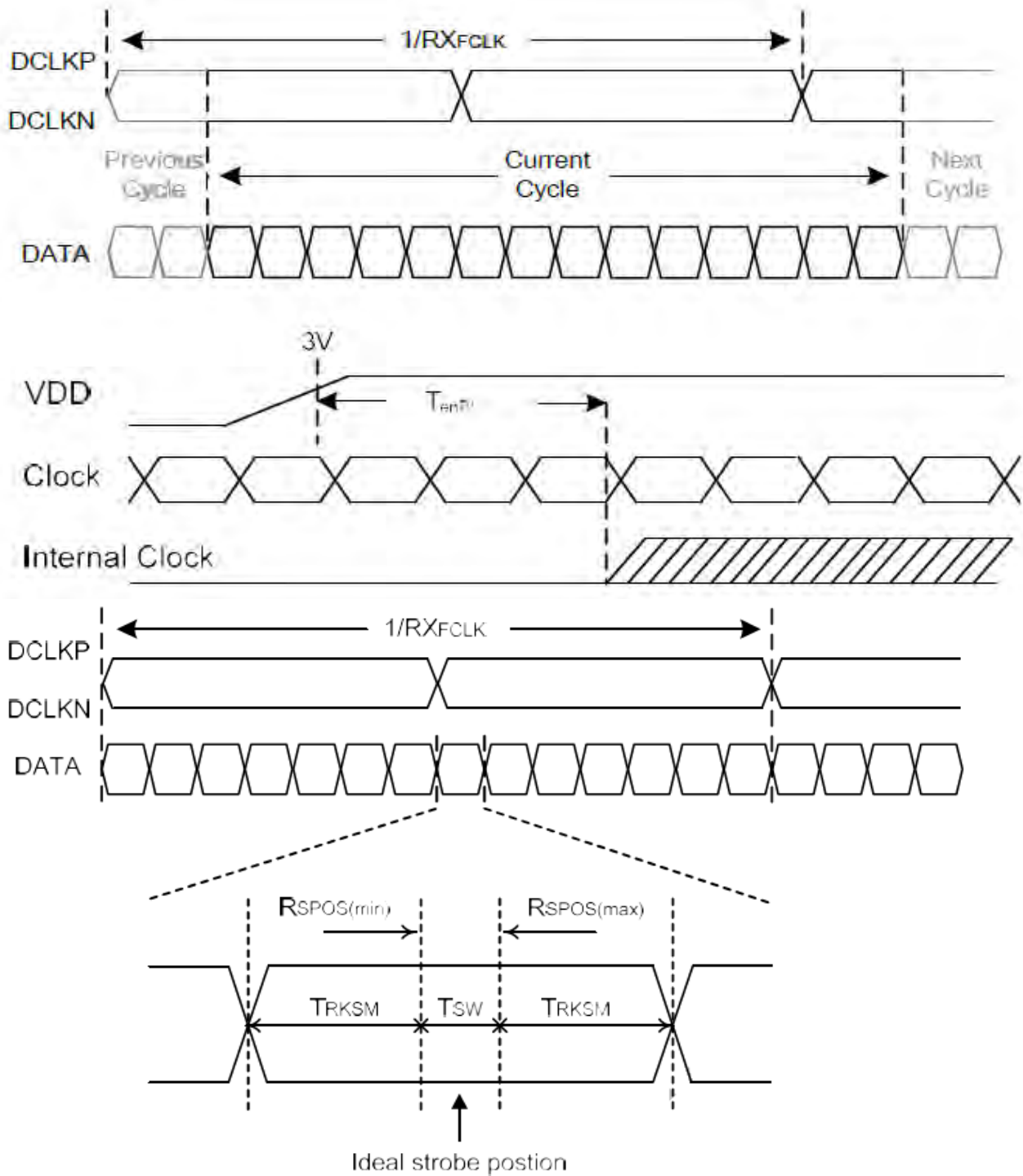


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5. 3 Lane JEIDA Mode Color Bit Map



6. LVDS Input Timing Table



$RRKSM$: Receiver strobe margin
 $RSPOS$: Receiver strobe position
 Tsw : Strobe width (internal DATA sampling window)



LVDS Input Timing (PVDD=PVDD1=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	RX _{FCLK}	23	25	27	MHz	
Input Data Skew Margin	T _{RSKM}	400			ps	
Clock High Time	T _{LVCH}	4/(7 x RX _{FCLK})			ns	
Clock Low Time	T _{LVCL}	3/(7 x RX _{FCLK})			ns	
PLL Wake-up Time	T _{enPLL}			150	us	
LVDS Spread Spectrum Clocking (SSC) Tolerance of LVDS Receiver						
Modulation Frequency	SSC _{MF}			100	KHz	
Modulation Rate	SSC _{MR}			+/-3	%	



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Optical Characteristics

Item	Symbol	Condition.	Min	Typ.	Max.	Unit	Remark	
Response time	Tr+Tf	$\theta=0^\circ$ 、 $\Phi=0^\circ$	-	30	40	.ms	Note 3	
Contrast ratio	CR	At optimized viewing angle	800	1000	-	-	Note 4	
Color Chromaticity	White	Wx	$\theta=0^\circ$ 、 $\Phi=0$	0.27	0.32	0.37		Note 2,6,7
		Wy		0.295	0.345	0.395		
Viewing angle	Hor.	Θ_R	$CR \geq 10$	70	80	-	Deg.	Note 1
		Θ_L		70	80	-		
	Ver.	Φ_T		70	80	-		
		Φ_B		70	80	-		
Brightness	-	-	400	500	-	cd/m ²	Center of display	
Uniformity	(U)	-	75	-	-	%	Note5	

Ta=25±2°C

Note 1: Definition of viewing angle range

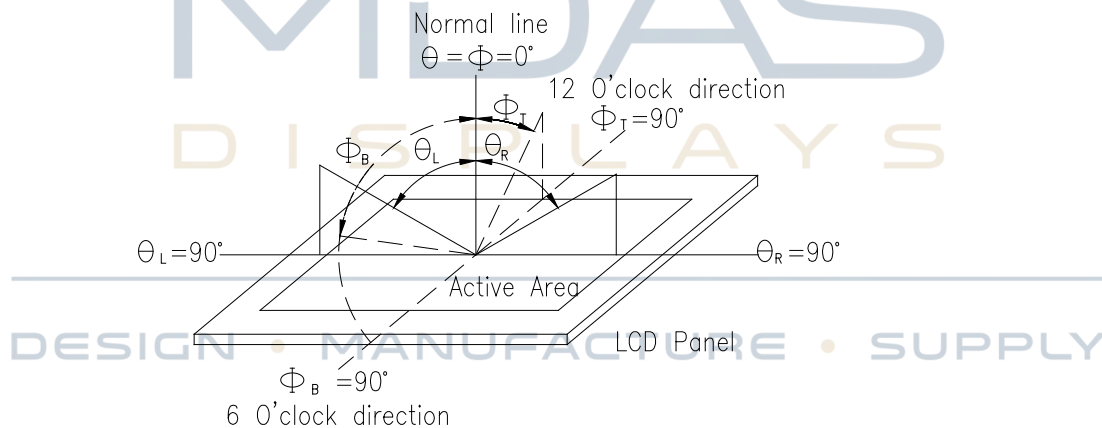


Fig. 10.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7 or BM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.



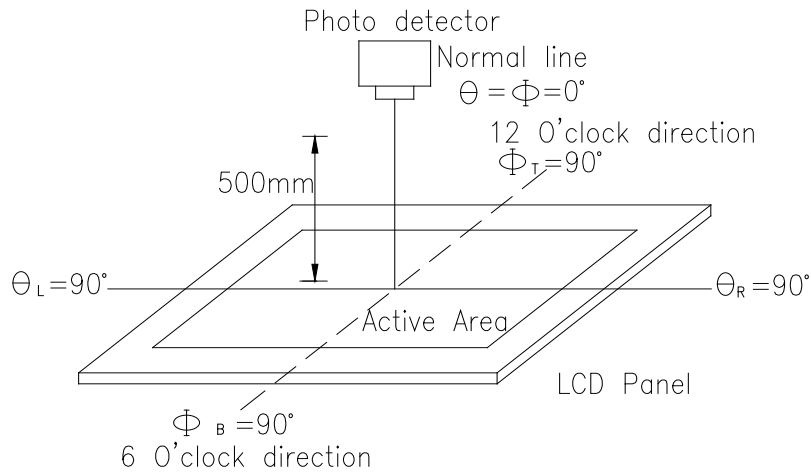
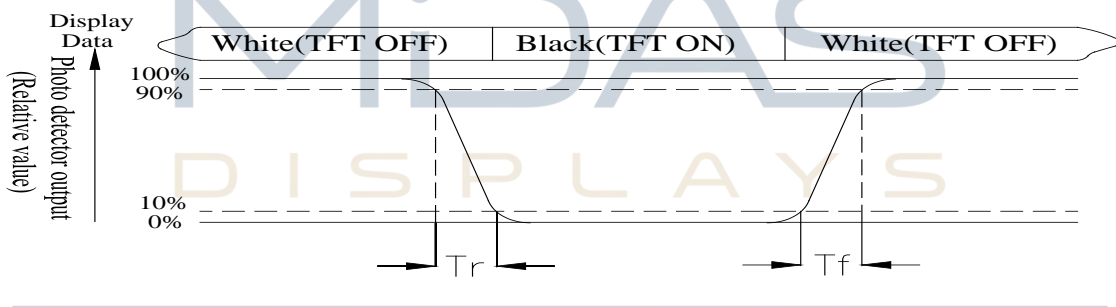


Fig. 10.2. Optical measurement system setup

Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time, T_r , is the time between photo detector output intensity changed from 90% to 10%. And fall time, T_f , is the time between photo detector output intensity changed from 10% to 90%



Note 4: Definition of contrast ratio:

The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$



Note 5: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = $L_{min}/L_{max} \times 100\%$

L = Active area length

W = Active area width

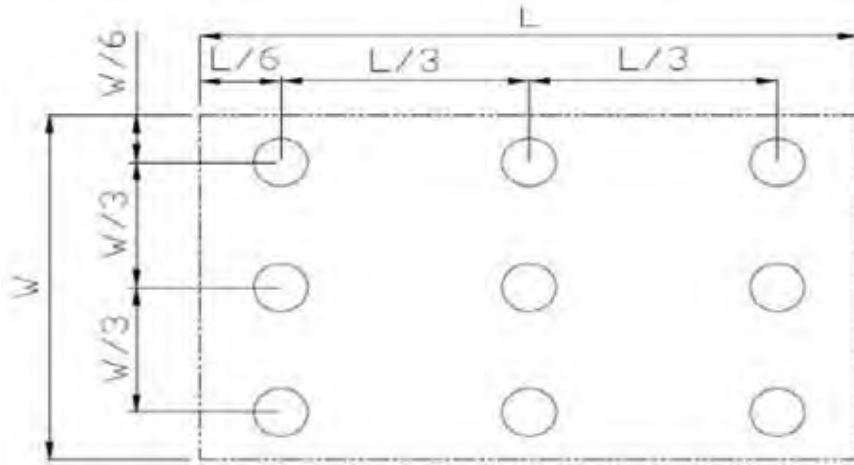


Fig10.3. . Definition of uniformity

Note 6: Definition of color chromaticity (CIE 1931)

Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

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Reliability

Content of Reliability Test (Super Wide temperature, -30°C~80°C)

Environmental Test			
Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	80°C 200hrs	—
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-30°C 200hrs	1
High Temperature/ Humidity storage	The module should be allowed to stand at 60°C,90%RH max	60°C,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation <div style="text-align: center;"> <p style="margin: 0;">-30°C 25°C 80°C</p> <p style="margin: 0;">30min 5min 30min</p> <p style="margin: 0;">1 cycle</p> </div>	-30°C/80°C 10 cycles	—
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±600V(contact) ,±800v(air), RS=330Ω CS=150pF 10 times	—

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: The packing have to including into the vibration testing.

