Evaluation Kit Available | Design Resources | Support

Click here to ask an associate for production status of specific part numbers.

Automotive Quad, Low-Voltage Step-Down DC-DC Converters with Low-Noise LDO

MAX20026/MAX20026S

General Description

The MAX20026/MAX20026S power-management ICs (PMICs) integrate four low-voltage, high-efficiency, step-down DC-DC converters and one low-noise LDO linear regulator. Each of the four step-down DC-DC converter outputs is factory set and can deliver up to 1.0A of current. The LDO linear regulator output is selectable to 2.5V or adjustable, and can deliver 200mA of current. The PMICs operate from 3.0V to 5.5V, making them ideal for automotive point-of-load and post-regulation applications.

The PMICs feature fixed-frequency PWM-mode operation with a switching frequency of 3.2MHz. High-frequency operation allows for an all-ceramic capacitor design and small-size external components. The low-resistance on-chip switches ensure high efficiency at heavy loads while minimizing critical inductances, making the layout a much simpler task with respect to discrete solutions. Internal current sensing and loop compensation reduce board space and system cost.

Two of the four buck converters operate 180° out-of-phase with the internal clock. This feature reduces the necessary input capacitance and improves EMI as well. All four buck converters operate in constant-PWM mode outside the AM band. The PMICs offer a SYNC input to synchronize to an external clock.

The PMICs provide individual enable inputs and one power-good output.

The PMICs offer several important protection features, including input overvoltage protection, input undervoltage monitoring, input undervoltage lockout, cycle-by-cycle current limiting, and overtemperature shutdown. The input undervoltage monitor indicates a brownout condition by driving PGOOD low when the input falls below the undervoltage monitoring (UVM) threshold.

The MAX20026/MAX20026S PMICs are available in a 28-pin TQFN package with an exposed pad and are specified for operation over the -40°C to +125°C automotive temperature range.

Applications

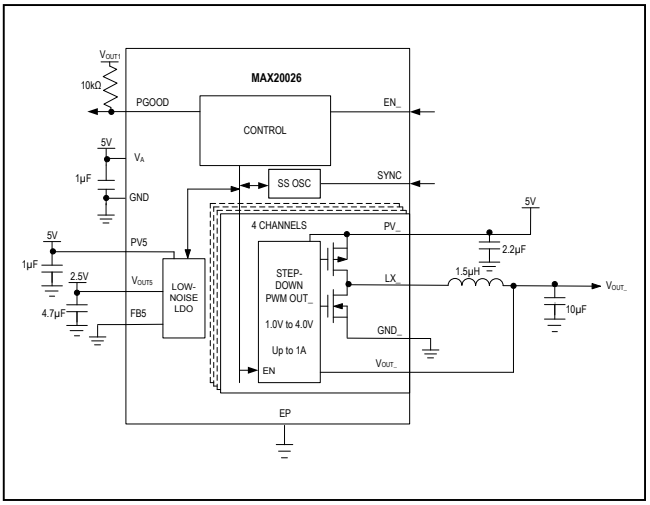
- Automotive
- Industrial

Benefits and Features

- High-Integration Shrinks Solution Size
  - Quad Step-Down DC-DC Converters with Integrated MOSFETs, Capable of Delivering 1.0A Each
  - One 200mA LDO with Adjustable Output Voltage
  - Hybrid Load-Line Architecture Enables Small Output Capacitors
- Performance Designed for Automotive Point-of-Load Regulation
  - Operates from 3.0V to 5.5V Supply Voltage
  - Individual Enable Signals for Each Output
  - UV/OV/UVM/PGOOD
  - Soft-Start and Supply Sequencing Reduces Inrush Current
- Low-Noise Features Improve EMI Performance
  - 3.2MHz Switching Frequency
  - Forced-PWM Operation
  - Two Channels 180° Out-of-Phase
  - SYNC Input
- Robust for the Automotive Environment
  - 28-Pin (4mm x 4mm x 0.8mm) TQFN-EP Package
  - -40°C to +125°C Operating Temperature Range
  - AEC-Q100 Qualified

*Ordering Information/Selector Guide** ***appear at end of data sheet.***

Simplified Block Diagram



19-5168; Rev 6; 3/19

Absolute Maximum Ratings

PV_ to GND_ ..... -0.3V to +6V
V_A to GND ..... -0.3V to +6V
SYNC, OUT_, EN_, PGOOD to GND ..... -0.3V to V_A + 0.3V
LX_ to GND_ ..... -0.3V to $V_{PV\_}$ +0.3V
FB5, OUT5 to GND ..... -0.3V to V_{PV5} + 0.3V
PV_ to PV_ (PV1, PV2, PV3, PV4 only) ..... -0.3V to +0.3V
LX_ and GND_ Continuous RMS Current 1.7A
PV_ Continuous RMS Current (Note 1) 0.85A
GND_ to GND ..... -0.3V to +0.3V
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
28-TQFN-EP (derate 28.6mW/°C > +70°C) 2285mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

Thermal Resistance, Single-Layer Board
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 48°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 3°C/W

Thermal Resistance, Four-Layer Board
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 35°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 3°C/W

Note 1: The PV1 and PV4 pins can provide full load from 4.5V to 5.5V. Below 4.5V, continuous current is limited to 0.85A per the *Absolute Maximum Ratings*.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = V_{PV4} = V_{PV5} = 5.0V; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
Supply Voltage Range	$V_{PV\_}$	(Note 1)	3.0		5.5	V
Supply Current	I_{PV}	No load, EN1 = EN2 = EN3 = EN4 = high, EN5 = low, T_A = +25°C, LX_ not switching	2.5	3.8	5	mA
Shutoff Current	I_{PVSD}	EN1 = EN2 = EN3 = EN4 = EN5 = low, T_A = +25°C		0.2	2	µA
		EN1 = EN2 = EN3 = EN4 = EN5 = low, T_A = +125°C		2.4		
		MAX20026S EN1 = EN2 = EN3 = EN4 = EN5 = low, T_A = +125°C		2		
Overvoltage Threshold		V_A rising	5.6	5.8	6	V
		Hysteresis		0.1		
Undervoltage Monitor Threshold		V_A falling	4.15	4.3	4.45	V
		Hysteresis		0.1		
UVLO Threshold		V_A falling	2.68			V
		V_A rising			3	

Electrical Characteristics (continued)

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = $V_{PV4=}$ V_{PV5} = 5.0V; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
PWM Switching Frequency	f_{SW}		3	3.2	3.4	MHz
SYNC Input Frequency Range	f_{SYNC}		2.8		3.5	MHz
SYNCHRONOUS STEP-DOWN CONVERTERS (OUT1, OUT2, OUT3, OUT4)						
Fixed DC Output Accuracy		I_{LOAD} = 0mA		1.5		%
		I_{LOAD} = 0mA to 1.0A	-3		+3	
		MAX20026S I_{LOAD} = 0mA		1		
		MAX20026S I_{LOAD} = 0mA to 500mA	-3		+3.75	
		MAX20026S I_{LOAD} = 0mA to 1A	-3.75		+3.75	
FB DC Output Accuracy	VFB_	MAX20026S I_{LOAD} = 0mA, V_{FB} = 0.8V		0.814		V
		MAX20026S I_{LOAD} = 0mA to 500mA, V_{FB} = 0.8V	0.776		0.83	
		MAX20026S I_{LOAD} = 0mA to 1A, V_{FB} = 0.8V	0.77		0.83	
Load Regulation		I_{LOAD} = 1.0A		-1.5	-2.5	%
		MAX20026S I_{LOAD} = 1.0A		-2.0	-3.0	
Line Regulation		$V_{PV\_}$ = 4.5V to 5.5V		0.3		%
		MAX20026S $V_{PV\_}$ = 4.5V to 5.5V		0.44		
pMOS On-Resistance		$V_{PV\_}$ = 5.0V, $I_{LX\_}$ = 0.2A		125	250	mΩ
nMOS On-Resistance		$V_{PV\_}$ = 5.0V, $I_{LX\_}$ = 0.2A		100	200	mΩ
pMOS Current-Limit Threshold			1.4	1.65	2	A
Soft-Start Ramp Time				500		µs
LX Leakage Current		$V_{PV\_}$ = 5V, $V_{LX\_}$ = $V_{PV\_}$ or $V_{PG\_}$, T_A = +25°C		±0.1		µA
Minimum On-Time				45	66	ns
LX Rise and Fall Time		(Note 6)		4		ns
Duty-Cycle Range					100	%
$V_{OUT\_}$ Discharge Resistance		$V_{EN\_}$ = 0V		30		Ω
OUT1, OUT2 Phasing		(Note 4)		0		°
OUT3, OUT4 Phasing		(Note 4)		180		°
LINEAR REGULATOR						
PV5 Operating Range	V_{PV5}		2.7		5.5	V
VOUT5 Output Voltage Range	V_{OUT5}	I_{LOAD} = 0mA	1.25	2.5	3.3	V
		MAX20026S I_{LOAD} = 0mA	1	2.5	3.3	
VOUT5 Load Capacitance	C_{OUT5}	I_{LOAD} = 200mA (Note 5)		4.7		µF
		MAX20026S I_{LOAD} = 200mA (Note 5)		2 x 4.7		

Electrical Characteristics (continued)

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = $V_{PV4=}$ V_{PV5} = 5.0V; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
FB5 Regulated Voltage	V_{FB5}	I_{LOAD} = 0mA	1.225	1.25	1.27	V
	V_{FB5L}	I_{LOAD} = 0mA to 200mA	1.21		1.27	
	V_{FB5}	MAX20026S I_{LOAD} = 0mA		1.01		
	V_{FB5L}	MAX20026S I_{LOAD} = 0mA to 150mA	0.973	1.01	1.04	
		MAX20026S I_{LOAD} = 0mA to 200mA	0.97	1.01	1.04	
		MAX20026S I_{LOAD} = 0mA to 250mA	0.96	1.01	1.04	
Line Regulation		I_{LOAD} = 10mA, V_{PV5} = 4.5V to 5.5V		±0.3		%
FB5 Pullup Current		V_{FB5} = 1.1V		100		nA
VOUT5 Regulated Voltage	V_{OUT5}	I_{LOAD} = 0mA, FB5 = GND	2.45	2.5	2.55	V
	V_{OUT5L}	I_{LOAD} = 0mA to 200mA, FB5 = GND	2.4		2.6	
	V_{OUT5}	MAX20026S I_{LOAD} = 0mA, FB5 = GND		2.516		
	V_{OUT5L}	MAX20026S I_{LOAD} = 0mA to 200mA, FB5 = GND	2.4	2.516	2.6	
VOUT5 Discharge Resistance	R_{OUT5}	V_{EN5} = 0V		70		Ω
VOUT5 Current-Limit Threshold	I_{LM5}	V_{PV5} = 5V	300		800	mA
VOUT5 Dropout	V_{DO5}	V_{PV5} = 2.7V, I_{LOAD} = 200mA		410		mV
Soft-Start Ramp Time		10% to 90% of V_{OUT}		400		µs
LDO Output Noise		10Hz to 100kHz, V_{PV5} = 5V, V_{OUT5} = 1.8V, I_{LOAD} = 200mA		32		µVrms
PSRR		V_{PV5} = 5V, V_{OUT5} = 1.8V, I_{LOAD} = 200mA, 1kHz		-55		dB
THERMAL OVERLOAD						
Thermal-Shutdown Temperature		T_J rising (Note 6)		+175		°C
Hysteresis		(Note 6)		15		°C
OUTPUT POWER-GOOD INDICATOR (PGOOD)						
Overvoltage Threshold		$V_{OUT\_}$ rising (percentage of nominal output)	106	110	114	%
Undervoltage Threshold		$V_{OUT\_}$ falling (percentage of nominal output)	92.5	94	96.5	%
		$V_{OUT\_}$ rising (percentage of nominal output)	93.5	95	97	
		MAX20026S $V_{OUT\_}$ falling (percentage of nominal output)	90.5	93	96	
		MAX20026S $V_{OUT\_}$ rising (percentage of nominal output)	91.5	94	97	
PGOOD Blanking Time		From any of UV/OV/UVM/SSDONE_/ PGOOD_ cleared to PGOOD rising		6		ms
UV/OV Propagation Delay	t_{MIN}	From UV/OV/UVM detection to PGOOD low		15		µs

Electrical Characteristics (continued)

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = $V_{PV4=}$ V_{PV5} = 5.0V; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 3)

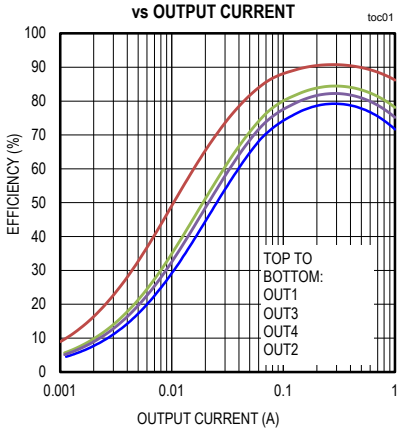
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
PGOOD Output High-Leakage Current				0.1		µA
PGOOD Output Low Level		V_A = 3.0V, sinking 3mA			0.22	V
ENABLE INPUTS (EN1, EN2, EN3, EN4, EN5)						
EN_ Input High Level		V_A = 5V, $V_{EN\_}$ rising	0.7	1.0	1.3	V
EN_ Hysteresis		V_A = 5V, $V_{EN\_}$ falling		50		mV
EN_ Pulldown Resistance				100		kΩ
EN2 Startup Delay		EN1 and EN2 high, from EN1 rising edge		8192		Cycles
		MAX20026S EN1 and EN2 high, from EN1 rising edge		2048		
EN3 Startup Delay		EN1 and EN3 high, from EN1 rising edge		16384		Cycles
		MAX20026S EN1 and EN3 high, from EN1 rising edge		4096		
EN4 Startup Delay		EN1 and EN4 high, from EN1 rising edge		24576		Cycles
		MAX20026S EN1 and EN4 high, from EN1 rising edge		6144		
EN5 Startup Delay		EN1 and EN5 high, from EN1 rising edge		32768		Cycles
		MAX20026S EN1 and EN5 high, from EN1 rising edge		8192		
DIGITAL INTERFACE (SYNC)						
Input Voltage High	V_{INH}		1.5			V
Input Voltage Low	V_{INL}				0.5	V
Input Voltage Hysteresis				70		mV
Pulldown Resistance				100		kΩ

Note 3: All units are 100% production tested at +25°C. All temperature limits are guaranteed by design.
Note 4: Phase measurement is in relation to the rising edge of LX_.
Note 5: See Table 1 to choose the proper load capacitor value.
Note 6: Guaranteed by design. Not production tested.

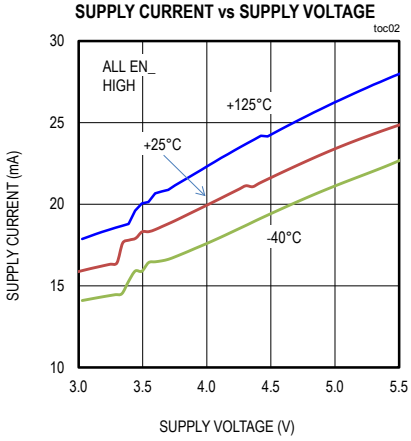
Typical Operating Characteristics

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = V_{PV4} = V_{PV5} = 5.0V, T_A = +25°C, unless otherwise noted, MAX20026ATIB/V+.)

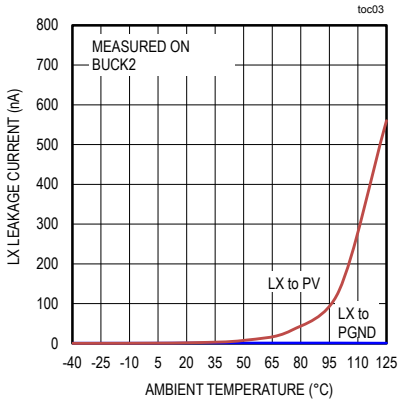
BUCK EFFICIENCY vs OUTPUT CURRENT



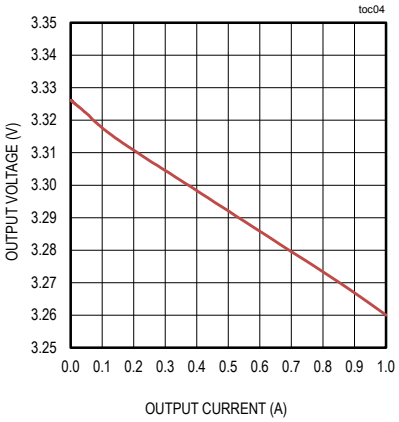
SUPPLY CURRENT vs SUPPLY VOLTAGE



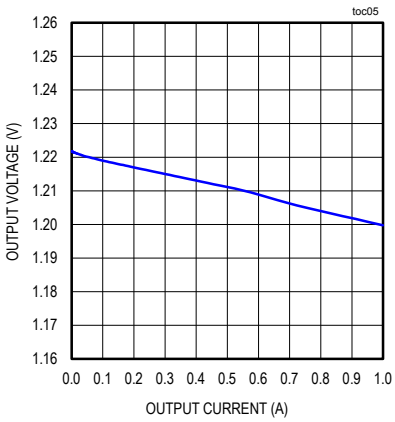
LX LEAKAGE CURRENT vs TEMPERATURE



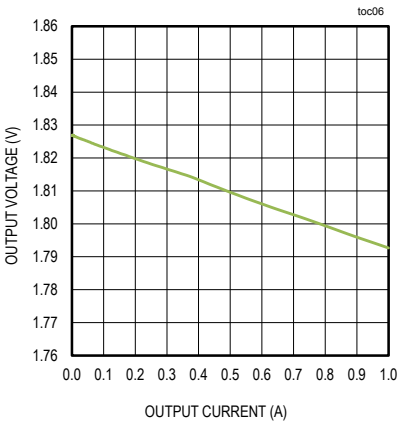
OUT1 LOAD REGULATION



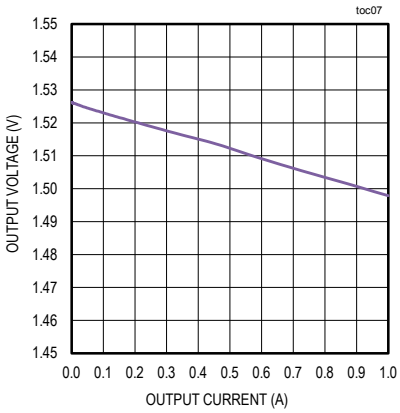
OUT2 LOAD REGULATION



OUT3 LOAD REGULATION



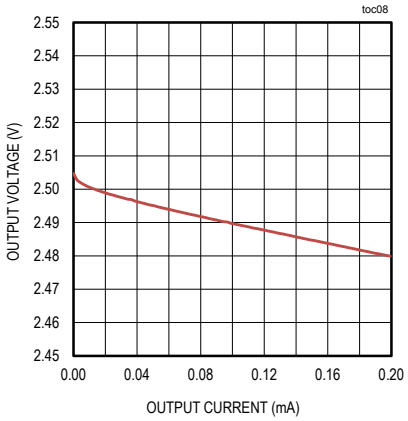
OUT4 LOAD REGULATION



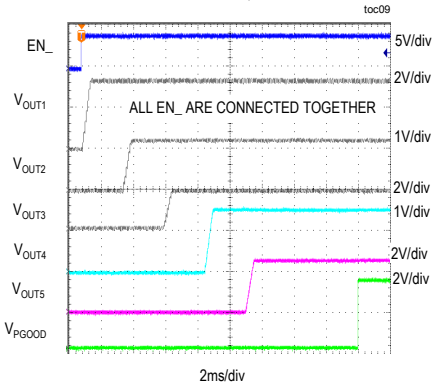
Typical Operating Characteristics (continued)

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = V_{PV4} = V_{PV5} = 5.0V, T_A = +25°C, unless otherwise noted, MAX20026ATIB/V+.)

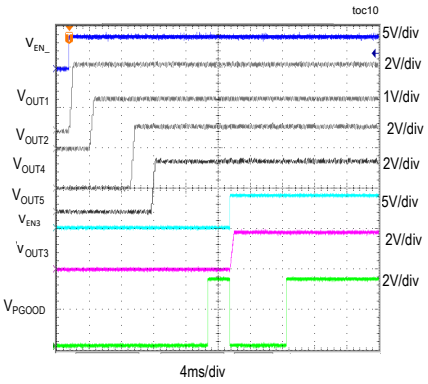
OUT5 LOAD REGULATION



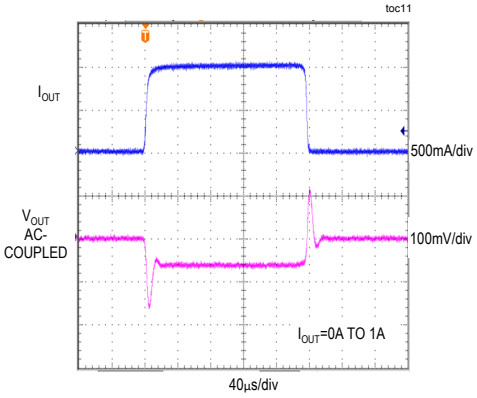
STARTUP SEQUENCE



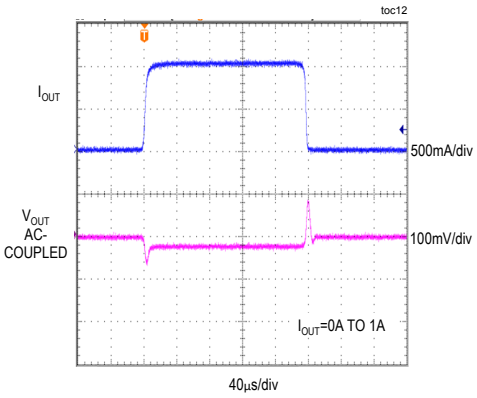
STARTUP WITH EN DELAY



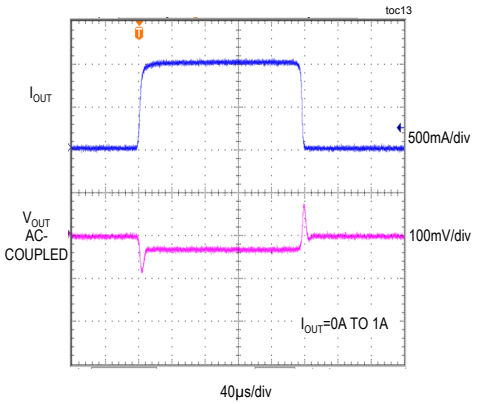
BUCK1 LOAD TRANSIENT RESPONSE



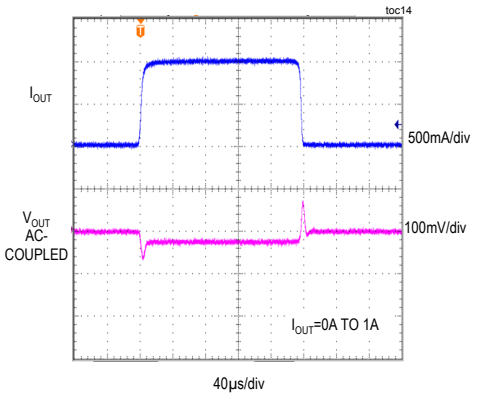
BUCK2 LOAD TRANSIENT RESPONSE



BUCK3 LOAD TRANSIENT RESPONSE



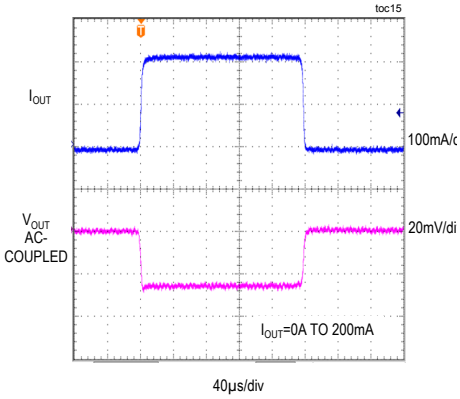
BUCK4 LOAD TRANSIENT RESPONSE



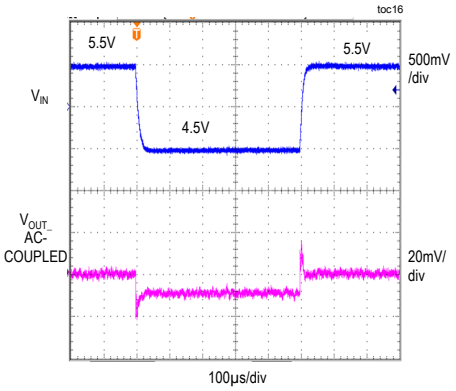
Typical Operating Characteristics (continued)

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = V_{PV4} = V_{PV5} = 5.0V, T_A = +25°C, unless otherwise noted, MAX20026ATIB/V+.)

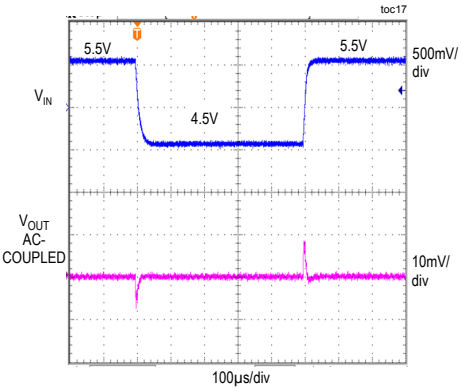
LDO LOAD TRANSIENT RESPONSE



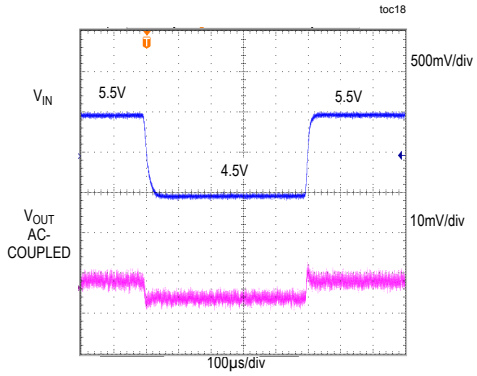
BUCK1 LINE TRANSIENT RESPONSE



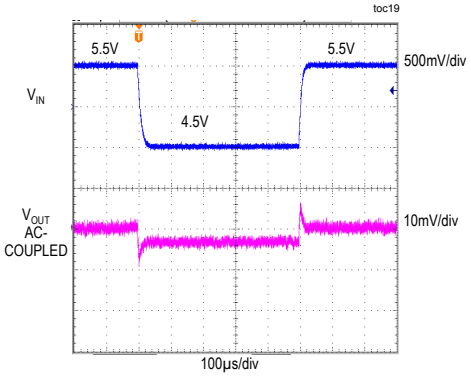
BUCK2 LINE TRANSIENT RESPONSE



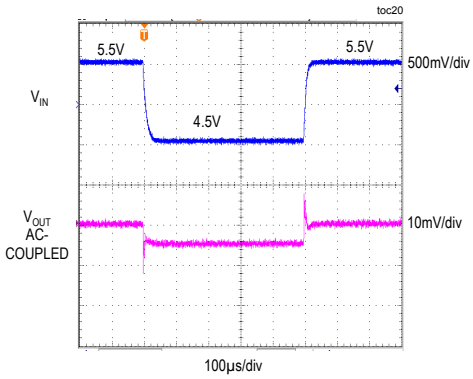
BUCK3 LINE TRANSIENT RESPONSE



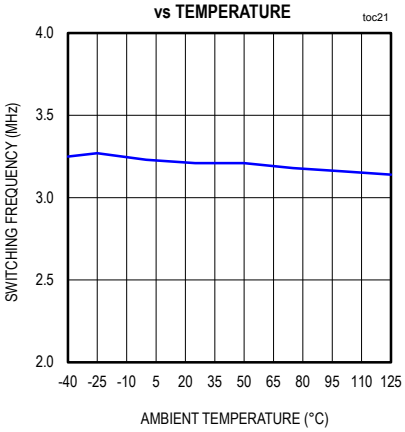
BUCK4 LINE TRANSIENT RESPONSE



LDO LINE TRANSIENT RESPONSE



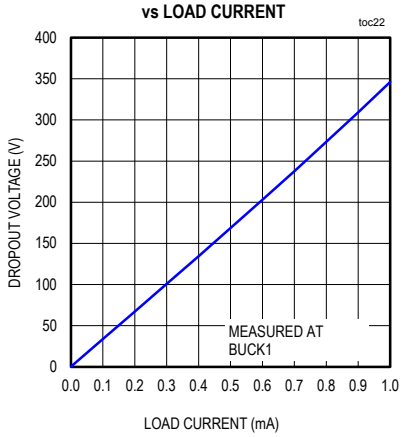
SWITCHING FREQUENCY vs TEMPERATURE



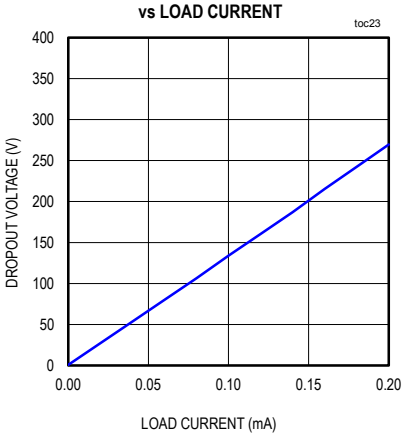
Typical Operating Characteristics (continued)

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = V_{PV4} = 5.0V; T_A = +25°C, unless otherwise noted.)

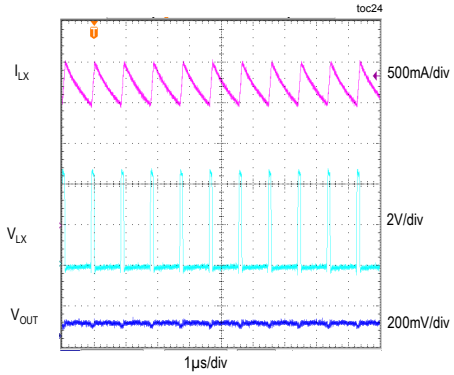
BUCK DROPOUT VOLTAGE vs LOAD CURRENT



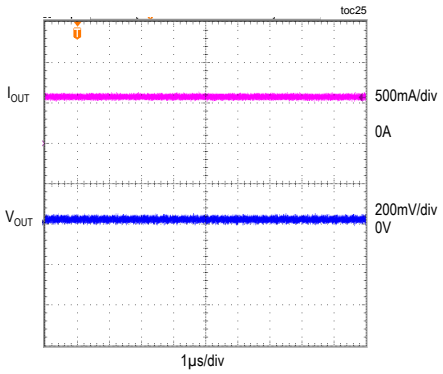
LDO DROPOUT VOLTAGE vs LOAD CURRENT



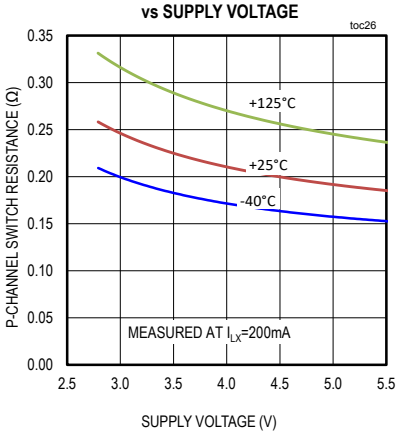
BUCK SHORT CIRCUIT BEHAVIOR



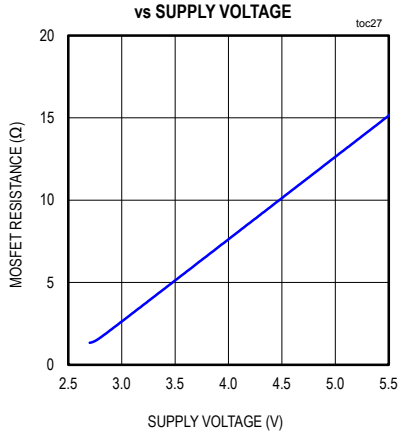
LDO SHORT CIRCUIT BEHAVIOR



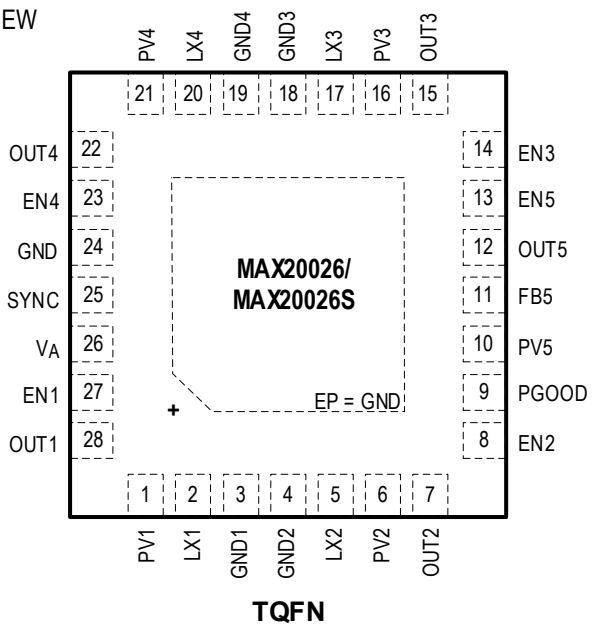
P-CHANNEL SWITCH RESISTANCE vs SUPPLY VOLTAGE



LDO MOSFET RESISTANCE vs SUPPLY VOLTAGE



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	PV1	Buck 1 Voltage Input. Connect a 2.2µF or larger ceramic capacitor from PV1 to GND1, placed as close as possible to the device.
2	LX1	Buck 1 Switching Node. LX1 is high impedance when the device is off.
3	GND1	Power Ground for Buck 1
4	GND2	Power Ground for Buck 2
5	LX2	Buck 2 Switching Node. LX2 is high impedance when the device is off.
6	PV2	Buck 2 Voltage Input. Connect a 2.2µF or larger ceramic capacitor from PV2 to GND2, placed as close as possible to the device.
7	OUT2	Buck 2 Voltage-Sense Input
8	EN2	Active-High Digital Enable Input for Buck 2. Driving EN2 high enables Buck 2.
9	PGOOD	Open-Drain, Active-High, Power-Good Output for All Rails. To obtain a logic signal, pull up PGOOD with an external resistor connected to a positive voltage equal to or lower than V_A.
10	PV5	LDO Voltage Input. Connect a 1µF or larger ceramic capacitor from PV5 to the ground plane, placed as close as possible to the device.
11	FB5	Feedback Input for the LDO. Connect to GND for preset output voltage.
12	OUT5	LDO Voltage Output. Connect a 4.7µF or larger ceramic capacitor from OUT5 to the ground plane, placed as close as possible to the device.

Pin Description (continued)

PIN	NAME	FUNCTION
13	EN5	Active-High Digital Enable Input for the LDO. Driving EN5 high enables the LDO.
14	EN3	Active-High Digital Enable Input for Buck 3. Driving EN3 high enables Buck 3.
15	OUT3	Buck 3 Voltage-Sense Input
16	PV3	Buck 3 Voltage Input. Connect a 2.2µF or larger ceramic capacitor from PV3 to GND3, placed as close as possible to the device.
17	LX3	Buck 3 Switching Node. LX3 is high impedance when the device is off.
18	GND3	Power Ground for Buck 3
19	GND4	Power Ground for Buck 4
20	LX4	Buck 4 Switching Node. LX4 is high impedance when the device is off.
21	PV4	Buck 4 Voltage Input. Connect a 2.2µF or larger ceramic capacitor from PV4 to GND4, placed as close as possible to the device.
22	OUT4	Buck 4 Voltage-Sense Input
23	EN4	Active-High Digital Enable Input for Buck 4. Driving EN4 high enables Buck 4.
24	GND	Analog Ground
25	SYNC	SYNC Input. Supply an external clock to control the switching frequency. Connect SYNC to GND to use the default switching frequency.
26	V_A	Analog Voltage Supply. Connect a 1µF or larger ceramic capacitor from V_A to GND, placed as close as possible to the device. Connect to the same supply as the PV_ inputs.
27	EN1	Active-High Digital Enable Input for Buck 1. Driving EN1 high enables buck 1.
28	OUT1	Buck 1 Voltage-Sense Input
—	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to GND1–GND4 and GND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

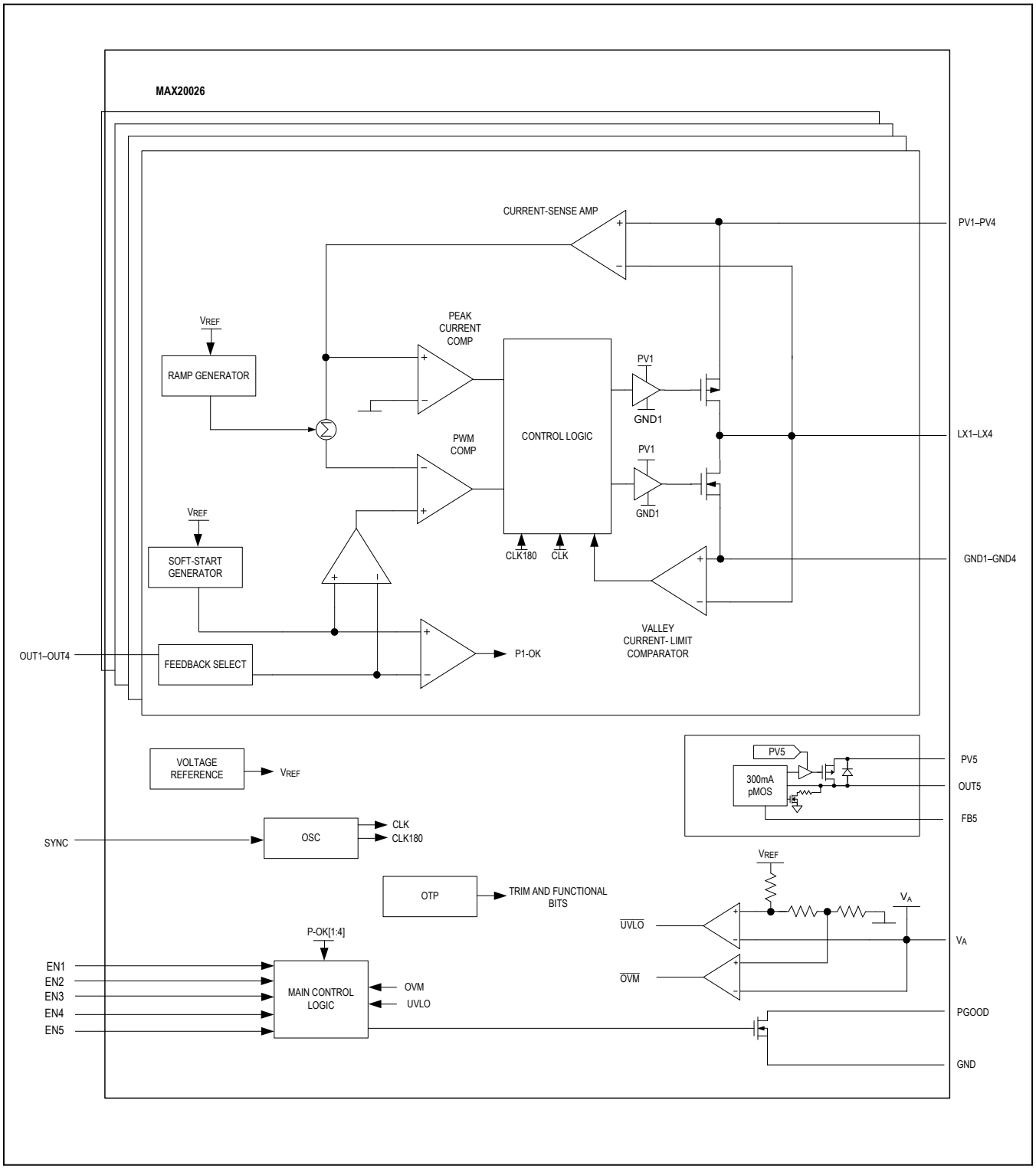


Figure 1. Internal Block Diagram

Detailed Description

The MAX20026/MAX20026S PMICs offer four high-efficiency, synchronous step-down converters and one LDO linear regulator that operate with a 3.0V to 5.5V input voltage range and provide a factory-set output voltage. The step-down converters deliver up to 1.0A of load current per output and the LDO linear regulator delivers up to 200mA of load current. The PMICs achieve ±3% output error over load, line, and temperature ranges.

The PMICs feature fixed-frequency PWM-mode operation with a 3.2MHz switching frequency. A synchronization input (SYNC) allows the device to synchronize to an external clock.

On-board low R_{DSON} switches help minimize efficiency losses at heavy loads and reduce critical/parasitic inductance, making the layout a much simpler task with respect to discrete solutions.

The device is offered in factory-preset output voltages to allow customers to achieve ±3% output-voltage accuracy, without using expensive 0.1% resistors.

Additionally, each converter features soft-start, overcurrent, and overtemperature protections.

Control Scheme

The step-down converters use peak current-mode control, and feature internal slope compensation and internal loop compensation, both of which reduce board space and allow a very compact solution.

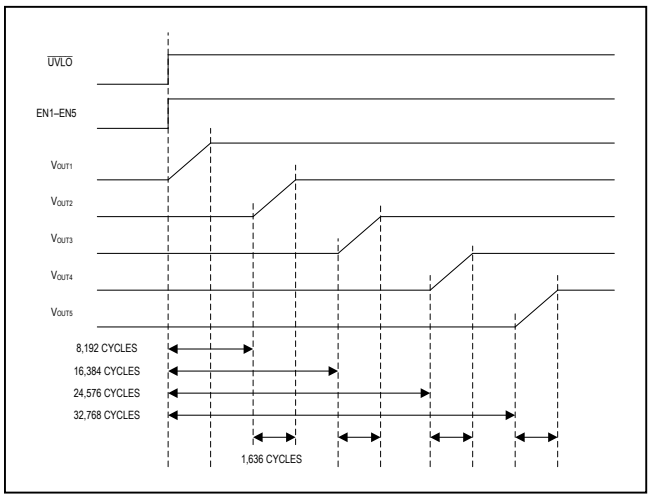


Figure 2. Startup Sequence for MAX20026

Hybrid Load-Line Architecture

The step-down converters feature hybrid load-line architecture to reduce the output capacitance needed, potentially saving system cost and size. This results in a measurable load-transient response.

Input Overvoltage Monitoring (OVM)

The PMICs feature an input circuit (OVM) on the input supply. When the input exceeds 5.8V (typ), the power-good indicator (PGOOD) goes low and the device outputs shut down to protect the PMIC. When the input supply returns to within the operating range of 5.7V (typ) or less, the IC initiates a soft-start sequence for outputs with EN_ high.

Input Undervoltage Monitoring (UVM)

The PMICs feature an input circuit (UVM) on the input supply. When the input drops below 4.3V (typ), PGOOD goes low to indicate a potential brownout condition. The device remains operational down to the UVLO threshold. When the input voltage exceeds the UV threshold above 4.4V (typ), PGOOD remains low for an active timeout period.

Input Undervoltage Lockout (UVLO)

The PMICs feature an undervoltage lockout on the PV_ inputs set at 2.77V (typ) falling. This prevents loss of control of the device by shutting down all outputs. This circuit is only active when at least one buck converter or the linear regulator is enabled.

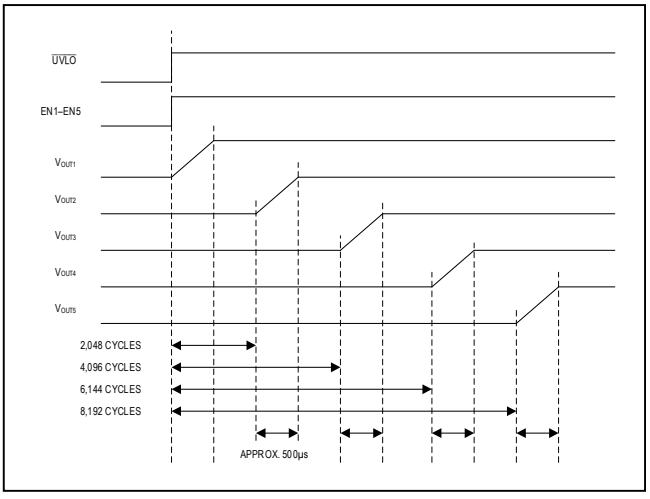


Figure 3. Startup Sequence for MAX20026S

Power-Good Outputs (PGOOD)

The PMICs feature an open-drain power-good output. PGOOD asserts when an enabled output voltage drops 6% below the regulated voltage, or 10% above the regulated voltage for approximately 15µs. PGOOD remains asserted for a fixed 20,480 switching cycles after the output returns to its regulated voltage. Connect PGOOD to a logic supply with a 10kΩ resistor.

Soft-Start

The PMICs include a fixed-duration soft-start time. The soft-start time limits startup inrush current by forcing the output voltage to ramp up towards its regulation point. During soft-start, the converters operate in skip mode to prevent the outputs from discharging.

When the PMICs exit undervoltage lockout, overvoltage lockout, or thermal-shutdown conditions, there is a fixed blanking time for EN2–EN5 to prevent all outputs from going through soft-start at the same time. After 32,768 switching cycles with $\overline{UVLO}$ high and at least one buck converter enabled, there is no blanking time between EN2–EN5 high and the start of soft-start.

Synchronization (SYNC)

The PMIC features a SYNC input to allow the internal oscillator to synchronize with an external clock. SYNC accepts signal frequencies in the range of 2.7MHz < f_{SYNC} < 3.5MHz. Connect SYNC to GND if the SYNC feature is not used.

Current Limit/Short-Circuit Protection

The PMICs offer a current-limit feature that protects them against short-circuit and overload conditions at an output. In the event of a short-circuit or overload condition at an output, the high-side MOSFET remains on until the inductor current reaches the high-side MOSFET's current-limit threshold. The converter then turns on the low-side MOSFET and the inductor current ramps down. The converter allows the high-side MOSFET to turn on only when the inductor current ramps down to the low-side MOSFET's current threshold. This cycle repeats until the short or overload condition is removed.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the PMICs. When the junction temperature exceeds +175°C (typ), an internal thermal sensor shuts down the step-down converters, allowing the IC to cool. The thermal sensor turns the IC on again after the junction temperature cools by 15°C and the IC goes through a standard power-up sequence, as defined in the *Soft-Start* section.

Applications Information

Step-Down Converter (Inductor Selection)

The step-down converters are optimized for use with a 1.5µH inductor.

Step-Down Converter (Input Capacitor)

The step-down converters are designed to operate with a single 2.2µF ceramic bypass capacitor on each PV_ input. Phase interleaving of the four buck converters contributes to a lower required input capacitance by canceling input-ripple currents. Place the bypass capacitors as close as possible to their corresponding PV_ input to ensure the best EMI and jitter performance.

Step-Down Converter (Output Capacitor)

All step-down converter outputs are optimized for use with a 10µF X7R ceramic capacitor. Additional output capacitance can be used if better voltage ripple or load-transient response is required. Due to the soft-start sequence, the device is unable to drive arbitrarily large output capacitors.

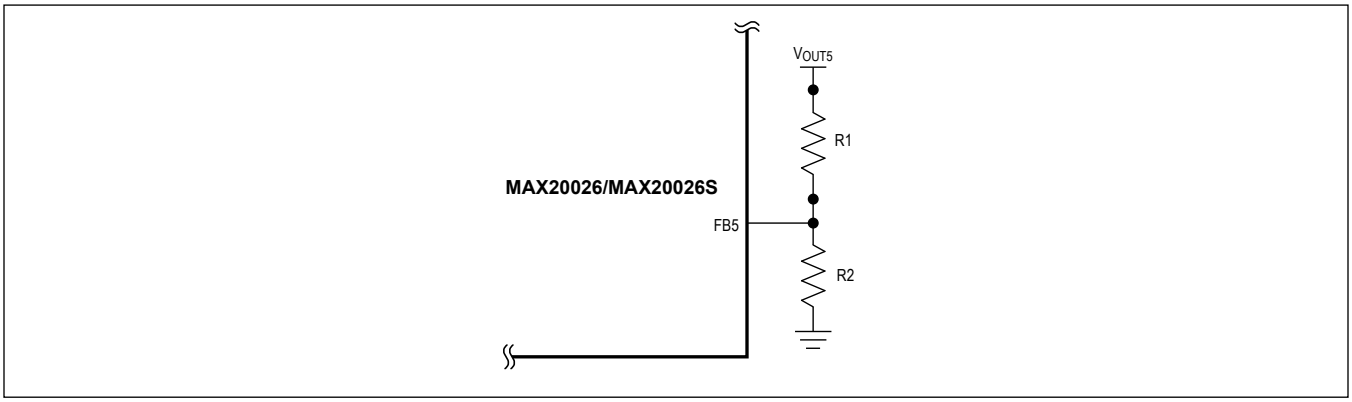


Figure 4. Adjustable Output-Voltage Configuration

LDO (Adjustable Output Voltage)

The MAX20026/MAX20026S features an adjustable output voltage for the LDO, which allows the customer to set the output to any voltage between 1.25V and 3.3V (for MAX20026) or between 1.015V and 3.3V (for MAX20026S). Connect a resistive divider from output (V_{OUT5}) to FB5 to GND to set the output voltage. Select R2 (FB5 to the GND resistor) ≤ 100kΩ. Calculate R1 (V_{OUT5} to the V_{FB5} resistor) with the following equation:

$$R1 = R2\left[\left(\frac{V_{OUT5}}{V_{FB5}}\right) - 1\right]$$

where $\mathbf{V_{FB5}}$ = 1250mV for MAX20026 and 1015mV for MAX20026S (see the *Electrical Characteristics* table).

LDO (Input Capacitor)

The LDO is designed to operate with a single 1µF ceramic bypass capacitor on the PV5 input. Place the bypass capacitor as close as possible to the PV5 input to ensure the best performance.

LDO (Output Capacitor)

The LDO preset output voltage is optimized for use with a 4.7µF X7R ceramic capacitor for MAX20026 or two 4.7µF X7R ceramic capacitors for MAX20026S. If a lower output current is required, a smaller output capacitor can be used (see Table 1).

Table 1. Recommended Output Capacitor

V_{OUT5} (V)	I_{LOAD} (mA)	OUTPUT CAPACITOR (µF)	CONFIGURATION
2.5	50	2.2	Internal FB5
2.5	100	2.2	
2.5	200	4.7	
1.25	50	10	External FB5
1.25	100	10	
1.25	200	10	
3.3	50	4.7	External FB5
3.3	100	4.7	
3.3	200	4.7	

Thermal Considerations

How much power the package can dissipate strongly depends on the mounting method of the IC to the PCB and the copper area for cooling. Using the JEDEC test standard, the maximum power dissipation allowed is 2285mW in the TQFN package. More power dissipation can be handled by the package if great attention is given during PCB layout. For example, using the top and bottom copper as a heatsink and connecting the thermal vias to one of the middle layers (GND) transfers the heat from the package into the board more efficiently, resulting in lower junction temperature at high power dissipation in some PMIC applications. Furthermore, the solder mask around the IC area on both top and bottom layers can be removed to radiate the heat directly into the air. The maximum allowable power dissipation in the IC is given in the following equation:

$$P_{MAX} = \frac{\left(T_{J(MAX)} - T_A\right)}{\theta_{JC} + \theta_{CA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature (+150°C), T_A is the ambient air temperature, θ_{JC} (3°C/W for the 28-pin TQFN) is the thermal resistance from the junction to the case, and θ_{CA} is the thermal resistance from the case to the surrounding air through the PCB, copper traces, and the package materials. θ_{CA} is directly related to system-level variables and can be modified to increase the maximum power dissipation. The TQFN package has an exposed thermal pad on its underside. This pad provides a low thermal-resistance path for heat transfer into the PCB. This low thermally resistive path carries a majority of the heat away from the IC. The PCB is effectively a heatsink for the IC. The exposed pad should be connected to a large ground plane for proper thermal and electrical performance. The minimum size of the ground plane is dependent upon many system variables. To create an efficient path, the exposed pad should be soldered to a thermal landing connected to the ground plane by thermal vias. The thermal landing should be at least as large as the exposed pad and can be made larger depending on the amount of free space from the exposed pad to the other pin landings. A sample layout is available on the MAX20026 evaluation kit to speed designs.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1) Use a large contiguous copper plane under the PMIC packages. Ensure that all heat-dissipating components have adequate cooling.
2) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high current path

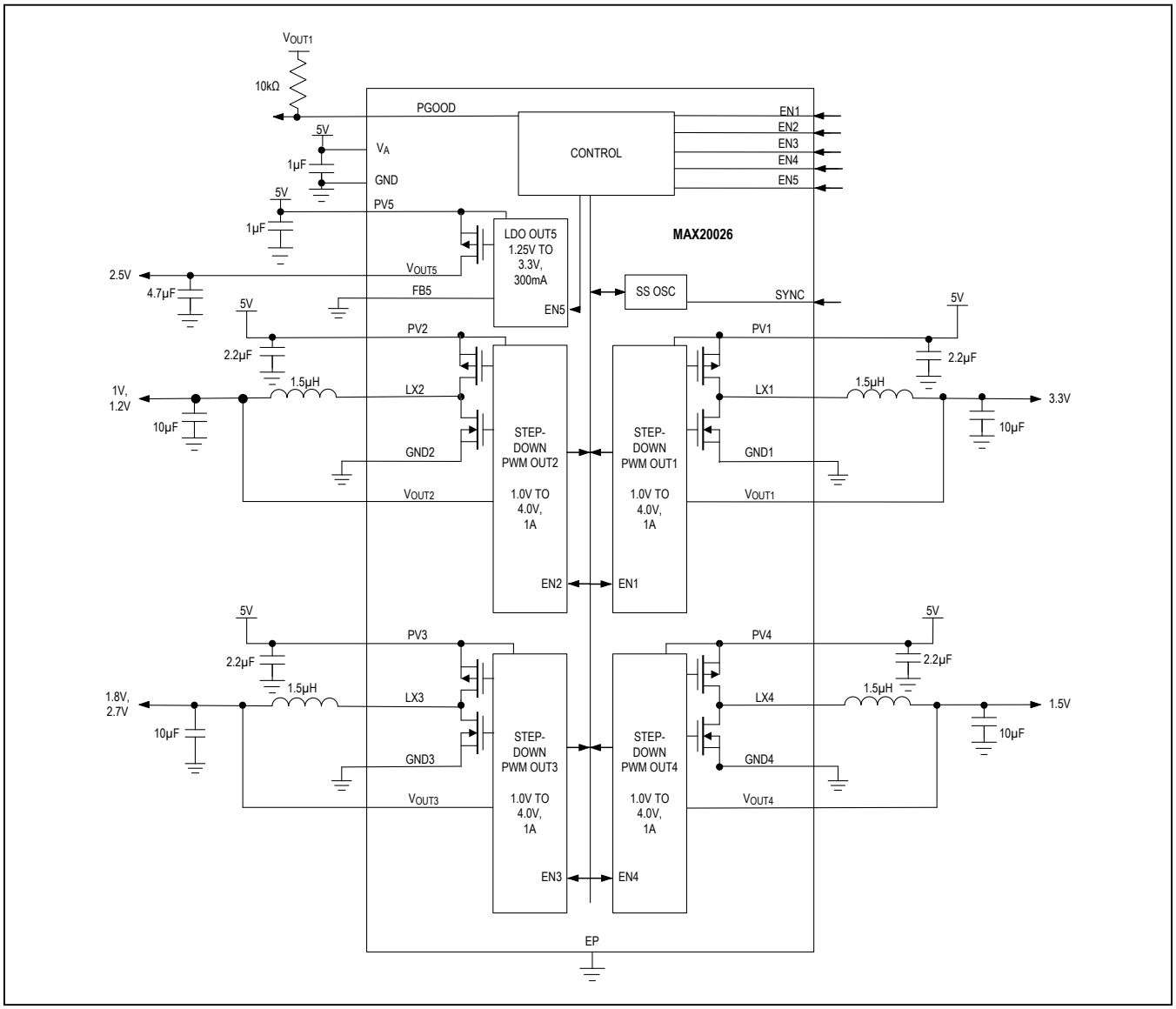


Figure 5. Typical Operating Circuit

comprising input capacitor, inductor, and the output capacitor should be as short as possible.

3) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
4) Use a single ground plane to reduce the chance of ground-potential differences. With a single ground plane, enough isolation between analog return signals and high-power signals must be maintained.
5) See Figure 6 for component placement. Input capacitors, CIN, (C6, C7, C8, and C9) are placed near the IC. The VA capacitor (C5) is placed next to the IC at pins 24 and 26. Inductors (L1, L2, L3, and L4) are placed next to the input capacitors. Output capacitors (C1, C, C3, and C4) are next to the inductors. These placements ensure short traces for power and grounding.

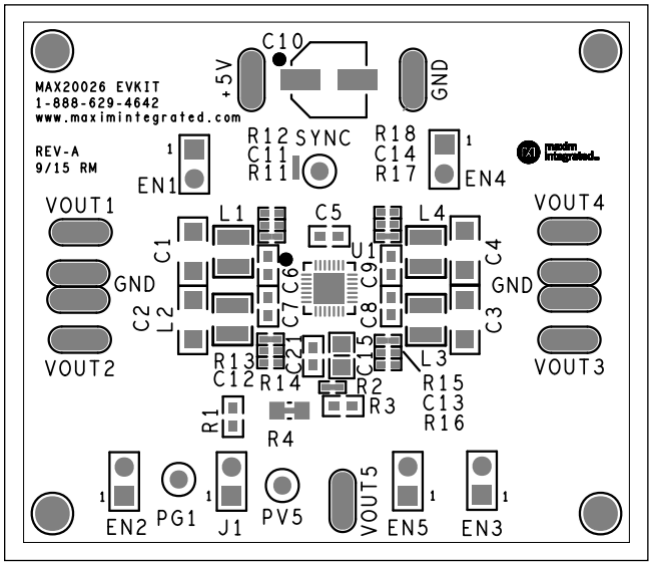


Figure 6. Component Placement

Selector Guide*

PART	CURRENT CONFIGURATION				DC-DC1	DC-DC2	DC-DC3	DC-DC4	LDO5	SPREAD SPECTRUM
	CH1	CH2	CH3	CH4	$V_{OUT\_}$ (V)					
MAX20026ATIA/V+	1.0A	1.0A	1.0A	1.0A	3.30	1.00	1.80	1.50	2.50	Disabled
MAX20026ATIB/V+	1.0A	1.0A	1.0A	1.0A	3.30	1.20	2.70	1.50	2.50	Disabled
MAX20026ATIC/V+	1.0A	1.0A	1.0A	1.0A	3.30	1.20	1.80	1.50	2.50	Disabled
MAX20026ATID/V+	1.0A	1.0A	1.0A	1.0A	3.30	ADJ	ADJ	1.35	ADJ	Disabled
MAX20026SATIE/V+	1.0A	1.0A	1.0A	1.0A	3.30	ADJ	ADJ	1.35	ADJ	Disabled

**Contact factory for options that are not included. Factory-selectable features include:*

- *DC-DC output voltages in 50mV steps between 1.0V and 4.0V (for MAX200026) or between 0.8V and 3.8V (for MAX20026S).*
- *Spread spectrum enabled or disabled.*
- *LDO output voltage 1.25V (min) for MAX20026 or 1V (min) for MAX20026S.*

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20026ATI_/V+	-40°C to +125°C	28 TQFN-EP*
MAX20026ATI_/V+T	-40°C to +125°C	28 TQFN-EP*
MAX20026SATIE/V+	-40°C to +125°C	28 TQFN-EP*

Note: *Insert the desired suffix letter (from the* Selector Guide*) into the blank area "_" to indicate factory-selectable features.*

/V denotes an automotive qualified part that conforms to AEC-Q100.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TQFN-EP	T2844+1C	21-0139	90-0035

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/16	Initial release	—
1	1/17	Added MAX20026ATIC/V+ to *Selector Guide* as a future product	17
2	5/17	Update min/max values for FB5 Regulated Voltage in *Electrical Characteristics*, and removed future product status from MAX20026ATIC/V+ in *Selector Guide*	3, 17
3	9/17	Updated FB5 and OUT5 Regulated Voltage in *Electrical Characteristics* and added MAX20026ATID/V+ in *Selector Guide*	3, 17
4	1/19	Updated *Electrical Characteristics, Applications Information, Selector Guide,* and *Ordering Information* to add MAX20026S	2–5, 15–18
5	2/19	Updated Soft-Start Ramp Time and Undervoltage Threshold in *Electrical Characteristics*	4
6	3/19	Added MAX20026S to all part references and added MAX20026S voltage values to *Selector Guide*	1–18