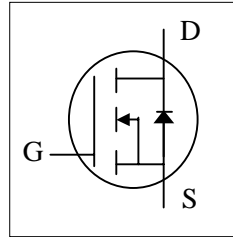


- ▼ Simple Drive Requirement
- ▼ SO-8 Compatible with Heatsink
- ▼ Low On-resistance
- ▼ RoHS Compliant & Halogen-Free

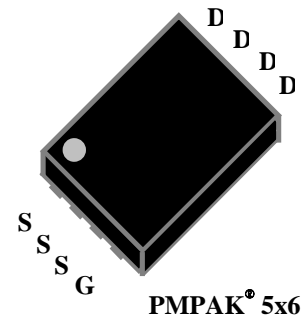


$BV_{DSS}$	40V
$R_{DS(ON)}$	5.5mΩ
$I_D$	75A

### Description

XP0504 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK<sup>®</sup> 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.



### Absolute Maximum Ratings @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	+20	V
$I_D@T_C=25^\circ\text{C}$	Drain Current (Chip)	75	A
$I_D@T_A=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	23.6	A
$I_D@T_A=70^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	19	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	300	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	56.8	W
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation	5	W
$E_{AS}$	Single Pulse Avalanche Energy <sup>4</sup>	28.8	mJ
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

### Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	2.2	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	25	$^\circ\text{C}/\text{W}$

**Electrical Characteristics @ $T_j=25^{\circ}\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=30A$	-	-	5.5	m $\Omega$
		$V_{GS}=4.5V, I_D=20A$	-	-	8	m $\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
$g_{fs}$	Forward Transconductance	$V_{DS}=10V, I_D=20A$	-	70	-	S
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=40V, V_{GS}=0V$	-	-	10	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge	$I_D=20A$	-	20	32	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=20V$	-	4	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	11	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=20V$	-	9	-	ns
$t_r$	Rise Time	$I_D=1A$	-	7	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	25	-	ns
$t_f$	Fall Time	$R_D=20\Omega$	-	29	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	1640	2620	pF
$C_{oss}$	Output Capacitance	$V_{DS}=25V$	-	340	-	pF
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	180	-	pF

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=20A, V_{GS}=0V$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_S=10A, V_{GS}=0V,$	-	31	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	29	-	nC

**Notes:**

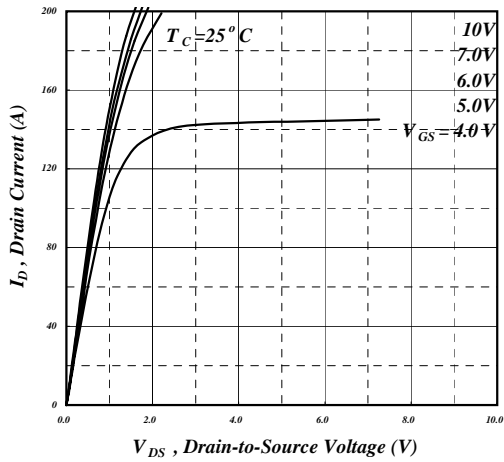
1. Pulse width limited by Max. junction temperature
2. Pulse test
3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board,  $t \leq 10\text{sec}$ ,  $60^{\circ}\text{C/W}$  at steady state.
4. Starting  $T_j=25^{\circ}\text{C}$ ,  $V_{DD}=30V$ ,  $L=0.1\text{mH}$ ,  $R_G=25\Omega$ ,  $I_{AS}=24A$ .

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

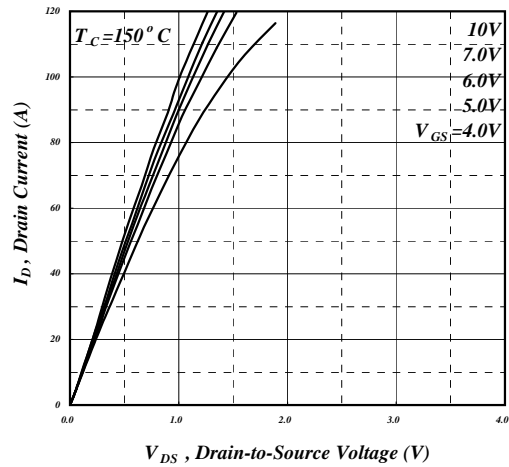
USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

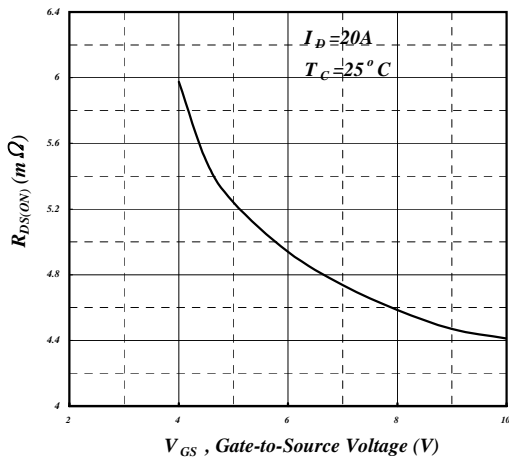
XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



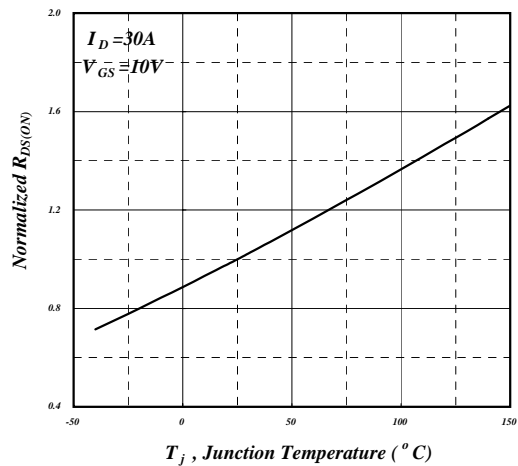
**Fig 1. Typical Output Characteristics**



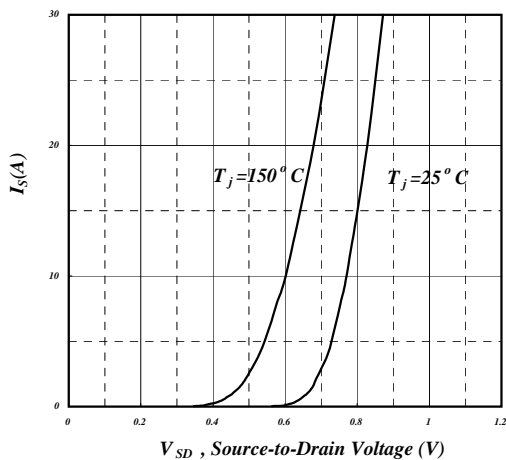
**Fig 2. Typical Output Characteristics**



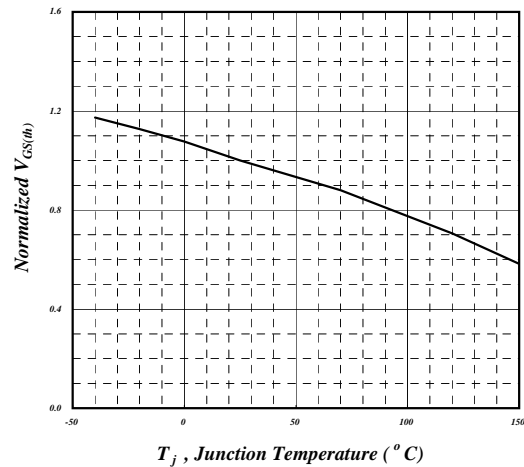
**Fig 3. On-Resistance v.s. Gate Voltage**



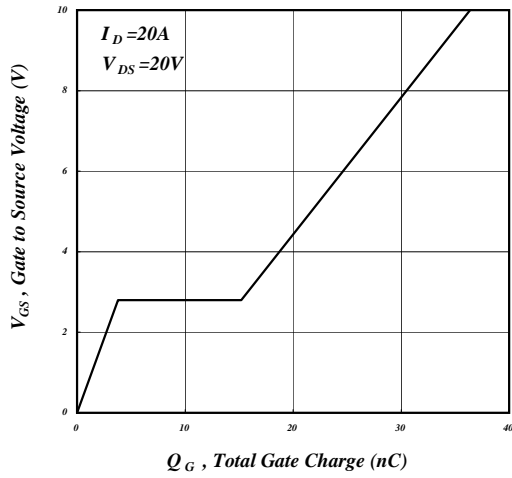
**Fig 4. Normalized On-Resistance v.s. Junction Temperature**



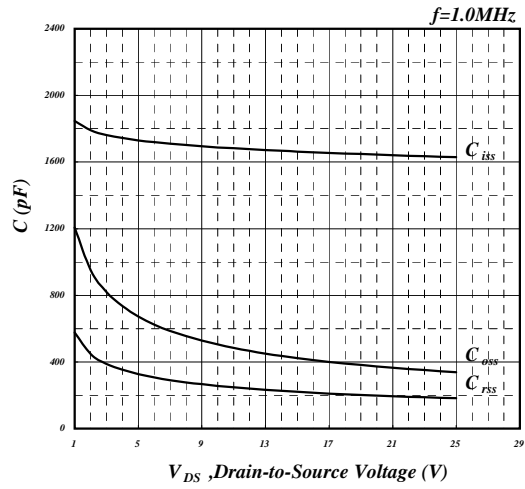
**Fig 5. Forward Characteristic of Reverse Diode**



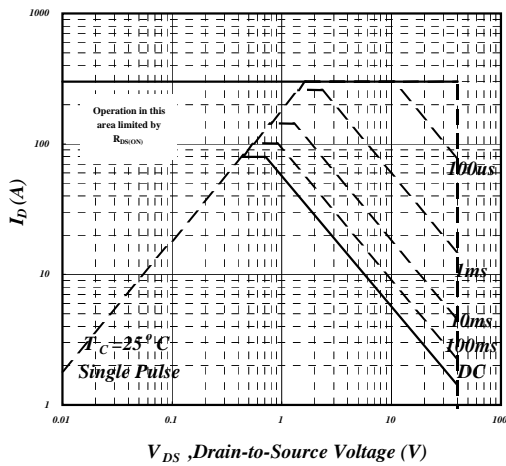
**Fig 6. Gate Threshold Voltage v.s. Junction Temperature**



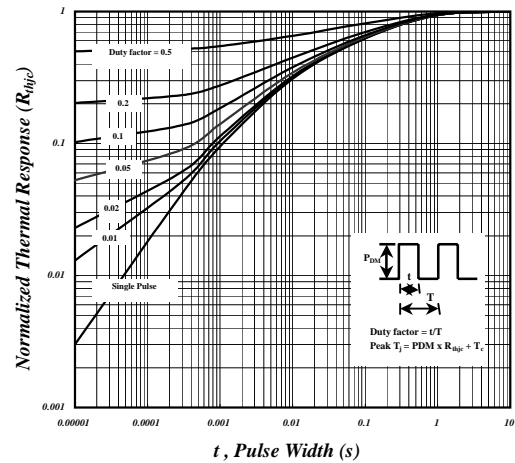
**Fig 7. Gate Charge Characteristics**



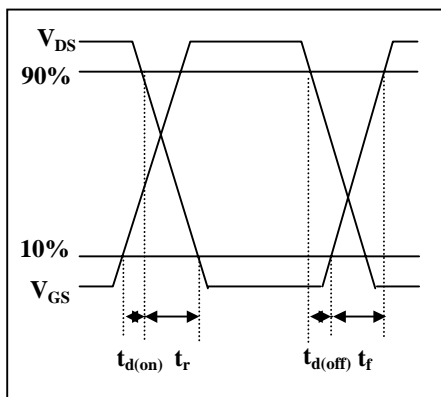
**Fig 8. Typical Capacitance Characteristics**



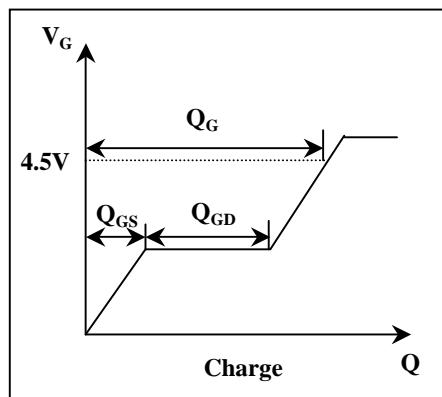
**Fig 9. Maximum Safe Operating Area**



**Fig 10. Effective Transient Thermal Impedance**



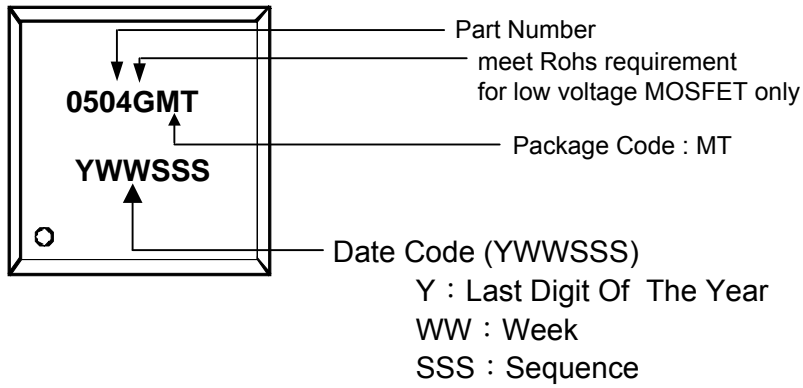
**Fig 11. Switching Time Waveform**



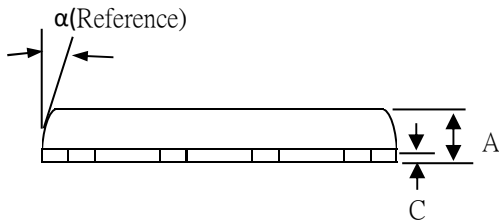
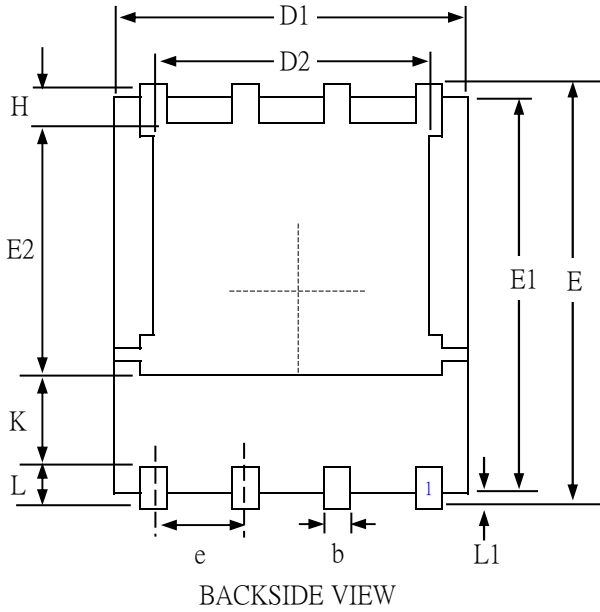
**Fig 12. Gate Charge Waveform**

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**MARKING INFORMATION**



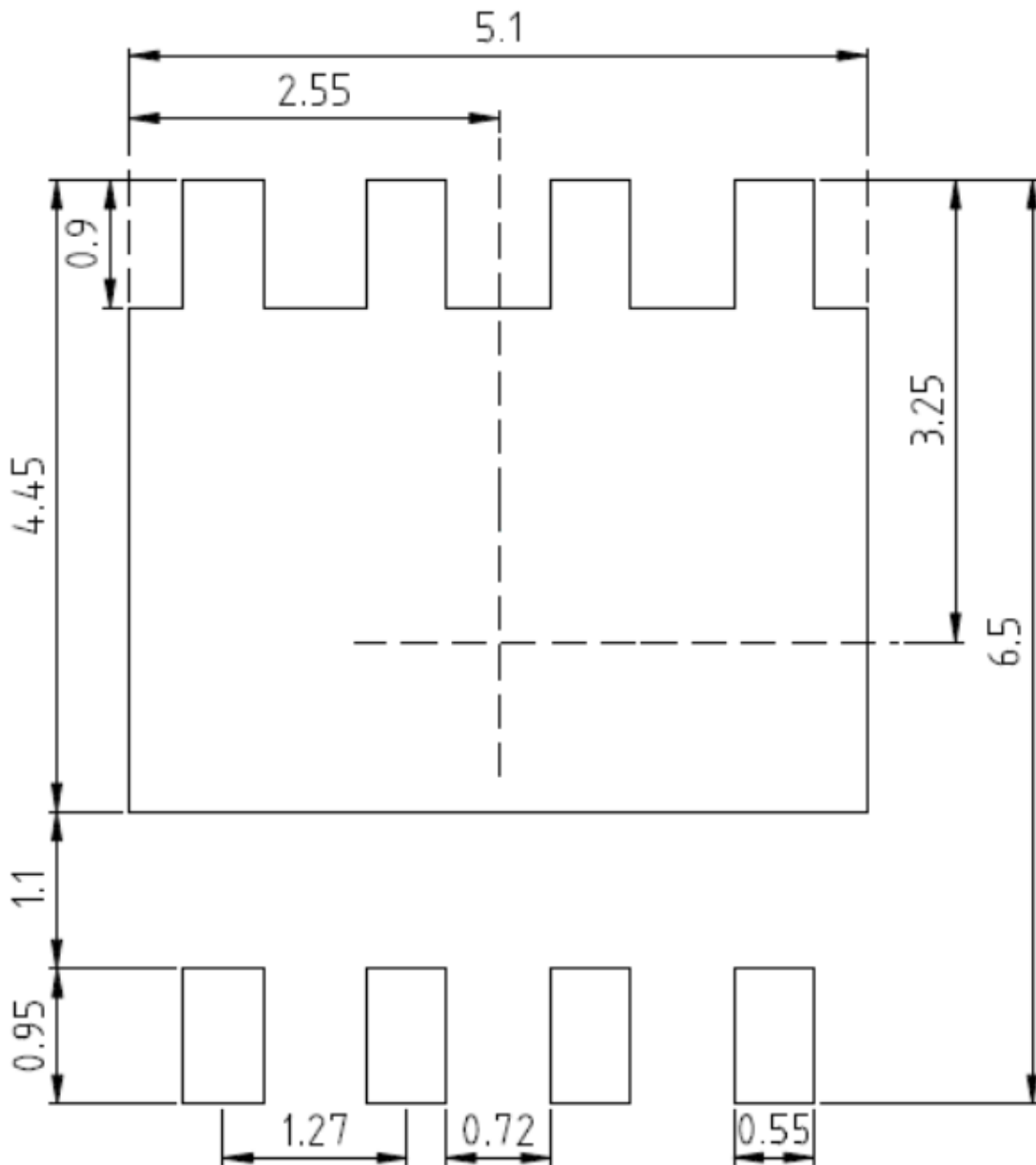
**Package Outline : PMPAK 5x6**



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.90	1.10	1.30
b	0.33	0.41	0.51
C	0.254(Ref.)		
D1	4.80	4.90	5.10
D2	3.61	4.00	4.40
E	5.80	6.03	6.25
E1 (Ref.)	5.60	5.75	5.90
E2 (Ref.)	3.30	3.55	3.80
e	1.27 BSC		
H	0.35	—	0.90
K (Ref.)	1.00	1.275	—
L	0.35	0.55	0.75
L1	0.06	0.13	0.20
$\alpha$ (Ref.)	0°	—	12°

- 1.All dimension are in millimeters.
- 2.Dimension does not include burrs and mold flash/protrusions.
- 3.The outline schematic is not to scale and slightly different from the actual product appearance.

**PMPAK 5X6(E-TYPE) FOOTPRINT :**



UNIT: mm