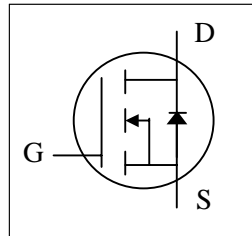
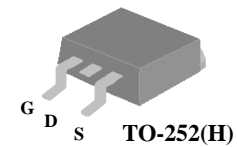


- ▼ 100% R<sub>g</sub> & UIS Test
- ▼ Simple Drive Requirement
- ▼ Lower On-resistance
- ▼ RoHS Compliant & Halogen-Free



BV <sub>DSS</sub>	100V
R <sub>DS(ON)</sub>	24mΩ
I <sub>D</sub>	25.8A



### Description

XP10N024 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

TO-252 package is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for high current application due to the low connection resistance.

### Absolute Maximum Ratings @T<sub>j</sub>=25°C (unless otherwise specified)

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	100	V
V <sub>GS</sub>	Gate-Source Voltage	+20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Drain Current, V <sub>GS</sub> @ 10V	25.8	A
I <sub>D</sub> @T <sub>C</sub> =100°C	Drain Current, V <sub>GS</sub> @ 10V	16.3	A
I <sub>DM</sub>	Pulsed Drain Current <sup>1</sup>	100	A
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation	31.2	W
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation	2	W
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>4</sup>	16.2	mJ
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C

### Thermal Data

Symbol	Parameter	Value	Units
R <sub>thj-c</sub>	Maximum Thermal Resistance, Junction-case	4	°C/W
R <sub>thj-a</sub>	Maximum Thermal Resistance, Junction-ambient (PCB mount) <sup>3</sup>	62.5	°C/W

**Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=12A$	-	-	24	m $\Omega$
		$V_{GS}=5V, I_D=6A$	-	-	40	m $\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	-	3	V
$g_{fs}$	Forward Transconductance	$V_{DS}=10V, I_D=12A$	-	20	-	S
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=80V, V_{GS}=0V$	-	-	25	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
$Q_g$	Total Gate Charge	$I_D=6A$	-	14.5	23.2	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=50V$	-	5	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=5V$	-	7	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=50V$	-	10	-	ns
$t_r$	Rise Time	$I_D=12A$	-	21	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega$	-	22	-	ns
$t_f$	Fall Time	$V_{GS}=10V$	-	6	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	1350	2160	pF
$C_{oss}$	Output Capacitance	$V_{DS}=50V$	-	185	-	pF
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	10	-	pF
$R_g$	Gate Resistance	$f=1.0\text{MHz}$	-	1.6	3.2	$\Omega$

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=12A, V_{GS}=0V$	-	-	1.3	V
$t_{rr}$	Reverse Recovery Time	$I_S=12A, V_{GS}=0V,$	-	55	-	ns
$Q_{rr}$	Reverse Recovery Charge	$dI/dt=100A/\mu s$	-	80	-	nC

**Notes:**

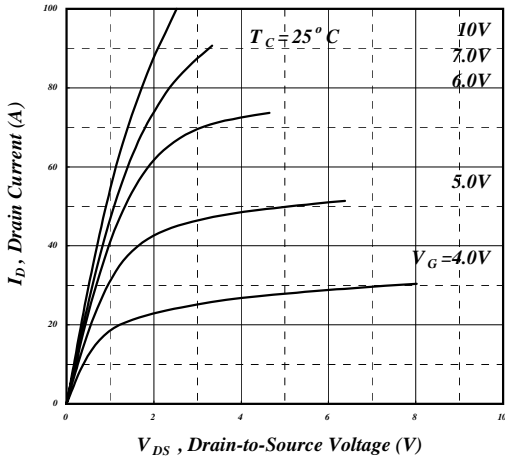
1. Pulse width limited by max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board
4. Starting  $T_j=25^{\circ}\text{C}$ ,  $V_{DD}=50V$ ,  $L=0.1\text{mH}$ ,  $R_G=25\Omega$ ,  $V_{GS}=10V$

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

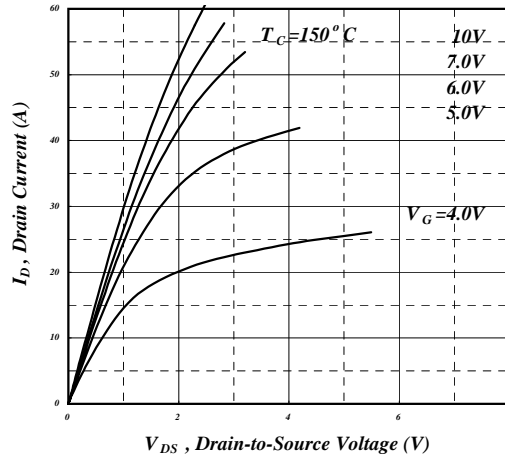
USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

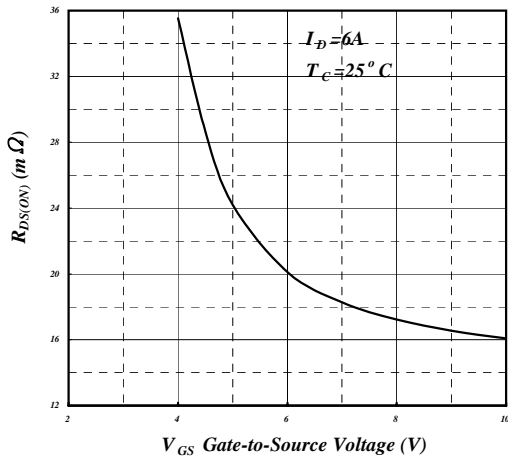
XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



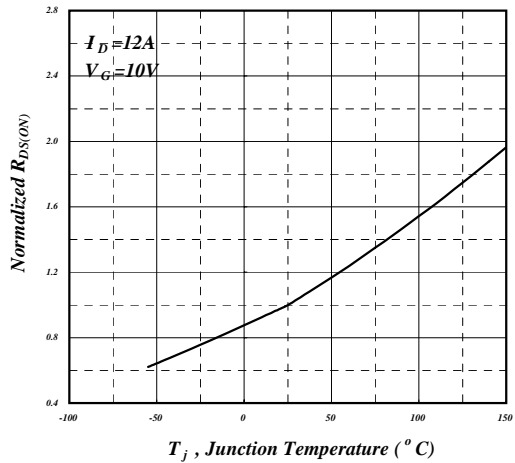
**Fig 1. Typical Output Characteristics**



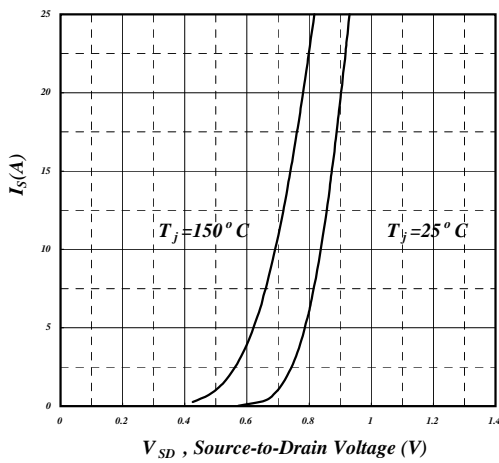
**Fig 2. Typical Output Characteristics**



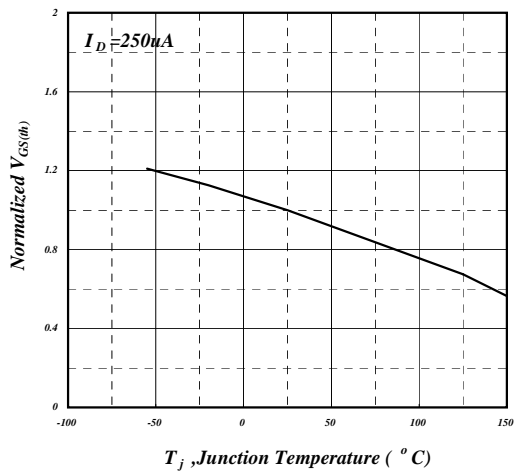
**Fig 3. On-Resistance v.s. Gate Voltage**



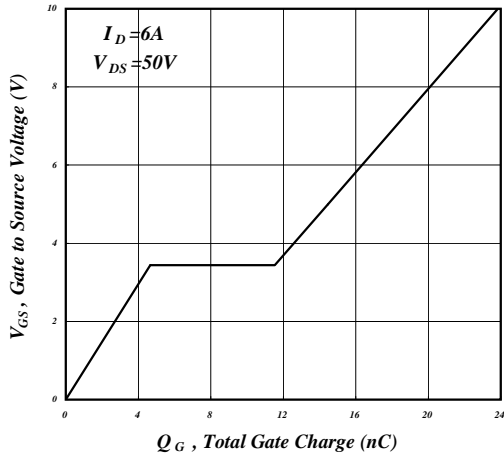
**Fig 4. Normalized On-Resistance v.s. Junction Temperature**



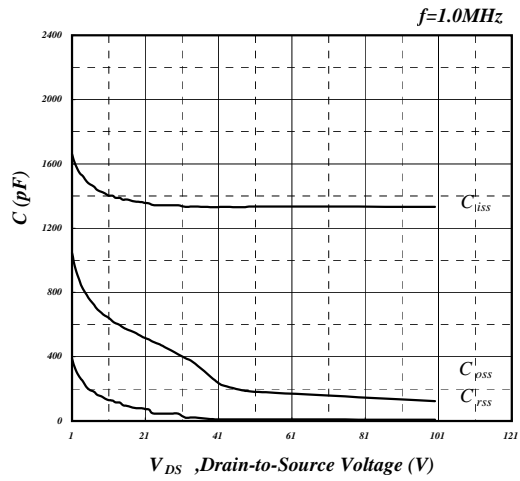
**Fig 5. Forward Characteristic of Reverse Diode**



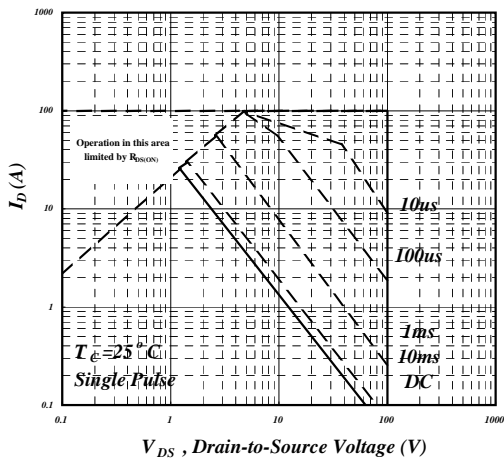
**Fig 6. Gate Threshold Voltage v.s. Junction Temperature**



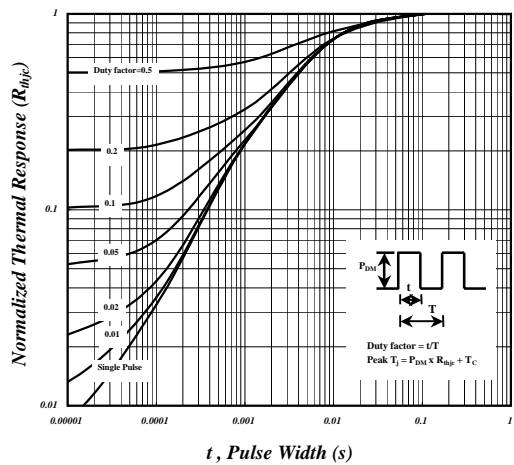
**Fig 7. Gate Charge Characteristics**



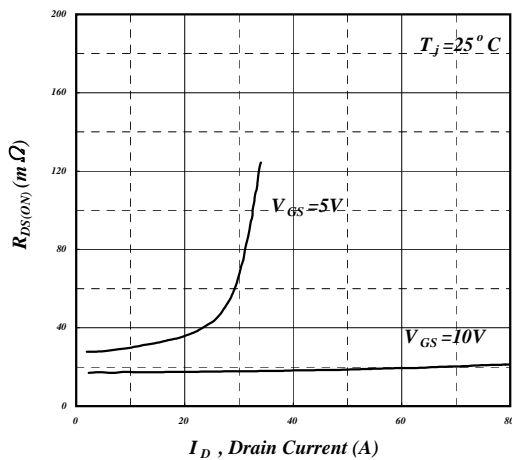
**Fig 8. Typical Capacitance Characteristics**



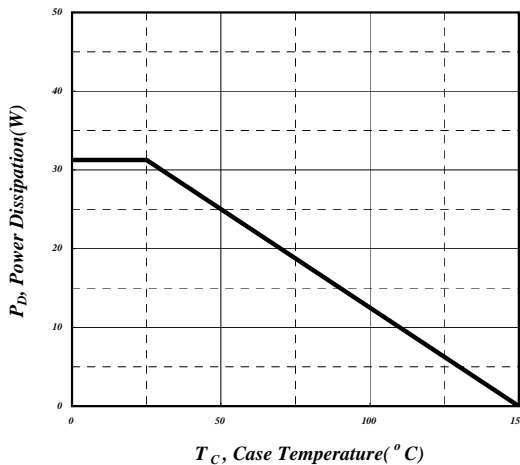
**Fig 9. Maximum Safe Operating Area**



**Fig 10. Effective Transient Thermal Impedance**



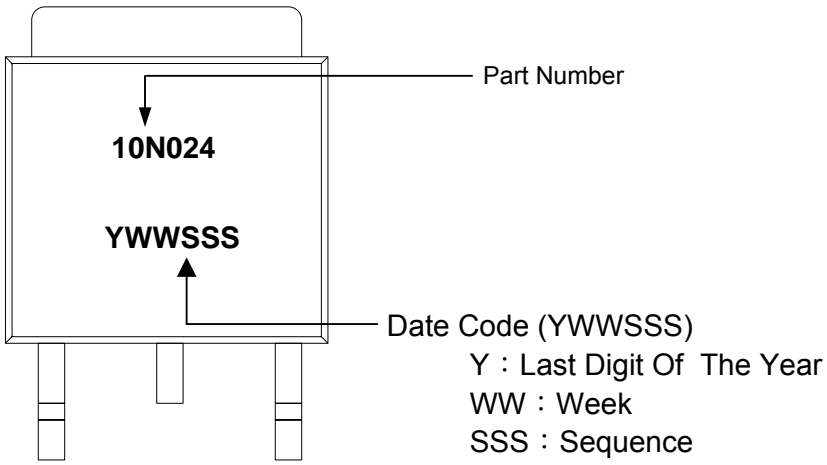
**Fig 11. Typ. Drain-Source on State Resistance**



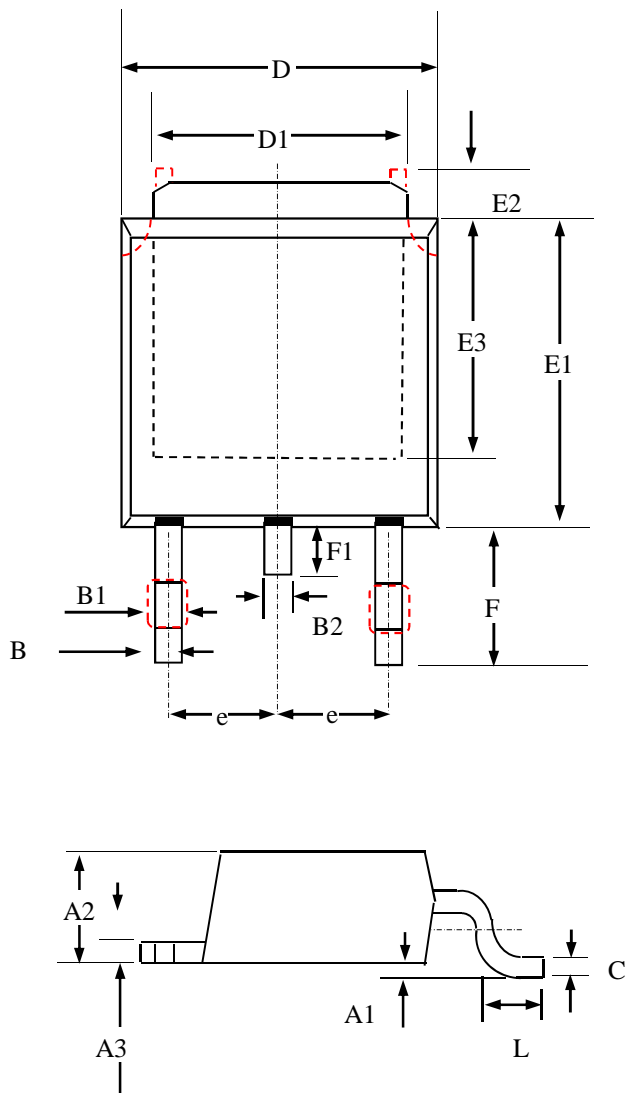
**Fig 12. Total Power Dissipation**

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**MARKING INFORMATION**



## Package Outline : TO-252



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A2	2.18	2.30	2.40
A3	0.40	0.50	0.65
B	0.40	0.70	1.00
B1	0.50	0.85	1.20
D	6.00	6.50	6.80
D1	4.80	5.35	5.90
E3	4.00 (ref.)		
F	2.00	2.63	3.05
F1	0.50	0.85	1.20
E1	5.00	5.70	6.30
E2	0.50	1.10	1.80
e	2.3 (ref)		
C	0.35	0.525	0.70
A1	0.00	—	0.25
B2	—	—	1.25
L	0.90	1.34	1.78

- 1.All Dimensions Are in Millimeters.
- 2.Dimension Does Not Include Mold Protrusions.
3. Thermal PAD, Body and Pin contour is for reference, it may has little difference by option.

**TO-252 FOOTPRINT :**

