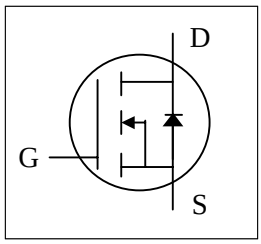
XP15NA3R9TL

Halogen-Free Product

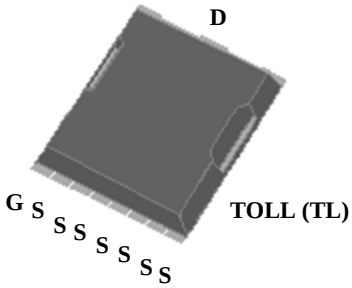
N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- **100% R_g & UIS Test**
- **Simple Drive Requirement**
- **Ultra Low On-resistance**
- **RoHS Compliant & Halogen-Free**



BV_{DSS}	150V
$R_{DS(ON)}$	3.9mΩ



Description

XP15NA3R9 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TOLL package is a perfect solution for high power density and high power efficiency application.

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	150	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V	191	A
I_D@T_C=100℃	Drain Current, V_{GS} @ 10V	135	A
I_{DM}	Pulsed Drain Current[1]	760	A
P_D@T_C=25℃	Total Power Dissipation	333.3	W
P_D@T_A=25℃	Total Power Dissipation[3]	3.75	W
E_{AS}	Single Pulse Avalanche Energy[5]	612.5	mJ
T_{STG}	Storage Temperature Range	-55 to 175	℃
T_J	Operating Junction Temperature Range	-55 to 175	℃

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	0.45	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient (PCB mount)[3]	40	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	150	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=50A	-	-	3.9	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2	-	4	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=50A	-	145	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=120V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}= ±20V, V_{DS}=0V	-	-	±0.1	uA
Q_g	Total Gate Charge[4]	I_D=50A	-	200	320	nC
Q_{gs}	Gate-Source Charge[4]	V_{DS}=75V	-	50	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge[4]	V_{GS}=10V	-	68	-	nC
$t_{d(on)}$	Turn-on Delay Time[4]	V_{DS}=75V	-	40	-	ns
t_r	Rise Time[4]	I_D=50A	-	126	-	ns
$t_{d(off)}$	Turn-off Delay Time[4]	R_G=6Ω	-	140	-	ns
t_f	Fall Time[4]	V_{GS}=10V	-	160	-	ns
C_{iss}	Input Capacitance[4]	V_{GS}=0V	-	9900	15840	pF
C_{oss}	Output Capacitance[4]	V_{DS}=100V	-	690	-	pF
C_{rss}	Reverse Transfer Capacitance[4]	f=1.0MHz	-	20	-	pF
R_g	Gate Resistance	f=1.0MHz	-	0.7	2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=50A, V_{GS}=0V	-	-	1.3	V
t_{rr}	Reverse Recovery Time[4]	I_S=50A, V_{GS}=0V	-	105	-	ns
Q_{rr}	Reverse Recovery Charge[4]	dI/dt=100A/μs	-	345	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board

4.Guaranteed by design.

5.Starting T_j=25°C , V_{DD}=50V , L=1mH , R_G=25Ω , V_{GS}=10V , I_{AS}=35A

6.These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.

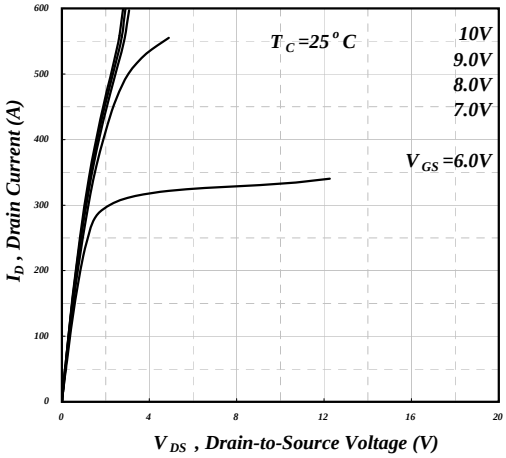


Fig 1. Typical Output Characteristics

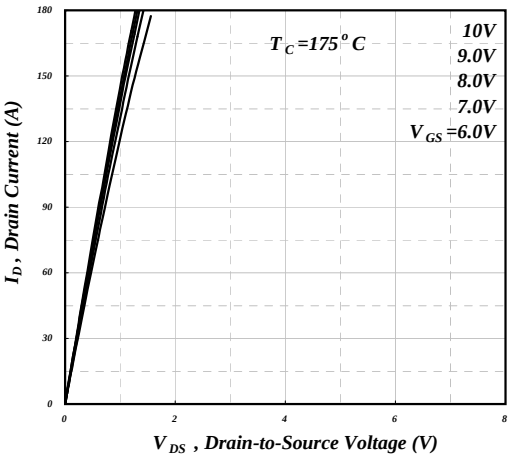


Fig 2. Typical Output Characteristics

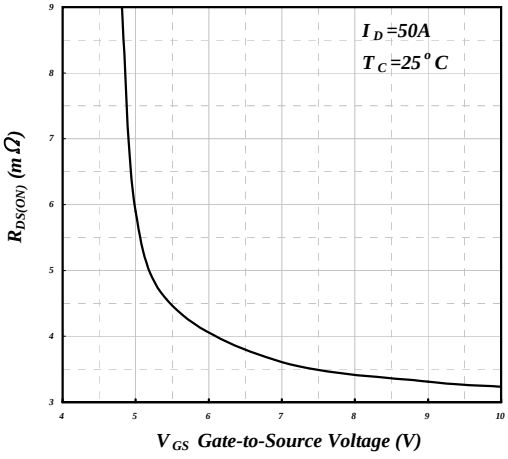


Fig 3. On-Resistance v.s. Gate Voltage

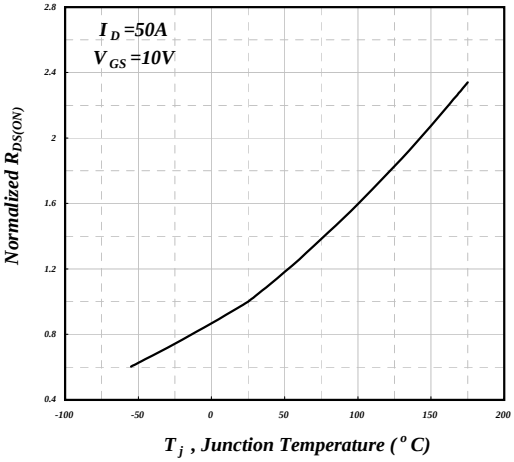


Fig 4. Normalized On-Resistance v.s. Junction Temperature

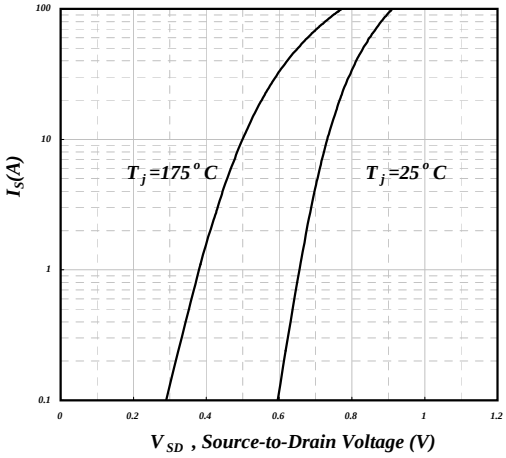


Fig 5. Forward Characteristic of Reverse Diode

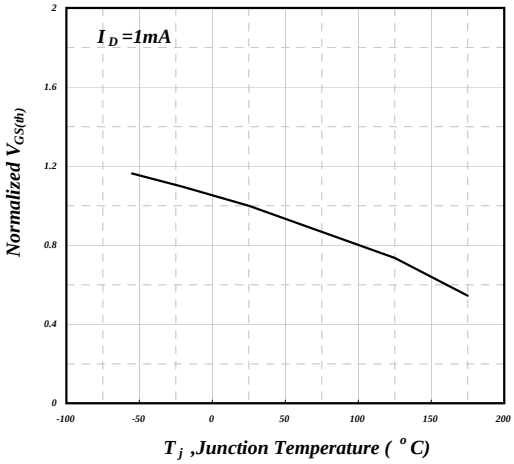


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

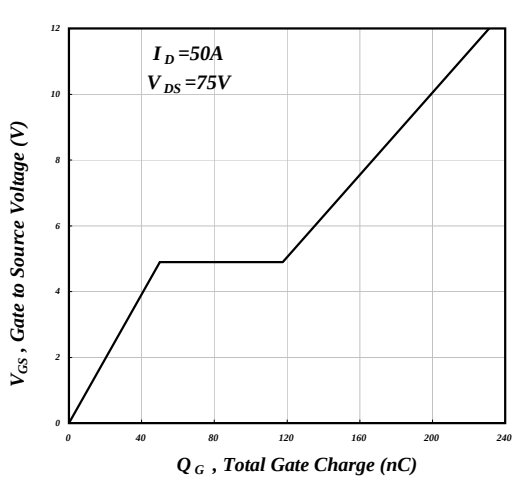


Fig 7. Gate Charge Characteristics

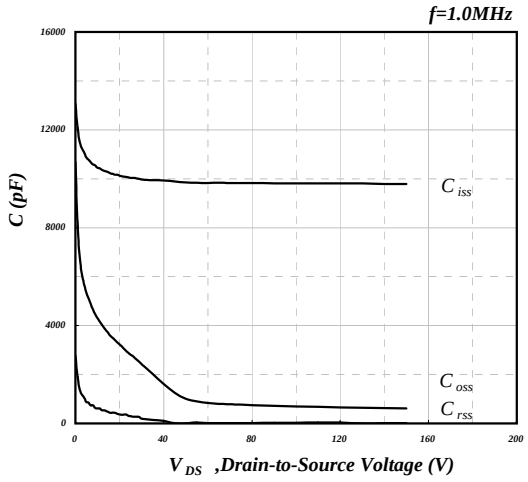


Fig 8. Typical Capacitance Characteristics

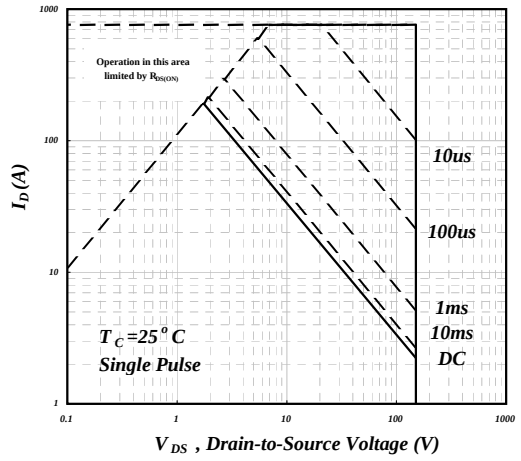


Fig 9. Maximum Safe Operating Area[6]

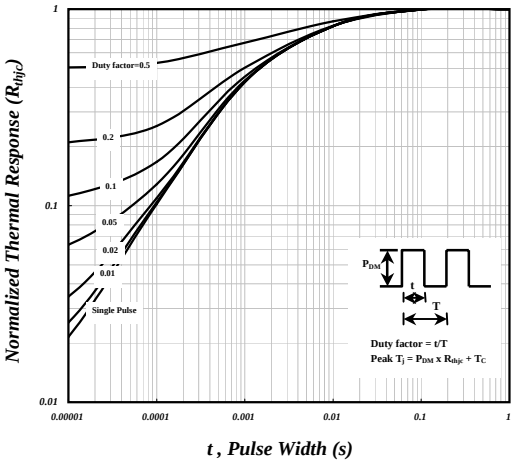


Fig 10. Effective Transient Thermal Impedance

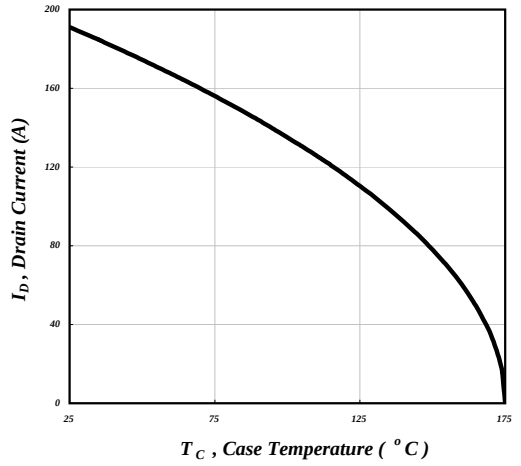


Fig 11. Drain Current v.s. Case Temperature

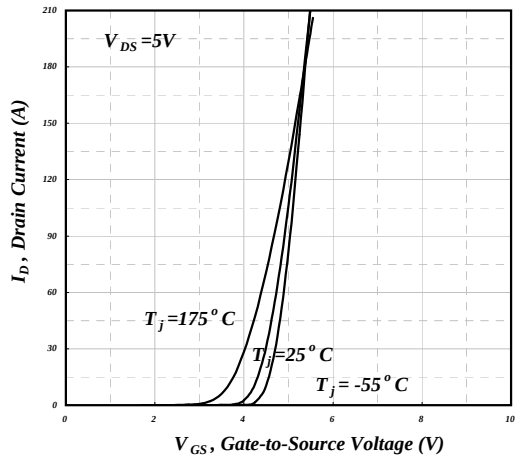


Fig 12. Transfer Characteristics

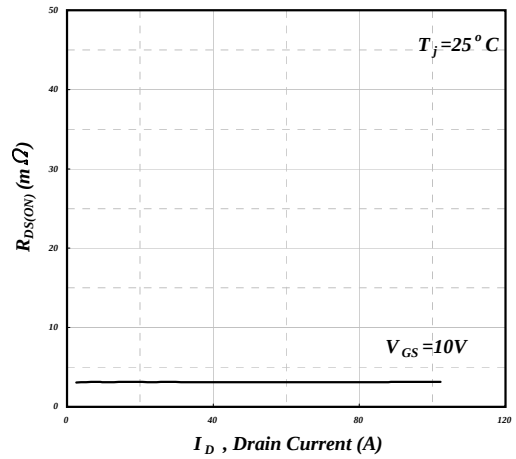


Fig 13. Typ. Drain-Source on State Resistance

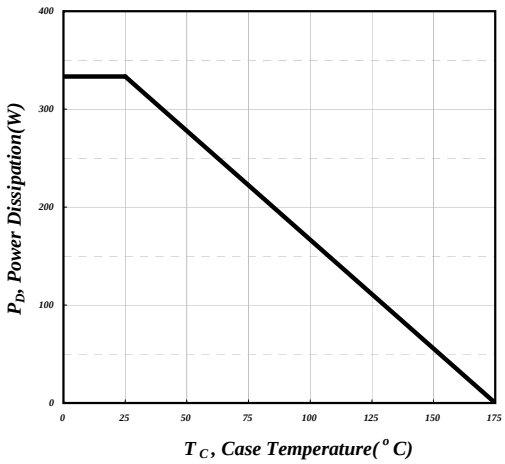


Fig 14. Total Power Dissipation

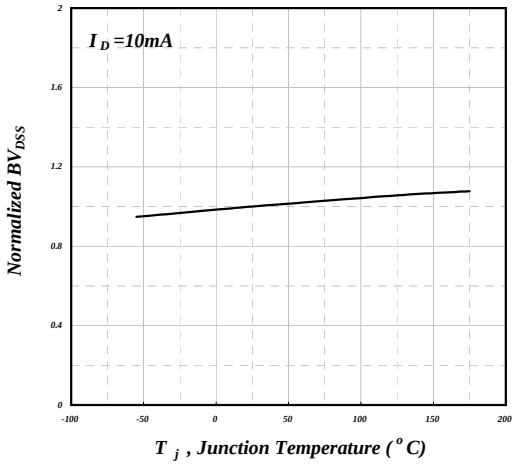
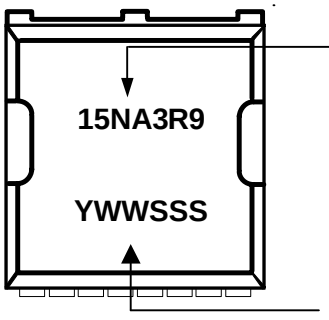


Fig 15. Normalized BV_{DSS} v.s. Junction Temperature

MARKING INFORMATION



Part Number

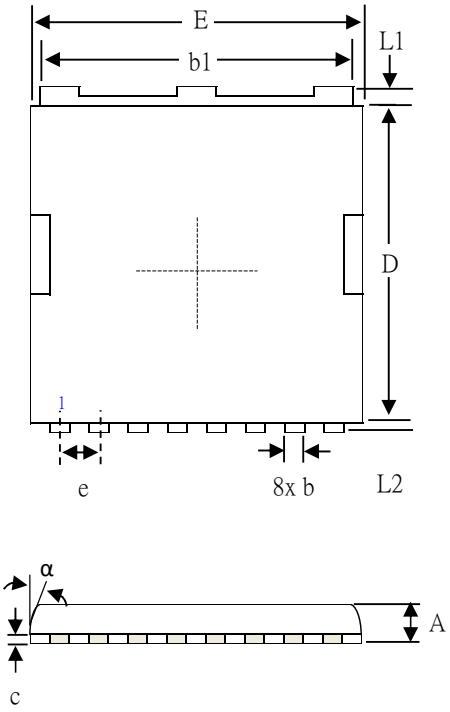
Date Code (YWWSSS)

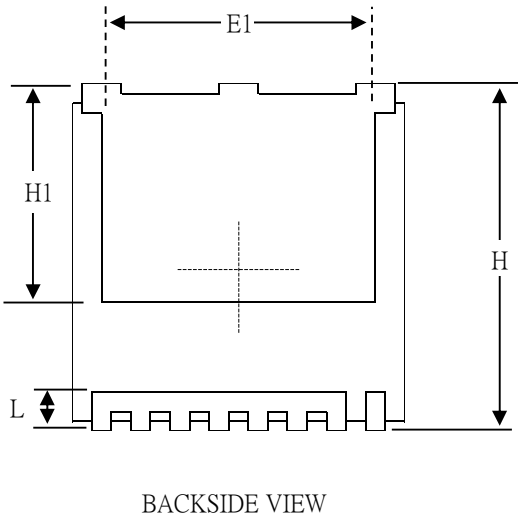
Y：Last Digit Of The Year

WW：Week

SSS：Sequence

Package Outline : TOLL





BACKSIDE VIEW

SYMBOLS	MIN	NOM	MAX
A	2.20	2.30	2.40
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
c	0.40	0.50	0.60
D	10.28	10.38	10.58
E	9.70	9.90	10.10
E1	7.90	8.70	9.50
e	1.20BCS		
H	11.48	11.68	11.88
H1	6.75	-	7.43
L	1.40	1.90	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
α	10° REF.		

1.All dimension are in millimeters.

2.Dimension does not include burrs and mold flash/protrusions.

3.The outline schematic is not to scale and slightly different from the actual product appearance.

Draw No. M1-TL-8-EFIM-G-V04

TOLL FOOTPRINT：