

# OPTIREG™ linear voltage regulator TLS830A4EPV50

## Ultra low quiescent current linear voltage regulator



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Technical documents



Simulation



Family overview



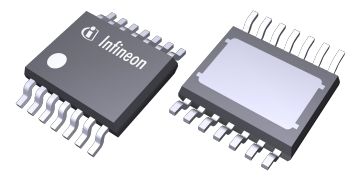
Support



RoHS

## Features

- Ultra low quiescent current, typically 4.3  $\mu\text{A}$  at light loads
- Wide input voltage range from 3.2 V to 40 V
- Output voltage 5 V
- Output voltage accuracy  $\pm 2\%$
- Output current capability up to 300 mA
- Low dropout voltage, typically 190 mV, at output current below 100 mA
- Stable with ceramic output capacitor of 4.7  $\mu\text{F}$
- Overtemperature shutdown
- Output current limitation
- Wide temperature range
- Green Product (RoHS compliant)



## Potential applications

- Automotive supply systems or other supply systems that are connected to the battery permanently
- Automotive systems that need to operate in cranking condition
- General automotive applications
- Automotive supply for CAN transceivers
- Remote keyless systems

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

## Description

The OPTIREG™ linear voltage regulator TLS830A4EPV50 is a linear voltage regulator with high performance, low dropout voltage and ultra low quiescent current. With only 4.3  $\mu\text{A}$  typical quiescent current at light load and an input voltage range of 3.2 V to 40 V the device is perfectly suitable for automotive supply systems or other supply systems that are permanently connected to the battery.

The loop concept combines fast regulation and very high stability while requiring only one small ceramic capacitor of 4.7  $\mu\text{F}$  at the output. The operating range starts at an input voltage of 3.2 V (extended operating range). This makes the device suitable for automotive systems that need to operate in cranking condition.

Internal protection features, such as output current limitation and overtemperature shutdown, are designed to protect the device from immediate damage caused by failures such as

- output shorted to GND

# OPTIREG™ linear voltage regulator TLS830A4EPV50

## Ultra low quiescent current linear voltage regulator

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### Description

- overcurrent condition
- overtemperature condition

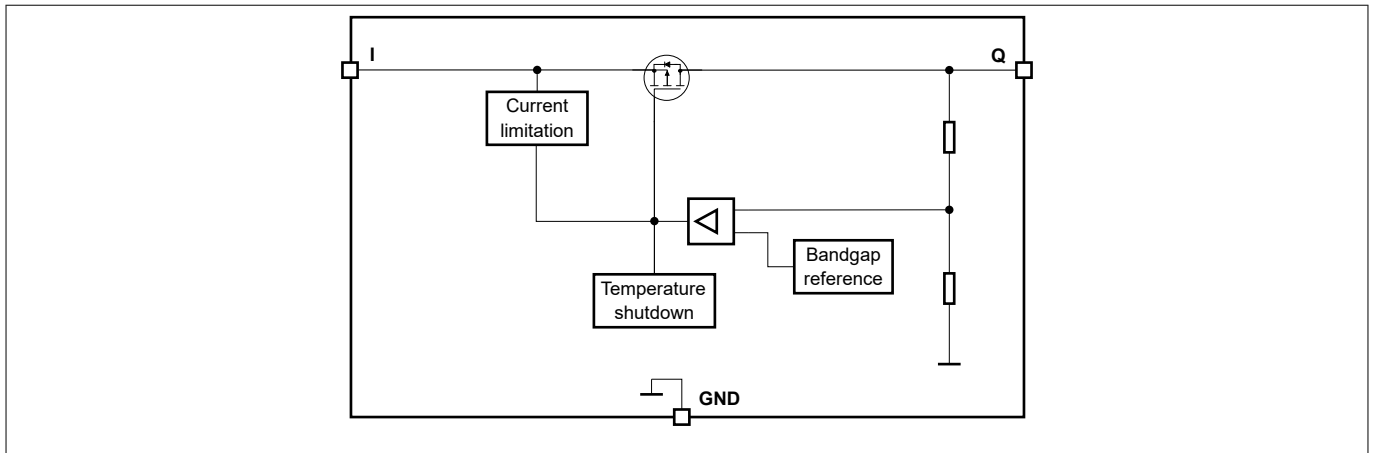
Type	Package	Marking
TLS830A4EPV50	PG-TSDSO-14	830A4V50

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**1 Block diagram**

**1 Block diagram**

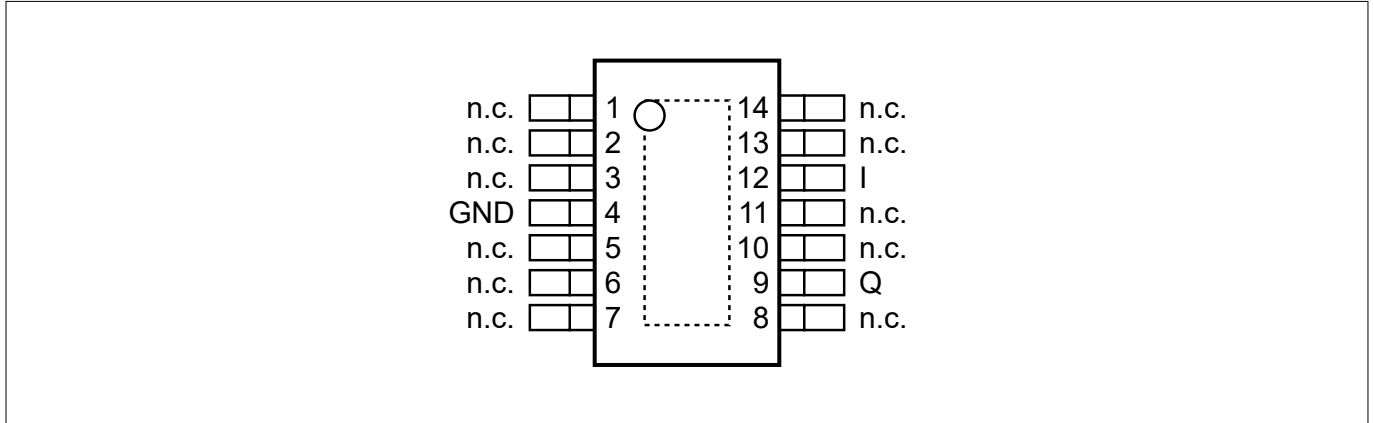


**Figure 1**      **Block diagram**

**2 Pin configuration**

**2 Pin configuration**

**2.1 Pin assignment**



**Figure 2 Pin assignment**

**2.2 Pin definitions and functions**

**Table 1 Pin definitions and functions**

Pin	Symbol	Function
1-3	n.c.	Not connected
4	GND	Ground
5-8	n.c.	Not connected
9	Q	Output voltage Connect output capacitor $C_Q$ to GND close to the pin, respecting the values specified for its capacitance and ESR in <a href="#">Table 3</a> .
10-11	n.c.	Not connected
12	I	Input It is recommended to place a small ceramic capacitor to GND, close to the pins, in order to compensate line influences.
13-14	n.c.	Not connected
Heat slug	GND	Heat slug Connect to heatsink area; Connect to GND

**3 General product characteristics**

**3 General product characteristics**

**3.1 Absolut maximum ratings**

**Table 2 Absolute maximum ratings**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltage on input I	$V_I$	-0.3	–	45	V	1)	PRQ-35
Voltage on output Q	$V_Q$	-0.3	–	7	V	1)	PRQ-36
Junction temperature	$T_j$	-40	–	150	°C	1)	PRQ-39
Storage temperature	$T_{stg}$	-55	–	150	°C	1)	PRQ-40

**ESD robustness**

ESD robustness all pins (HBM)	$V_{ESD\_HBM}$	-2	–	2	kV	1) 2)	PRQ-41
ESD robustness all pins (CDM)	$V_{ESD\_CDM}$	-750	–	750	V	1) 3)	PRQ-194

1) Not subject to production test, specified by design.

2) Human body model (HBM) robustness according to AEC-Q100-002.

3) Charged device model (CDM) robustness according to AEC-Q100-011 Rev-D; voltage level refers to test condition (TC) mentioned in the standard.

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as outside the normal operating range. Protection functions are not designed for continuous repetitive operation.*

**3 General product characteristics**

**3.2 Functional range**

**Table 3 Functional range**

$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Input voltage range	$V_I$	$V_{Q,nom} + V_{dr}$	–	40	V	1)	PRQ-43
Extended input voltage range	$V_{I,ext}$	3.2	–	40	V	2)	PRQ-44
Capacitance of output capacitor for stability	$C_Q$	4.7	–	–	$\mu\text{F}$	3) 4)	PRQ-201
Equivalent series resistance of output capacitor	$ESR_{CQ}$	–	–	40	$\Omega$	3)	PRQ-46
Junction temperature	$T_j$	-40	–	150	$^\circ\text{C}$	–	PRQ-47

- 1) Output current is limited internally and depends on the input voltage, see electrical characteristics for more details.  
 2) If  $V_{I,ext,min} \leq V_I \leq V_{Q,nom} + V_{dr}$ , then  $V_Q = V_I - V_{dr}$ . If  $V_I < V_{I,ext,min}$ , then  $V_Q$  can drop to 0 V.  
 3) Not subject to production test, specified by design.  
 4) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.

*Note: Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.*

**3 General product characteristics**

**3.3 Thermal resistance**

**Table 4 Thermal resistance**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to case	$R_{thJC}$	–	23	–	K/W	<sup>1)</sup>	PRQ-204
Junction to ambient	$R_{thJA}$	–	57	–	K/W	<sup>1) 2)</sup> 2s2p board	PRQ-206
Junction to ambient	$R_{thJA}$	–	145	–	K/W	<sup>1) 3)</sup> 1s0p board, footprint only	PRQ-207
Junction to ambient	$R_{thJA}$	–	79	–	K/W	<sup>1) 3)</sup> 1s0p board, 300 mm <sup>2</sup> heatsink area on PCB	PRQ-208
Junction to ambient	$R_{thJA}$	–	70	–	K/W	<sup>1) 3)</sup> 1s0p board, 600 mm <sup>2</sup> heatsink area on PCB	PRQ-209

1) Not subject to production test, specified by design.

2) Specified  $R_{thJA}$  value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with two inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable, a thermal via array next to the package contacted the first inner copper layer.

3) Specified  $R_{thJA}$  value is according to JEDEC JESD51-3 at natural convection on FR4 1s0p board; the product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with one copper layer (1 × 70 μm Cu).

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information visit [www.jedec.org](http://www.jedec.org).*



## 4 Voltage regulation

# 4 Voltage regulation

### 4.1 Functional description voltage regulation

The output voltage  $V_Q$  is internally divided by a resistor network. The device compares this fractional voltage to an internal voltage reference and drives the pass transistor accordingly.

The control loop stability depends on the following factors:

- output capacitor  $C_Q$
- load current
- chip temperature
- internal circuit design

#### Output capacitor

To ensure stable operation, the capacitance of the output capacitor and its equivalent series resistor (ESR) requirements as specified in [Table 3](#) must be maintained. The output capacitor must be sized according to the requirements of the application to be able to buffer load steps.

#### Input capacitors, reverse polarity protection diode

An input capacitor  $C_I$  is recommended to compensate for line influences.

In order to block influences such as pulses and high frequency distortion at the input, an additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the component's terminals.

#### Smooth ramp-up

In order to prevent overshoots during startup, a smooth ramp-up function is implemented. This ensures a reduced output voltage overshoot during startup, mostly independent from load and output capacitance.

#### Output current limitation

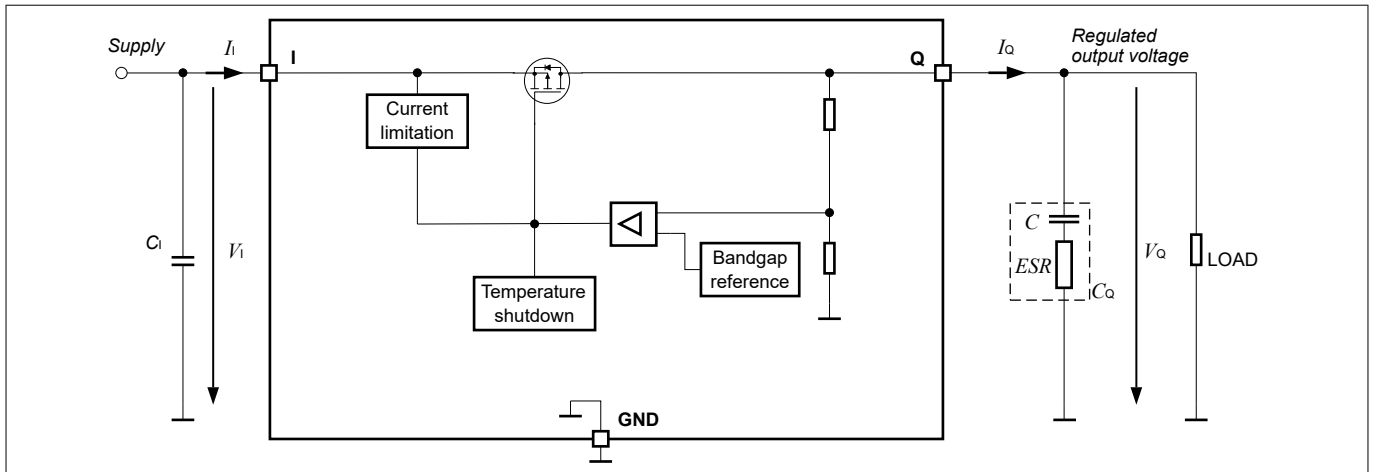
If the load current exceeds the specified limit, due to a short-circuit for example, then the device limits the output current and the output voltage decreases.

#### Overtemperature shutdown

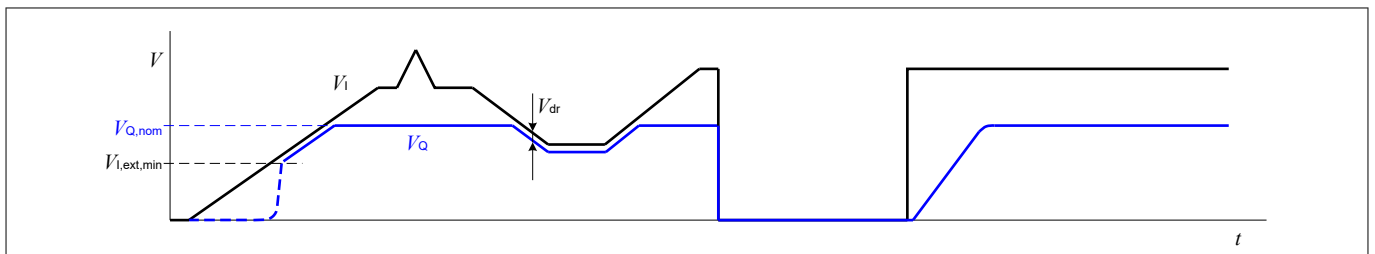
The overtemperature shutdown circuit prevents the device from immediate destruction by switching off the power stage in the case of a fault condition, which could occur due to a permanent short-circuit at the output, for example. After the device cools down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault condition is removed.

However, any junction temperature above the maximum junction temperature  $T_J$  is outside the maximum ratings and therefore significantly reduces the lifetime of the device.

**4 Voltage regulation**



**Figure 3 Voltage regulation**



**Figure 4 Output voltage versus input voltage**

**4 Voltage regulation**

**4.2 Electrical characteristics voltage regulation**

**Table 5 Electrical characteristics voltage regulation**

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ,  $V_I = 13.5\text{ V}$ , all voltages with respect to ground (unless otherwise specified)

Typical values are given at  $T_j = 25\text{ °C}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage accuracy	$V_Q$	4.9	5.0	5.1	V	$0.05\text{ mA} \leq I_Q \leq 300\text{ mA}$ ; $6.2\text{ V} \leq V_I \leq 28\text{ V}$	PRQ-166
Output voltage accuracy	$V_Q$	4.9	5.0	5.1	V	$0.05\text{ mA} \leq I_Q \leq 150\text{ mA}$ ; $5.6\text{ V} < V_I < 40\text{ V}$	PRQ-50
Dropout voltage	$V_{dr}$	–	550	1200	mV	<sup>1)</sup> $V_{dr} = V_I - V_Q$ ; $I_Q = 300\text{ mA}$	PRQ-172
Dropout voltage	$V_{dr}$	–	190	400	mV	<sup>1)</sup> $V_{dr} = V_I - V_Q$ ; $I_Q = 100\text{ mA}$	PRQ-56
Power supply ripple rejection	$PSRR$	–	55	–	dB	<sup>2)</sup> $f_{ripple} = 100\text{ Hz}$ ; $V_{ripple} = 0.5\text{ V}_{pp}$ ; $I_Q = 10\text{ mA}$	PRQ-57

**Output current limitation**

Output current limitation	$I_{Q,max}$	301	450	700	mA	$0\text{ V} < V_Q < V_{Q,nom} - 0.1\text{ V}$ ;	PRQ-153
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**Line regulation, load regulation**

Load regulation steady-state	$\Delta V_{Q,load}$	-25	-5	–	mV	$I_Q = 0.05\text{ mA}$ to $300\text{ mA}$ ; $V_I = 6.5\text{ V}$	PRQ-155
Line regulation steady-state	$\Delta V_{Q,line}$	–	1	10	mV	$V_I = 8\text{ V}$ to $32\text{ V}$ ; $I_Q = 5\text{ mA}$	PRQ-62

**Overtemperature shutdown**

Overtemperature shutdown threshold	$T_{j,sd}$	151	175	200	°C	<sup>2)</sup> $T_j$ increasing	PRQ-63
Overtemperature shutdown threshold hysteresis	$T_{j,sdh}$	–	10	–	°C	<sup>2)</sup> $T_j$ decreasing	PRQ-64

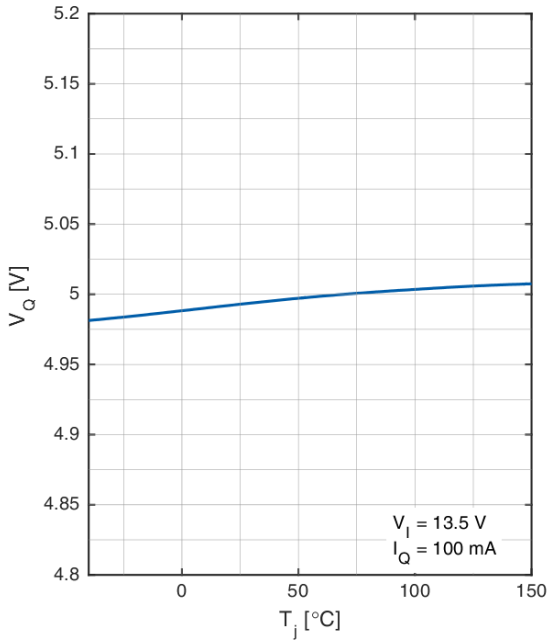
1) Measured when the output voltage  $V_Q$  has dropped by 100 mV while input voltage was gradually decreased.

2) Not subject to production test, specified by design.

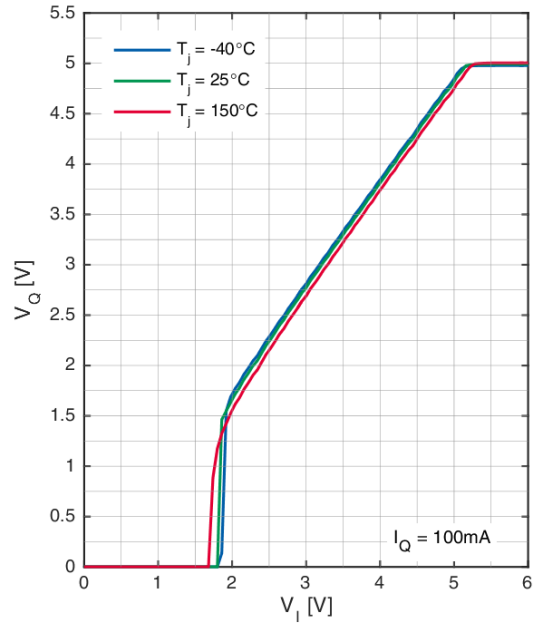
**4 Voltage regulation**

**4.3 Typical performance characteristics voltage regulation**

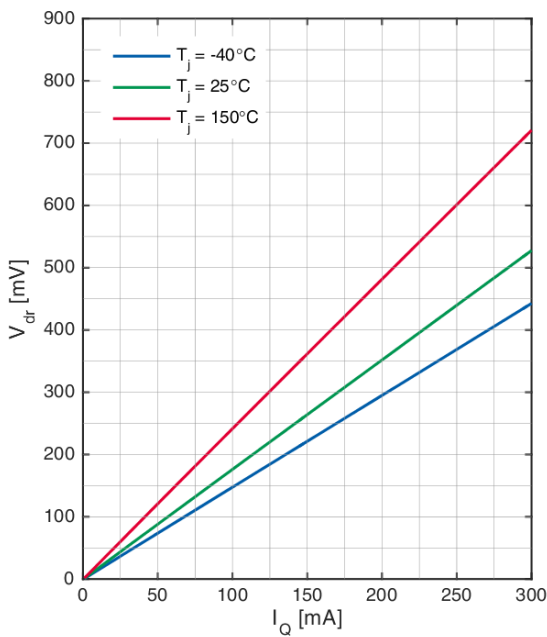
Output voltage  $V_Q$  versus junction temperature  $T_j$



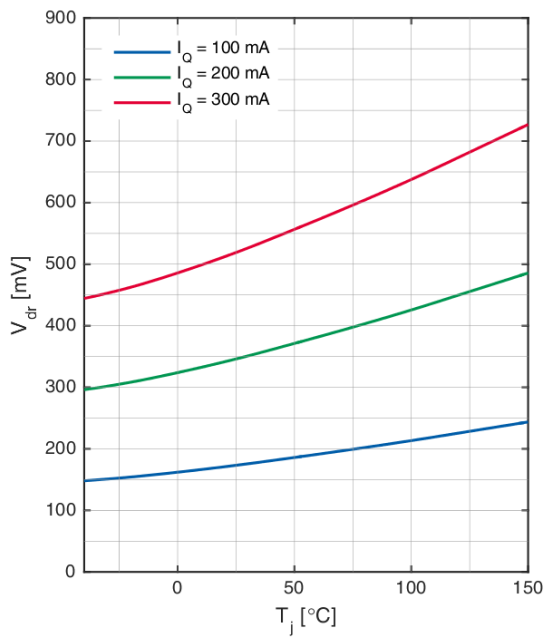
Output voltage  $V_Q$  versus input voltage  $V_I$



Dropout voltage  $V_{dr}$  versus output current  $I_Q$

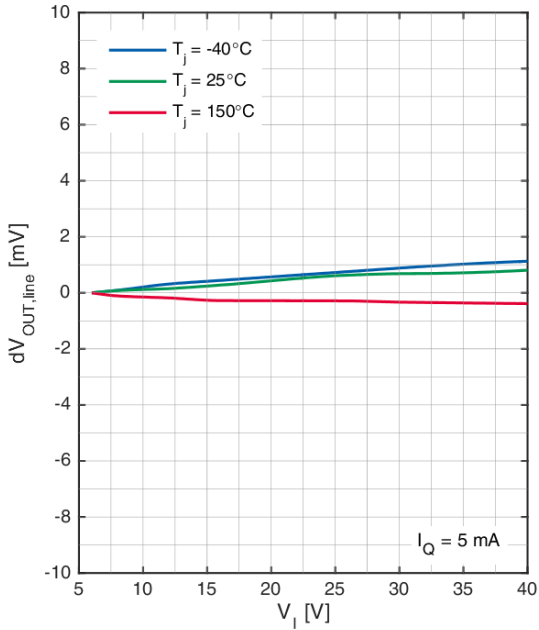


Dropout voltage  $V_{dr}$  versus junction temperature  $T_j$

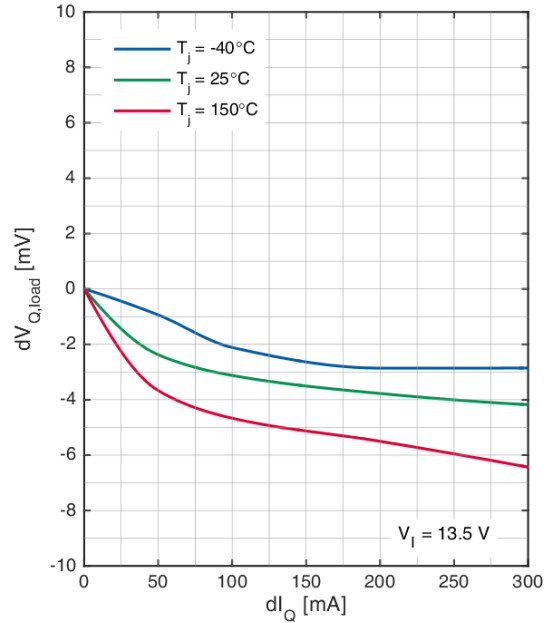


**4 Voltage regulation**

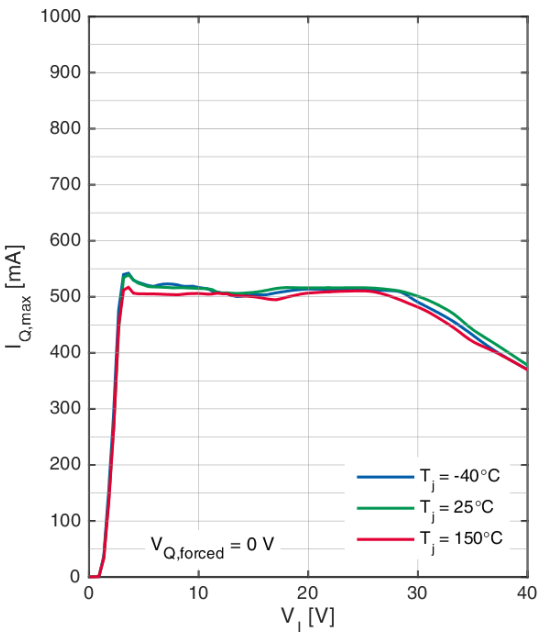
Line regulation  $\Delta V_{Q,line}$  versus input voltage  $V_I$



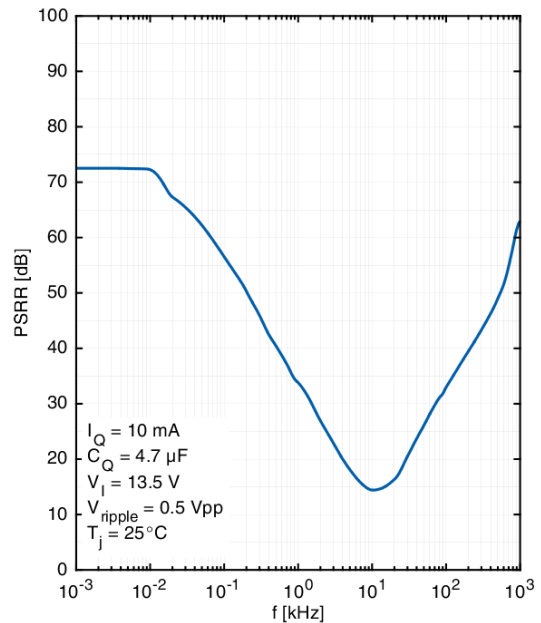
Load regulation  $\Delta V_{Q,load}$  versus output current change  $\Delta I_Q$



Maximum output current  $I_{Q,max}$  versus input voltage  $V_I$

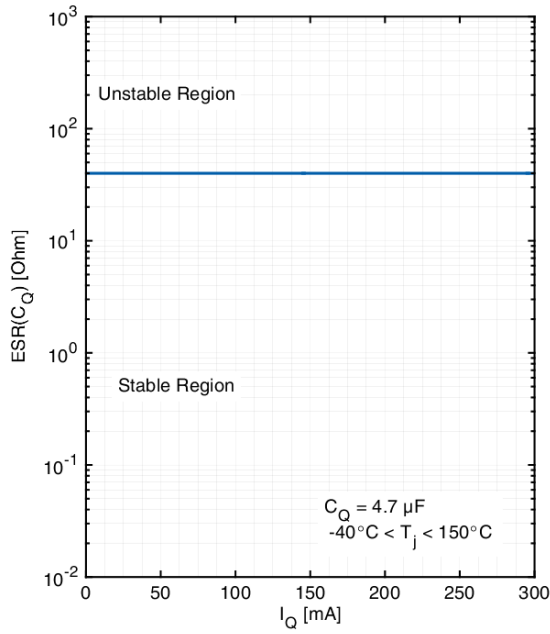


Power supply rejection ratio  $PSRR$  versus ripple frequency  $f$



#### 4 Voltage regulation

Equivalent series resistance  $ESR_{C_Q}$  versus  
output current  $I_Q$



**5 Current consumption**

**5 Current consumption**

**5.1 Electrical characteristics current consumption**

**Table 6 Electrical characteristics current consumption**

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ,  $V_I = 13.5\text{ V}$ , all voltages with respect to ground (unless otherwise specified)

Typical values are given at  $T_j = 25\text{ °C}$

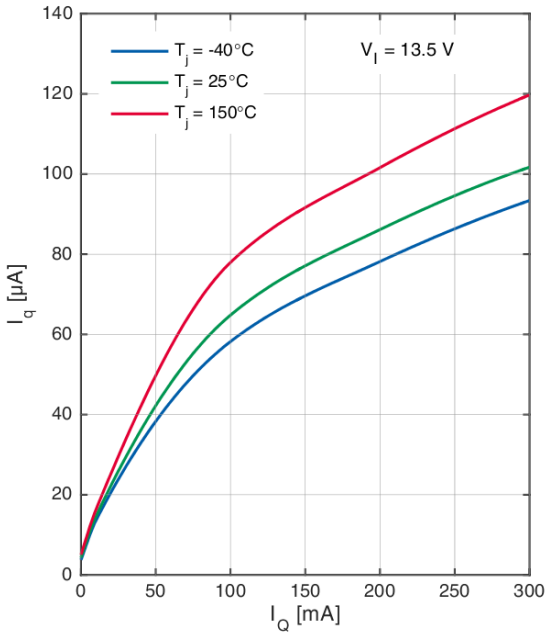
Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current consumption	$I_q$	–	4.3	8	$\mu\text{A}$	$I_q = I_I - I_Q$ ; $I_Q = 0.05\text{ mA}$ ; $T_j < 125\text{ °C}$	PRQ-66
Current consumption	$I_q$	–	8	12	$\mu\text{A}$	$I_q = I_I - I_Q$ ; $I_Q = 1\text{ mA}$ ; $T_j < 125\text{ °C}$	PRQ-202
Current consumption	$I_q$	–	16	21	$\mu\text{A}$	$I_q = I_I - I_Q$ ; $I_Q = 10\text{ mA}$ ; $T_j < 125\text{ °C}$	PRQ-190
Current consumption	$I_q$	–	115	170	$\mu\text{A}$	<sup>1)</sup> $I_q = I_I - I_Q$ ; $I_Q = 300\text{ mA}$ ; $T_j < 125\text{ °C}$	PRQ-191

1) Not subject to production test, specified by design.

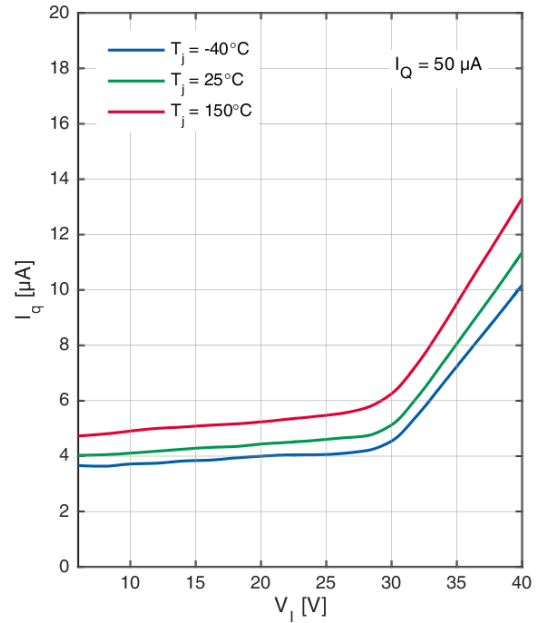
**5 Current consumption**

**5.2 Typical performance characteristics current consumption**

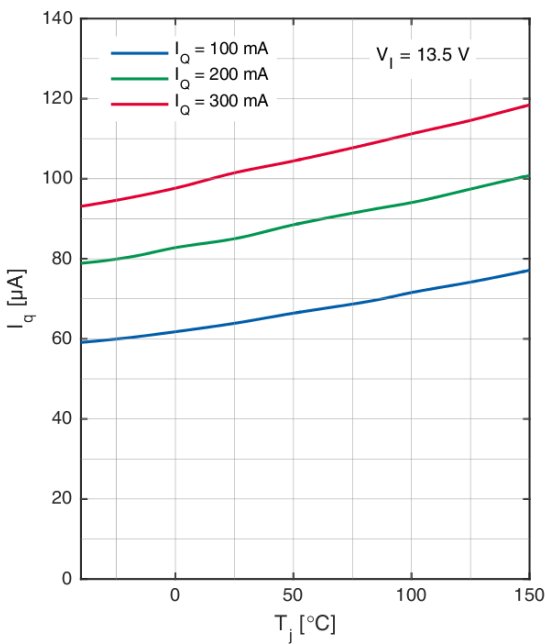
Current consumption  $I_q$  versus output current  $I_Q$



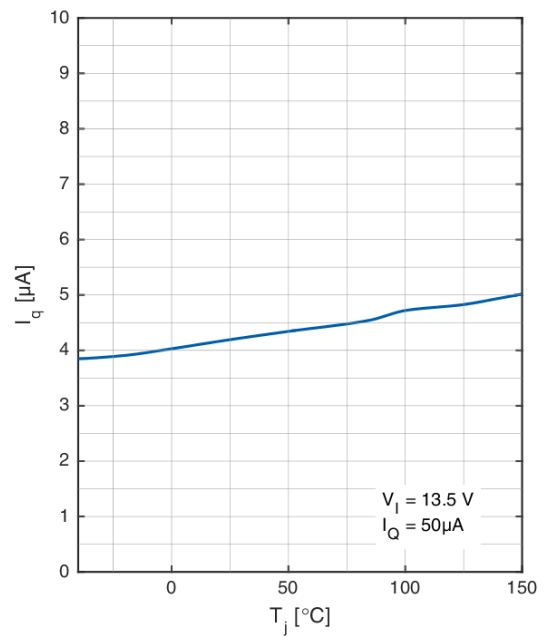
Current consumption  $I_q$  versus input voltage  $V_I$



Current consumption  $I_q$  versus junction temperature  $T_j$



Current consumption  $I_q$  versus junction temperature  $T_j$



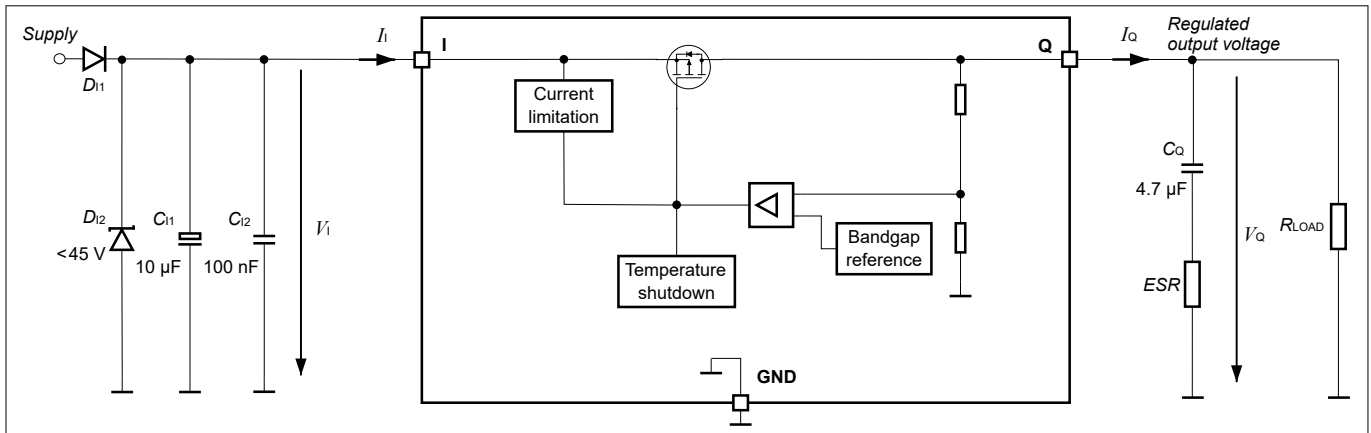


**6 Application information**

**6 Application information**

**6.1 Application diagram**

*Note: The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*



**Figure 5 Application diagram**

*Note: This figure is a simplified example of an application circuit. The function must be verified in the application.*

**6.2 Selection of external components**

**6.2.1 Input pin**

Figure 5 shows an example of the input circuitry for a linear voltage regulator. A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line, for example ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 μF to 470 μF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor must be placed close to the input pin of the linear voltage regulator.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and to protect the device from damage due to overvoltage.

The external components at the input pin are optional, but they are recommended to deal with possible external disturbances.

**6.2.2 Output pin**

An output capacitor is mandatory for the stability of linear voltage regulators. Furthermore, it serves as an energy buffer during load jumps, to compensate and maintain a constant output voltage potential. It must be dimensioned according to the specific requirements of the application. The requirements for the output capacitor are given in Table 3.

The device is designed to be stable with low ESR capacitors as well. According to automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the voltage regulator’s output and GND pin and on the same side of the PCB as the regulator itself.

## 6 Application information

In case of a possible transient voltage on the input or a transient load current, the capacitance should be dimensioned accordingly.

The configuration must be verified in the real application to ensure that the output stability requirements are fulfilled.

### 6.3 Thermal considerations

From the known input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated as follows:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q$$

#### Equation 1

with

- $P_D$ : continuous power dissipation
- $V_I$ : input voltage
- $V_Q$ : output voltage
- $I_Q$ : output current
- $I_q$ : quiescent current

The maximum acceptable thermal resistance  $R_{thJA}$  is given by:

$$R_{thJA} = \frac{T_{j,max} - T_a}{P_D}$$

#### Equation 2

with

- $T_{j,max}$ : maximum allowed junction temperature
- $T_a$ : ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined by referring to the specification for thermal resistance in [Table 4](#).

### 6.4 Reverse polarity protection

The device has no internal protection against reverse polarity and thus requires an external reverse polarity protection diode against negative supply voltage.

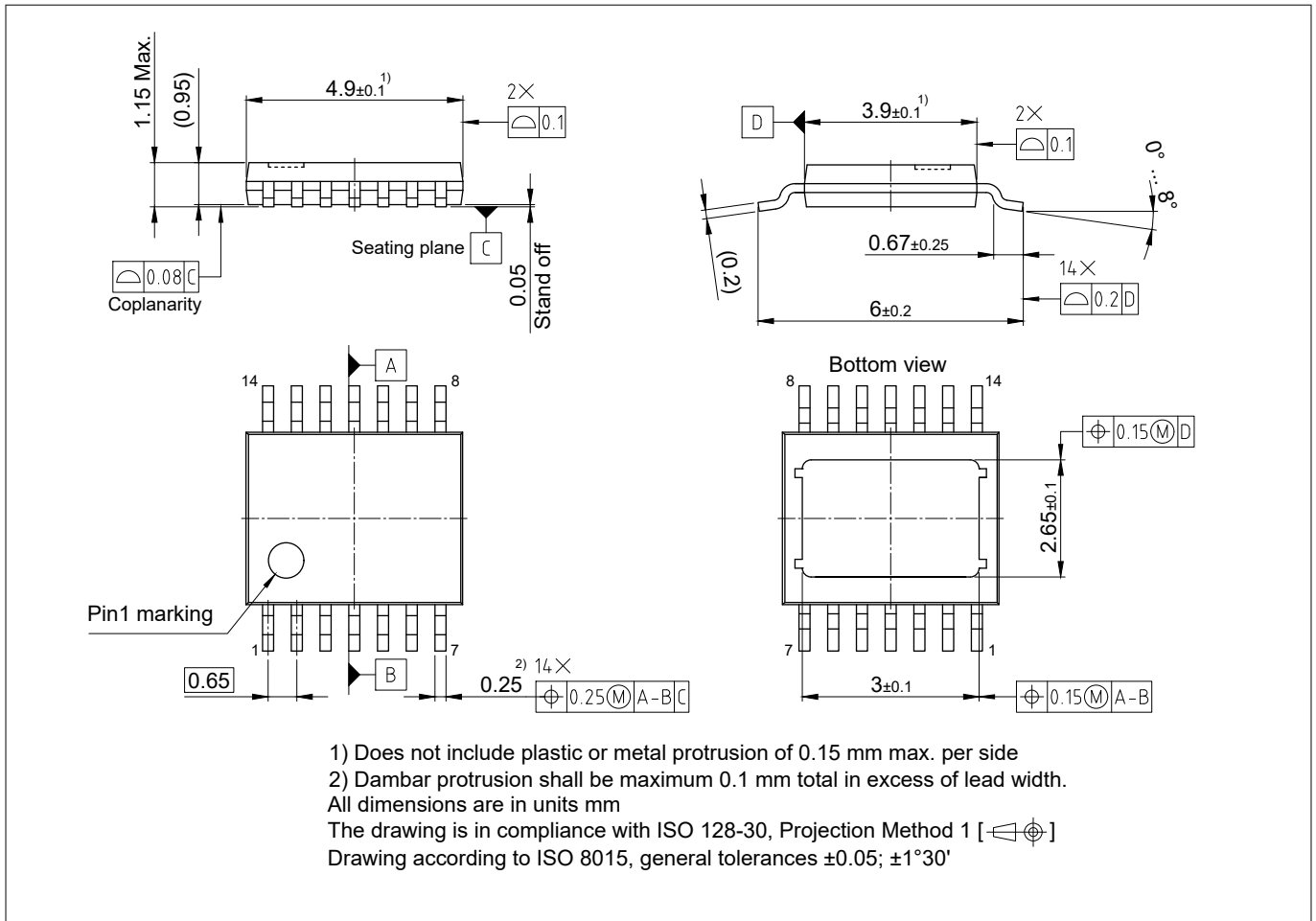
The absolute maximum ratings of the device as specified in [Table 2](#) must be maintained.

### 6.5 Further application information

For further information, you may contact [www.infineon.com](http://www.infineon.com).

**7 Package information**

**7 Package information**



**Figure 6 PG-TSDSO-14**

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

**Information on alternative packages**

Please visit [www.infineon.com/packages](http://www.infineon.com/packages).

**8 Revision history**

**8 Revision history**

Revision	Date	Changes
1.0	2023-07-17	Datasheet created

## Trademarks

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**Document reference**

**IFX-Z8F68809041**

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