1000 W telecom power supply for 5G edge computing and small cells using CoolSIC™ 650 V and CoolMOS™ 600 V CDF7 in TOLL package

About this document

Scope and purpose

This document provides the REF_1KW_PSU_5G_SIC reference board, which is a complete system solution for a 1000 W power supply unit (PSU) from Infineon targeting the new 5G specifications for outdoor small-cell telecom rectifiers.

This document also describes the converter system architecture and hardware with a summary of the experimental results.

Intended audience

This document is intended for design engineers who use the REF_1KW_PSU_5G_SIC reference board for developing the 1000 W PSU for 5G outdoor small-cell telecom rectifiers.

Reference Board

Product(s) embedded on a PCB, with focus on specific applications and defined use cases that can include software. PCB and auxiliary circuits are optimized for the requirements of the target application.

Note: *Boards do not necessarily meet safety, EMI, and quality standards (for example UL, CE) requirements.*

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Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Warning**: *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the drive system, wait 5 minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the grid input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by an oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*

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1 Introduction

1.1 Edge computing application

In the context of the upcoming 5G technology era, the development of the new generation of communications networks (5G networks, satellite networks, etc.) addresses important challenges, attempting to provide a wide variety of services and applications with unseen data rates.

5G and edge computing are two linked key elements of the modern information and communications technology (ICT) ecosystem. They both aim to significantly improve the performance of applications and enable huge amounts of data to be processed in real time. 5G increases speeds by up to ten times more than 4G, whereas mobile edge computing reduces latency by bringing compute capabilities into the network and closer to the end user.

The main focus of the present work is the edge computing. Edge computing is a distributed open platform integrating the core capabilities of network such as computing, storage, and application, which provides intelligent services at the network edge close to devices/terminals or data sources. In other words, it directly analyzes data collected from the terminals at (or near) the device where data is generated. This eliminates the need to transmit every time data to the cloud data processing center. Edge computing then features “real-time” data processing and quicker response and therefore, it is ideal to support the Internet of Things (IoT) architecture.

The typical edge computing architecture (Figure 1) can be described as follows:

- **Terminal:** The terminal layer consists of various IoT devices, such as sensors, cameras, and smartphones, which collect and report raw data. At this layer, the IoT devices need to provide only sensing capabilities but not computational ones.
- **Edge computing node:** Edge computing nodes enable the response to basic services by deploying and allocating the computing and storage capabilities at the network edge.
- **Network node:** A network node uploads useful data obtained through edge computing nodes to cloud computing nodes for analysis and processing.
- **Cloud computing node:** The data reported by the edge computing layer is permanently stored on cloud computing nodes.

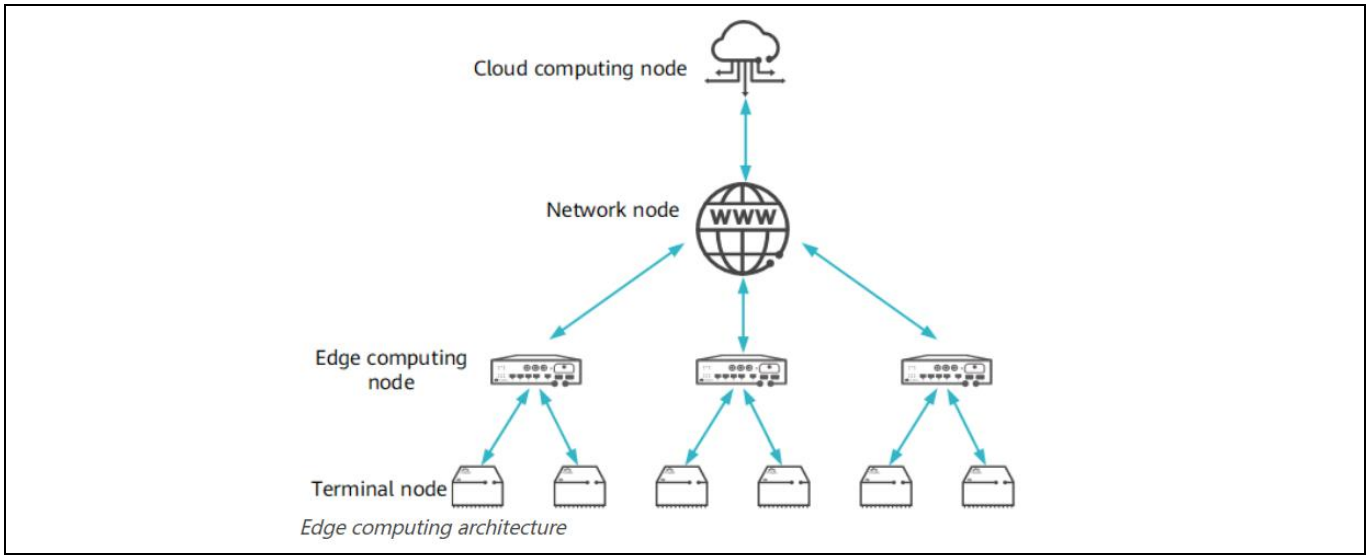


Figure 1 Edge computing architecture

Introduction

Typically, edge computing is deployed through highly scalable and compact micro datacenters with extremely variable sizes, from the “shoebox-like” one (≤1 kW needed power) to containerized solutions up to 500 kW.

In recent signal tower installations, the edge system includes an IP65 enclosure, which can be assembled either at the telecom radio access network (RAN) tower, on buildings, or on lighting infrastructure, similar to the latest generation of 5G outdoor small-cell base stations.

The success of edge computing then depends on the availability of suitable hardware, systems that can economically provide the necessary processing speed and power that can survive in the less-regulated and more unpredictable environments encountered away from the conventional datacenter. The edge computing hardware must comprise compact, energy-efficient solutions that can be widely deployed, even in space-constrained and harsh environments to locate computing as closer as possible to sensors and other data sources. This will have an impact on the needed AC-DC power supply requirements. Compact and thin form factor is the first key feature of a PSU for this application. Efficiency must also be high, because of the ubiquitous micro-datacenters installation, either in remote locations or in areas with high population density: in both these cases, due to different reasons, the cost of the kWh is not cheap.

Also due to the ubiquitous installation, the maintenance cost of such a micro-datacenter is a significant portion of the operating expense sustained by the operator companies. The intensive use of convection cooling is an excellent way to drastically reduce the need of maintenance (no fans and filters replacement required). In general, the outdoor operation, even though inside an IP65 enclosure, has several implications on the environmental conditions of the PSU, which is required to operate in a wide AC input voltage (typically 85-305 V AC) and ambient temperature range (–40°C/+85°C). Therefore, heat dissipation and thermal management are indeed key aspects of such a SMPS design. To conclude that a PSU for outdoor edge servers has to fulfill most of the typical requirements of a telecom rectifier, e.g., for outdoor small cells, including the compliance to standards like Telcordia GR-3108 and GR-487. The present work addresses the main challenges in the design of a compact and efficient 1 kW AC-DC power supply for edge computing outdoor applications.

All these requirements have been translated in a power supply specification for edge computing and outdoor small-cell application that has driven the design of REF_1KW_PSU_5G_SiC. The full specification is described in the following section.

1.2 REF_1KW_PSU_5G_SiC introduction

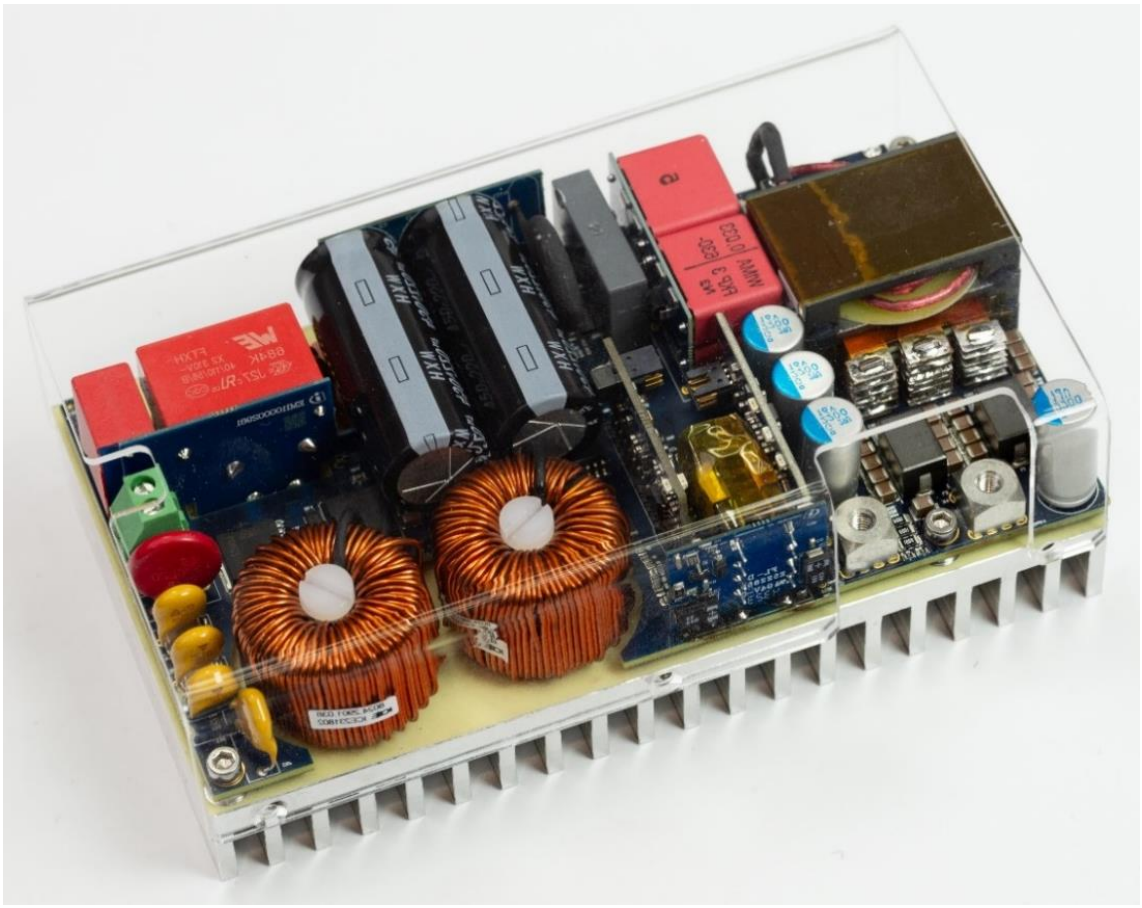


Figure 2 1000 W fanless power supply with CoolSiC™ in TOLL package

- This design is developed to meet the demand for high efficiency in power supply units for modern applications.
- The power supply unit (PSU) consists of two converters:
  - An interleaved totem pole power factor correction (PFC) converter.
  - A DC-DC isolated half-bridge (HB) LLC converter.
- The front-end converter (Figure 2) provides PFC and total harmonic distortion (THD) control, and use as an interleaved totem-pole topology to achieve high efficiency.
- The back-end converter (Figure 2) is a DC-DC isolated half-bridge LLC converter, which provides safety isolation and a tightly regulated output voltage of 12 V DC.
- The PSU design and control system have been optimized to achieve high efficiency, with peak efficiency measured at 96.4% at 230 V AC and 95.4% at 115 V AC.
- The overall dimensions of the PSU are 150 mm x 80 mm x 27 mm, yielding a power density in the range of 50 W/inch^3.

The main Infineon components used in the REF_1KW_PSU_5G_SiC are:

- CoolSiC™ 650 V, 72 mΩ in TOLL package (IMT65R072M1H) in the PFC high-frequency MOSFETs
- CoolMOS™ 600 V, S7 22 mΩ in TOLL package (IPT60R022S7) in the PFC line-rectification MOSFETs
- CoolMOS™ 600 V, CFD7 55 mΩ in TOLL package (IPT60R055CFD7) in the DC-DC primary-side HB
- OptiMOS™ 6 40 V, 0.9 mΩ in PG-WSON-8 package (BSC009N04LSSC) in the DC-DC secondary-side bridge

- EiceDRIVER™ 1EDB9275F and 1EDN9550B gate drivers for driving the PFC high- and low-side CoolSiC™ switching controllers, respectively
- EiceDRIVER™ 1EDB8275F and 1EDN8511B gate drivers for driving the PFC high- and low-side CoolMOS™ MOSFETs, respectively
- EiceDRIVER™ 2EDS8265H gate driver for driving the DC-DC primary-side CoolMOS™ MOSFET
- EiceDRIVER™ 1EDN7511B gate driver for driving the DC-DC secondary-side OptiMOS™ MOSFET
- XMC4200 MCU for the PFC control implementation
- XMC4402 MCU for the DC-DC control implementation
- ICE2QR2280G switching controller for the bias supply implementation

1.3 Features for REF_1KW_PSU_5G_SiC for edge computing application

This application note provides a detailed description of the design considerations and experimental results of a high-efficiency, high-power-density, ultra-compact telecom rectifier for 5G small-cell and edge computing applications.

Here are the key features of this reference board:

- Attractive **compact design** in 50 W/in^3 form factor for a 1000 W PSU
- **Low profile** – 27 mm maximum PSU height
- Very **high efficiency** for 12 V output PSU: Above 96 percent from 45 percent of the rated load upward when V_{in} is equal to 230 V AC, and above 95 percent from 35 percent of the rated load upward when V_{in} is equal to 115 V AC
- **Fanless** design with the possibility of attaching the reference board to a heatsink
- **Fully digital control** implementation using XMC™ MCU
- **High thermal performance** achieved by using best-in-class devices in the TOLL package from Infineon
- **Robust and reliable** operation under different abnormal conditions:
  - Load-jump reaction and output regulation
  - Inrush current during startup
- **Relay replacement with static switch** because of CoolMOS™ S7 MOSFET

Table 2 shows a summary of the main specifications and requirements of the telecom rectifier.

Table 2 Summary of the requirements and specifications for the 5G PSU

Requirements	Conditions	Specification
Input voltage V_{in}	85 V AC to 265 V AC	100 V AC to 240 V AC nominal
Output voltage V_{ref}	–	12 V DC nominal
Output power	85 V AC to 265 V AC 12 V DC	1000 W
Efficiency target	230 V AC input, 12 V DC output 115 V AC input, 12 V DC output	η ≥ 96% (peak efficiency) η ≥ 95% (peak efficiency)
Steady-state V_{out} ripple	Nominal input, 12 V DC output	$\lvert\Delta V_{out}\rvert \le 50\ mV_{pk\text{-}pk}$
Power factor and THD	100 V AC to 240 V AC	Lower < 10% from 20% of load
Load transient	0 A ↔ 83 A, 1 A/µs	$\lvert\Delta V_{out}\rvert \le 1.2\ V_{pk}$
	83 A ↔ 0 A, 1 A/µs	

Requirements	Conditions	Specification
Dimensions	Not including plastic cover	H_{max} = 27 mm W_{max} = 80 mm L_{max} = 150 mm
Cooling	–	Natural/convection
Hold-up time	100% of power	10 ms with V DC greater or equal to 10.8 V
EMI	–	EN 55022 Class A with a 6 dB margin

2 System description

Figure 3 shows the simplified circuit diagram of the REF_1KW_PSU_5G_SiC reference board.

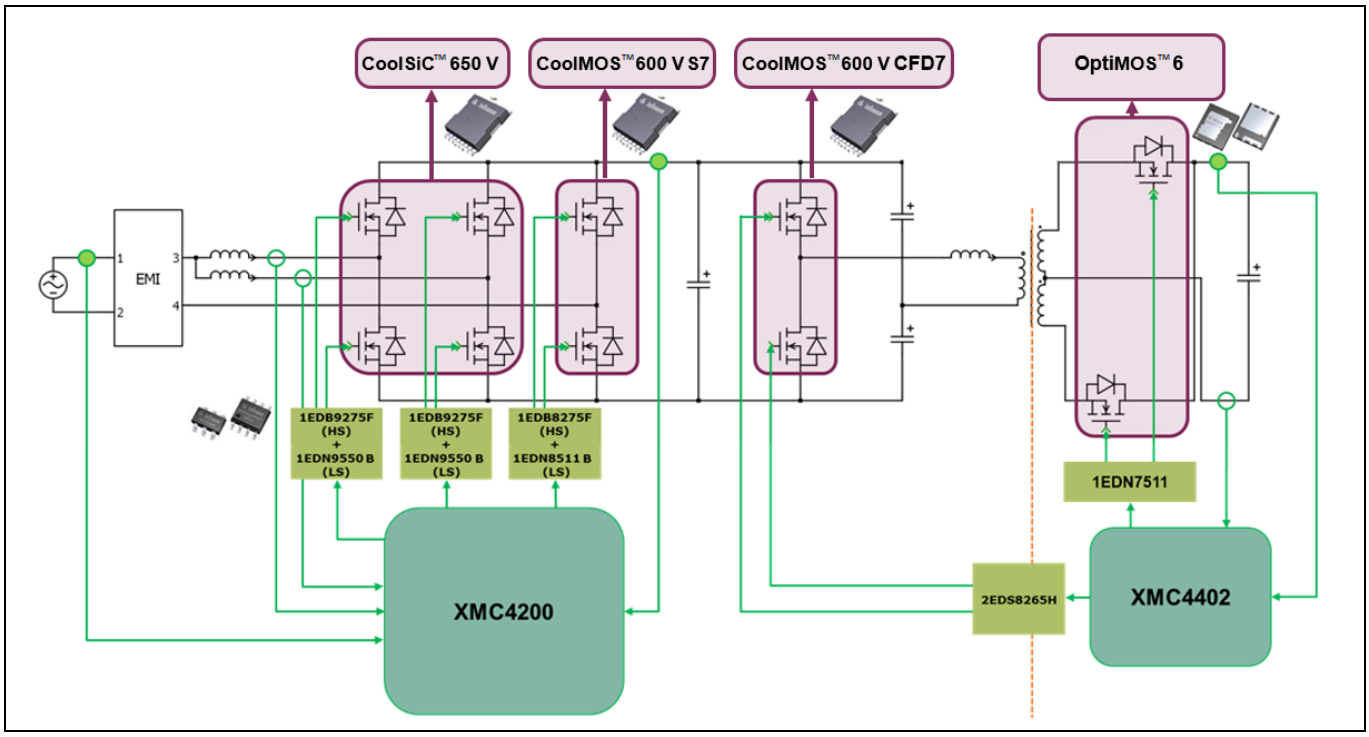


Figure 3 Simplified schematic of REF_1KW_PSU_5G_SiC reference board with Infineon components used

The PSU comprises a front-end AC-DC bridgeless interleaved totem-pole converter followed by a back-end DC-DC isolated LLC converter. The front-end converter provides PFC and control of the THD. The LLC converter provides safety isolation and a tightly regulated output voltage at 12 V DC.

The control of the interleaved totem-pole AC-DC converter is implemented with a dedicated control card PCB based on XMC4200 MCU from Infineon that includes PFC, THD, voltage regulation, input overcurrent protection (OCP), overvoltage protection (OVP), and undervoltage protection (UVP), and start up.

Furthermore, to increase power density, the standard inrush current relay has been replaced with CoolMOS™ S7 MOSFET that is placed on the DC-link capacitor PCB as shown by the implementation view of Figure 4a. Benefits of relay replacement with a static switch MOSFET have been described in detail in [1].

The PFC is operated in both high-line (230 V AC) and low-line (115 V AC) in continuous conduction mode (CCM) with 65 kHz of switching frequency. The bulk capacitance is designed to comply with 10 ms hold-up time at full load condition.

The control of the LLC converter is implemented with another dedicated control card PCB based on XMC4400 MCU from Infineon that includes open-loop/overload protection with extended blanking time, two levels of OCP: frequency shift and latch off, mains input UVP with adjustable hysteresis, adjustable minimum switching frequency with high accuracy, built-in digital and non-linear soft start, and burst mode operation.

Figure 4 b/c shows the placement of the different sections of the REF_1KW_PSU_5G_SiC telecom PSU with Infineon TOLL packages. The board shown is 150 mm long with a width of 80 mm and a height of 27 mm.

Figure 4 shows the PSU, with the left-most component being the AC connector. Adjacent to the AC connector is the single-stage EMI filter. Above the filter, two PFC chokes are strategically placed on a PCB cutout to facilitate thermal connection to the metal base plate using thermal interface material. Similar placement and thermal management techniques have been used for the LLC main transformer, which is located on the center-right side of the PSU board.

Moving to the middle of the board, a daughter card is installed containing bulk capacitors, NTC thermistor, and static switch. This compact arrangement aims to optimize the use of space and enhance the overall efficiency of the PSU. Lastly, the main switches for both stages of the PSU are found on the top-side layer of the main PCB, along with all the drivers. Additionally, the bias supply circuit and the two controllers are implemented in a daughter card. This design ensures that all crucial components are strategically placed for optimal performance and to minimize thermal issues.

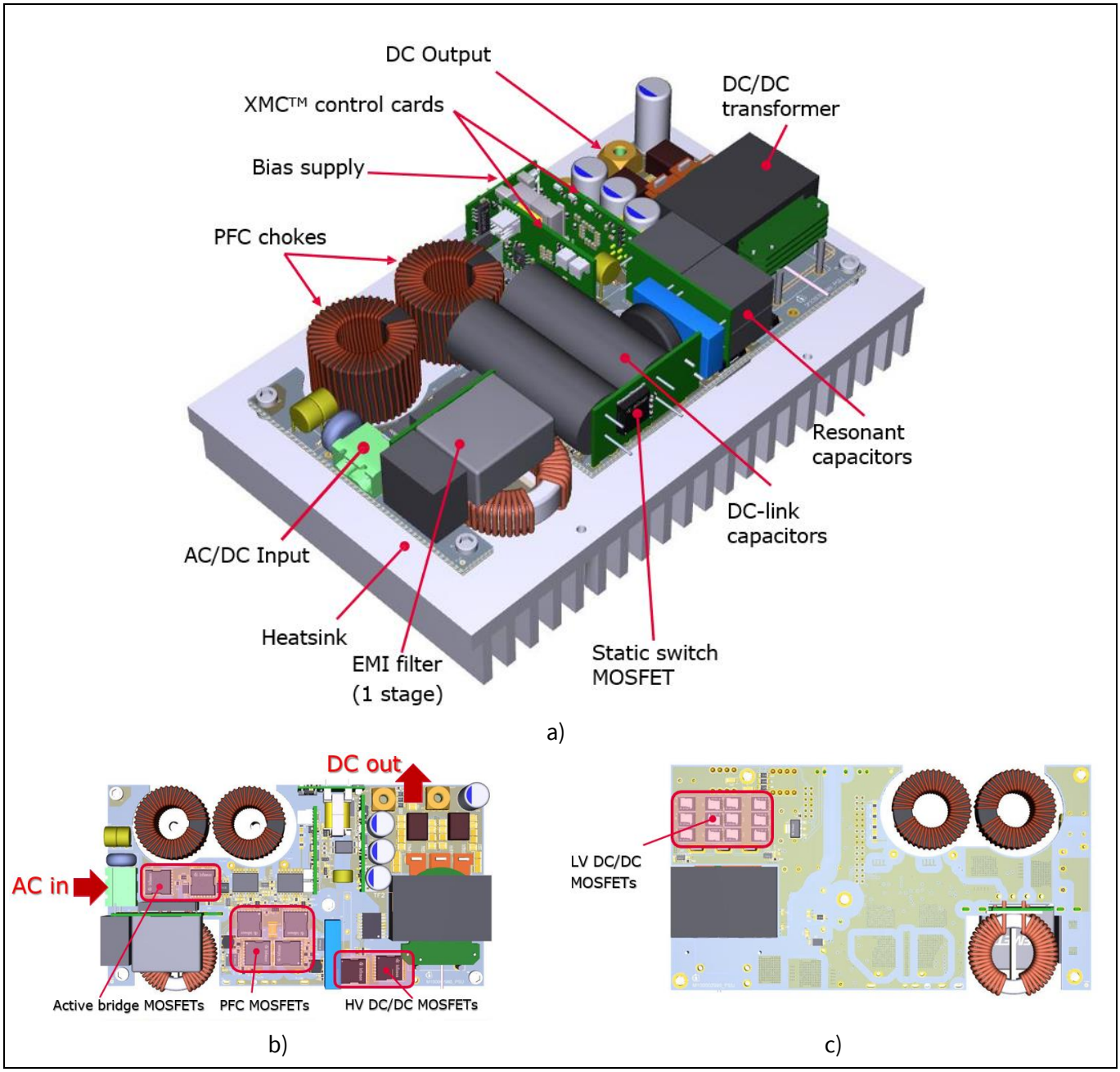


Figure 4 PSU implementation with main PCBs and magnetic components - a) device placement view, b) top view, and c) bottom view

The components used from Infineon in the implementation of REF_1KW_PSU_5G_SIC reference board are interleaved PFC are listed as follows:

- CoolSiC™ 650 V, 72 mΩ (IMT65R072M1H) in TOLL package, as totem-pole PFC high frequency switches.
- CoolMOS™ 600 V, 22 mΩ S7 (IPT60R022S7) in TOLL package, for the totem-pole PFC return path (low frequency bridge) as well as relay replacement.
- EiceDRIVER™ 1EDB9275F, 1EDB8275F, 1EDN9550B, and 1EDN8511B gate drivers.
- XMC42 MCU in QFN 48-pin package for PFC control implementation.

Figure 5 shows a simplified block diagram of the bridgeless topology with the mentioned components from the Infineon portfolio. The diodes in front of the PFC choke are meant to be a current path for startup or surge conditions and it is not part of the current path during the steady-state converter operation.

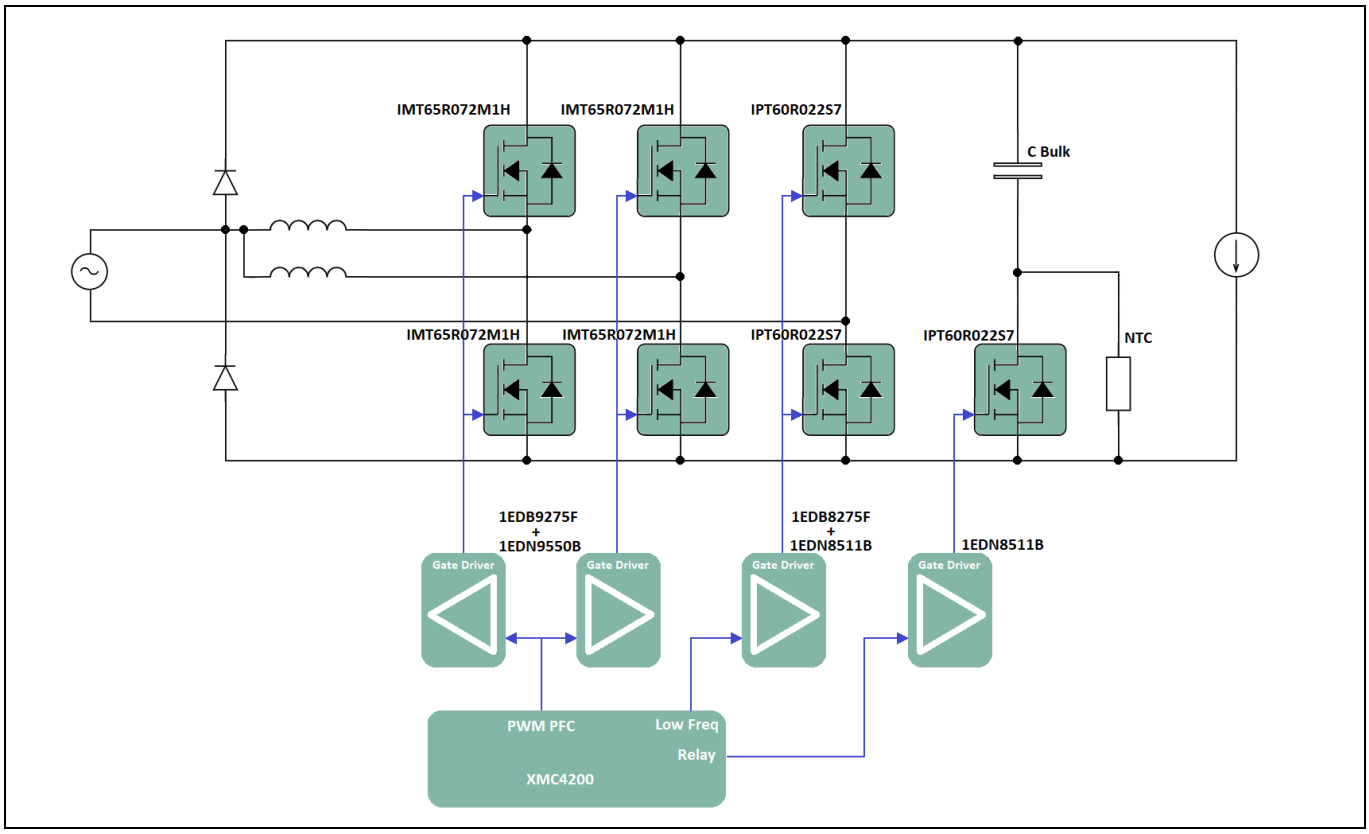


Figure 5 Bridgeless interleaved totem-pole PFC of 1 kW fanless PSU board (REF_1KW_PSU_5G_SIC) with the Infineon components used

This document will describe the REF_1KW_PSU_5G_SIC board implementation, as well as the specifications and main test results. For more information on Infineon devices, visit the Infineon website, the Infineon evaluation board search, and the different websites for the different implemented components:

- CoolSiC™ power MOSFET
- CoolMOS™ power MOSFET
- Gate driver ICs
- XMC™ microcontrollers

2.1 Signal conditioning for digital control of totem-pole CCM PFC

The interleaved PFC of REF_1KW_PSU_5G_SIC board implements CCM average current mode control with duty feed-forward (DFF). Unlike the classic PFC, in which the AC voltage is rectified by the diode bridge in the bridgeless totem-pole PFC converter, the inductor current is both positive and negative. In addition, isolation or common mode rejection is required to measure the inductor current if the control ground in place in the negative rail of the bulk voltage, as it has been traditionally done in classic PFC. Therefore, a Hall-effect sensor is a good solution for this type of system.

The output of the Hall-effect sensor matches very well the analog-to-digital converter (ADC) inputs when supplied with the same voltage: positive and negative current are measured with the span of the ADC and a shift to half of the ADC range for zero current. If a sensor with proper bandwidth is selected, also the high frequency ripple can be sensed and the signal can be used for peak current limitation as well. In case of lower BW, the Hall-effect sensor typically offers an overcurrent detection signal which could be used for the same purpose.

Because of the control reference location, the bulk voltage sense is as simple as a resistive partition as shown in Figure 6. In the case of the of AC voltage sense, to avoid issues during AC zero crossing if no current is flowing into the PFC, both lines are sensed against ground and then added. As the total AC sensing signal is rectified, a comparison of both line and neutral sensing voltages provide the polarity signal.

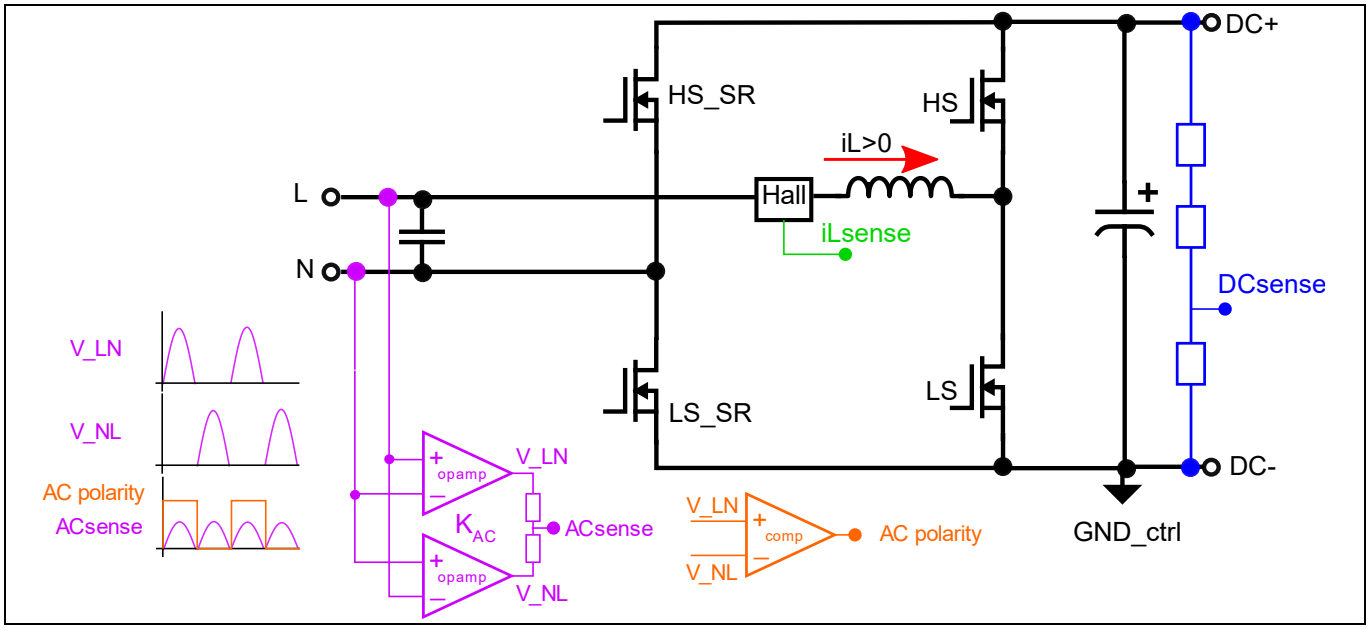


Figure 6 Block diagram of the sensing circuitry required for bidirectional totem-pole control with XMC™ MCU and control reference in the AC rail in series with the PFC choke

As the AC voltage is used for the current reference generation in the selected average current mode structure, the current reference is a full wave rectified sinusoidal sequence. However, the current sense after the ADC is a sinusoidal sequence with offset at half of the ADC span. Therefore, the ADC result from the current sense requires first the offset to be removed and then rectified according to the AC polarity signal. These two steps, together with extra gain, are implemented by software in the XMC™ controller.

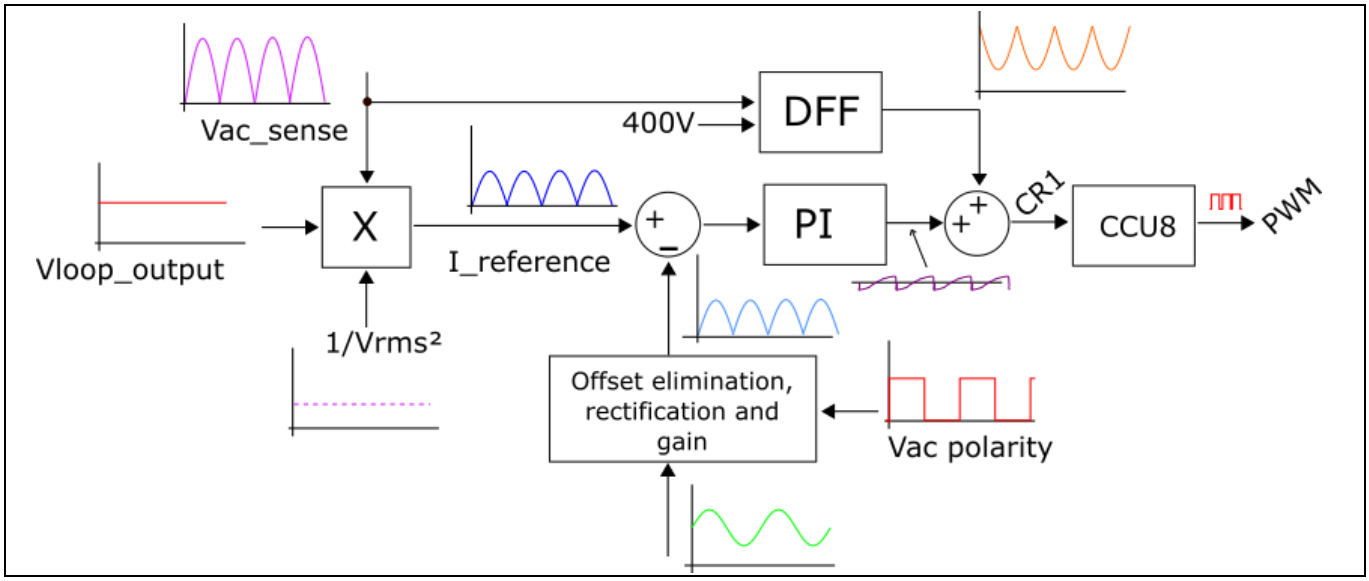


Figure 7 **Current loop structure with duty cycle feed-forward and the required current manipulation**

2.2 Interleaved totem-pole PFC: Estimated efficiency

This section will analyze the interleaved PFC converter with 115 V and 230 V AC RMS input and operating with a switching frequency of 65 kHz.

In particular, Figure 8 presents a comparison between the estimated design efficiency of the PFC (blue plot) and the actual measured efficiency (red plot) at an input voltage of 230 V AC. The data indicates a close alignment at full-load condition with some variances observed at light and middle load conditions.

Despite these discrepancies, the estimation provides valuable insights into the behavior of the PFC across the entire load range, offering a comprehensive understanding from light to full-load conditions.

Note that the PFC unit demonstrates high peak efficiency of 99% at nearly 1000 W of output power.

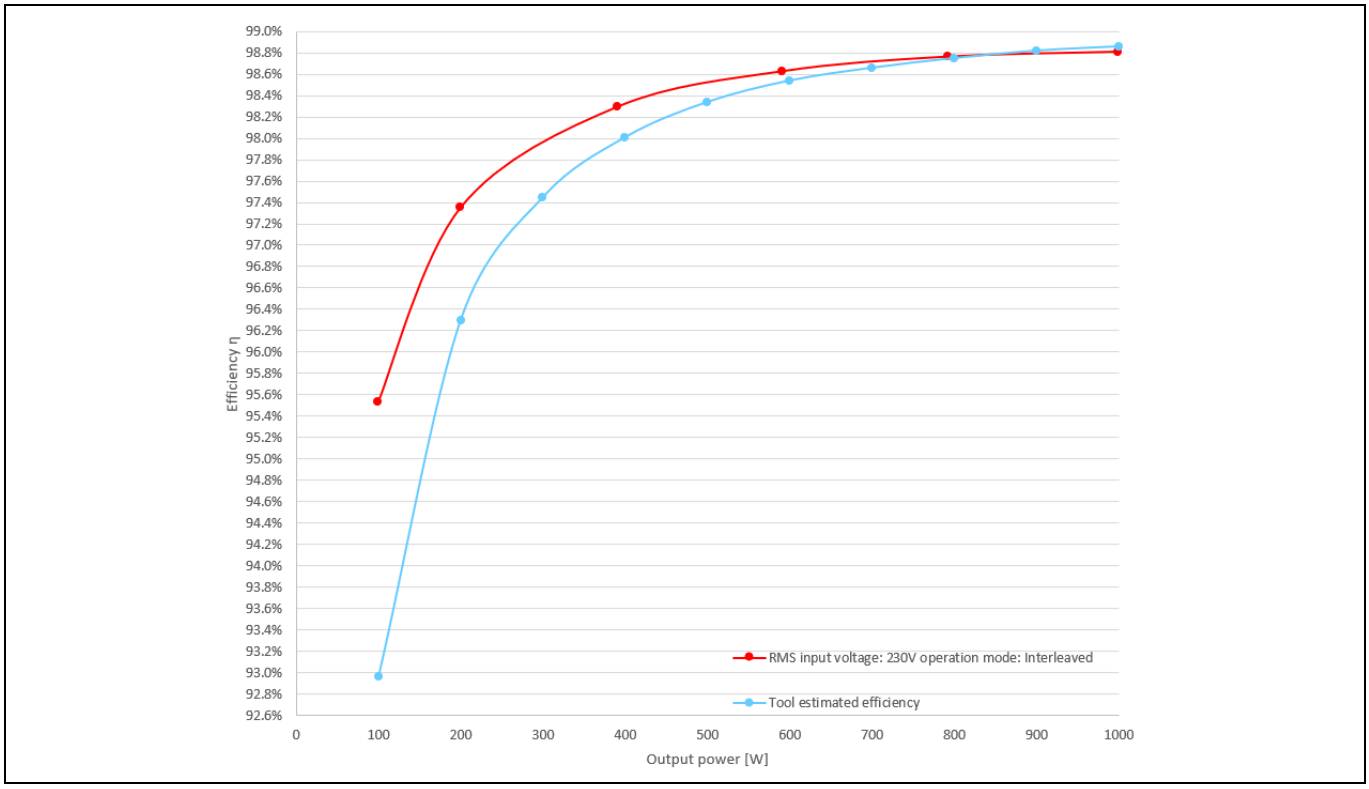


Figure 8 Comparison between estimated and measured efficiency of the interleaved PFC converter

Figure 9 illustrates the distribution of losses across various devices at different operating points for the PFC. The bar plot shows the distribution of losses across the PFC components, highlighting that the majority of losses are concentrated in the main PFC inductor.

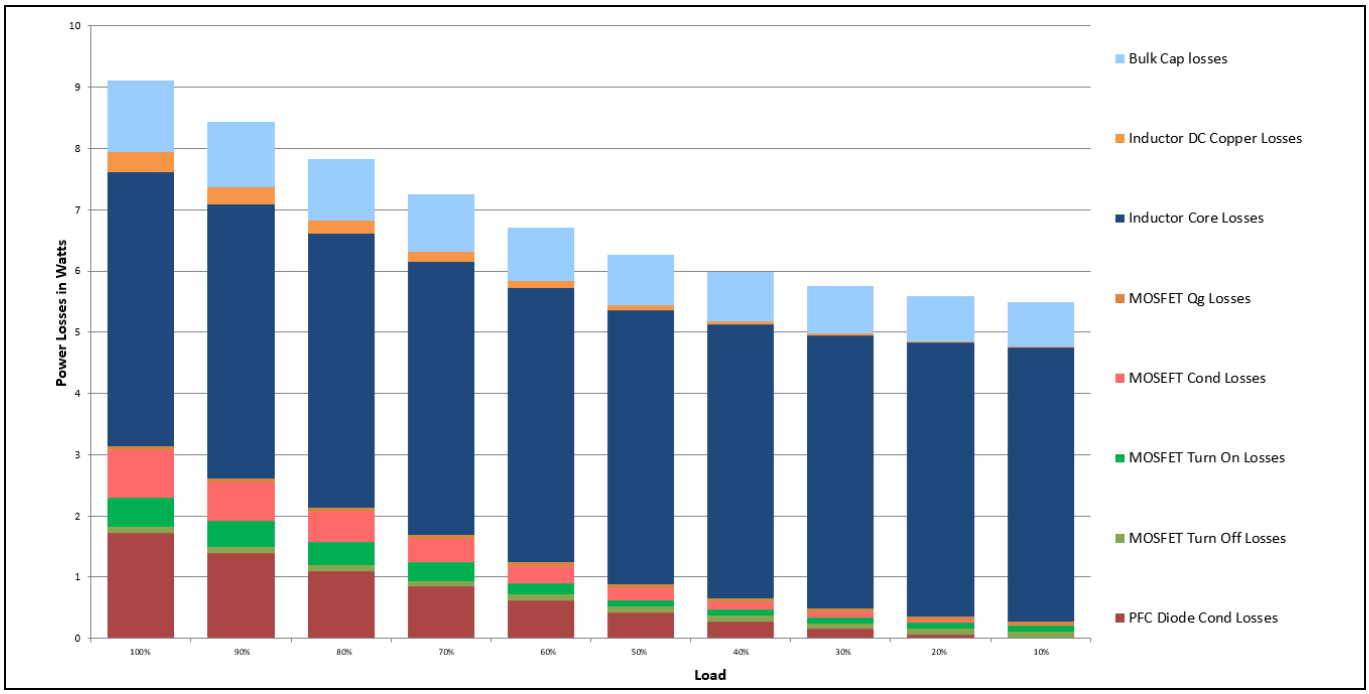
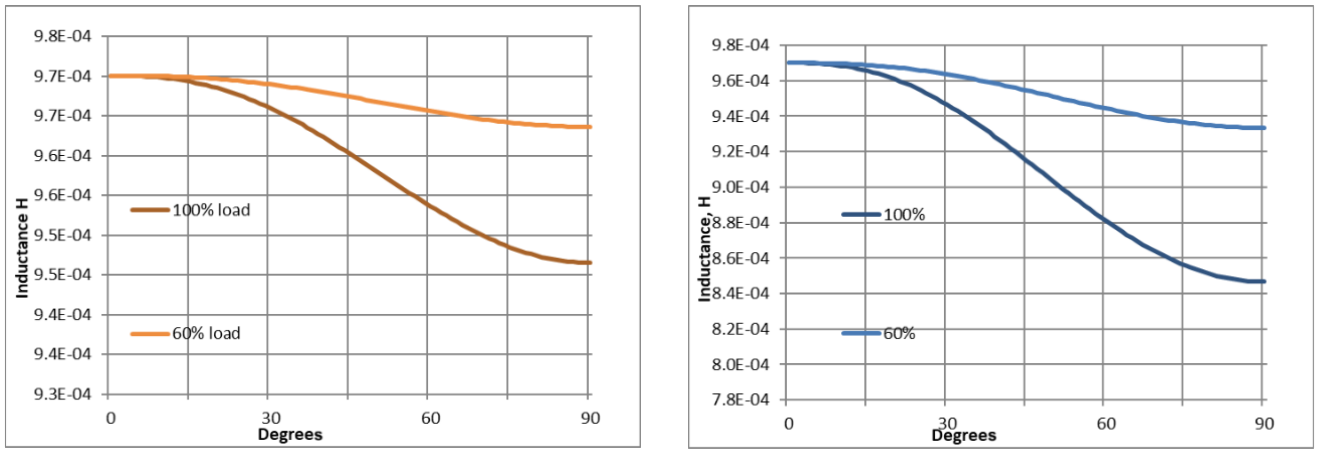


Figure 9 Estimated distribution losses of the interleaved PFC

2.2.1 PFC magnetics

The other main contributors to the losses to consider in the design of the dual-boost AC-DC converter are the main inductor and the EMI filter. The PFC choke design is based on a toroidal high-performance magnetic powder core. Toroidal chokes have a large surface area and allow a good balance, minimizing core and winding losses, and achieving a homogeneous heat distribution without hot spots. For this reason, they are suitable for systems that are targeting the highest power density; very small choke sizes are feasible. The chosen core material CH270060GTE18 is high flux from Chang Sung Corporation (CSC), which has an excellent DC bias and good core loss behavior. The outer diameter of the core is 27 mm with a height of 19 mm. The winding was implemented using enameled AWG 18 (1.1 mm diameter) copper wire. The winding covers approximately two layers represented in Figure 11. This arrangement allows a good copper fill factor, while still having good AC characteristics, and is a preferred fill form factor for high-power toroidal inductors. There are 90 turns, taking advantage of the high permitted DC bias. The resulting small-signal bias inductance is 1 mH. The effective inductance with current bias is determined by the core material B-H characteristics, illustrated in Figure 10.



a) 230 V AC b) 115 V AC

Figure 10 Angle of input current depending on the PFC choke inductance value

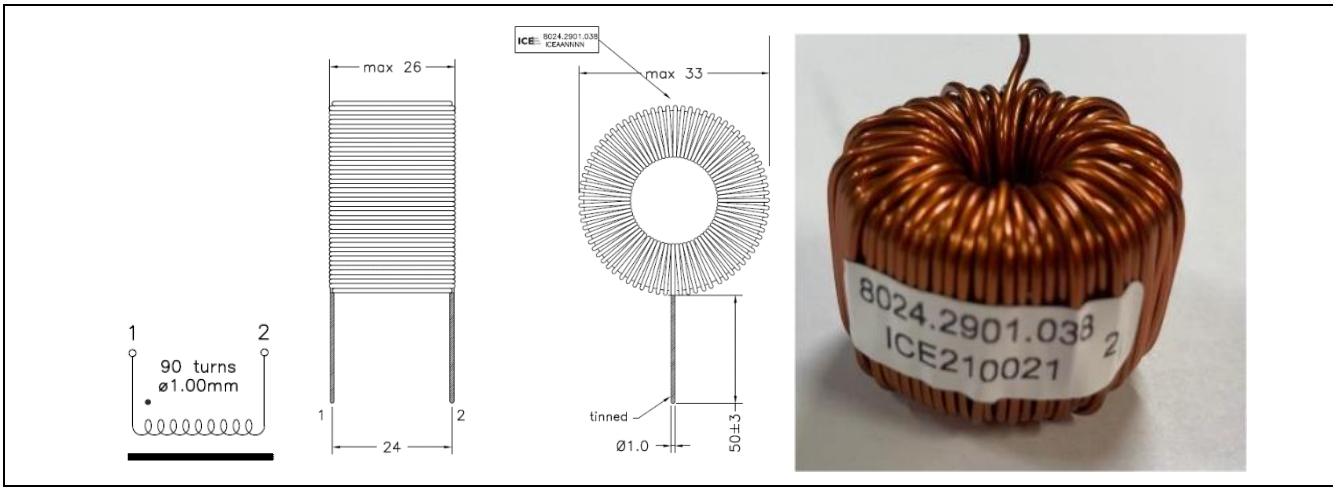


Figure 11 PFC choke

2.2.2 Driving CoolSiC™ and CoolMOS™ in the interleaved totem-pole PFC

To ensure the proper functioning of the PFC converter, the driving stage plays a critical role. In accordance with the recommended driving voltage for CoolSiC™ devices, an 18 V/0 V unipolar driving voltage is used. The bias supplies are initially created by charging the flyback PRI_12 V output to 24 V. From the 24 V supply, the two high-side supplies are generated through bootstrapping and post-regulation, while the low-side is created via post-regulation to 18 V.

This selected approach is both uncomplicated and cost-efficient, making it an excellent solution for implementation. By utilizing the bootstrap method, the high-side gate driver voltage supply can be generated with minimal components, requiring only a high-voltage diode and a resistor from the low-side gate driver supply.

For instance, Figure 12 shows the bootstrap circuit utilized in the interleaved totem-PFC with CoolSiC™ from Infineon and isolated gate driver.

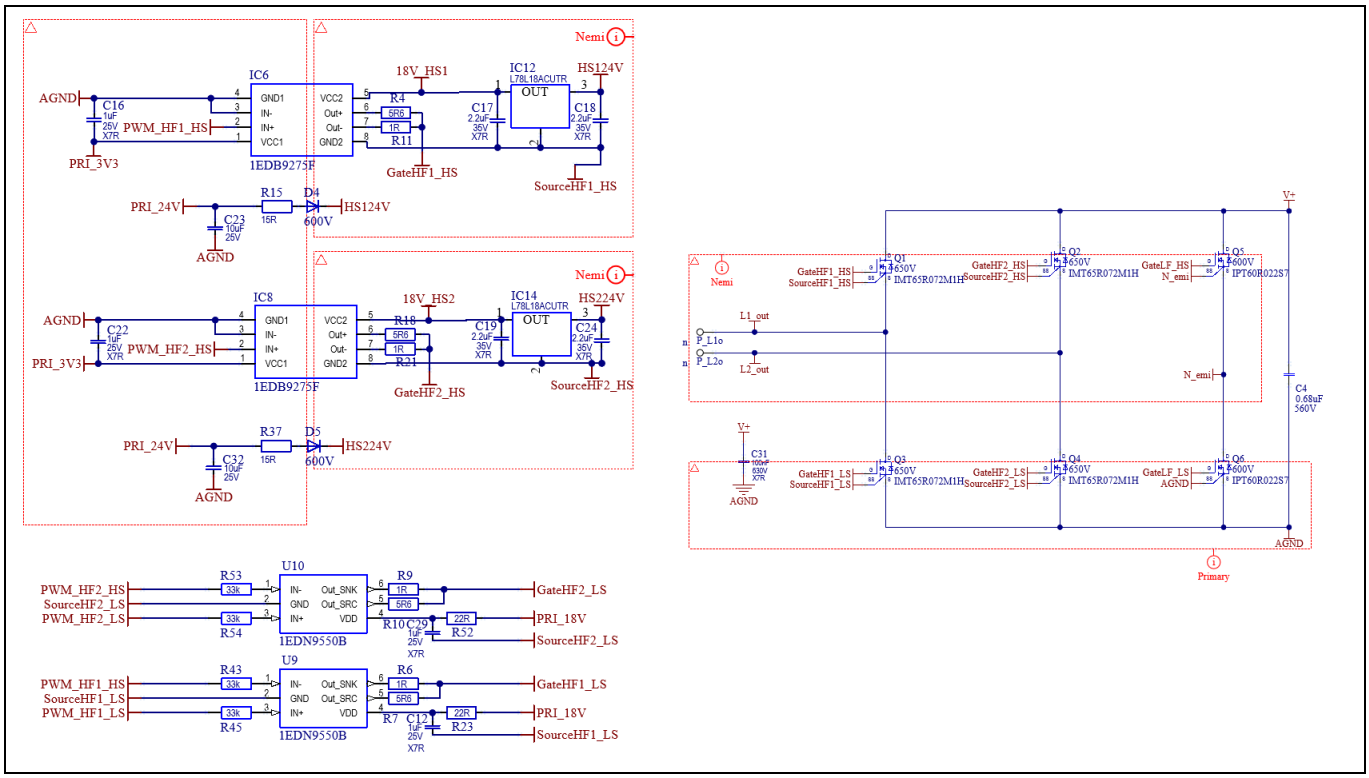


Figure 12 Driving CoolSiC™ with 1EDB9275 + 1EDN9550 gate drivers

The SiC MOSFETs can be affected by the gate voltage supply and reducing the recommended voltage can result in an increase in channel resistance. In PFC CCM totem-pole topology, the use of a bootstrap circuit can cause modulation of the high-side gate voltage under certain conditions. This modulation, shown in Figure 13, stems from the body diode conduction of the SiC MOSFETs. Essentially, when the high-side MOSFET device functions as a “diode”, the gate voltage follows the shape of the input AC, decreasing when the input peaks and leading to the largest duty cycle. Consequently, this results in increased conduction losses in the high-side device while it acts as a diode and conducts with the channel. Conversely, when the high side is the active switch, the gate voltage increases. To address this cross-modulation issue, the classic bootstrap is enhanced with a low-dropout regulator (LDO) post-regulation stage for the gate driver bias supplies.

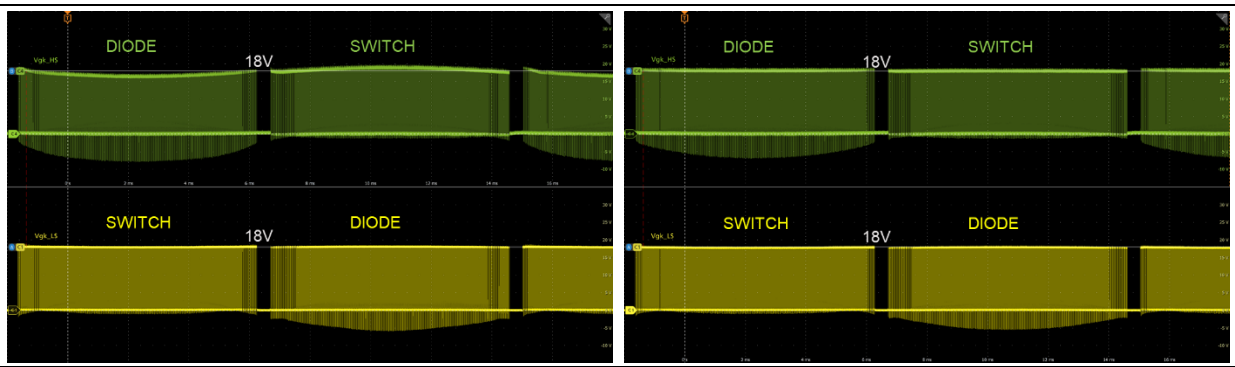


Figure 13 Vgs voltages of CoolSiC™ in the high frequency leg of a totem pole PFC

The driving of the CoolMOS™ MOSFET is shown in Figure 14. A hybrid driving approach with an isolated high-side and non-isolated low-side switch has been adopted. In addition, for the four CoolMOS™ MOSFETs synchronous rectification legs that are switching at 50 Hz a bootstrap approach has been adopted to minimize costs. In this case, proper capacitor dimensioning is required to discharge and avoid hitting the undervoltage lockout (UVLO) threshold of the driver.

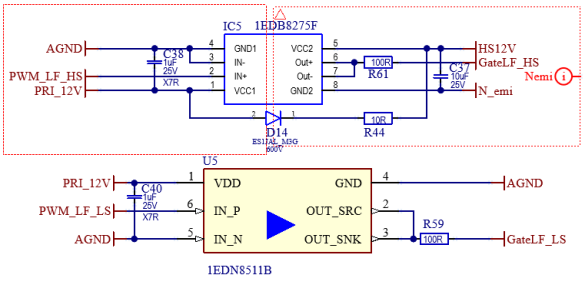


Figure 14 Driving CoolMoS™ MOSFET with hybrid driving (1EDB8275F + 1EDN8511B gate drivers)

2.3 Experimental results: Interleaved PFC steady state-operation

This section provides a summary of the experimental results pertaining to the steady-state operation of the interleaved PFC with a specific focus on the steady-state waveforms at 115 V RMS and 230 V RMS AC. It will showcase the behavior of the PFC during full-load operation and the efficiency of the PFC at 115 V and 230 V AC RMS.

2.3.1 Steady-state operation

Figure 15 shows the main steady-state waveforms of the PFC for a 115 V AC at 50 Hz and Figure 16 for a 230 V AC at 50 Hz under nominal load conditions. These figures show the interleaved totem-pole PFC in a steady-state condition. The top of both figures shows the AC input voltage (Ch1), while the second channel (Ch2) represents the input current. Ch3 and Ch4 exhibit the inductor current in the first and second PFC chokes, respectively, followed by the bulk voltage (Ch5) at the end.

Figure 17 shows the benefit of the interleaving PFC of the AC input current of the converter.

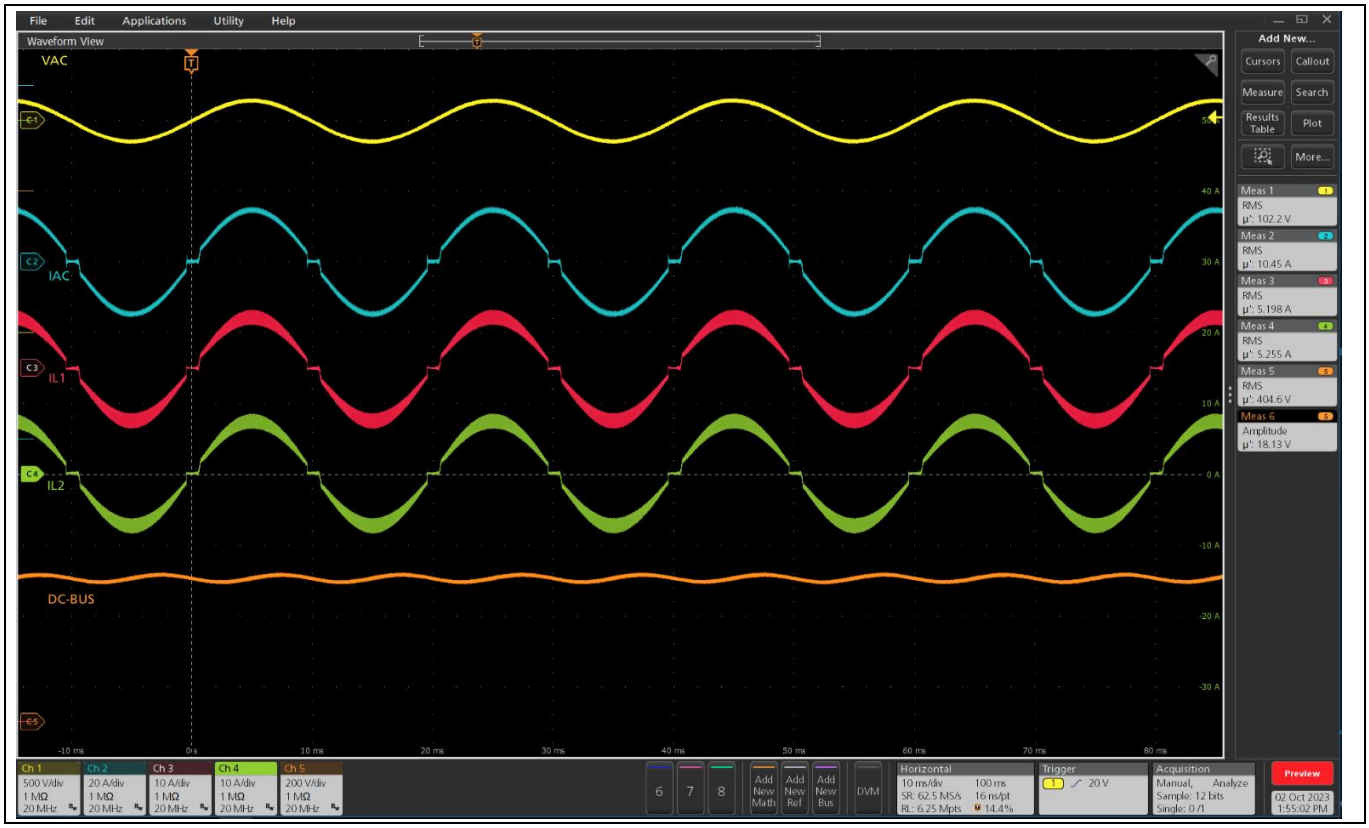


Figure 15 PFC steady-state waveforms at 115 V AC and at full load condition

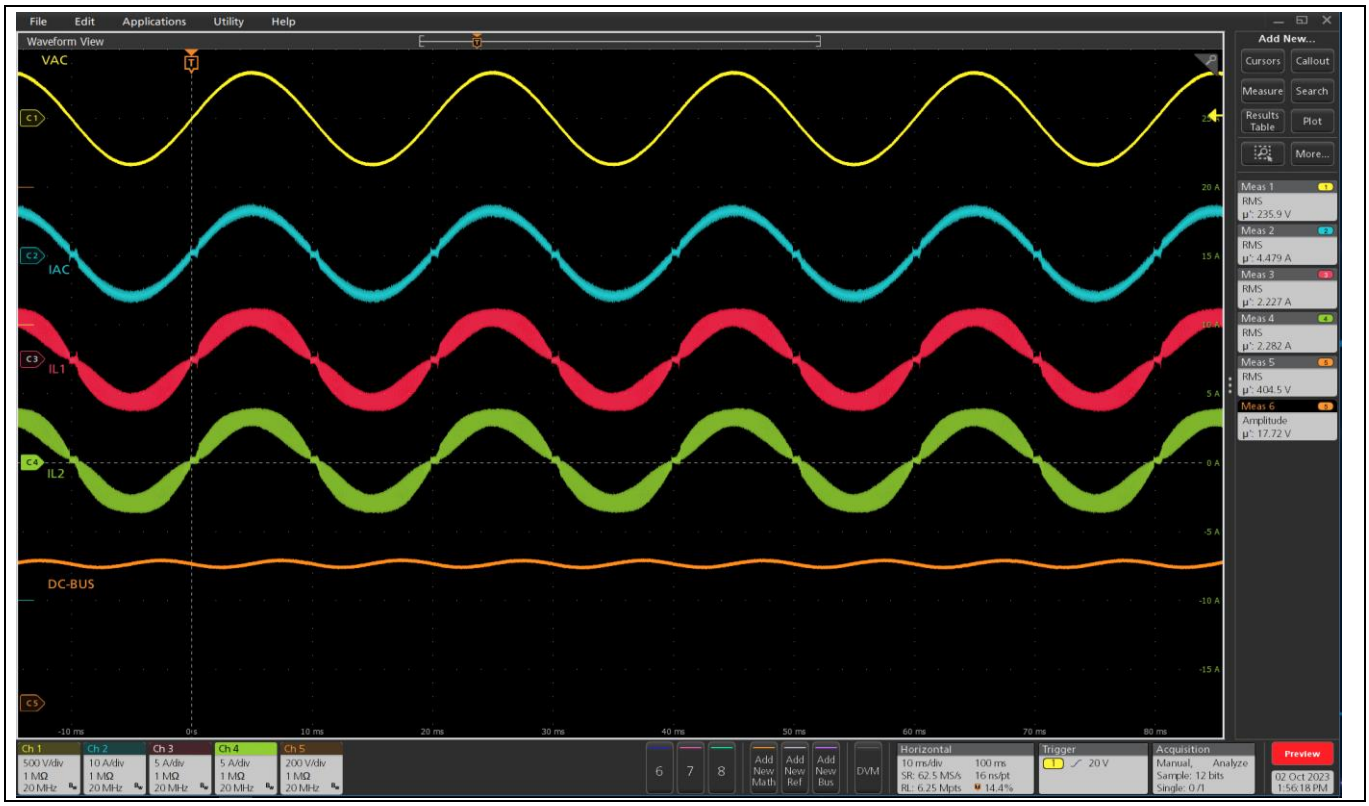


Figure 16 PFC steady-state waveforms at 230 V AC and at full load condition

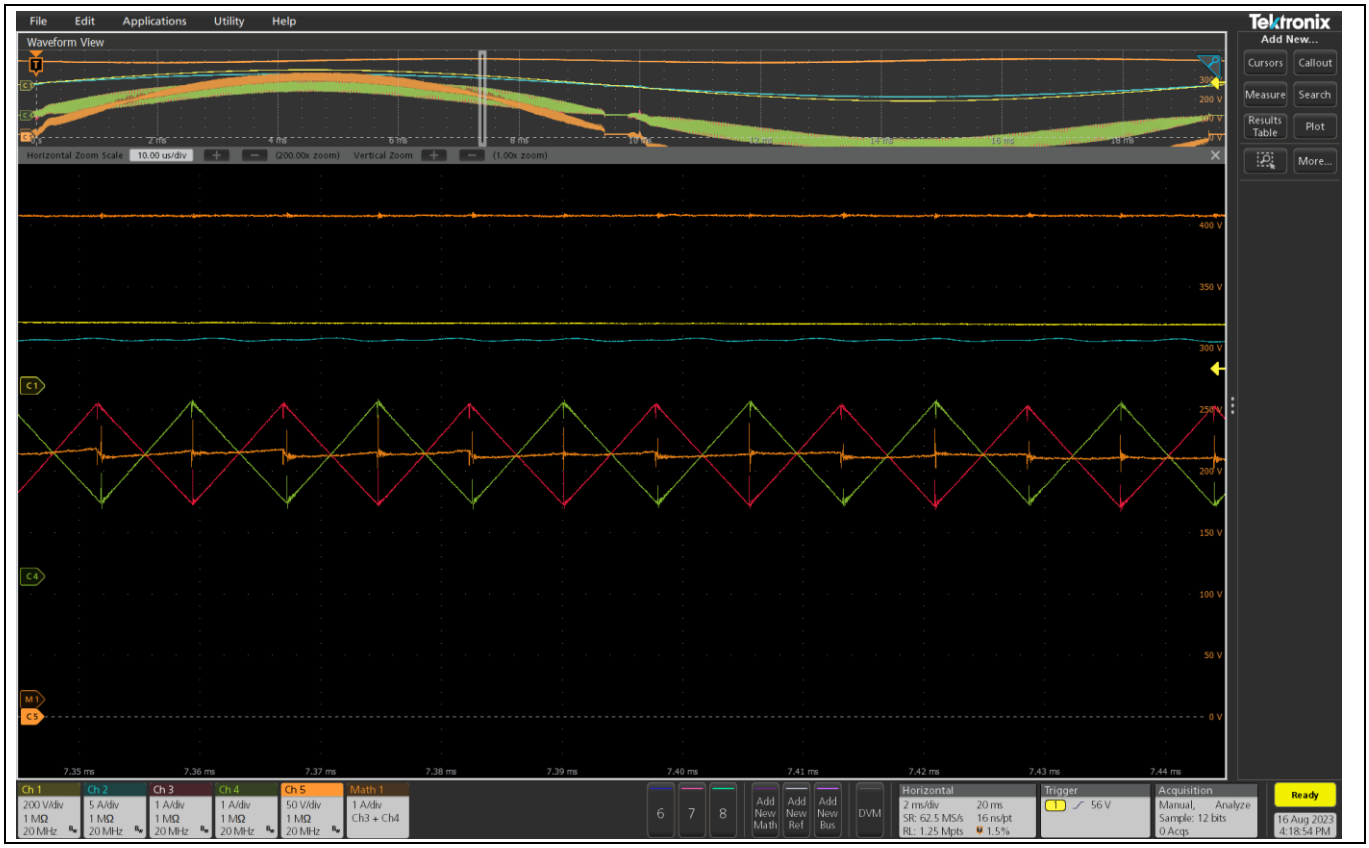


Figure 17 Interleaving effect in the input current of the PFC

2.3.2 Interleaved PFC efficiency

The efficiency of the single PFC stage is determined at ambient temperature, following 30 minutes of operation at full-load condition to attain a stable temperature of the PSU. Figure 18 shows the efficiency outcomes obtained at both low- and high-line conditions. In particular, the PFC is running in interleaving mode in both cases.

As shown efficiency in Figure 18, the peak is 98.8% at nearly 1000 W of output power. At 115 V AC, the efficiency level reaches a peak value of 97.7% at approximately 600 W.

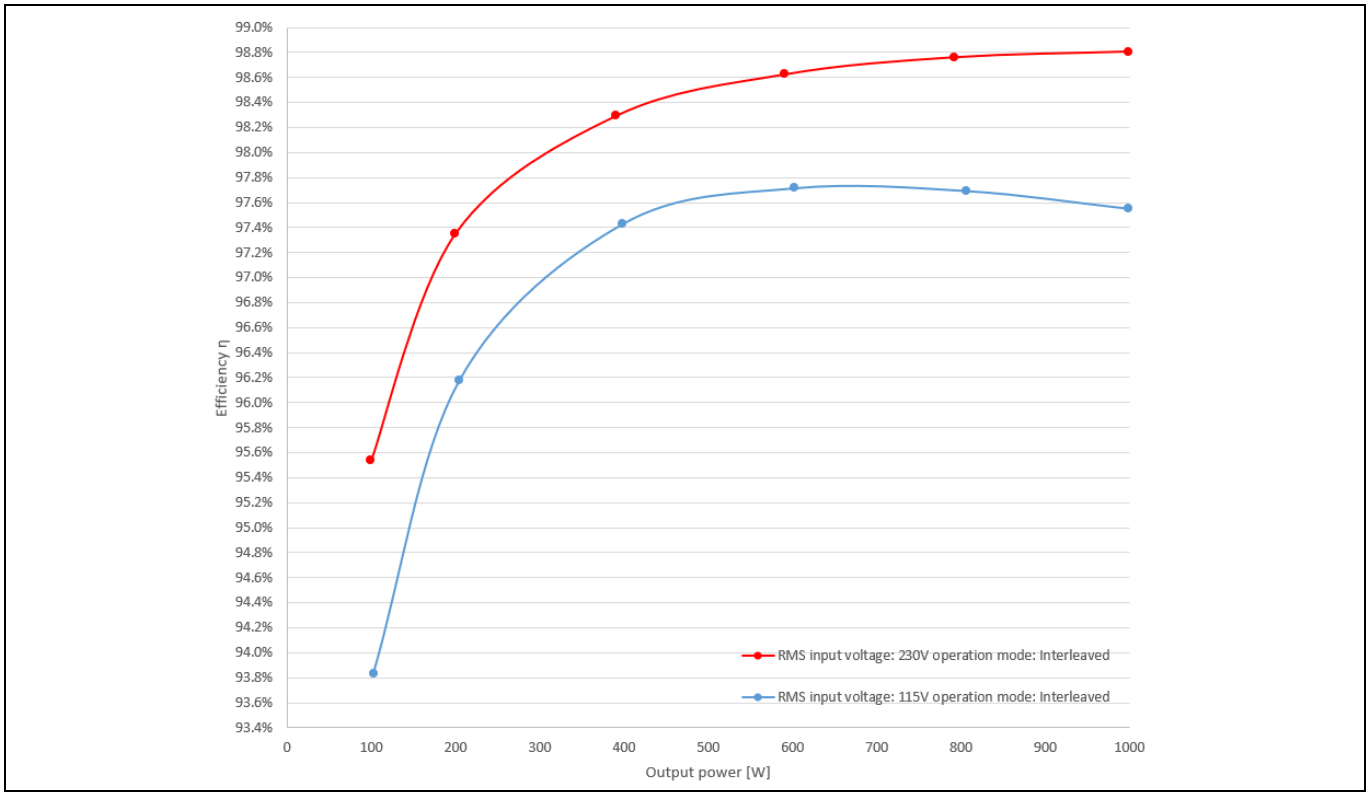


Figure 18 Measured PFC efficiency in interleaving mode at 230 V and 115 V RMS AC

2.4 Half-bridge LLC

The efficiency of the LLC converter with 400 V input and 12 V output considering a variable switching frequency ranging from 90 kHz to 135 kHz. The resonant tank values are 132 nF for the resonant capacitor and a 15 µH for the resonant inductor for an equivalent resonance frequency of 113 kHz.

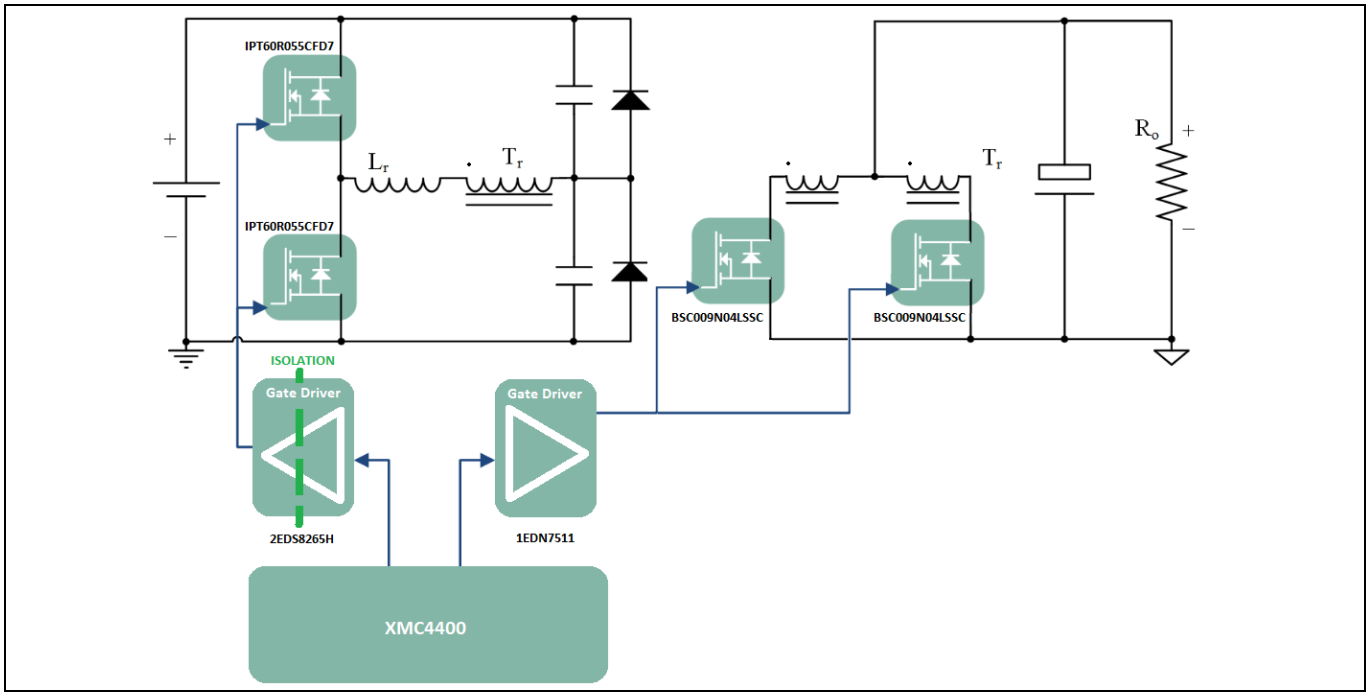


Figure 19 Schematic of the LLC HB DC-DC converter

Figure 20 shows a comparison between the estimated efficiency of the LLC (orange plot) and the actual measured efficiency (yellow plot). The data indicates a close alignment at mid-load, with some variances observed at light and full-load conditions. Despite these discrepancies, the tool provides valuable insights into the behavior of the LLC converter across the entire load range, offering a comprehensive understanding from light to full load conditions.

It is worth mentioning the high peak efficiency, nearly 97.3 percent at 50 percent of the rated load condition. Note that the overall efficiency of the complete PSU is the result of multiplying the separate efficiencies of the conforming blocks and is necessarily lower than any of them separately. However, some of the loss contributions are shared between the two blocks (e.g., auxiliary bias) and therefore, the resulting overall efficiency is still expected to fall within the target specifications.

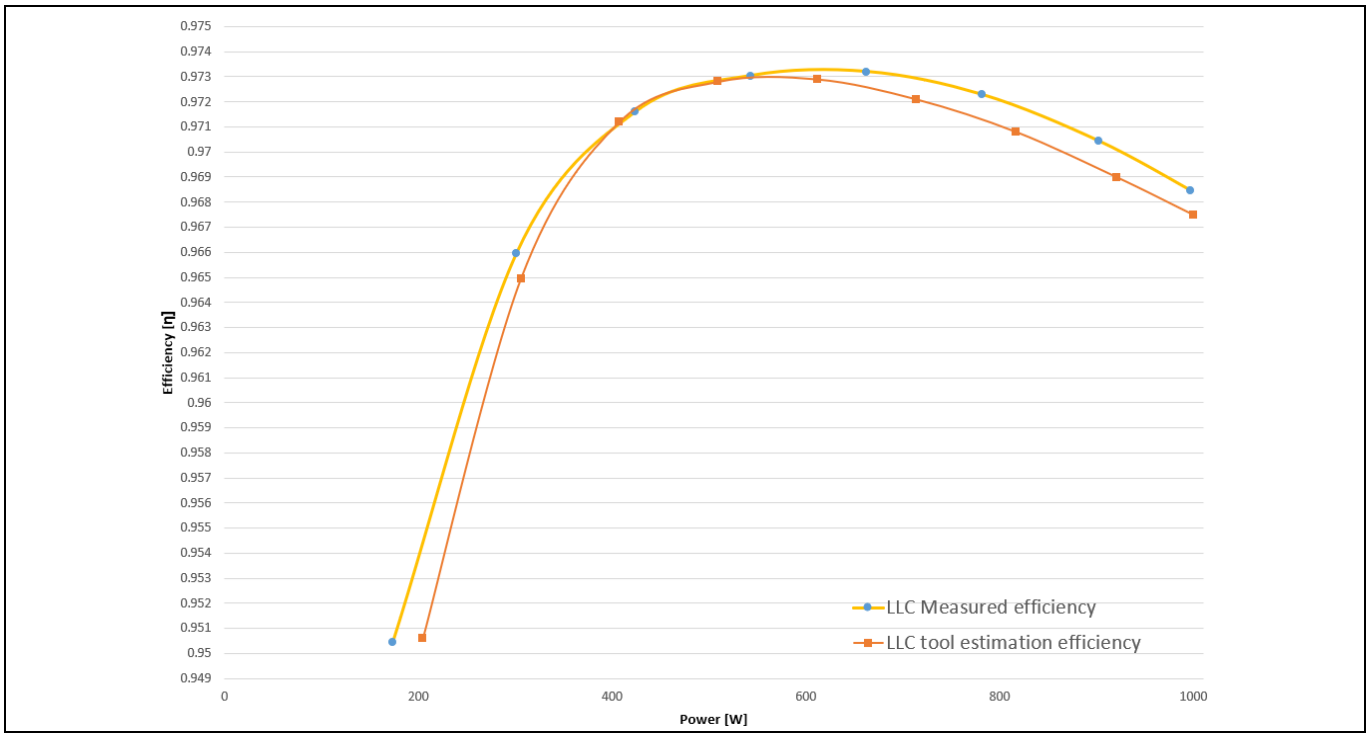


Figure 20 Estimated efficiency of the LLC DC-DC converter at 400 V DC input and 12 V DC output

Figure 21 shows the distribution of losses across various devices at different operating points for the LLC. It is evident that the majority of losses are primarily concentrated on the LLC transformer, aligning with expectations.

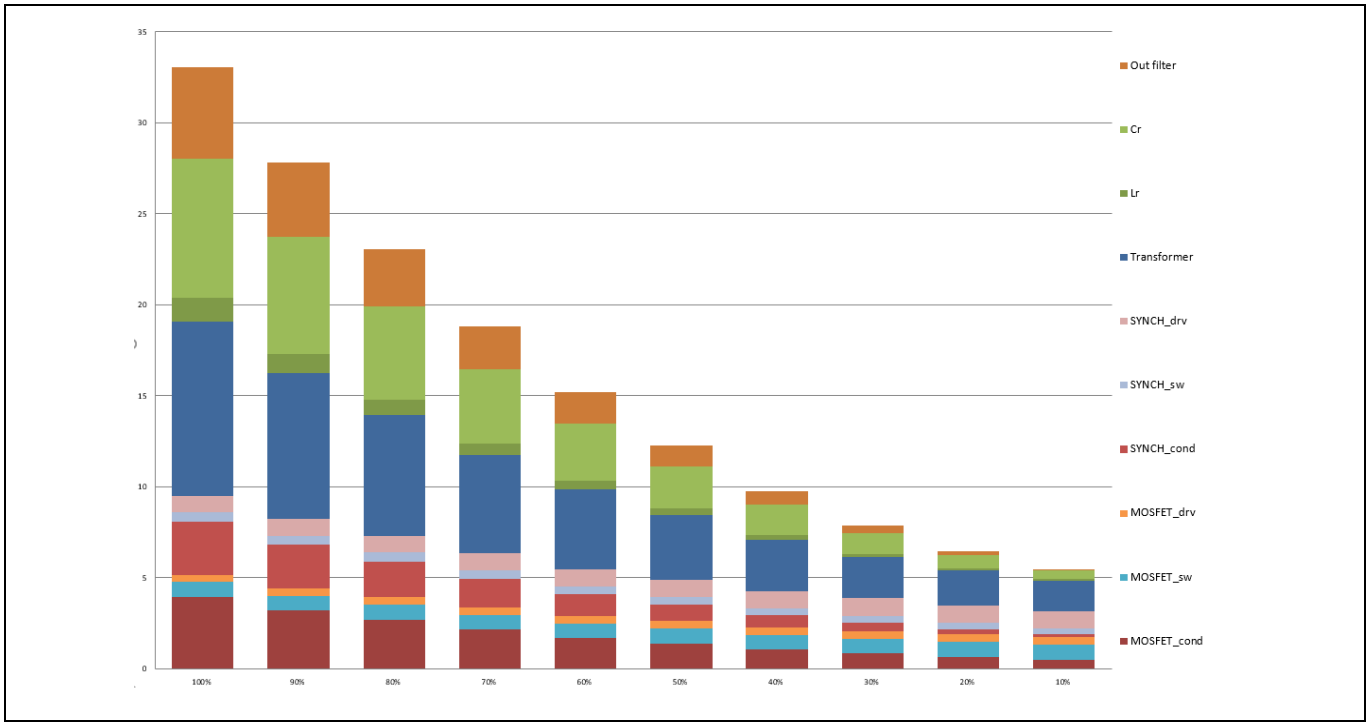


Figure 21 Estimated distribution losses of the LLC at different loads

2.4.1 LLC magnetics

The resonant tank of the LLC series-parallel resonant converter comprises two equivalent inductors and one equivalent capacitor.

One of the advantages of this topology is that it is possible to realize the series resonant inductor (L_r) by the leakage of the main transformer and the parallel resonant inductor (L_m) by the magnetizing inductance of the main transformer.

Nevertheless, the full integration approach constrains the design and compromises the performance of the converter. Therefore, in the LLC the series inductor (L_r) has been realized as discrete components, although L_r is integrated within the same magnetic structure of the main transformer.

Figure 22 shows a simplified view of the construction of the resonant inductor (L_r) and the main transformer. The resonant inductor is built with a 3C95 PQ38/8/25 core from Ferroxcube, while the main transformer is built with two pieces of the same core and material. The L_r is stacked on the top of the main transformer and wound in the same direction as the primary-side winding. As a result of this, the flux in part of the volume is effectively canceled and the total core loss is partly reduced.

The main transformer is characterized by a 16:1 turn ratio, with the primary windings spread across four PCBs aimed at minimizing the equivalent series resistance (ESR) and optimizing efficiency. On the secondary side, 12 interleaved copper plates, arranged in a center-tapped mode as shown in Figure 23, serve two specific purposes: to accommodate high circulating currents and minimize losses while enhancing thermal dissipation. Additionally, the winding of L_r is constructed using Litz wire, comprising 512 strands of 0.05 mm diameter.

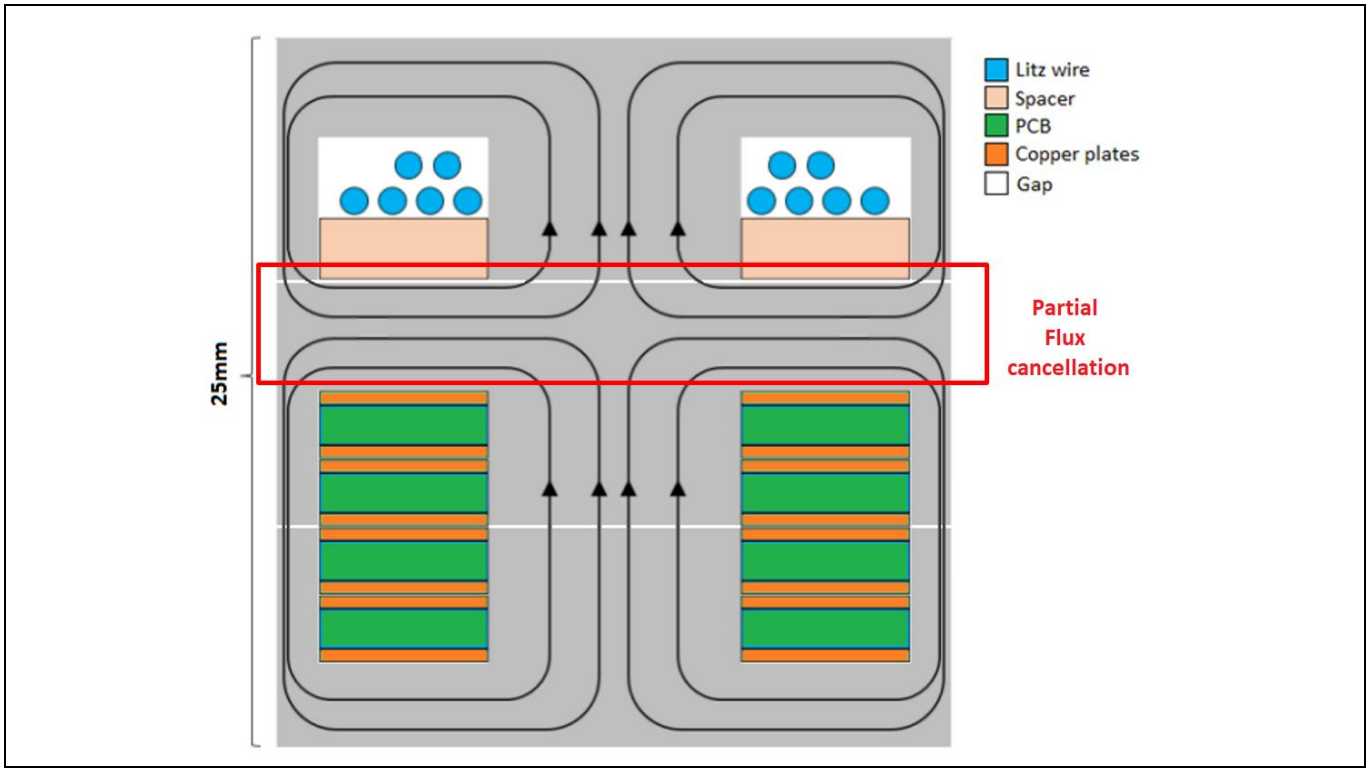


Figure 22 Structure of the LLC transformer

Because of the height limitation of the PSU (27 mm), cut the main board to accommodate the height of the integrated L_r plus of the main transformer structure (approximately 25 mm). The cutout helps at the same time with the thermal management due to a direct thermal connection of the magnetic core with the aluminum base plate by using a thermal interface.

Figure 23 displays the mechanical internal construction of the LLC main transformer. The detailed figure helps to visualize the internal composition of the transformer and enhances the comprehension of its structure.

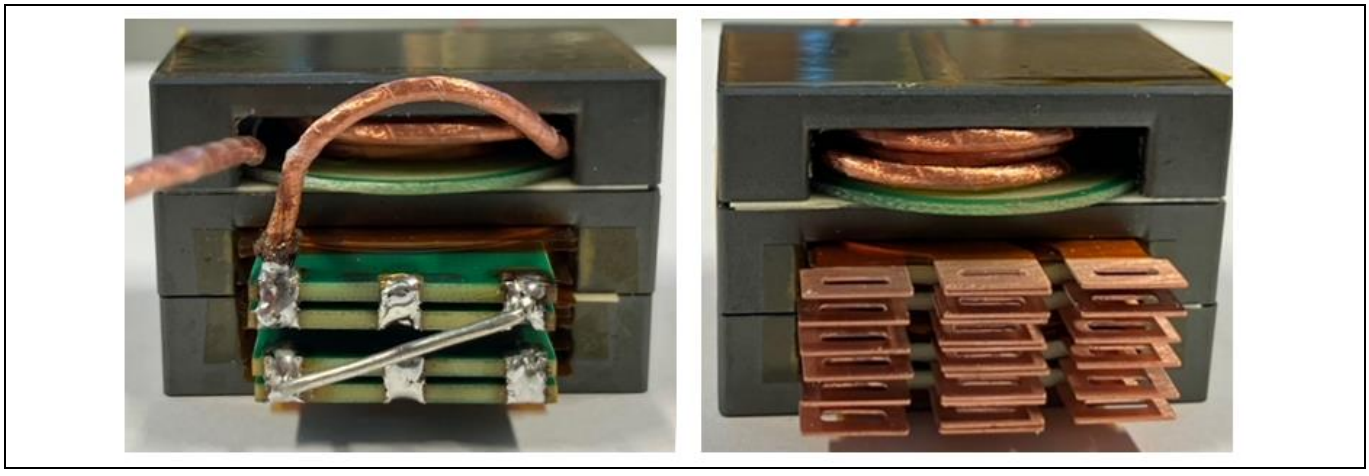


Figure 23 Detailed view of the fully assembled LLC transformer

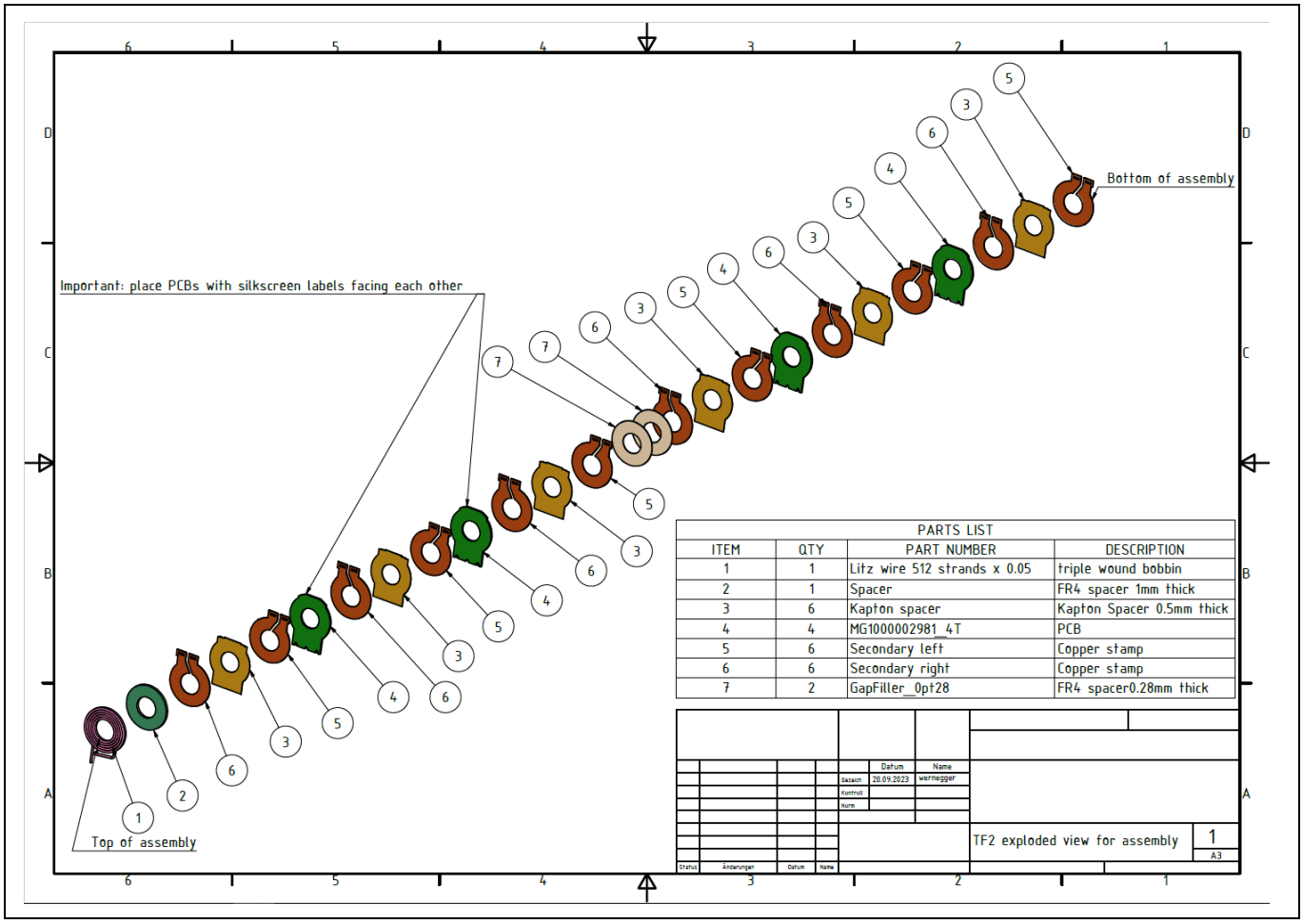


Figure 24 Mechanical drawing of LLC main transformer winding arrangement

2.5 Driving CoolMOS™ in the LLC converter

The LLC converter primary side uses two CoolMOS™ 55 mΩ devices in TOLL package (CoolMOS™ IPT60R055CFD7).

XMC4400 MCU ground pertains to the LLC converter's secondary side. To control the LLC half-bridge and ensuring isolation between the primary and secondary sides, a EiceDRIVER™ 2EDB8265H gate driver has been used as shown in Figure 25.

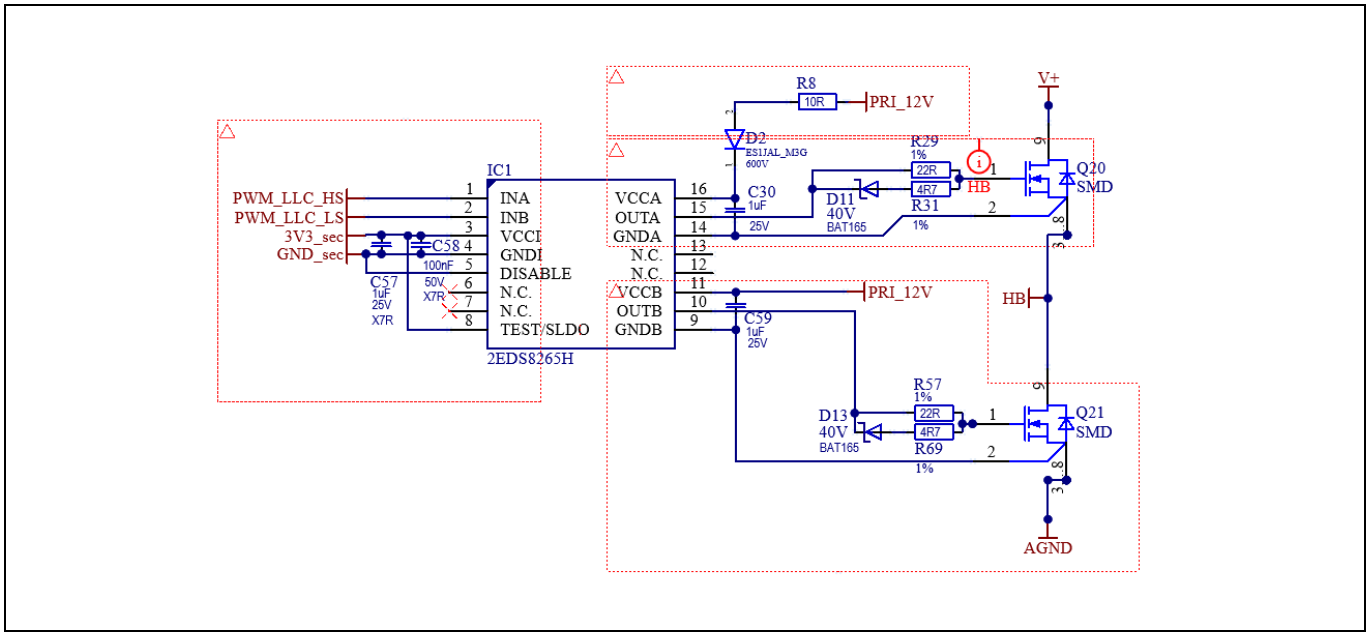


Figure 25 Driving LLC half-bridge CoolMoS™ (using EiceDRIVER™ 2EDS8265H)

2.6 Primary side: LLC steady-state operation

The LLC steady-state waveforms are shown in Figure 26 and Figure 27 for both 100% and 50% load conditions.

These figures showcase the resonant current waveform (Ch4), half-bridge low-side MOSFET drain-to-source voltages (Ch3), and half-bridge MOSFETs gate-to-source voltages (Ch1 and Ch2) at nominal input/output voltages. These waveforms provide a visual representation of the behavior of the LLC in steady-state operation under different load conditions.

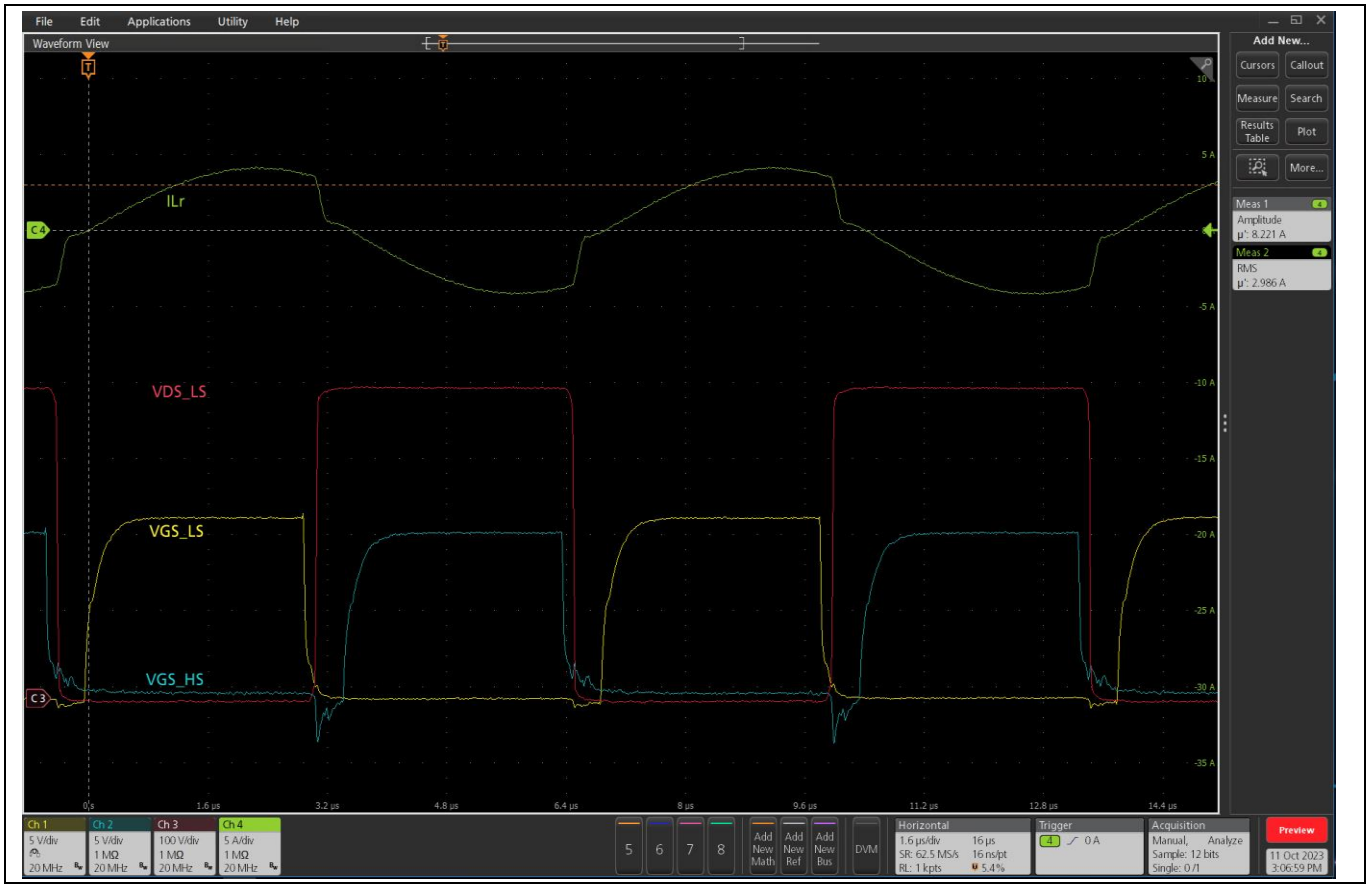


Figure 26 Primary side steady-state operation at 50% of the load

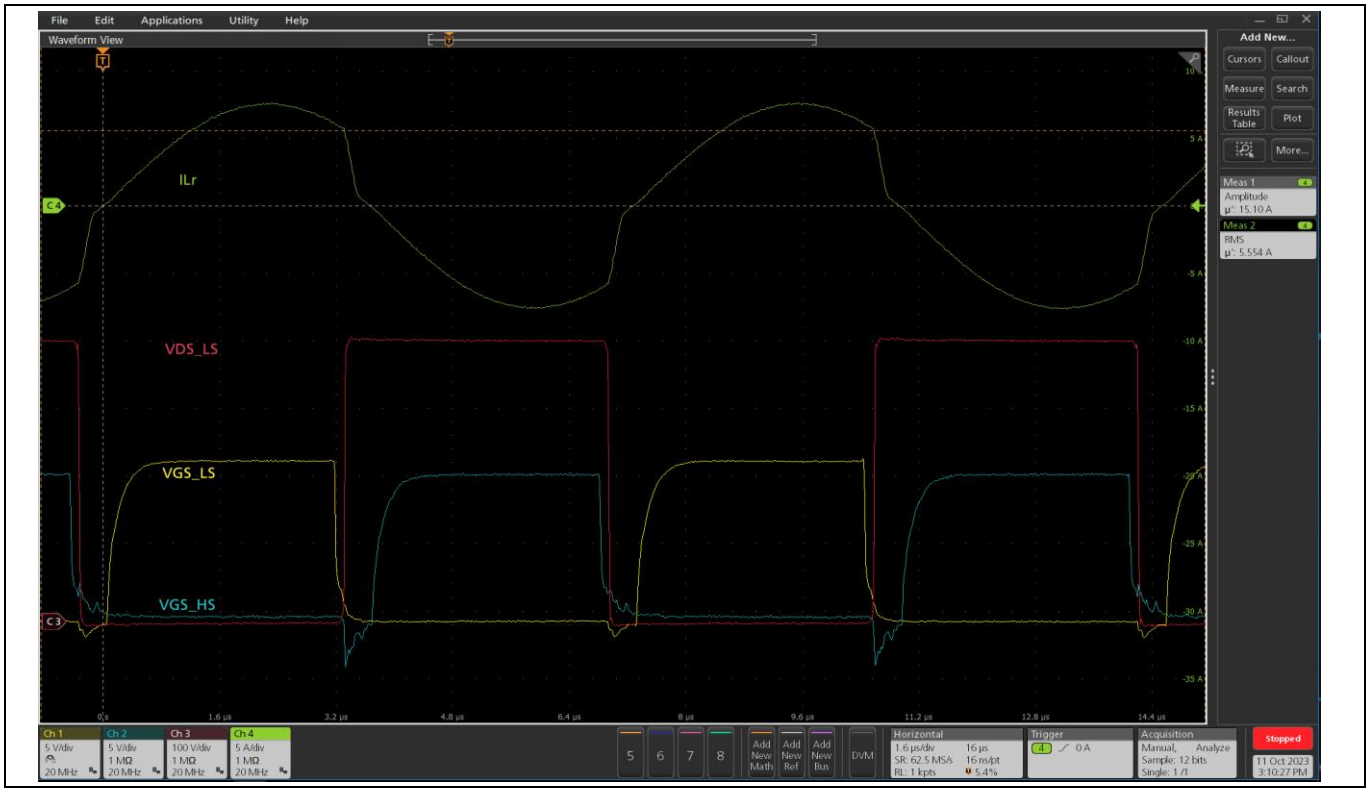


Figure 27 Primary side steady-state operation at 100% of the load

Figure 27 and Figure 28 provide a comprehensive view of the LLC converter's steady-state performance at 100% and 50% load from a secondary side perspective.

The middle of the picture displays the resonant current waveform (Ch4), while the output voltage waveform of the converter is shown at the bottom of the figure (Ch3).

Across the figures, it is evident that the maximum peak for the drain-source voltage of the synchronous secondary MOSFETs is consistently below 27 V.

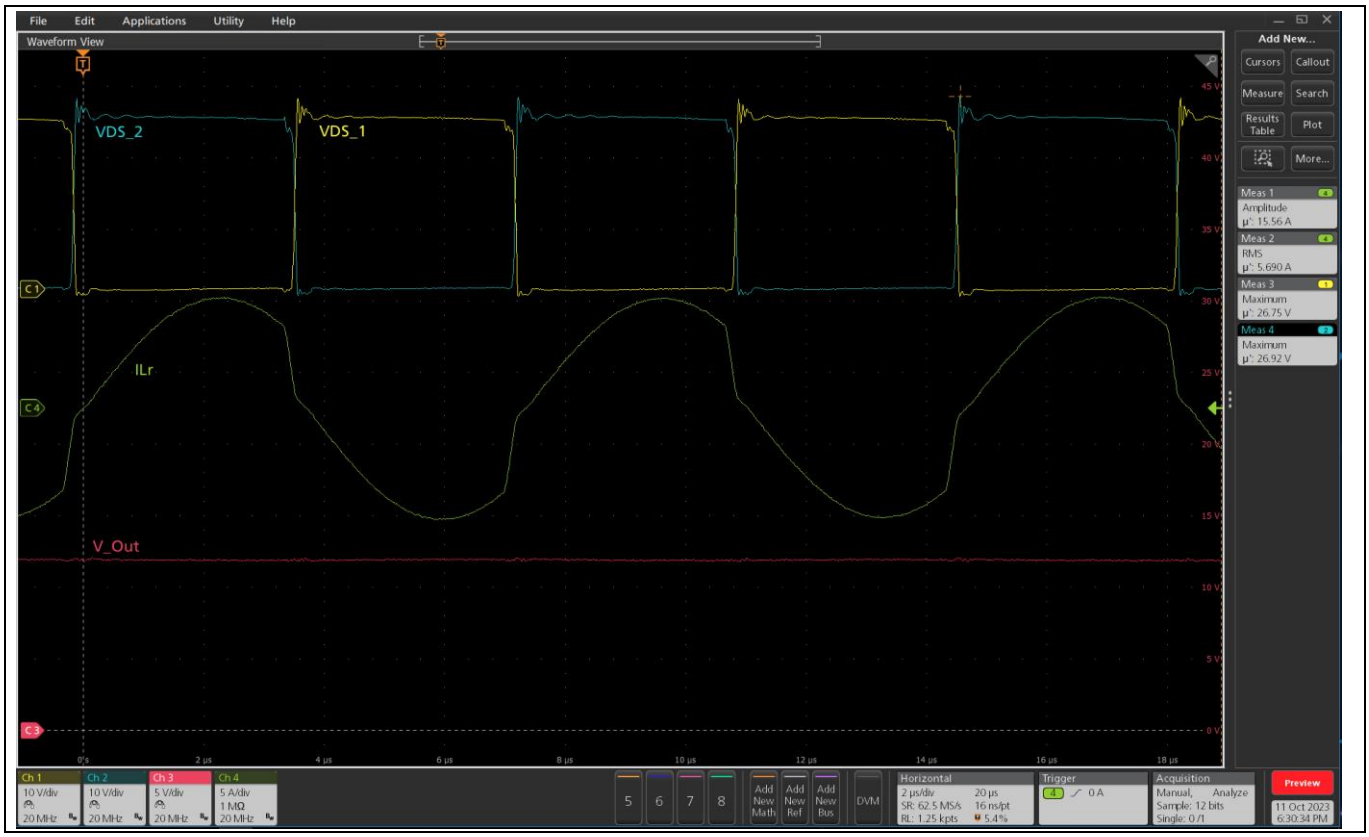


Figure 28 LLC in steady-state condition when running at full load condition

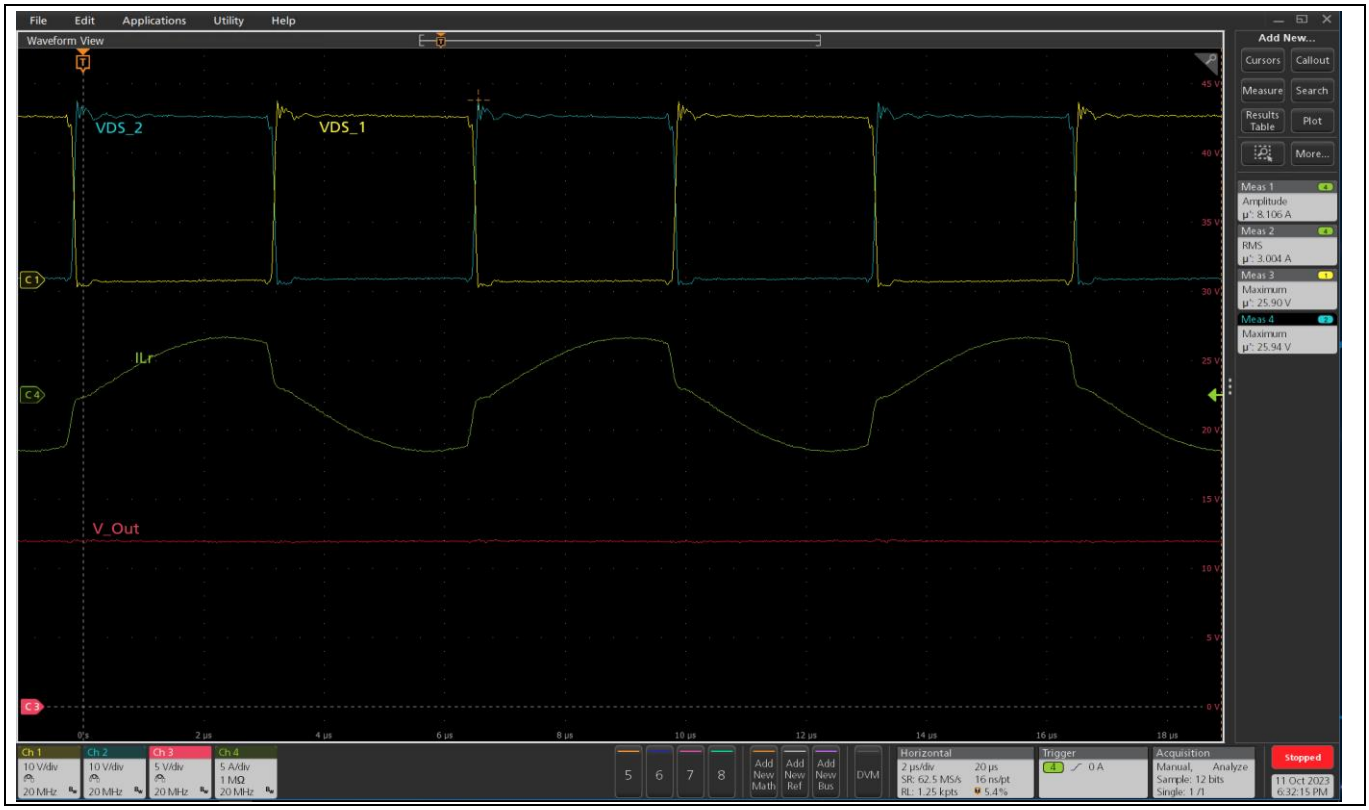


Figure 29 LLC in steady-state condition when running at 50 percent load

2.6.1 LLC efficiency

The efficiency of the only LLC stage has been measured at ambient temperature after running the converter for 60 minutes at full load condition to reach the steady-state temperature of the integrated transformer. In Figure 30, the efficiency results are displayed.

The LLC efficiency reaches an outstanding peak of almost 97.35 percent near 600 W of output power in the case of 400 V input voltage.

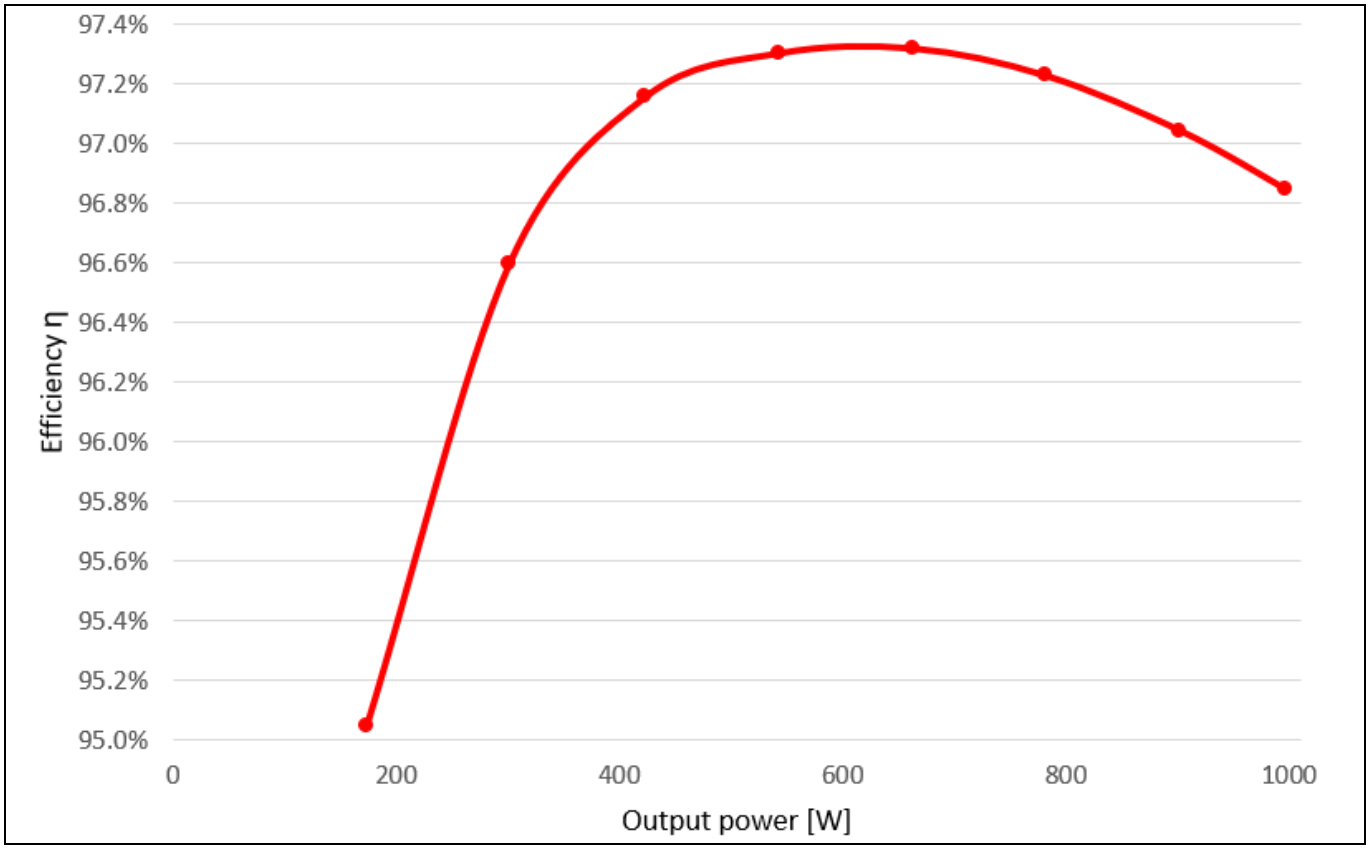


Figure 30 Measured LLC efficiency at 400 V input and 12 V output

3 Full power supply unit

This section provides a summary of the experimental results of the complete power supply.

3.1.1 Efficiency

The efficiency of the complete power supply is measured following a 60-minute run of the converter at full load condition.

In Figure 31, the efficiency results for 115 V and 230 V AC RMS input and 12 V DC output are presented together with the efficiency target.

Under high-line input voltage, the REF_1KW_PSU_5G_SiC board demonstrates a peak efficiency of nearly 96.4 percent at approximately 650 W. The PSU fully complies with the initial specification, maintaining an efficiency above 96 percent from around 45% of the load to full load condition.

Similarly, when supplied with 115 V AC, the power supply unit achieves an outstanding peak efficiency of almost 95.5 percent at a load of approximately 550 W, aligning with the original specification.

Furthermore, the measurements indicate that the PSU operates at an efficiency level above 95 percent from approximately 35% of the load up to full load at 115 V AC.

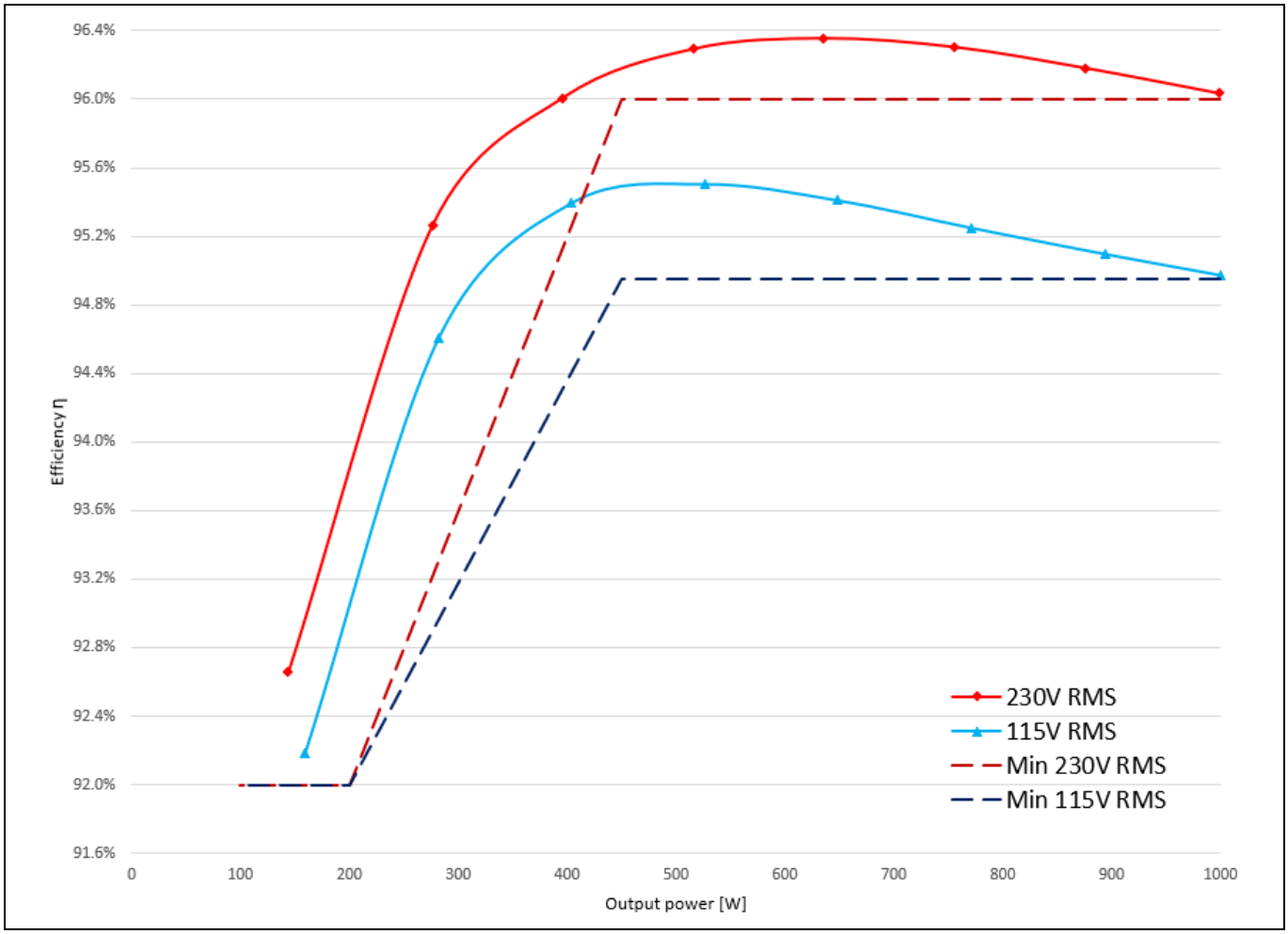


Figure 31 Measured efficiency of the complete PSU at 115 V and 230 V AC RMS

3.1.2 Start up

Figure 32 and Figure 33 show the PSU startup sequence at 100 V AC and 230 V AC respectively. These figures demonstrate the startup condition of the full power supply at full load conditions. The top portion of both figures displays the different parameters being measured, which includes PFC input voltage (Ch1), PFC input current (Ch2), current in the first PFC choke (Ch3), current in the second PFC choke (Ch4), LLC resonant current (Ch5), and the LLC output voltage (Ch6). At an input voltage of 100 V AC, the input current peaks at 20 A, and the sharing of this current in both PFC chokes is evident in Ch3 and Ch4. The last two channels, Ch5 and Ch6, show the LLC resonant current and output voltage, respectively.

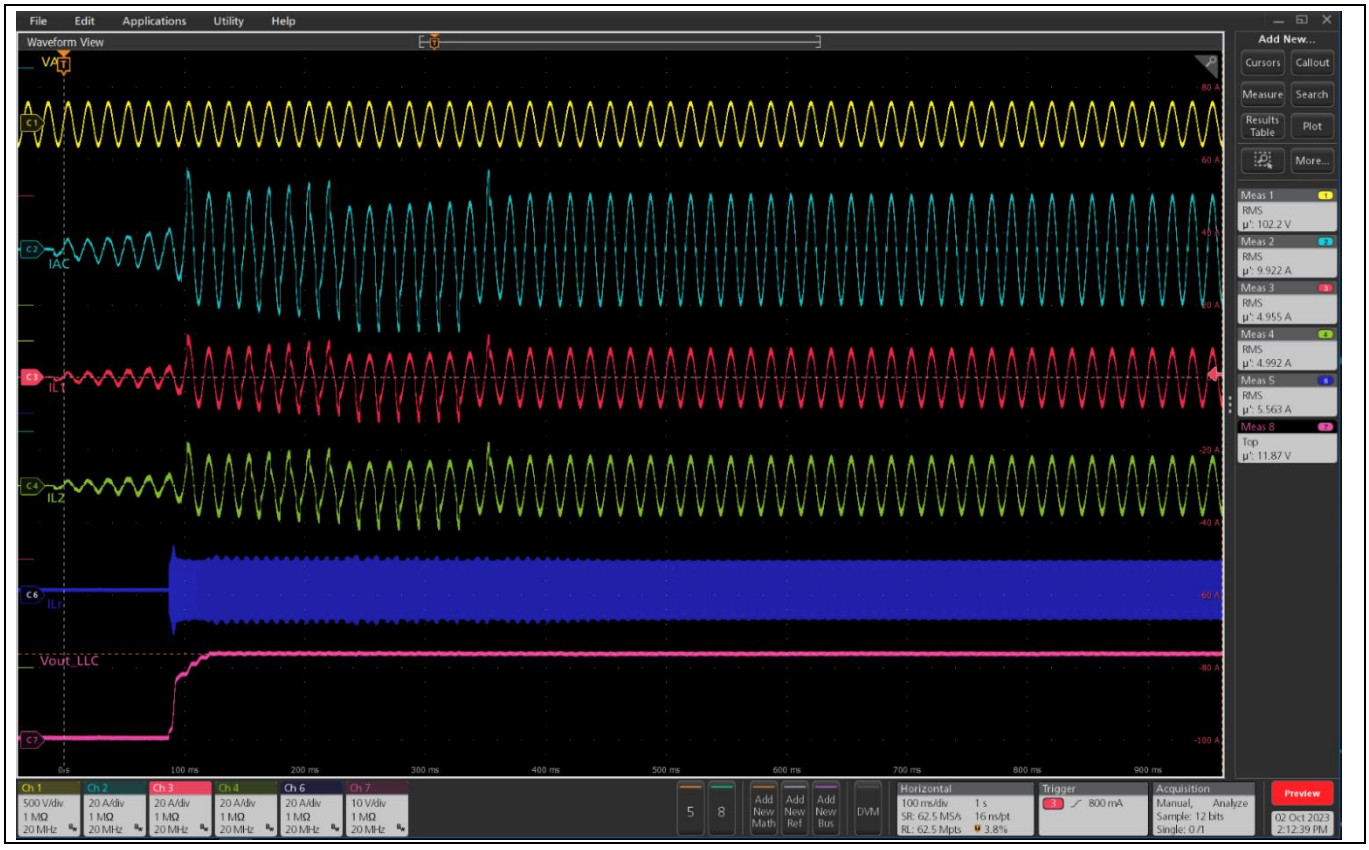


Figure 32 Startup sequence of the full PSU at full load at 100 V AC

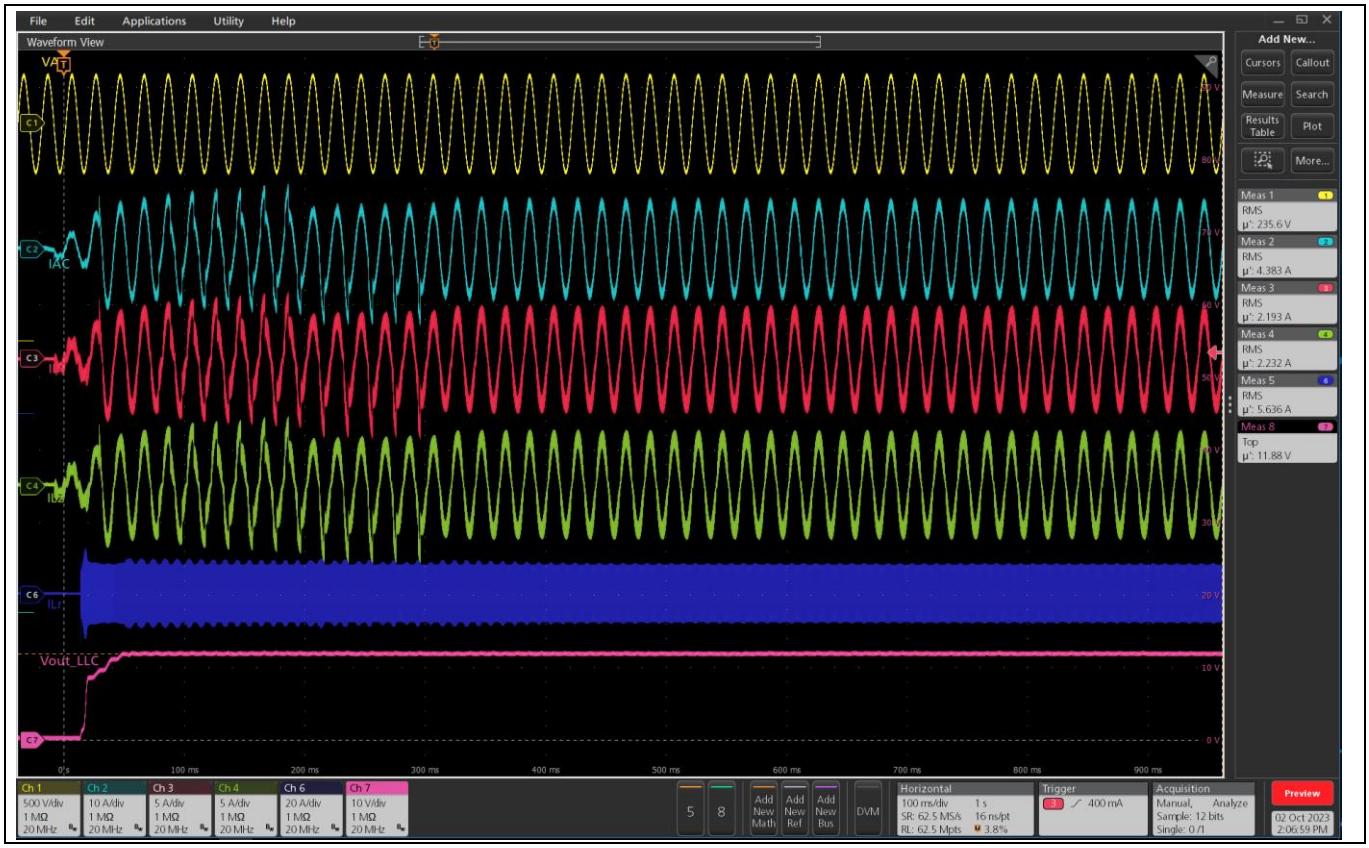


Figure 33 Startup sequence of the full PSU at full load at 230 V AC

The power factor (PF) and the THD have been measured at both low- and high-line V AC, as shown in Figure 34 and Figure 35. The PF is higher than 95% from 18% of the load at 230 V AC and always above 99% at 115 V AC.

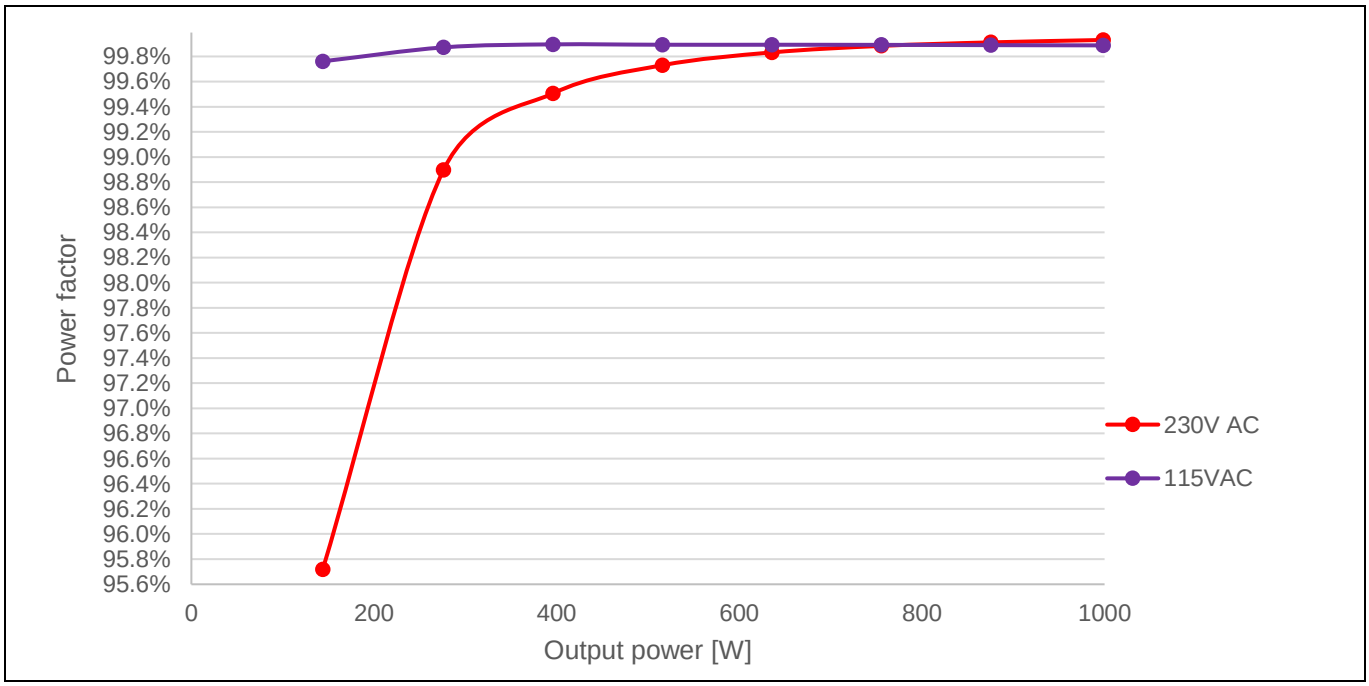


Figure 34 Measured PF of the complete power supply prototype

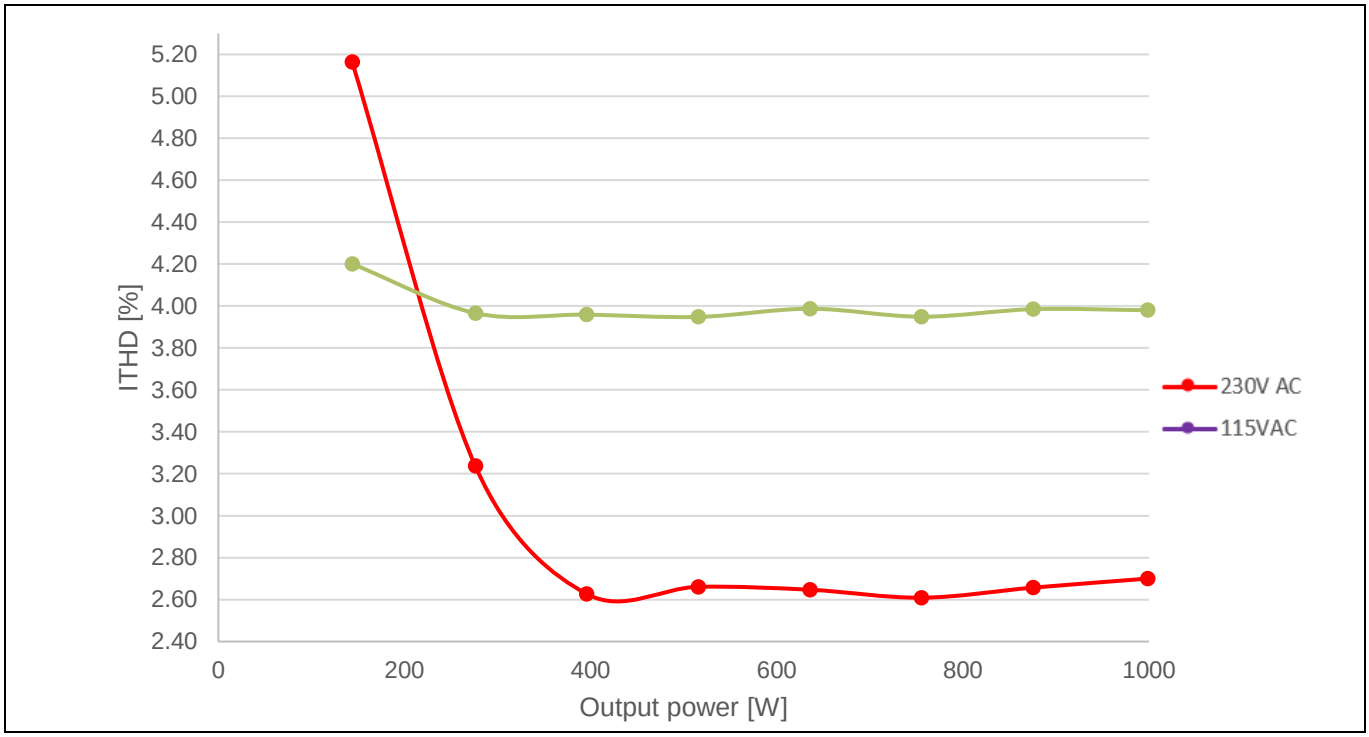


Figure 35 Measured current THD of the complete power supply prototype

3.1.3 Hold-up time

The PFC response and output voltage of the PSU during a 10 ms hold-up time at 100 percent load and an input voltage of 230 V AC is captured in Figure 36, with the event repeated for ten times every 100 ms. The bulk voltage drops to a minimum of approximately 328 V DC, while the output voltage complies with the specification, exhibiting a peak-to-peak variation of 1.2 V DC.

Furthermore, Figure 37 shows the same event as Figure 36, but with a line cycle drop-out applied at 45 degrees of the input voltage.

Moreover, Figure 38 and Figure 39 exhibit the same events as shown in Figure 36 and Figure 37, but with an input voltage of 115 V AC.

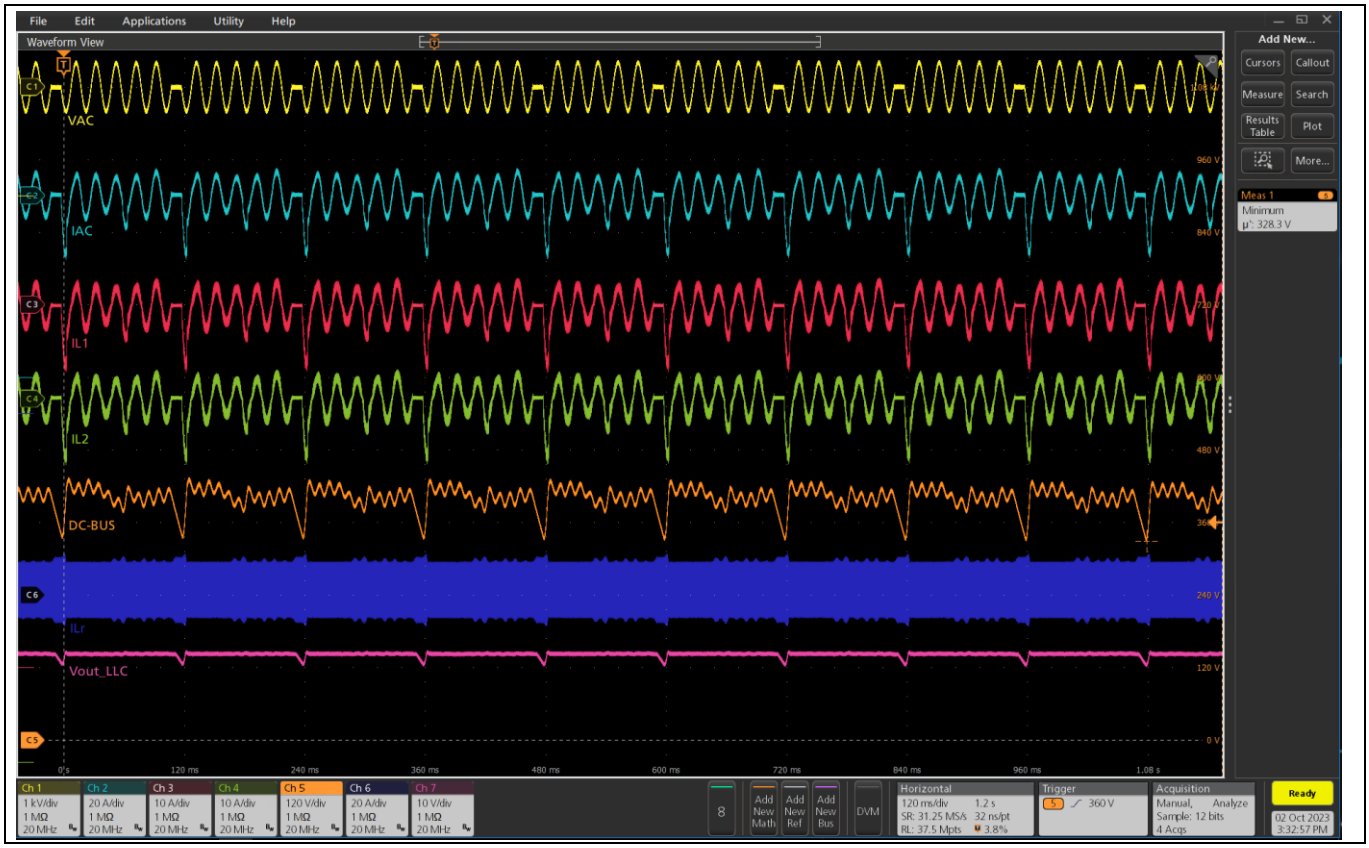


Figure 36 10 ms, 230 V AC, 50 Hz line cycle drop out at 0° and 100% load

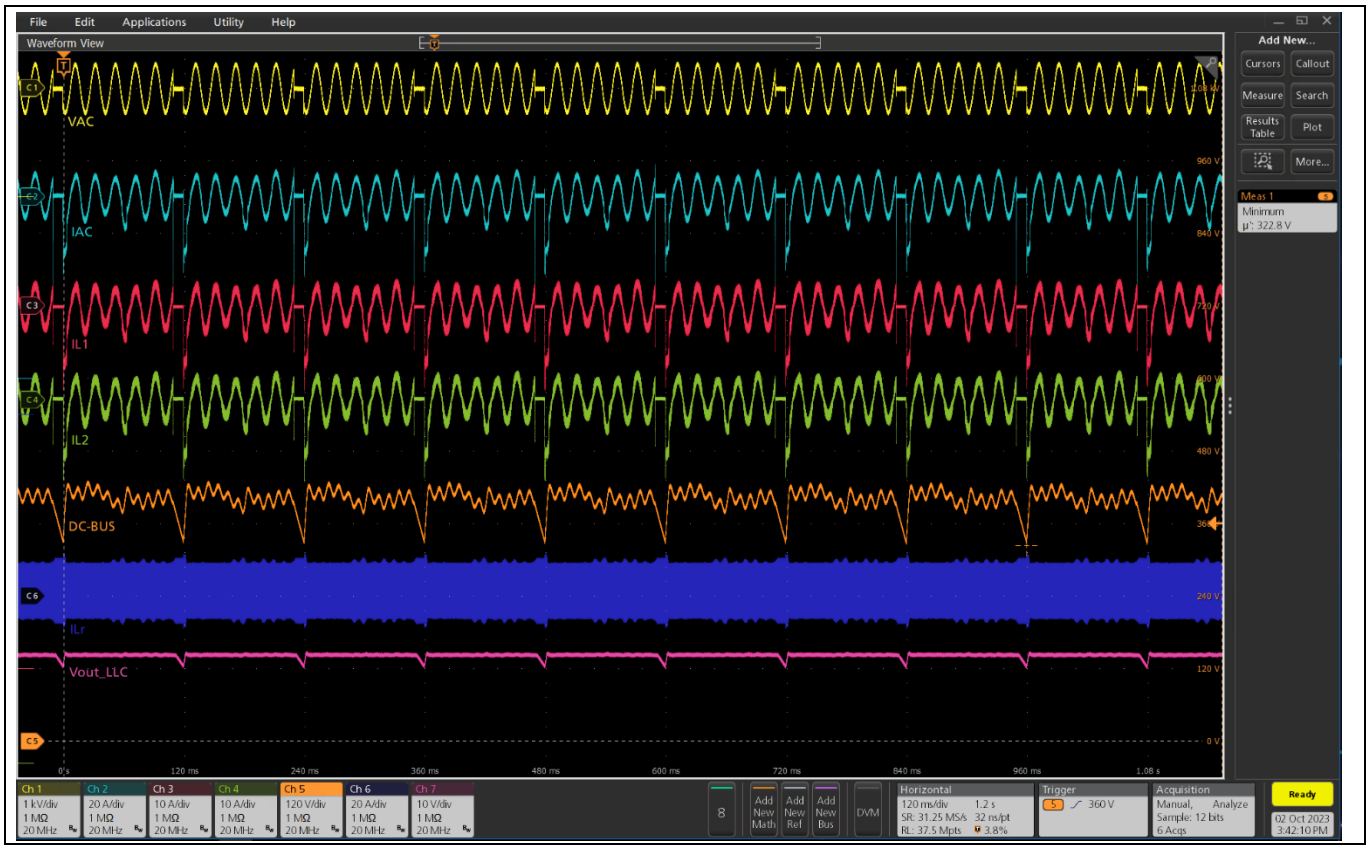


Figure 37 10 ms, 230 V AC, 50Hz line cycle drop out at 45° and 100% load

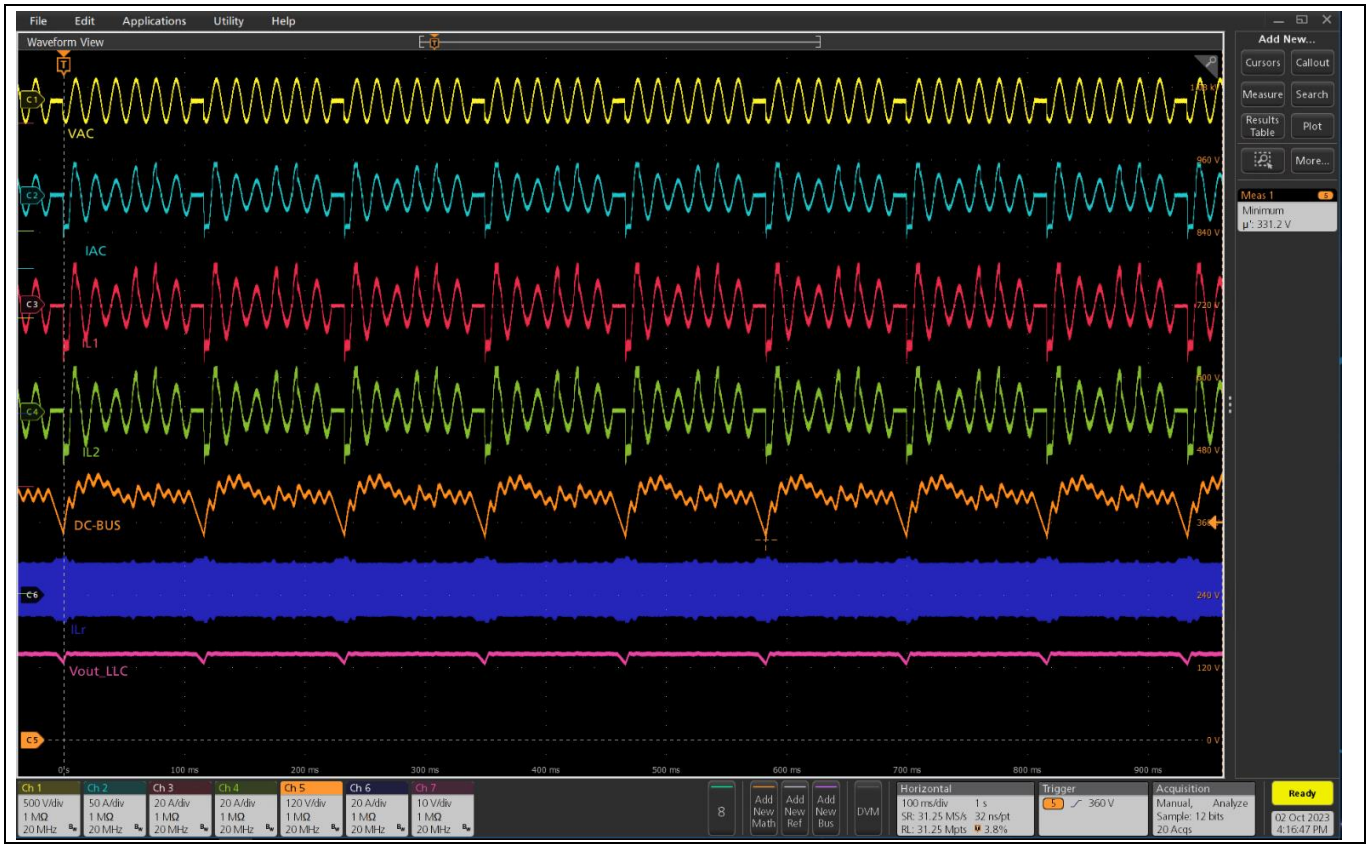


Figure 38 10 ms, 115 V AC, 50 Hz line cycle drop out at 0° and 100% load

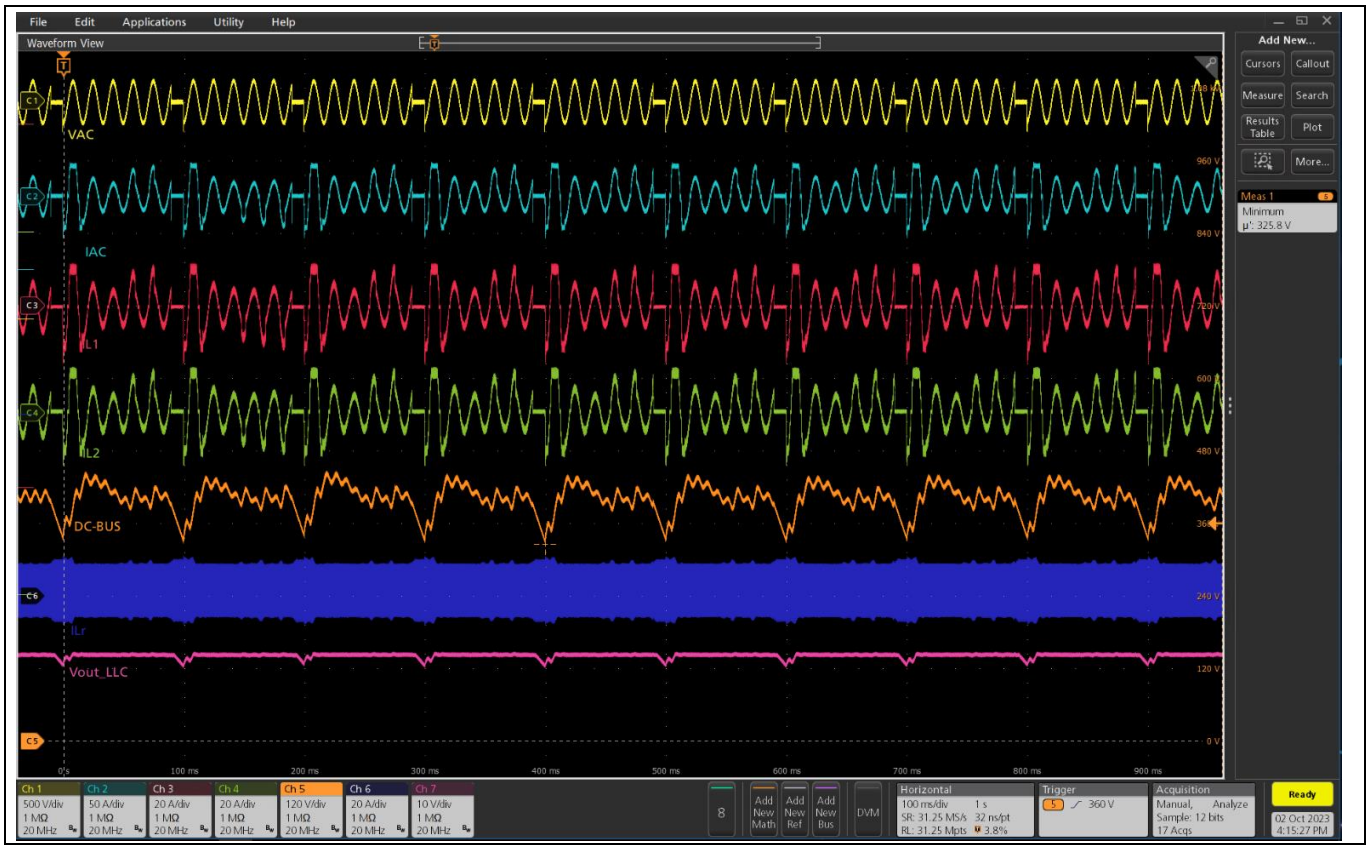


Figure 39 10 ms, 115 V AC, 50 Hz line cycle drop out at 45° and 100% load

3.1.4 Load-jump

These graphs show the output of the PSU, which is subjected to a load increase from 0 A to 83 A (Figure 40) and then to a load decrease from 83 A back to 0 A (Figure 41). These load jump tests demonstrate the PSU ability to handle sudden changes in current load and maintain a well-regulated output. The PSU is reliable even under challenging conditions.

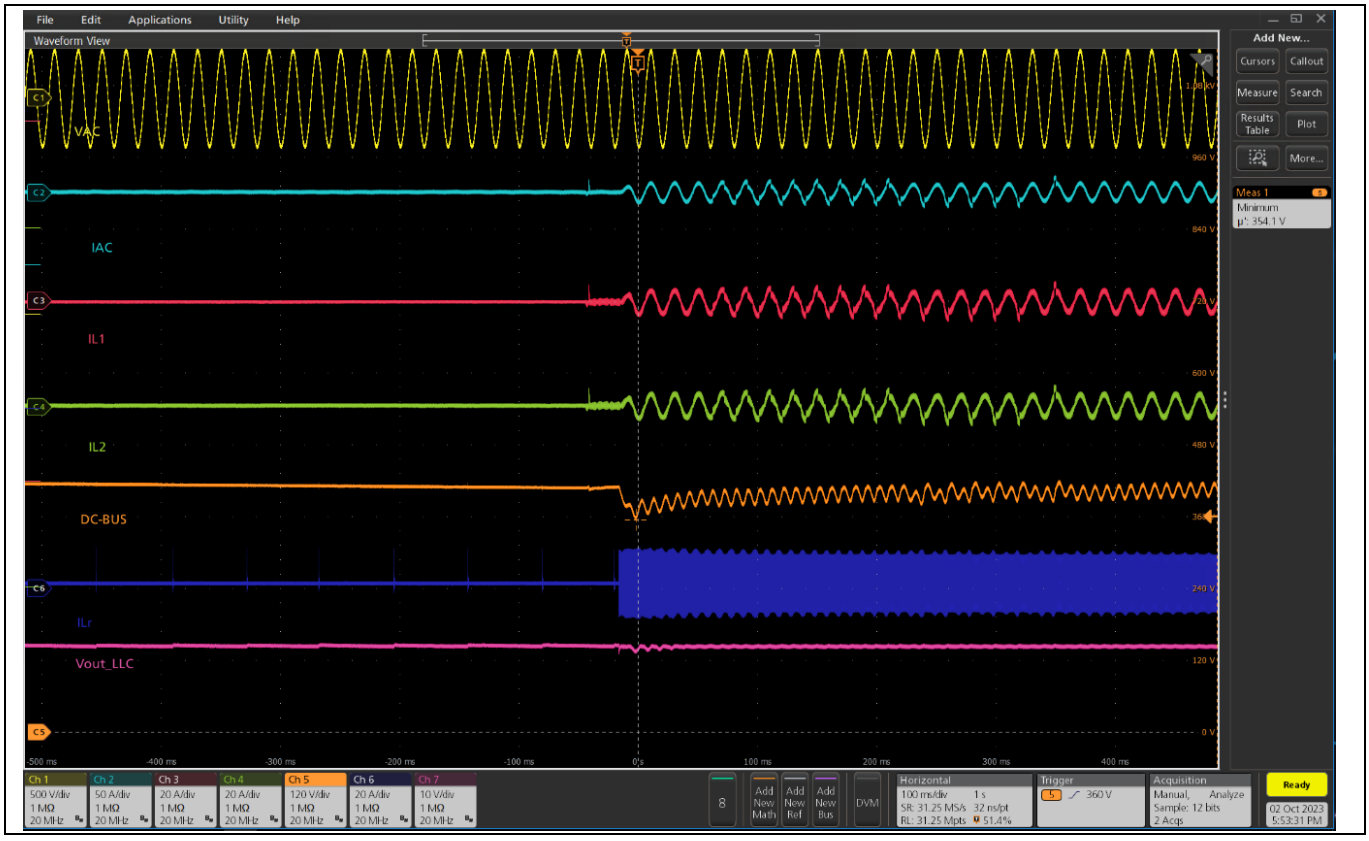


Figure 40 Load-jump of the complete PSU from 0% to 100% of load

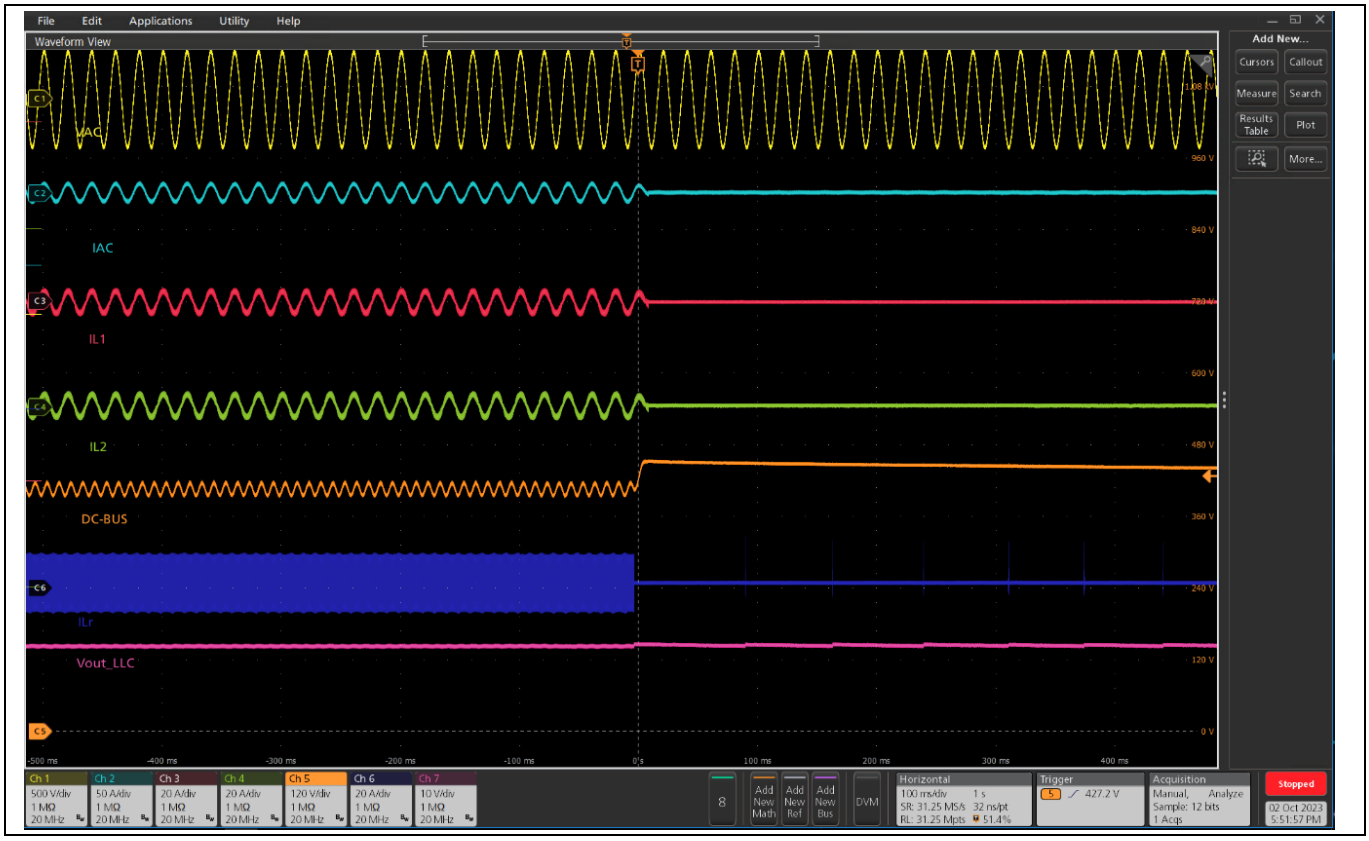


Figure 41 Load-jump of the complete PSU from 100% to 0% of load

3.1.5 Thermal characterization

The PSU has been thermally characterized by operating it at 100% load for 30 minutes and at 230 V AC and 115 V AC. The thermal behavior of the PSU is analyzed and is shown in Figure 42, providing a detailed overview of the PSU's behavior after a warm-up period of 30 minutes at 100% load at 230 V AC.

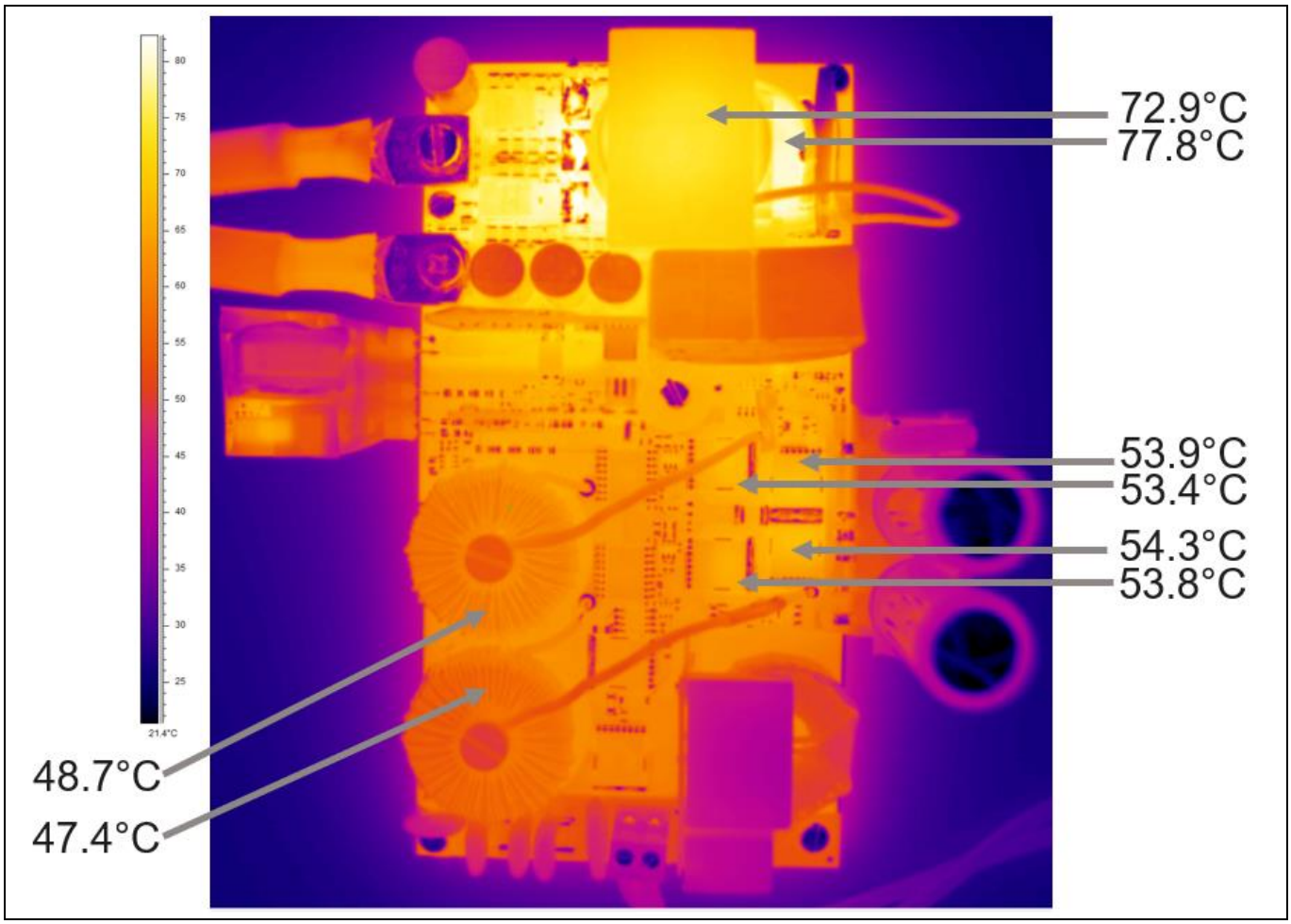


Figure 42 Total PSU thermal characterization at 230 V AC at 100% of the load

The thermal behavior of the PSU after a warm-up period of 30 minutes at 100% load and with an input voltage of 115 V is analyzed and is shown in Figure 43.

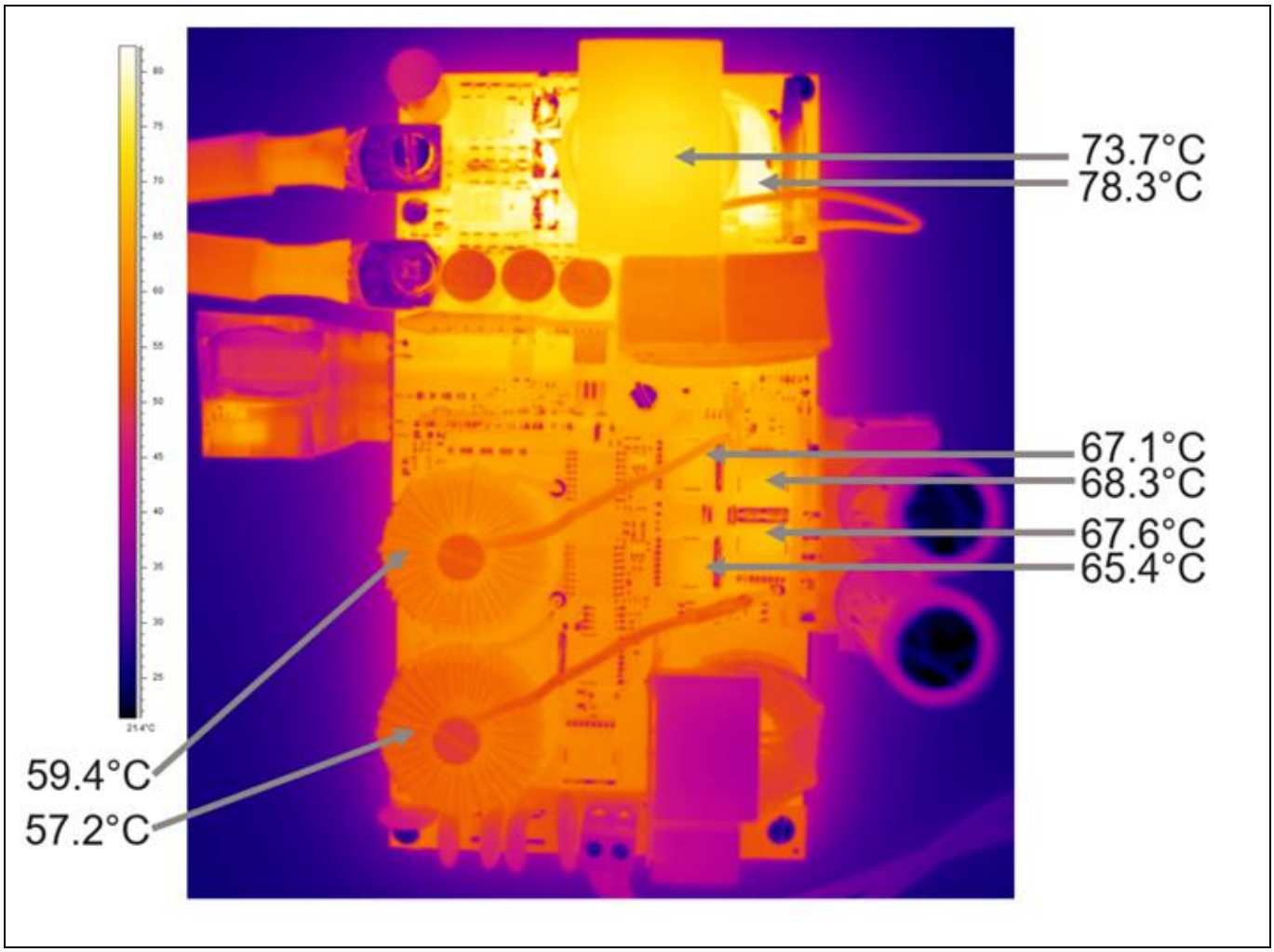


Figure 43 Total PSU thermal characterization at 115 V AC at 100% of the load

Figure 44 shows a detailed overview of the temperature for the LLC transformer stack.

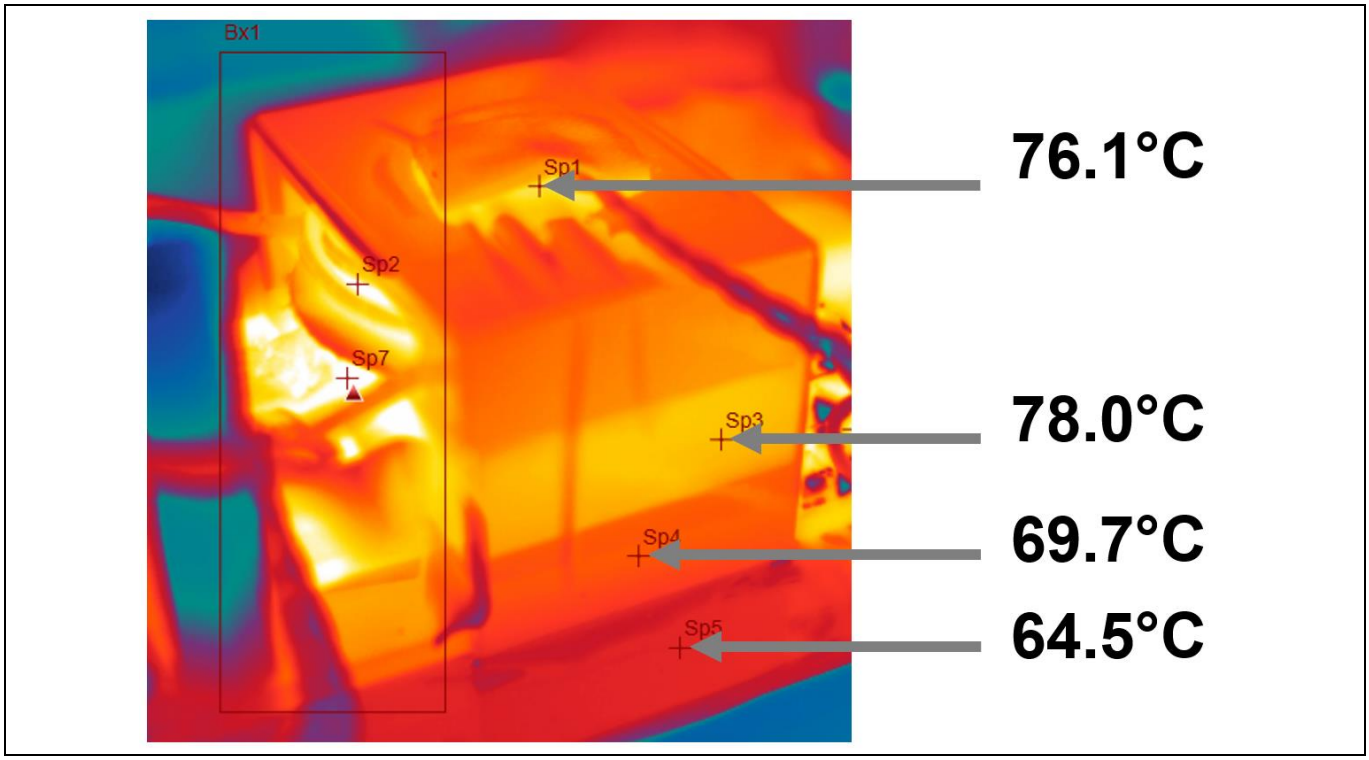


Figure 44 Thermal camera acquisition of the LLC main transformer at full load

3.1.6 EMI

The conducted electromagnetic interference (EMI) of the converter has been measured with a passive resistive load for not having possible interactions with the control of an active load. Figure 45 and Figure 46 show the results of the average and the positive peak measurements at 115 V AC and 230 V AC, respectively.

As seen, the PSU is fully compliant with Class A limits in both peak and average measurements. Furthermore, positive peak measurements represent a worst case compared to the quasi-peak of the standard. A margin of 6 dB is always achieved.

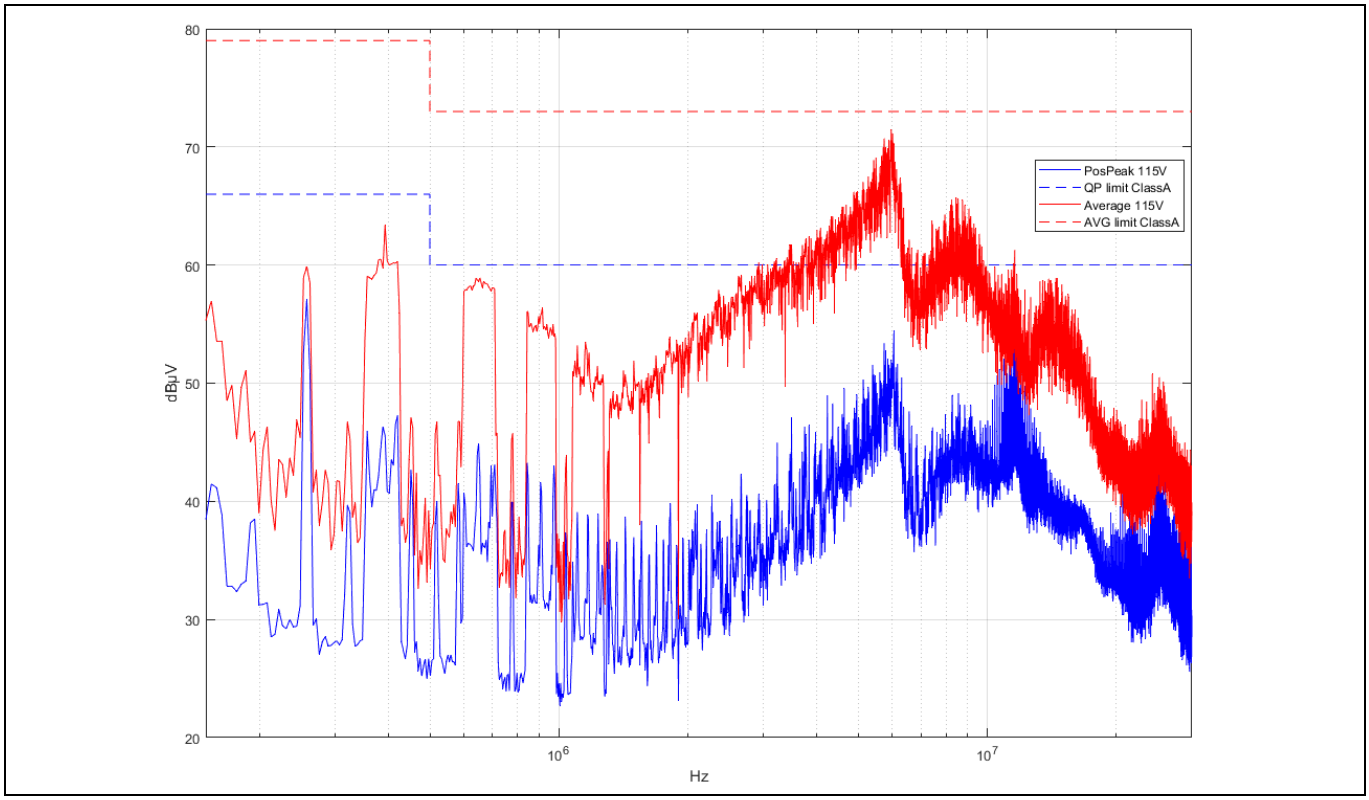


Figure 45 **Measured EMI spectrum of the complete power supply prototype at 115 V AC**

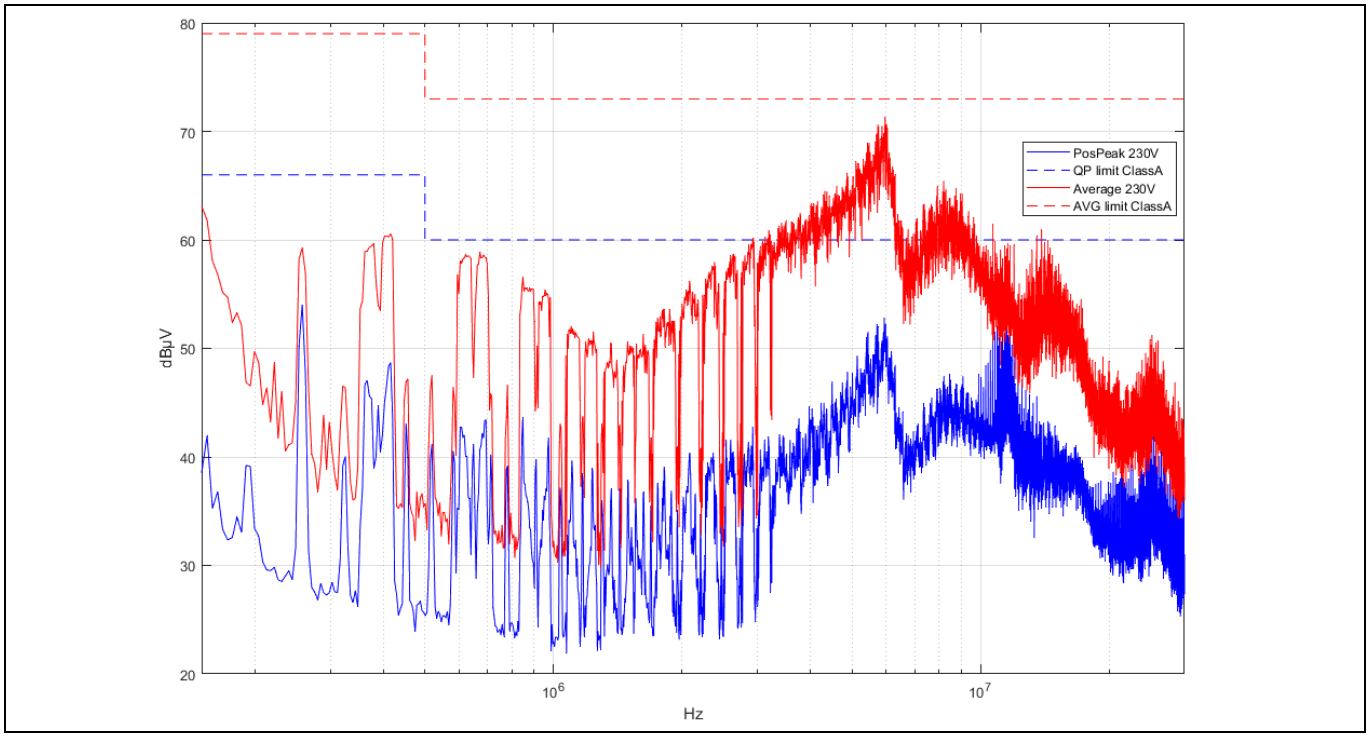


Figure 46 **Measured EMI spectrum of the complete power supply prototype at 230 V AC**

4 Summary

This document provides the fanless system solution from Infineon designed for 5G edge computing and small cells. The solution incorporates a bridgless interleaved totem-pole PFC converter and a DC-DC isolated half-bridge (HB) LLC converter, achieving efficiency levels of 96.4% at 230 V AC and 95.5% at 115 V AC, along with a power density of 50 W/in^3.

REF_1KW_PSU_5G_SIC reference board utilizes CoolSiC™ 650 V, CoolMOS™ 600 V MOSFETs in TOLL package, and OptiMOS™ 6 in WSON package from Infineon. This combination of CoolSiC™, CoolMOS™, and OptiMOS™ MOSFETS enables high performance within a compact form factor, as detailed in this application note.

The bridgless PFC topology and the half-bridge LLC incorporate full digital control through an XMC™ 4000 series microcontroller from Infineon.

Note that the PSU's performance excels not only in steady-state conditions, offering high efficiency, but also meets power line disturbance and hold-up time requirements.

Furthermore, the REF_1KW_PSU_5G_SIC board has been tested using a programmable AC source and electronic load. Efficiency, THD, and PF results are obtained using the WT3000 power analyzer from Yokogawa, alongside waveform analysis with the MSO58 (1 GHz; 6.25 GS/s) oscilloscope from Tektronix.

5 Schematics

5.1 Main board

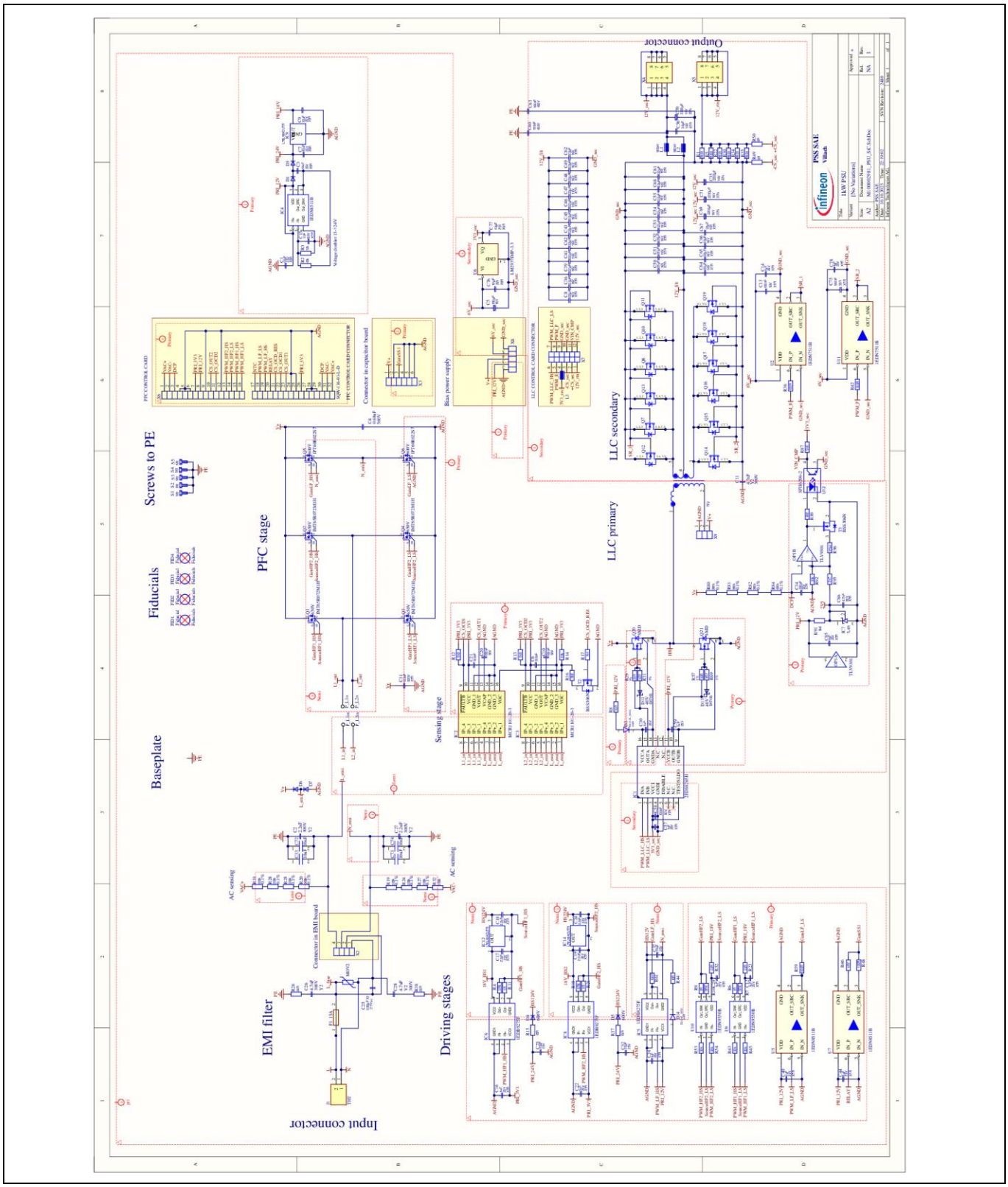


Figure 47 Main board

5.2 Control cards

5.2.1 PFC controller card

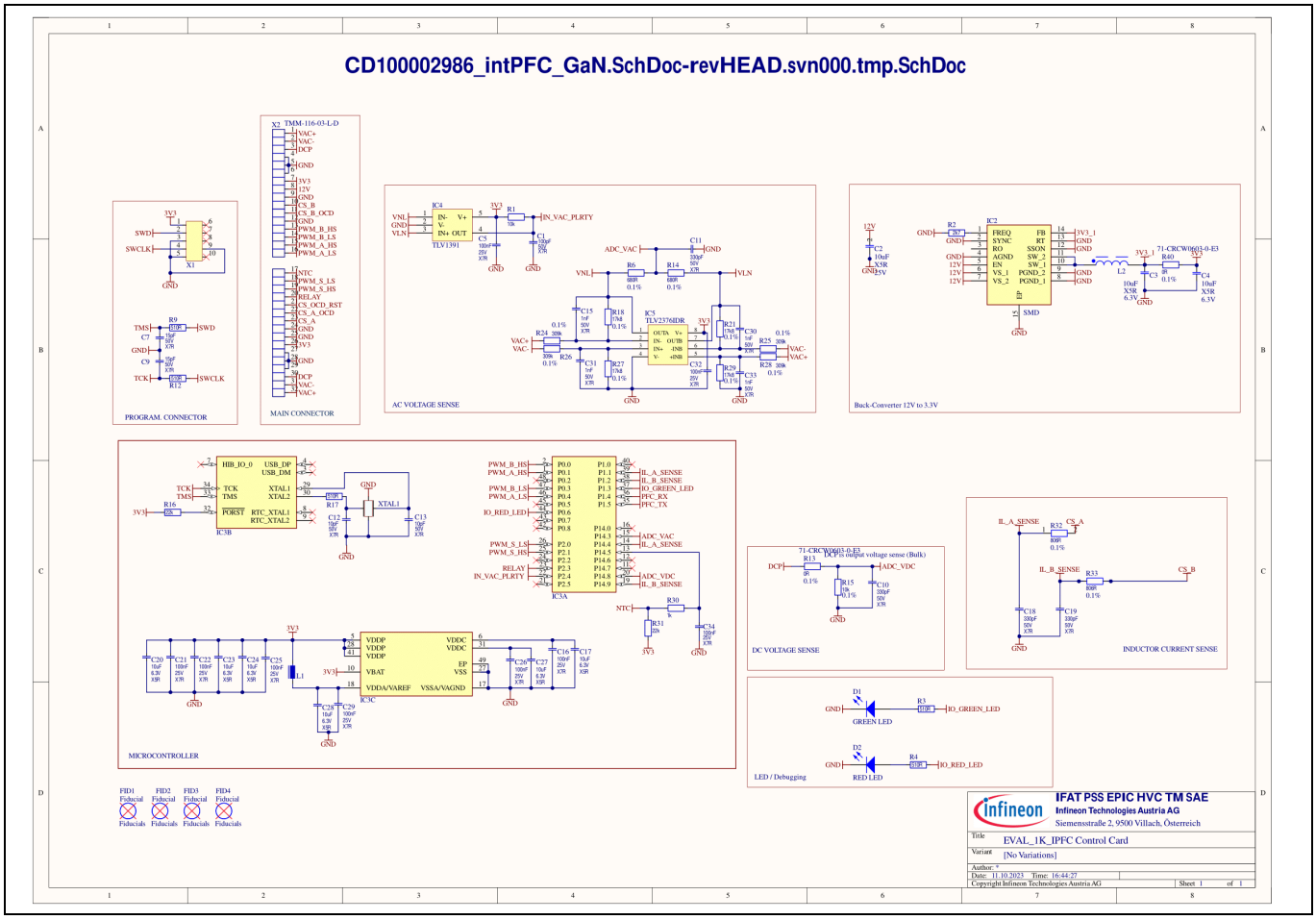


Figure 48 PFC controller card

5.2.2 LLC controller card

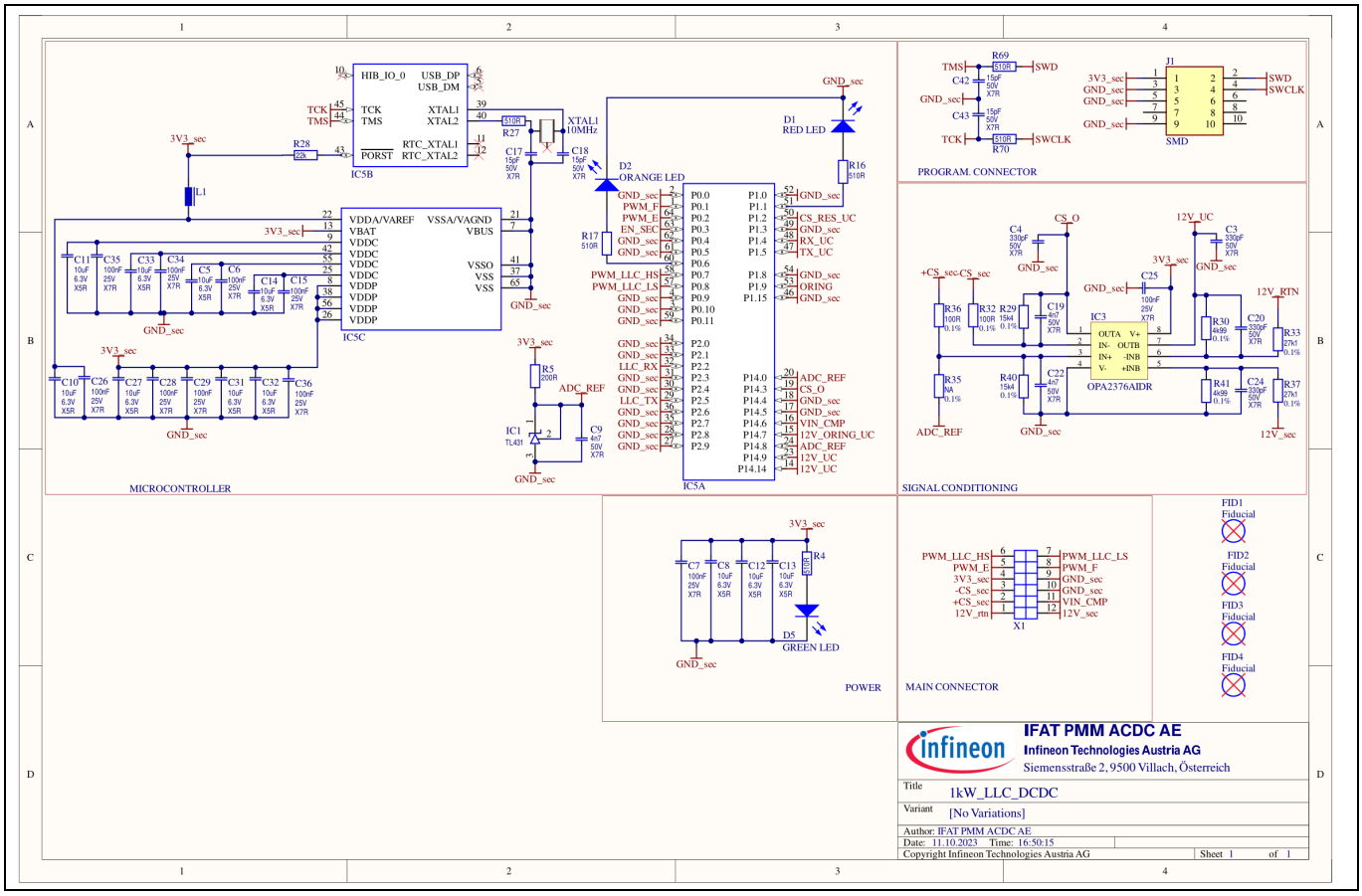


Figure 49 LLC controller card

5.2.3 Bias board

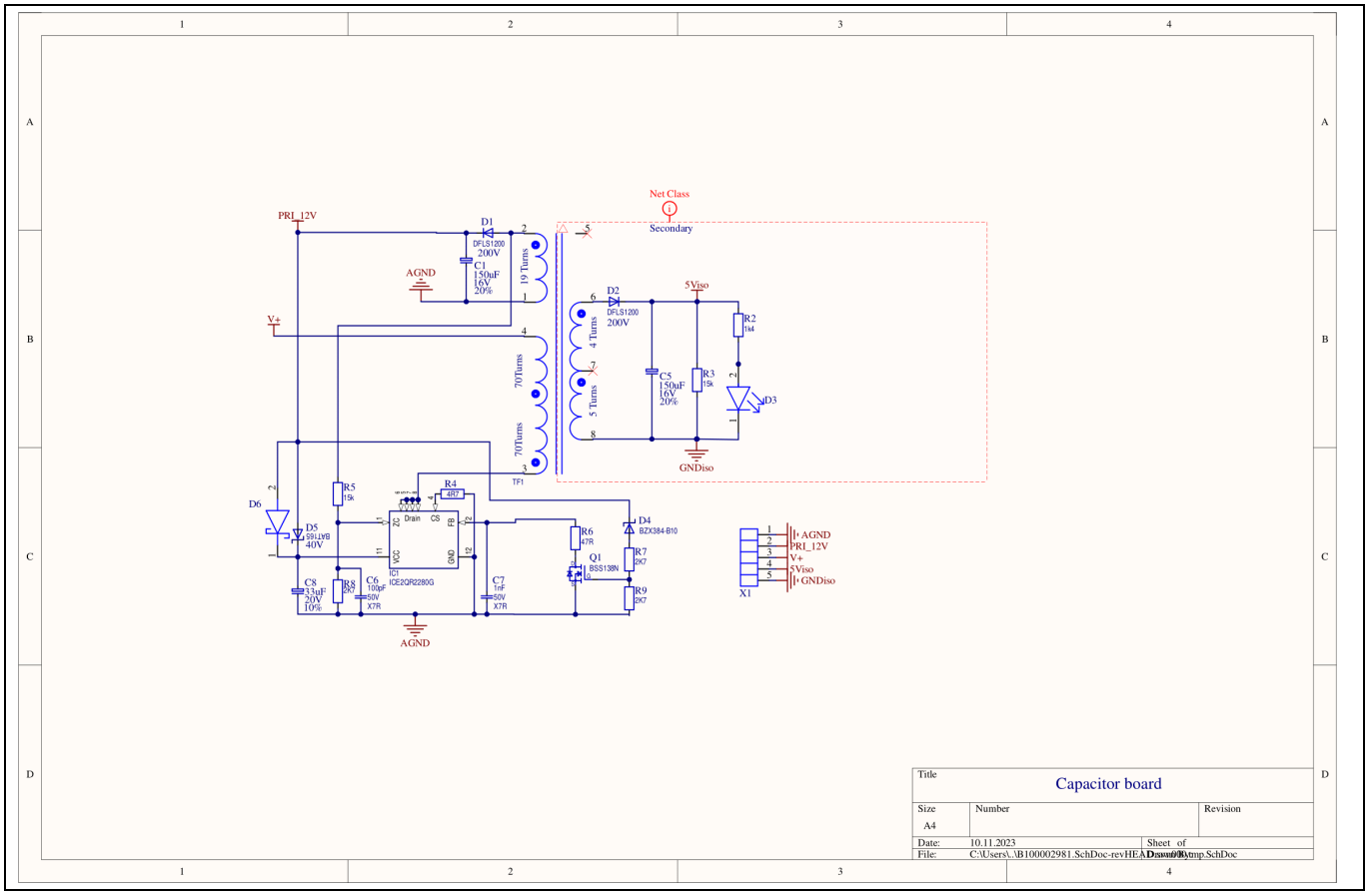


Figure 50 Bias board

5.2.4 Capacitor card

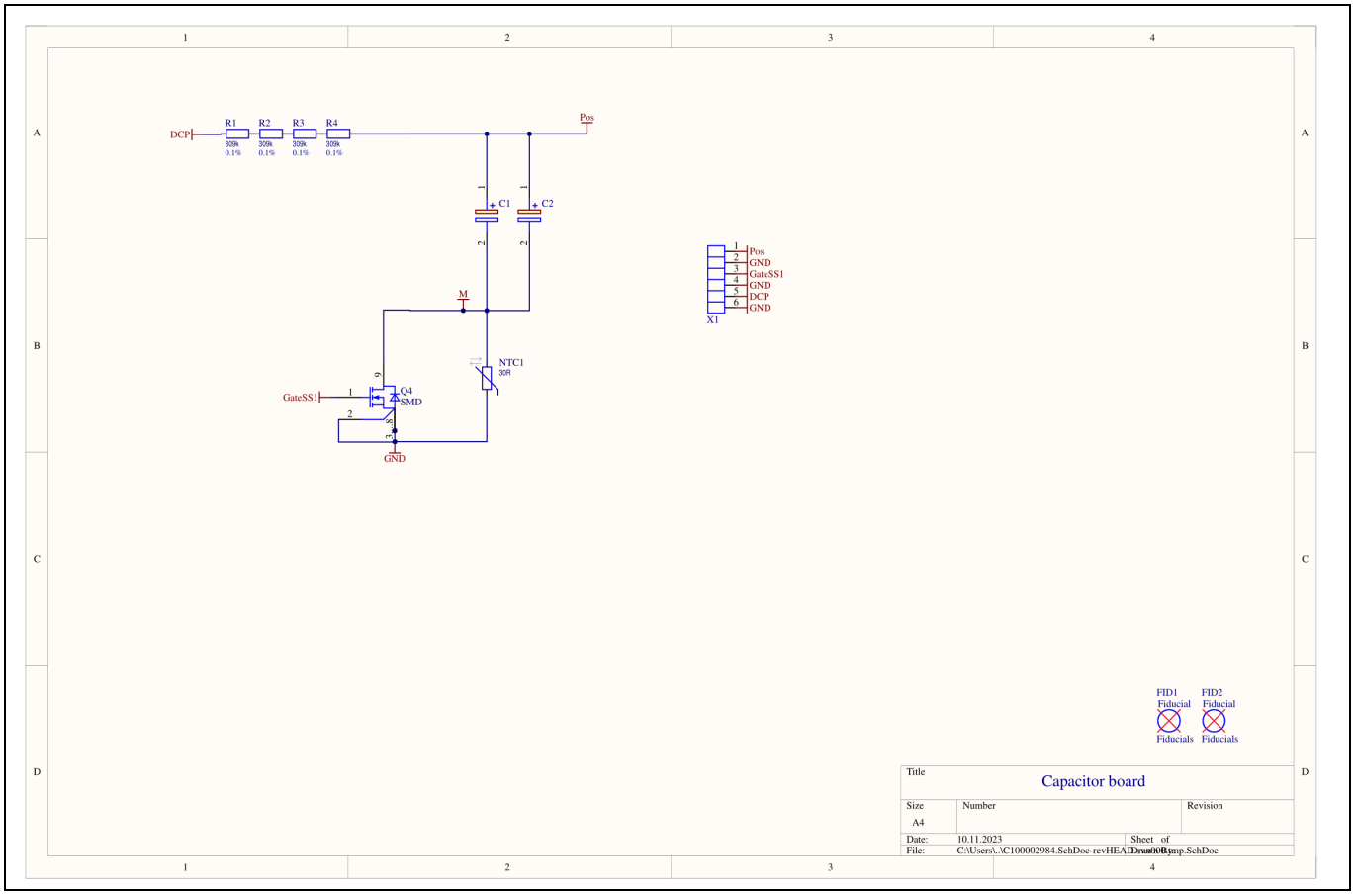


Figure 51 Capacitor card

5.2.5 EMI filter card

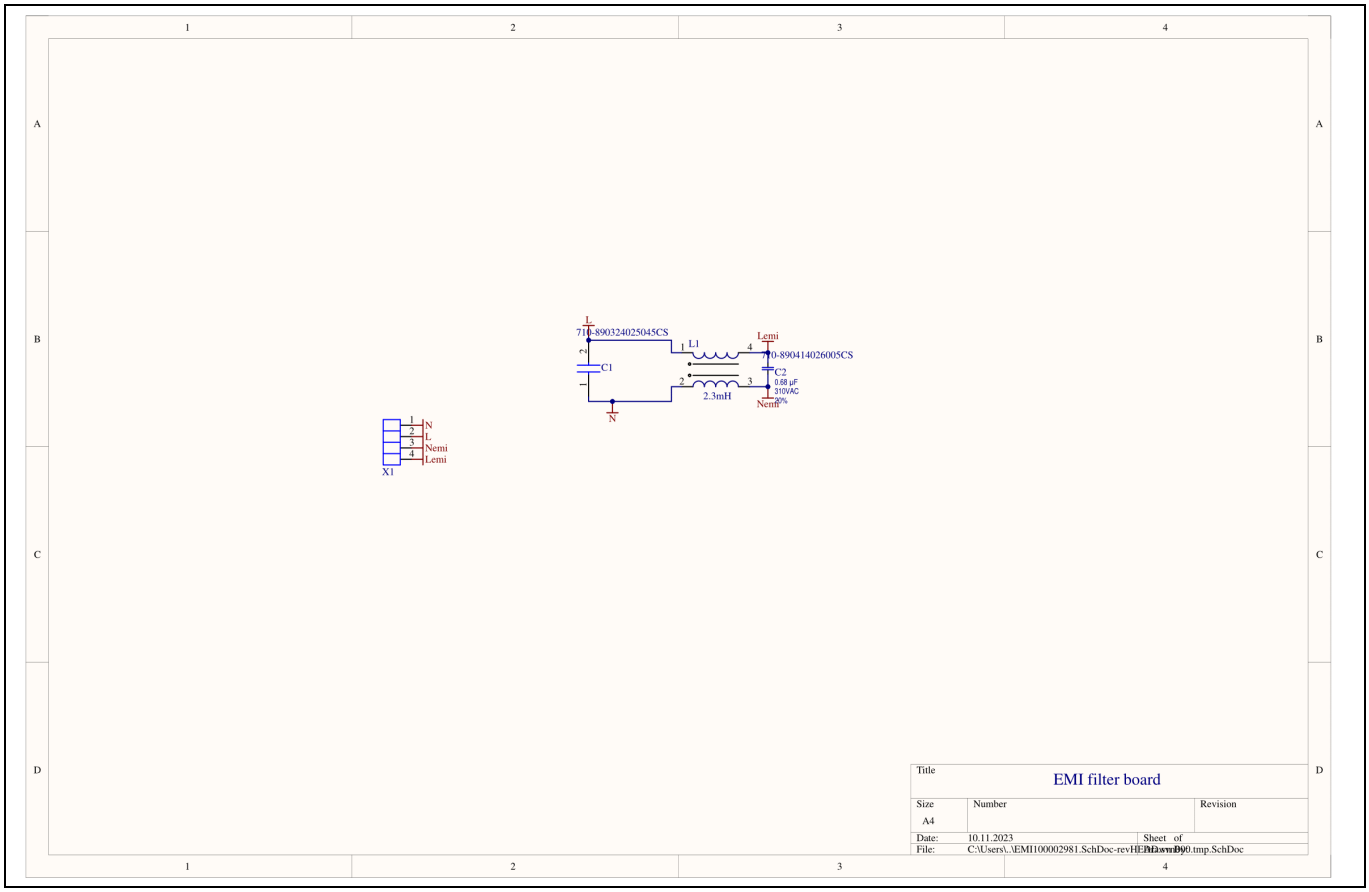


Figure 52 EMI filter card

5.2.6 Assembling view

PARTS LIST			
ITEM	QTY	PART NUMBER	DESCRIPTION
1	1	MP100002987 SiC	Aluminium chassis
2	1	IS100002986	Isolation foil
3	1	HO100002981 acrylic glass cover	Acrylic glass cover
4	1	M100002985 SiC	Mainboard assembly
5	2	M5x30 flat countersunk head screw	Must be made of non-conductive plastic!
6	6	M3x6 flat countersunk head	only one side pictured
7	4	M3 x 8mm cylinderhead screw	

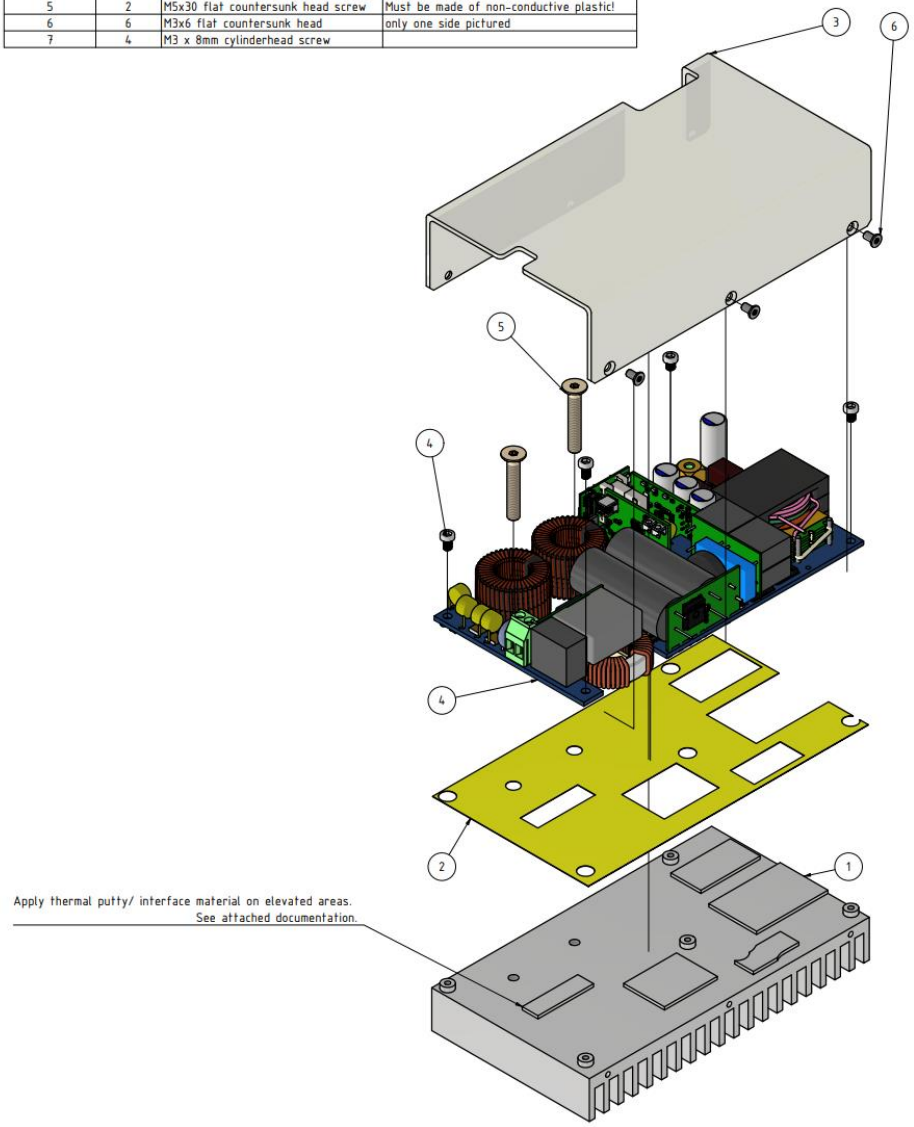


Figure 53 Assembling view

6 Bill of materials

The complete BOM is available from the downloads section of the Infineon website. A log-in is required to download this material.

Table 3 BOM of the main board

Quantity	Ref. designator	Part number	Description	Manufacturer
4	**Q1, Q2, Q3, Q4**	**IMT65R072M1H**	**NMOSFET**	**Infineon**
2	**Q5, Q6**	**IPT60R022S7**	**NMOSFET**	**Infineon**
12	**Q7, Q8, Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17, Q18, Q19**	**BSC009N04LSSC**	**NMOSFET**	**Infineon**
2	**Q20, Q21**	**IPT60R055CFD7**	**NMOSFET**	**Infineon**
2	**U2, U11**	**1EDN7511B**	**Gate driver IC**	**Infineon**
2	**U5, U7**	**1EDN8511B**	**Gate driver IC**	**Infineon**
2	**U9, U10**	**1EDN9550B**	**Gate driver IC**	**Infineon**
1	**IC4**	**1EDN8511B**	**Integrated circuit**	**Infineon**
1	**IC5**	**1EDB8275F**	**Gate driver IC**	**Infineon**
2	**IC6, IC8**	**1EDB9275F**	**Integrated circuit**	**Infineon**
1	**IC1**	**2EDS8265H**	**Gate driver IC**	**Infineon**
2	**D11, D13**	**BAT165**	**Schottky-diode**	**Infineon**
4	C1, C3, C7, C9	10 µF	Capacitor ceramic	–
2	C2, C27	2.2 nF	Capacitor ceramic	Farnell
1	C4	0.68 µF	Capacitor film	RS Components
1	C5	150 µF	Capacitor polarized	Farnell
7	C6, C10, C13, C20, C21, C58, C75	100 nF	Capacitor ceramic	Farnell
25	C8, C36, C39, C41, C42, C43, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C61, C62, C64, C65, C66, C67, C68	22 µF	Capacitor ceramic	Farnell
9	C12, C14, C29, C38, C40, C44, C57, C78, C85	1 µF	Capacitor ceramic	Farnell
1	C15	1 nF	Capacitor ceramic	–
4	C16, C22, C30, C59	1 µF	Capacitor ceramic	Farnell
4	C17, C18, C19, C24	2.2 µF	Capacitor ceramic	DigiKey
3	C23, C32, C37	10 µF	Capacitor ceramic	Farnell

Bill of materials

Quantity	Ref. designator	Part number	Description	Manufacturer
2	C26, C28	4.7 nF	Capacitor ceramic	Farnell
1	C31	100 nF	Capacitor ceramic	Farnell
4	C33, C72, C73, C74	10 nF	Capacitor	Mouser
1	C34	330 pF	Capacitor ceramic	Farnell
4	C35, C69, C70, C71	2200 µF	Capacitor polarized	DigiKey
2	C60, C63	100 nF	Capacitor ceramic	Farnell
2	C76, C77	10 µF	Capacitor ceramic	–
1	C86	4.7 nF	Capacitor ceramic	Farnell
2	D1, D3	DFLS140L-7	Standard diode	DigiKey
2	D2, D14	ES1JAL_M3G	Diode	Mouser
2	D4, D5	ES1JAL M3G	Standard diode	Mouser
2	D6, D7	S8KCDICT	Standard diode	DigiKey
1	F1	15 A	Fuse	Farnell
2	IC2, IC3	MCR1101-20-3	Hall sensor	Mouser
1	IC7	TL431	Shunt regulator	DigiKey
3	IC9, IC12, IC14	L78L18ACUTR	Integrated circuit	RS Components
1	J1	1711026	Connector	Mouser
2	L1, L2	180 nH	Filter inductor	DigiKey
1	L3	60 mR	Ferrite bead	Farnell
1	MOV2	V320LA20AP	Varistor	Farnell
1	OP1	TLV9301	SINGLE OPA	Mouser
6	R1, R5, R22, R30, R34, R35	R001	Resistor	Mouser
1	R2	43k	Resistor	–
1	R3	12k	Resistor	–
4	R4, R7, R10, R18	5R6	Resistor	Farnell
4	R6, R9, R11, R21	1R	Resistor	Farnell
2	R8, R44	10R	Resistor	Farnell
4	R12, R13, R16, R89	6k8	Resistor	Farnell
5	R14, R43, R45, R53, R54	33k	Resistor	Farnell
2	R15, R37	15R	Resistor	DigiKey
1	R17	1k4	Resistor	Farnell
8	R19, R20, R24, R25, R27, R28, R32, R33	309k	Resistor	DigiKey
4	R23, R29, R52, R57	22R	Resistor	Mouser
2	R26, R38	20R	Resistor	–
3	R31, R46, R69	4R7	Resistor	Farnell

Quantity	Ref. designator	Part number	Description	Manufacturer
3	R36, R42, R48	100R	Resistor	Farnell
2	R49, R50	0R	Resistor	Farnell
2	R59, R61	100R	Resistor	Farnell
3	R80, R81, R82	390k	Resistor	DigiKey
1	R84	430k	Resistor	Mouser
2	R87, R91	5k6	Resistor	Farnell
1	R92	30k	Resistor	Farnell
1	R95	2k7	Resistor	–
1	R96	17k4	Resistor	DigiKey
2	T2, T3	BSS306N	NMOSFET	DigiKey
1	TF2	8077.0304.003	–	ICE
1	U6	LM2937IMP-3.3	3.3 V regulator	RS Components
1	U12	SFH6206-2	Optocoupler	Farnell
1	X2	EMI100002981	Pin header, 4 contacts	–
1	X3	C100002984	Pin header, 6 contacts	–
2	X4, X5	7460307	Screw terminal	Mouser
1	X8	B100002981	Pin header, 5 contacts	–
1	X9	CR100002980	Pin header, 3 contacts	–

Table 4 BOM of PFC controller card

Quantity	Ref. designator	Part number	Description	Manufacturer
1	**IC2**	**TLS4120D0EPV33XUMA1**	**Integrated circuit**	**Infineon**
1	**IC3**	**XMC4200Q48K256BAXUMA1**	**Arm® Cortex®-M4**	**Infineon**
1	C1	100 pF	Capacitor ceramic	–
3	C2, C3, C4	10 µF	Capacitor	–
9	C5, C16, C21, C22, C25, C26, C29, C32, C34	100 nF	Capacitor ceramic	–
2	C7, C9	15 pF	Capacitor ceramic	–
4	C10, C11, C18, C19	330 pF	Capacitor ceramic	–
2	C12, C13	10 pF	Capacitor ceramic	–
4	C15, C30, C31, C33	1 nF	Capacitor ceramic	–
6	C17, C20, C23, C24, C27, C28	10 µF	Capacitor ceramic	–
1	D1	Green LED	LED	DigiKey
1	D2	Red LED	LED	DigiKey
1	IC4	TLV1391IDBVT	TLV1391: Single differential comparators	DigiKey

Quantity	Ref. designator	Part number	Description	Manufacturer
1	IC5	TLV2376IDR	Integrated circuit	Farnell
1	L1	742792602	Magnetic	Digikey
1	L2	100 µH	Power inductor	Mouser
1	R1	10k	Resistor	–
1	R2	2k7	Resistor	–
5	R3, R4, R9, R12, R17	510R	Resistor	–
2	R6, R14	680R	Resistor	–
2	R13, R40	0R	Resistor	Mouser
1	R15	10k	Resistor	DigiKey
2	R16, R31	22k	Resistor	–
4	R18, R21, R27, R29	17k8	Resistor	DigiKey
4	R24, R25, R26, R28	309k	Resistor	Digikey
1	R30	1k	Resistor	–
2	R32, R33	806R	Resistor	–
1	X1	–	Connector	DigiKey
1	X2	TMM-116-03-L-D	Pin header	Farnell
1	XTAL1	QT325S-12.000MEEQ-T	Crystal oscillator	DigiKey

Table 5 BOM of the LLC control card

Quantity	Ref. designator	Part number	Description	Manufacturer
1	**IC5**	**XMC4402-F64K256BA**	**Arm® Cortex®-M4**	**Infineon**
4	C3, C4, C20, C24	330 pF	Capacitor ceramic	–
11	C5, C8, C10, C11, C12, C13, C14, C27, C31, C32, C33	10 µF	Capacitor ceramic	–
10	C6, C7, C15, C25, C26, C28, C29, C34, C35, C36	100 nF	Capacitor ceramic	–
3	C9, C19, C22	4n7	Capacitor ceramic	–
4	C17, C18, C42, C43	15 pF	Capacitor ceramic	–
1	D1	Red LED	LED	DigiKey
1	D2	Orange LED	LED	DigiKey
1	D5	Green LED	LED	DigiKey
1	IC1	TL431	Integrated circuit	DigiKey
1	IC3	OPA2376AIDR	Integrated circuit	Farnell
1	J1	FTSH-105-01-L-DV-K	Connector	Mouser
1	L1	Ferrite bead 60 Ω at 100 MHz	Magnetic	Farnell
6	R4, R16, R17, R27, R69, R70	510R	Resistor	–

Quantity	Ref. designator	Part number	Description	Manufacturer
1	R5	200R	Resistor	–
1	R28	22k	Resistor	–
2	R29, R40	15k4	Resistor	RS Components
2	R30, R41	4k99	Resistor	DigiKey

Table 6 BOM of the bias board

Quantity	Ref. designator	Part number	Description	Manufacturer
1	**IC1**	**ICE2QR2280G**	**Integrated circuit**	**Infineon**
2	C1, C5	150 µF	Capacitor polarized	Farnell
1	C6	100 pF	Capacitor ceramic	–
1	C7	1 nF	Capacitor ceramic	–
1	C8	33 µF	Capacitor polarized	Farnell
2	D1, D2	DFLS1200	Diode	Farnell
1	D3	LGT67K-H2K1-24-Z	LED	Mouser
1	D4	BZX384-B10	Zener 10 V	RS Components
1	D5	BAT165	Schottky-diode	Infineon
1	D6	NRVBSS14HE	Schottky-diode	Mouser
1	Q1	BSS138N	NMOS FET	Farnell
1	R2	1k4	Resistor	–
1	R3	15k	Resistor	–
1	R4	4R7	Resistor	–
1	R5	15k	Resistor	–

Table 7 BOM of the bias board

Quantity	Ref. designator	Part number	Description	Manufacturer
1	**Q4**	**IPT60R022S7**	**NMOSFET**	**Infineon**
2	C1, C2	220 µF	Capacitor polarized	Mouser
1	NTC1	30R	Resistor NTC	Farnell

Table 8 BOM of the EMI board

Quantity	Ref. designator	Part number	Description	Manufacturer
1	C1	680 nF	Film capacitor	Mouser
1	C2	680 nF	Capacitor foil	Mouser
1	L1	2.3 mH	Inductor 2.3 mH	ICE

References

[1] Infineon Technologies AG: *High efficiency 3 kW bridgeless dual-boost PFC demo board, AN_201708_PL52_025, September 2017*; Available online.

[2] Infineon Technologies AG: *XMC4100/XMC4200 reference manual. July 2016*; Available online.

[3] Infineon Technologies AG: *XMC1400 AA-step reference manual. August 2016*; Available online.

Acronyms/abbreviations

Table 9 Acronyms/abbreviations

Acronym	Description
ADC	analog-to-digital converter
CCM	continuous conduction mode
CE	Conformité Européenne
DFF	duty feed-forward
EMI	electromagnetic interference
ESR	equivalent series resistance
HB	half-bridge
ICT	information and communications technology
IoT	Internet of Things
LDO	low-dropout regulator
OCP	overcurrent protection
OVP	overvoltage protection
PFC	power factor correction
PSU	power supply unit
PSU	power supply unit
RAN	radio access network
THD	total harmonic distortion
THD	total harmonic distortion
TOLL	To-Leadless
UL	Underwriters Laboratories
UVLO	undervoltage lockout
UVP	undervoltage protection

Revision history

Document revision	Date	Description of changes
V 1.0	2024-05-10	Initial release

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Edition 2024-05-10

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Infineon Technologies AG

81726 Munich, Germany

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AN085359

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