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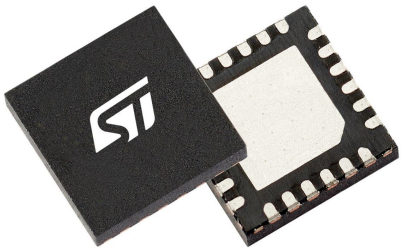
L9800

Datasheet

Automotive 8-channel LS driver



TFQFN24 4x4x0.9

Product status link
L9800

Product summary	
Order code	**L9800**
Package	TFQFN24 4x4x0.9
Packing	Tray
Order code	**L9800-TR**
Package	TFQFN24 4x4x0.9
Packing	Tape and reel

Features

Symbol	Parameter	Values
V_{BATT}	Supply voltage	3 V to 28 V
V_{DDIO}	Supply and SO buffer voltage	3 V to 5.5 V
$R_{DS(ON)}$	Maximum on-state resistance at T_J = 150 °C	1.7 Ω
$I_{L(NOM)}$	Nominal load current (T_A = 85 °C, all channels)	330 mA
E_{AR}	Maximum energy dissipation - repetitive	10 mJ at I_L = 220 mA
$V_{DS(CL)}$	Minimum drain-source clamping voltage	42 V
$I_{L(OVL0)}$	Maximum overload switch off threshold	3 A
f_{SCLK}	Maximum SPI clock frequency	8 MHz

- AEC-Q100 qualified
- Full ISO26262 compliant, ASIL-B systems ready
- General
  - Eight LS drivers
  - 16-bit SPI interface for outputs control and for diagnosis data communication
  - Daisy chain compatible and available even with 8-bit SPI
  - 2 parallel input pins with input mapping functionality
  - Cranking capability down to V_{BATT} = 3 V
  - Digital supply voltage range compatible with 3.3 V and 5 V MCU
  - Bulb inrush mode (BIM) to drive 2 W lamps and electronic loads
  - Two independent internal PWM generators for MCU offloads and to drive LEDs
  - Very low quiescent current (with usage of IDLE pin)
  - Limp-home mode (with usage of IDLE and IN pins)
  - Safety features
    - Temperature sensor and monitoring
    - Serial communications using address feedback, 1 parity bit, frame counter and short frame detection
  - Fail-safe activation via input pins
  - Safe operation at low battery voltage (cranking)
- Protective functions
  - Overcurrent latch off
  - Lower supply voltage range for extended operation
  - Electrostatic discharge (ESD) protection
  - Reverse battery protection on VBATT without external components
  - Short circuit battery protection
  - Thermal shutdown latch off

- Diagnostic features
  - Latched diagnostic information via SPI register
  - Overcurrent and overtemperature detection at on state
  - Off state diagnosis, able to detect and distinguish open load and short to GND conditions

Applications

- Low-side switches for 12 V in automotive or industrial applications such as lighting, heating, motor driving, energy and power distribution
- Especially designed for driving relays, LEDs and motors

Description

The L9800 is an 8-channel LS driver designed for automotive applications (LEDs and relays) and compatible with resistive, inductive and capacitive loads. The device offers advanced diagnostic and protection functionalities such as open load, overcurrent and overtemperature detections, short to GND. The eight output channels can be driven by SPI or by dedicated parallel inputs. Limp-home functionality is present. Daisy chain available (no constraint on SPI number of bits of devices in chain). The device is able to guarantee cranking scenario down to V_{BATT} = 3 V and ensures very low-quiescent current under RESET.

The device is an 8-channel low-side power switch in a TFQFN24 4x4x0.9 package. It is specially designed to control relays and LEDs in automotive and industrial applications.

A serial peripheral interface (SPI) is used for control and diagnosis of the loads as well as of the device. For direct control and PWM there are two input pins (IN0 and IN1) available, connected to two outputs by default (OUT2 and OUT3). Additional or different outputs can be controlled by the same input pins if programmed by SPI.

1 Detailed description

The L9800 is an 8-channel IC, made of low-side drivers. All the outputs have typical $R_{DS(ON)}$ = 0.77 Ω at T_J = 25 °C. The 16-bit serial peripheral interface (SPI) is used to control and diagnose the device and the loads. The SPI interface provides daisy chain capability to assemble multiple devices in one SPI chain by using the same number of microcontroller pins.

This device is designed for low supply voltage operation, it is able to maintain its functionality at low battery voltage (VBATT ≥ 3 V). The SPI communication, including the ability to program the device, are present only when the digital power supply is available (VDDIO ≥ 3 V).

The L9800 has two input pins (IN0 and IN1) respectively connected by default to the outputs OUT2 and OUT3, making them controllable even when the digital supply voltage is not available. Thanks to the input mapping functionality, it is possible to connect the input pins to different outputs, or to assign more outputs to the same input pin. In this case, when the device is in fail-safe mode (limp-home), more channels can be controlled with one signal applied to one input pin.

In limp-home mode the IN0 is mapped on channel 2 and IN1 is mapped on channel 3. When the IDLE pin is “low”, it is possible to activate the two channels using the input pins independently from the presence of the digital supply voltage VDDIO.

The device provides diagnosis of the load by detecting the open-load in the off state and the short-circuit. For diagnosis of the off state (triggered by the SPI request), two current sources (pull-up and pull-down current) are activated in two separate steps. The device detects an abnormal voltage on the output and, in case of fault detection, it is able to differentiate open-load from short condition.

Each output stage is able to avoid short circuits. In case of overload, the affected channel is switched off with an increased slew rate (gate kill) when the overload detection current $I_{L(OVLn)}$ is reached and can be reactivated via SPI after clearing the register in which the fault is registered.

In limp-home state, the channel linked to an input pin set to 'high' where an OVL fault is detected is automatically restarted after the restart time of the t_{RETRY} output.

Temperature sensors are available for each channel to protect the device in case of over-temperature in the on condition.

The power transistors are built by N-channel power MOSFET. The device is integrated in Smart Power technology.

2 Block diagram and pin description

Figure 1. **Block diagram**

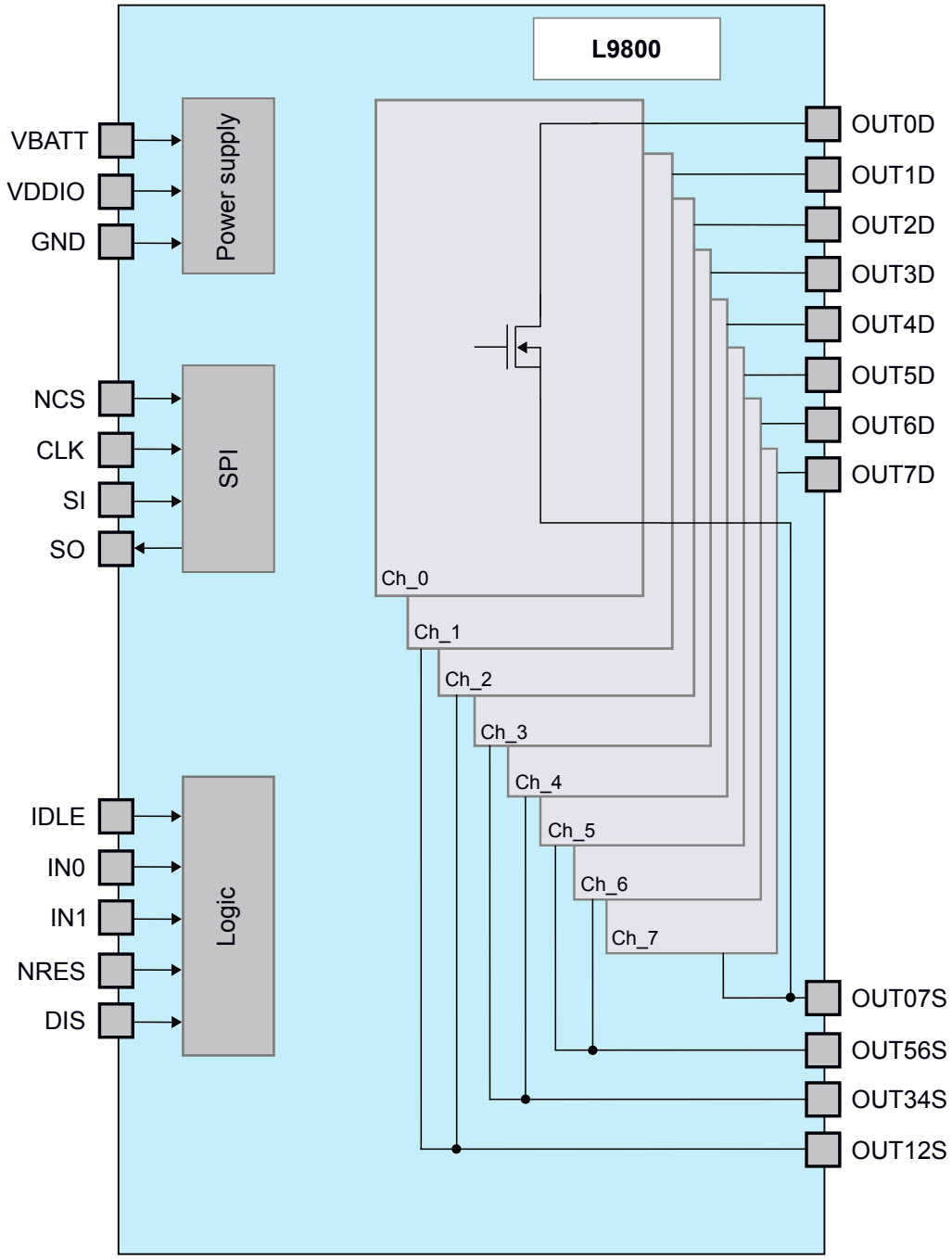


Figure 2. Pin configuration (bottom view)

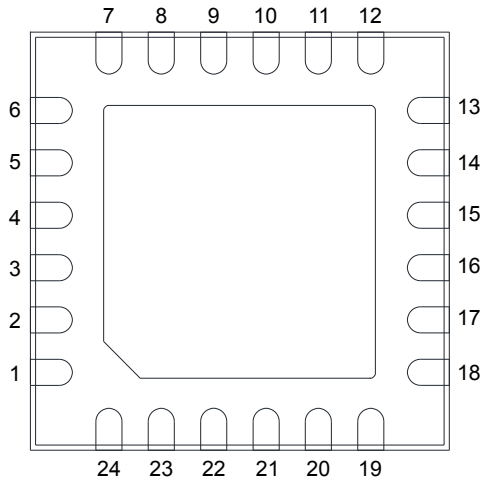


Table 1. Pin description

Pin #	Pin name	Description	I/O type
1	OUT7D	Drain 7	O
2	OUT6D	Drain 6	O
3	OUT56S	Source 5–6	O
4	OUT5D	Drain 5	O
5	NRES	NRES function	I
6	IN1	Parallel command input 1	I
7	IN0	Parallel command input 2	I
8	GND	Ground pin	
9	IDLE	Idle function	I
10	VDDIO	IO supply	
11	SO	SPI output stream	O
12	CLK	SPI clock	I
13	NCS	SPI chip select	I
14	SI	SPI input stream	I
15	OUT4D	Drain 4	O
16	OUT34S	Source 4	O
17	OUT3D	Drain 3	O
18	DIS	Channel disable	I
19	OUT2D	Drain 2	O
20	OUT12S	Source 1–2	O
21	OUT1D	Drain 1	O
22	VBATT	Battery voltage	
23	OUT07S	Source 0–7	O
24	OUT0D	Drain 0	O

3 Application circuit

Here below a general application circuit with the TFQFN24 package.

Figure 3. L9800 application circuit

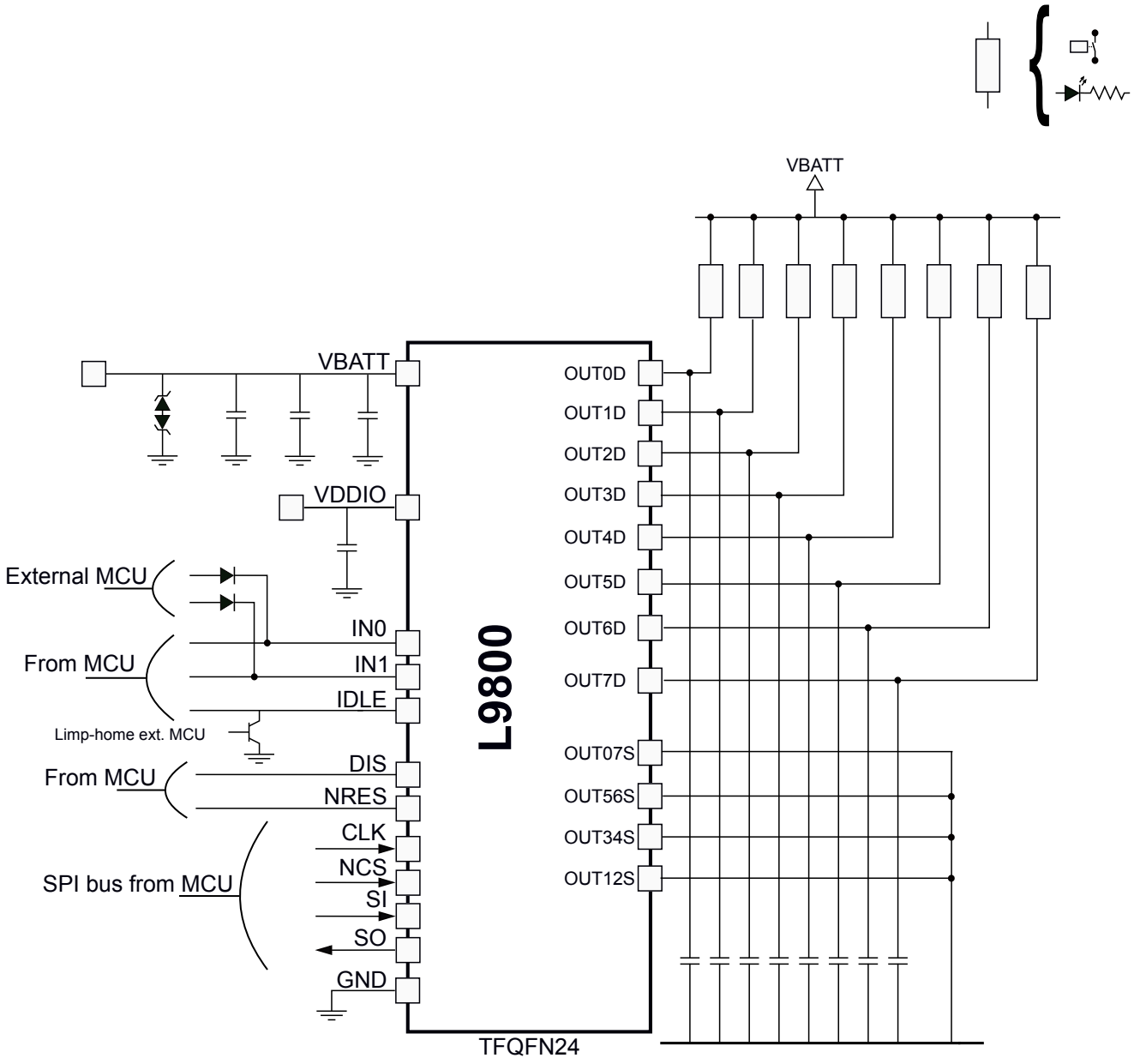


Table 2. External components list

Pin	External components					Requirement[1]	Comment
	Type	Min.	Typ.	Max.	Unit		
VBATT	Capacitor		120		nF	2., 3.	Tolerance ±20% 50 V
	Capacitor		100		µF	2.	50 V, Transient and load dump protection
	TVS	-15		38	V	4.	Transient voltage suppressor
	Capacitor		10		µF	2., 3.	Tolerance ±20% 50 V, Transient and load dump protection
VDDIO	Capacitor		100		nF	2.	Tolerance ±10% 50 V
OUT2D–OUT7D	Capacitor			12	nF	3.	Maximum total capacitance value at output load

1. *Refer to the following Items.*

In the list of external components, the different parts are marked following the items reported below:

1. Mandatory components for L9800 functionality.
2. Recommended components for EMC robustness.
3. Recommended components for ESD trials.
4. Recommended system component.

Note: Recommended components may depend on the requirements at system level and shall be confirmed by specific tests on the final applications.

4 Product characteristics

4.1 Operating range

Within the operating range, the part operates as specified and without parameter deviations. The device may not operate properly if maximum operating conditions are exceeded.

Exceeding operating conditions and going back within, the part recovers with no damage or degradation.

Additional supply voltage and temperature conditions are given separately at the beginning of each electrical specification table.

All voltages are related to the GND ground pin.

Table 3. Operating conditions

Symbol	Description	Min.	Typ.	Max.	Unit
Operating ranges					
VBATT	Supply voltage range for normal operations	6	-	18	V
	Upper supply voltage range for extended operations	18	-	28	V
	Load dump voltage range for extended operations	28	-	42	V
	Lower supply voltage range for extended operations	3	-	6	V
	Supply voltage range for normal operations while shorted externally to VDDIO	3	-	5.5	V
VDDIO	Logic supply voltage	3	-	5.5	V
T_J	Operating junction temperature range	-40	-	150	°C

4.1.1 Supply voltage ranges

The device operates on the 12 V system. Transient operation for these systems can reach 40 V maximum. Particular care has to be taken in PCB manufacturing to keep thermal dissipation to a reasonable level.

- For VBATT < 3 V, if VDDIO is included in its operative range, the device is in a safety state (internal circuitries are on but all the outputs are off). VS_UV function can be disabled by VS_UV_MASK bit of the CFG_0 register.
- For VBATT up to 40 V, all the functions are granted with increased power dissipation and no reset is asserted during the transient.

For detailed functionality description, refer to the Table 9.

4.2 Absolute maximum ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

All voltages are related to the potential at the ground pin (GND).

Table 4. Absolute maximum rate capabilities

Symbol	Description	Min.	Typ.	Max.	Unit
AMR - supplies					
VBATT	Battery voltage	-16	-	42	V
VDDIO	I/O voltage	-0.3	-	20	V
$V_{BATT(LD)}$	Supply voltage in load dump		-	42	V
$V_{BATT(SC)}$	Supply voltage in short circuit (single pulse)		-	28	V
V_{DS0}	Voltage at power transistor OUT0	-0.3	-	$V_{DS(CL)}$	V
V_{DS7}	Voltage at power transistor OUT7	-0.3	-	$V_{DS(CL)}$	V
V_{OUT07S}	Power transistor source voltage OUT07	-0.3	-	0.3	V

Symbol	Description	Min.	Typ.	Max.	Unit
V_{OUT0D}	Power transistor drain voltage OUT0	- 1(1)	-	42	V
V_{OUT7D}	Power transistor drain voltage OUT7	- 1(1)	-	42	V
V_{DS1}	Voltage at power transistor OUT1	-0.3	-	$V_{DS(CL)}$	V
V_{DS2}	Voltage at power transistor OUT2	-0.3	-	$V_{DS(CL)}$	V
V_{OUT12S}	Power transistor source voltage OUT12	-0.3	-	0.3	V
V_{OUT1D}	Power transistor drain voltage OUT1	- 1(1)	-	42	V
V_{OUT2D}	Power transistor drain voltage OUT2	- 1(1)	-	42	V
V_{DS3}	Voltage at power transistor OUT3	-0.3	-	$V_{DS(CL)}$	V
V_{DS4}	Voltage at power transistor OUT4	-0.3	-	$V_{DS(CL)}$	V
V_{OUT34S}	Power transistor source voltage OUT34	-0.3	-	0.3	V
V_{OUT3D}	Power transistor drain voltage OUT3	- 1(1)	-	42	V
V_{OUT4D}	Power transistor drain voltage OUT4	- 1(1)	-	42	V
V_{DS5}	Voltage at power transistor OUT5	-0.3	-	$V_{DS(CL)}$	V
V_{DS6}	Voltage at power transistor OUT6	-0.3	-	$V_{DS(CL)}$	V
V_{OUT56S}	Power transistor source voltage OUT56	-0.3	-	0.3	V
V_{OUT5D}	Power transistor drain voltage OUT5	- 1(1)	-	42	V
V_{OUT6D}	Power transistor drain voltage OUT6	- 1(1)	-	42	V
IDLE pin					
V_{IDLE}	Voltage at IDLE pin	-0.3	-	20	V
IN0,1 pins					
V_{IN0}	Voltage at input pins IN0	-0.3	-	20	V
V_{IN1}	Voltage at input pins IN1	-0.3	-	VDDIO + 0.3	V
DIS, NRES pins					
V_{DIS}	Voltage at DIS pin	-0.3	-	20	V
V_{RES}	Voltage at RES pin	-0.3	-	20	V
SPI pins–SI, NCS, SCLK					
V_{SI}	Voltage at SI pin	-0.3	-	20	V
V_{NCS}	Voltage at NCS pin	-0.3	-	20	V
V_{CLK}	Voltage at CLK pin	-0.3	-	20	V
V_{SO}	Voltage at serial output pin SO	-0.3	-	VDDIO + 0.3	V

1. *Case of short to GND with GND shift or ISOPULSE condition1.*

Table 5. ESD requirements

Item	Test condition	Min.	Max.	Unit
All pins	HBM	-2	2	kV
All pins	CDM (values for corner pins in brackets)	-500/(-750)	500/(750)	V
Pins to connector(1)	HBM	-4	4	kV

1. *All pins are connected to GND.*

4.3 Temperature ranges and thermal data

Table 6. Temperature ranges

Symbol	Description	Min.	Max.	Unit
T_A	Operating temperature (ECU environment)	-40	125	°C
T_J	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	-55	150	°C
T_{ot}	Thermal shut-down temperature	175	200	°C
O_{Thys}	Thermal shut-down temperature hysteresis	5	15	°C

Table 7. Thermal data

Symbol	Parameter	Typ.	Unit
R_{thJA}	Thermal resistance, junction-to-ambient–TFQFN24 package(1)	42	°C/W

1. *With 2s2p PCB thermally enhanced.*

5 Input/output

5.1 Control pins

The device has three pins (IN0, IN1 and IDLE) to check directly the device without using SPI.

5.2 Input pins (IN0, IN1)

The L9800 has two input pins, IN0 and IN1, by default IN0 is connected to channel 2, IN1 is connected to channel 3. It is possible through programming MAP_IN0 and MAP_IN1 (input mapping registers) to link different channels to each input IN0 or IN1 with priority assigned to MAP_IN0. If for example, both mapping registers are written to control the same channel, it follows the IN0 pin. The Figure 23 describes how the actuation of the channels is managed. The channels are driven by the signals that are the OR combination between PWM_SPI_register status, PWM generators (PWM generator output mapping status), IN0 and IN1. The STA_0 (status register) shows the logic level of the input pins. See Section 7: Power stages for further details.

The logic level of the input pins can be monitored via the STA_0 register. In the STA_0 register, it is also possible to monitor the status of DIS and NRES pins. The input status monitor is operative also when the device is in limp-home mode. If one of the input pins is set to “high” and the IDLE pin is set to “low”, the device switches into limp-home mode and activates the channel mapped by default to the input pins.

5.3 Reset pin

The NRES pin is the reset input for the device. As default, the state of the NRES pin is masked by the logic. The user must send a specific SPI frame (setting NRES_EN or NRES_N_EN bit on the CFG_0 register) to force the logic to take into account the state of the NRES pin. The function uses the inverse logic, if the NRES pin is low, the device is held in an internal reset state, all output channels are disabled, and all registers are reset to their default values. An internal pull-down holds the NRES pin asserted in case of an open pin.

Both NRES_EN and NRES_N_EN are intended to enable/disable the NRES pin.

- When the NRES_EN bit is 1 the NRES pin is enabled; in this case, a reset event on the NRES pin puts the registers in the default conditions, and the NRES pin in this case is disabled.
- When the NRES_N_EN is set to 1, the NRES pin is enabled, but the reset event puts the registers in default conditions while the NRES pin remains enabled.

5.4 DIS pin

The DIS pin is used to enable/disable the output stages. As default, the DIS pin is masked by the logic. The user needs to send a specific SPI frame (setting the DIS_EN bit on the CFG_0 register) to force the logic to take into account the state of the DIS pin:

- When the DIS pin is high, all channels are disabled if the pin is not masked. An internal pull-up holds the DIS pin asserted in case of an open pin.
- When the DIS pin is set low, all channels are enabled based on their configuration settings. The status of the DIS pin can be monitored reading the STA_0 register.

The DIS pin can be connected to a general purpose output pin of the microcontroller or to an alternative safety circuit.

5.5 IDLE pin

The device enters in sleep state through IDLE pin when it is set to "low" together with IN0 and IN1. Instead if IDLE pin is in "low" state and one of the two inputs are in "high" state the device is brought in limp-home mode.

To ensure a correct transition IDLE pin should be set at least for a time duration of $t_{IDLEFLT_max}$.

Setting the IDLE pin to “low”, with both IN0 and IN1 also at “low” value, has the following consequences:

- The SPI registers are reset to default value if IN0 and In1 are set to "low".
- To decrease the current consumption the voltage detection circuits on VDDIO and VBATT are disabled, if both IN0 and IN1 are set to "low". Instead if one of the two inputs is set to "high", the core is enabled with channel 2 and channel 3 driving circuits.
- No SPI communication is kept, the SO pin remains in "HighZ" even if NCS pin is active and the SPI communication is not allowed.

5.6 Electrical parameters

3V < VBATT < 18 V, 3 V < VDDIO < 5.5 V, T_J = -40 °C to 150 °C, unless otherwise noticed.

Table 8. Digital input/output electrical performance

Symbol	Description	Test condition	Min.	Nom.	Max.	Unit
$V_{IDLE(L)}$	L-input level			-	0.8	V
$V_{IDLE(H)}$	H-input level		2.0	-		V
R_{IDLE}	Input pull-down resistor at IDLE pin	VDDIO = 5 V, V_{DIS} = 2 V	50	-	180	kΩ
Input pins IN0 and IN1						
$V_{IN(L)}$	L-input level			-	0.8	V
$V_{IN(H)}$	H-input level		2.0	-		V
R_{IN}	Input pull-down resistor at IN0 and IN1 pin	VDDIO = 5 V, V_{IN} = 2 V	50	-	180	kΩ
Input pin NRES						
$V_{NRES(L)}$	L-input level			-	0.8	V
$V_{NRES(H)}$	H-input level		2.0	-		V
R_{NRES}	Input pull-down resistor at NRES pin	VDDIO = 5 V, V_{NRES} = 2 V	50	-	180	kΩ
Input pin DIS						
$V_{DIS(L)}$	L-input level			-	0.8	V
$V_{DIS(H)}$	H-input level		2.0	-		V
R_{DIS}	Input pull-up resistor at DIS pin	VDDIO = 5 V, V_{DIS} = 0.8 V	35	-	100	kΩ

6 Power supply

The L9800 is fed by two supply voltages:

- VBATT (general supply for analog and digital part)
- VDDIO (supply for digital output buffers)

The VBATT supply line is connected to a battery feed and used for the driving circuitry of the power stages.

VBATT and VDDIO supply voltages have an undervoltage detection circuit, which prevents the activation of the associated function in case the measured voltage is below the undervoltage threshold.

An undervoltage on the VBATT supply voltage prevents the activation of the power stages. All channels are disabled, and are enabled again as soon as VBATT exits from the undervoltage condition.

An undervoltage on the VDDIO supply prevents any SPI communication. SPI read/write registers are reset to default values.

The device drains all the needed current from the highest supply among the two.

Table 9. Supply ranges

Condition	VDDIO ≤ $VDDIO_{(UV)}$	VDDIO > $VDDIO_{(UV)}$
VBATT ≤ $VBATT_{(UV)}$	Channels cannot be controlled	Channels can be controlled only if the VS_UV_MASK bit is set to 1
	SPI registers reset	SPI registers available
	SPI communication not available	SPI communication available
	Limp-home mode not available	Limp-home mode available (channels are off)
VBATT > $VBATT_{(UV)}$	Channels cannot be controlled by SPI	Channels can be switched on and off
	SPI registers reset	SPI registers available
	SPI communication not available	SPI communication available

6.1 Operating modes

The L9800 has four operative states:

- Sleep mode
- Idle mode
- Active mode
- Limp-home mode

The transition between operation modes is determined according to the following levels and states:

- Logic level at IDLE pin
- Logic level at INn pins
- PWM_SPI.OUTn bits state
- CFG_1.ACT bit state
- MAP_PWM.OUTn and PWM_SEL.OUTn bits state

The state diagram including the possible transitions is shown in the Figure 4. The behavior of the device as well as some parameters may change depending on its operation mode. Furthermore, due to the undervoltage detection circuitry, which monitors VBATT and VDDIO supply voltages, some changes within the same operation mode can be seen accordingly.

In the case of VBATT < VBATT(UV_L) and IDLE = IN0 = IN1 = high channel outputs are disabled.

The operation mode of the device can be observed by:

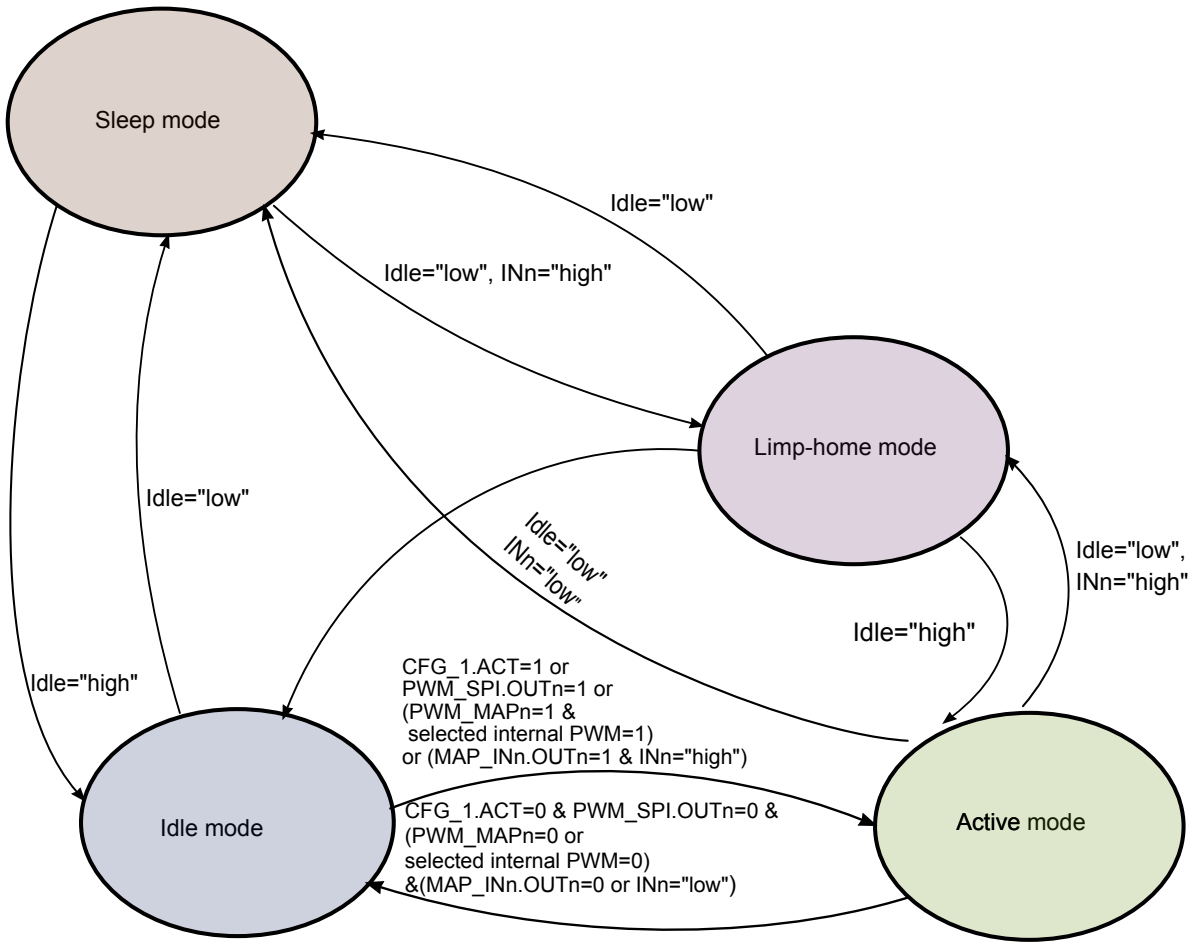
- Status of output channels
- Status of SPI registers
- Current consumption at VBATT pin (I_{VBATT})

The default operation mode to switch on the loads is active mode. If the device is not in active mode and a request to switch on one or more outputs occurs (via SPI or via input pins) it switches into active or limp-home mode, according to IDLE pin status. Due to the time needed for such transitions, output turn-on time t_{ON} is extended due to the mode transition latency.

The state diagram is described in the Figure 4. It is valid if the digital NPOR is '1'. In the case of POR='0' transitions from active to idle and from limp-home to sleep do not ensure switch off behavior with functional timings, but the switch off times extended to t_{OFF_POR}. An NPOR condition is registered in clear on the read NPOR bit of the STA_1 register.

In the case of condition IDLE='0' and INn='0' (corresponding to the transition from active to sleep) the device moves in sleep mode. The transition ACTIVE2SLEEP is not effective if at least one channel is on (only when SPI and PWM drive the channels). In order to turn off a channel before the transition from active to sleep, the bit CFG_0. ACTIVE TO SLEEP DIS SWR shall be set to 1.

Figure 4. State diagram



The Table 10 shows the correlation between device operation modes, VBATT and VDDIO supply voltages, and the state of the most important functions (channels operativity, SPI communication, and SPI registers).

Table 10. Supply ranges and operative modes

Function	Undervoltage condition on VBATT		VBATT not in undervoltage		Operating modes
	VDDIO ≤ $VDDIO_{UV}$	VDDIO > $VDDIO_{UV}$	VDDIO ≤ $VDDIO_{UV}$	VDDIO > $VDDIO_{UV}$	
Channels	u	u	u	u	Sleep
	u	u	u	u	Idle
	u	u(1)	a(2)	a	Active
	u	u(3)	a(2)	a(2)	Limp-home
SPI communication	u	u	u	u	Sleep
	u	a	u	a	Idle
	u	a	u	a	Active
	u	a(4)	u	a(4)	Limp-home
SPI registers	r	r	r	r	Sleep
	r	a	r	a	Idle
	r	a	r	a	Active
	r	a(4)	r	a	Limp-home

1. *Available in case VS_UV_MASK bit is set to 1.*
2. *IN pins only.*
3. *Only OUT2 and OUT3 available in case VS_UV_MASK bit is set to 1.*
4. *Read only.*

Where:

- "a" stands for available
- "u" stands for unavailable
- "r" stands for reset

6.1.1 Power-up

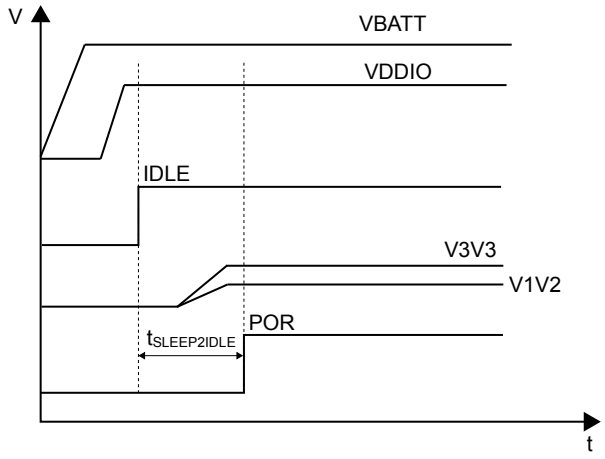
The power-up condition is satisfied if, at least, one of the supply voltages (VBATT or VDDIO) is applied to the device and the INn or IDLE pins are set to “high”.

In case of both VBATT and VDDIO device pins connected to external sources, the VBATT voltage must be included in its supply voltage range for normal operations (VBATT > 6 V).

In case of only the VBATT device pin connected to an external source, the VBATT voltage must be included in its supply voltage range for normal operations (VBATT > 6 V).

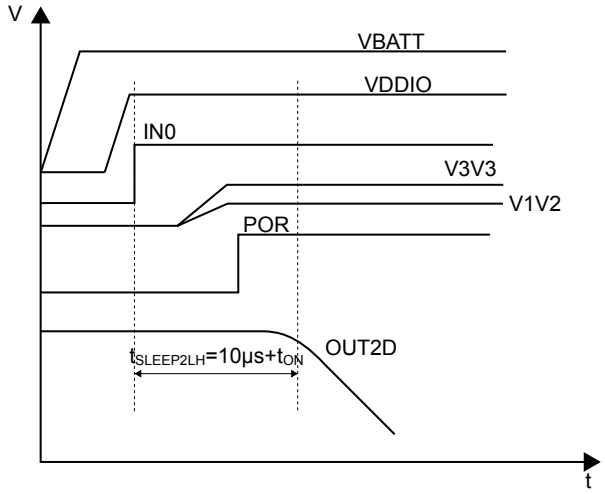
All the possible power-up scenarios are described below:

Figure 5. **Scenario 1 power-up**



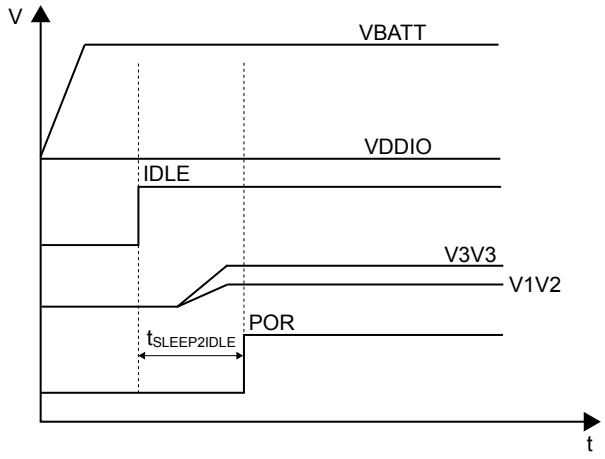
Scenario 1: power-up by VBATT with VDDIO present in sleep to idle transition. Both VBATT and VDDIO are applied in their operative range (6 V to 18 V and 3 V to 5.5 V respectively). IDLE is set to high and the POR signal is released after $t_{SLEEP2IDLE}$ (about 10 µs).

Figure 6. **Scenario 2 power-up**



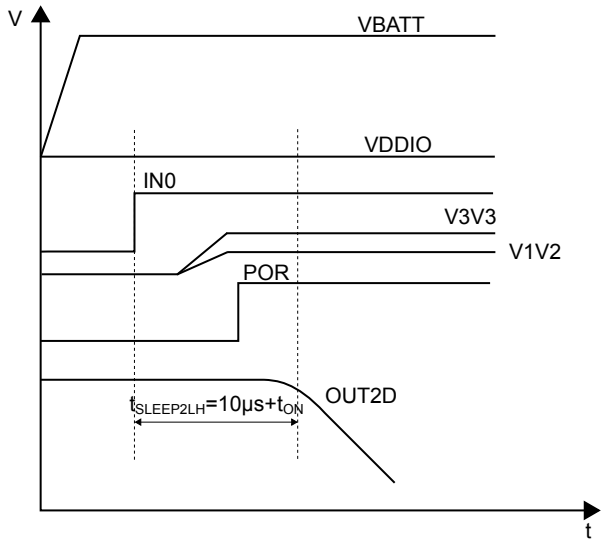
Scenario 2: power-up by VBATT with VDDIO present in sleep to limp-home transition. Both VBATT and VDDIO are applied in their operative range (6 V to 18 V and 3 V to 5.5 V respectively). IN0 (or IN1) is set to high; the POR signal is released after 10 µs and OUTD2 reaches 90% of VBATT in t_{ON} time.

Figure 7. **Scenario 3 power-up**



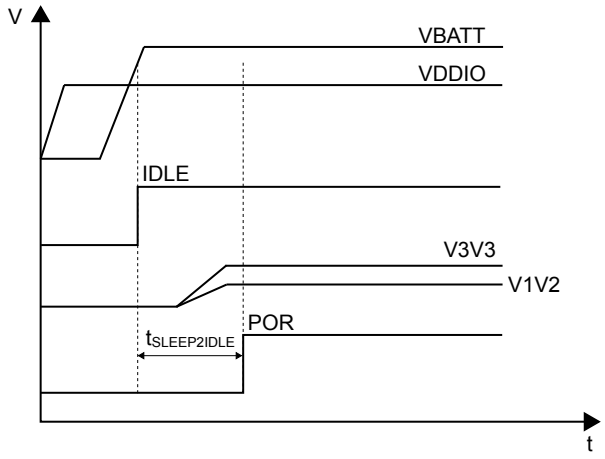
Scenario 3: power-up by VBATT without VDDIO (0 V) in sleep to idle transition. VBATT is applied in its operative range (6 V to 18 V). IDLE is set to high and the POR signal is released after $t_{SLEEP2IDLE}$ (about 10 µs). SPI communication is not available and registers are reset.

Figure 8. **Scenario 4 power-up**



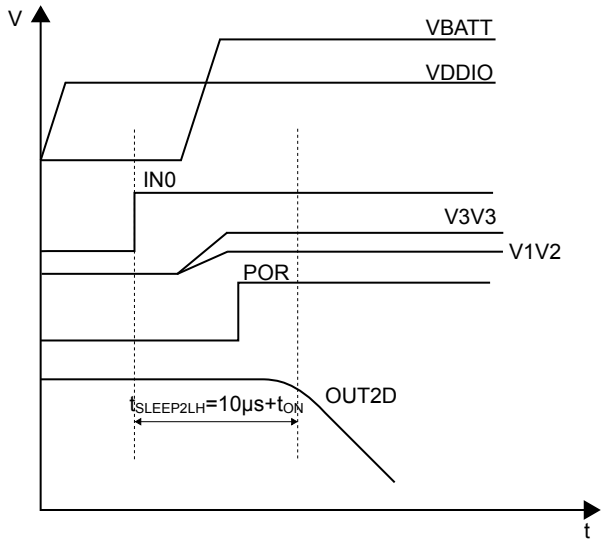
Scenario 4: power-up by VBATT without VDDIO (0 V) in sleep to limp-home transition. VBATT is applied in its operative range (6 V to 18 V). IN0 (or IN1) is set to high; the POR signal is released after about 10 µs and OUT2D reaches 90% of VBATT in t_{ON} time. SPI communication is not available and registers are reset.

Figure 9. **Scenario 5 power-up**



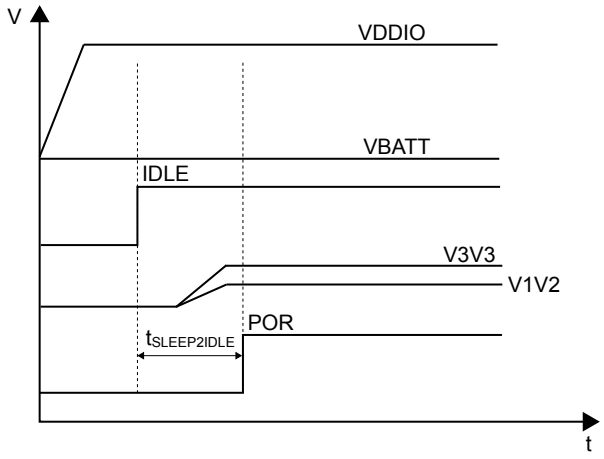
Scenario 5: power-up by VDDIO with VBATT present in sleep to idle transition. Both VBATT and VDDIO are applied in their operative range (6 V to 18 V and 3 V to 5.5 V respectively). IDLE is set to high and the POR signal is released after $t_{SLEEP2IDLE}$.

Figure 10. **Scenario 6 power-up**



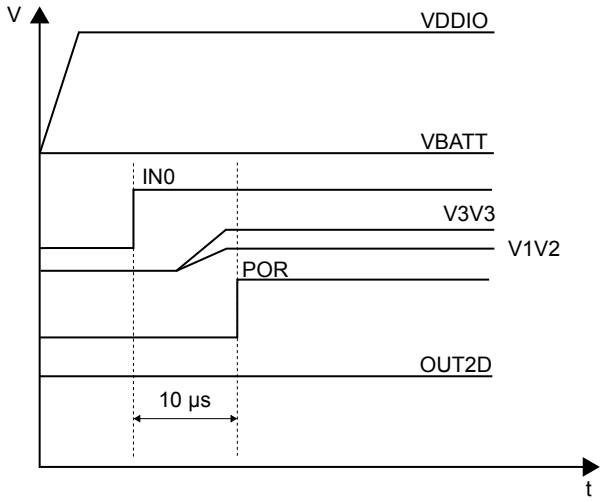
Scenario 6: power-up by VDDIO with VBATT present in sleep to limp-home transition. Both VBATT and VDDIO are applied in their operative range (6 V to 18 V and 3 V to 5.5 V respectively). IN0 (or IN1) is set to high; the POR signal is released after about 10 µs and DRAIN OUT2 reaches 90% of VBATT in t_{ON} time.

Figure 11. **Scenario 7 power-up**



Scenario 7: power-up by VDDIO without VBATT (0 V) in sleep to idle transition. VDDIO is applied in its operative range (3 V to 5.5 V). IDLE is set to high and the POR signal is released in $t_{SLEEP2IDLE}$ (about 10 µs).

Figure 12. **Scenario 8 power-up**



Scenario 8: power-up by VDDIO without VBATT (0 V) in sleep to limp-home transition. VDDIO is applied in its operative range (3 V to 5.5 V). IN0 (or IN1) is set to high; the POR signal is released after 10 µs but OUT2D does not turn on.

6.1.2 Sleep mode

In sleep mode, the outputs of L9800 are OFF and the SPI registers are reset to default values. The current consumption is reduced to the $I_{VDDIO(SLEEP)}$ and $I_{VBATT(SLEEP)}$. Refer to the parameters $I_{VDDIO(SLEEP)}$ and $I_{VBATT(SLEEP)}$ in the Table 11. Power supply.

6.1.3 Idle mode

In idle mode, the current consumption of the device reaches the parameters $I_{VDDIO(IDLE)}$ and $I_{VBATT(IDLE)}$.The on diagnosis functions are available only in read mode. During idle mode the output channels are disabled. The SPI communication is properly working, when the VDDIO is present. In idle mode DIAG_OVC_OVT bits are not clearable.

6.1.4 Active mode

The active mode is needed when there are loads to drive. Voltage levels of VDDIO and VBATT influence the behavior as described at the beginning of Section 6: Power supply. The current consumption is described through these two parameters: $I_{VDDIO(ACTIVE)}$ and $I_{VBATT(ACTIVE)}$. In case CFG_1.ACT is set to “1”, the device enters in active mode and remains in this state independently of the status of input pins, internal PWM generators, and PWM_SPI.OUTn bits.

If CFG_1.ACT is set to “0”, the device comes back to idle mode as soon as all inputs pins are set to “low”, PWM_SPI.OUTn bits are set to “0” and in case of turn off command by PWM generators if properly configured.

If CFG_1.ACT is set to “1”, the device remains in active mode independently of the status of input pins, PWM_SPI.OUTn register and PWM generators registers status. An undervoltage condition on VDDIO supply brings the device into idle mode if IN0 and IN1 are set to “low”. If CFG_1.ACT is set to “0”, the registers MAP_IN0, MAP_IN1 (together with the input pins) and MAP_PWM (together with the related PWM duty cycle) have to be correctly configured to switch to active mode.

6.1.5 Limp-home mode

The L9800 is brought into limp-home mode when one of the two input pins is asserted (this means the enabling of the channel connected to it) and also the idle pin is set to "low". The SPI communication is possible only in read-only mode (SPI registers can be read but cannot be written). If the application is used in limp-home mode, in IDLE and ACTIVE the channels 2 and 3 cannot be used in BIM mode.

More in detail:

- MODE bits are set to “01B” (limp-home mode).
- Overload and overtemperature diagnostics on channel 2 and 3 are available and the related DIAG_OVC_OVT bits can be read.
- DIAG_OPL_OFF and DIAG_SHG bits, referred to diagnostics executed during a previous active phase, can be read via SPI request.

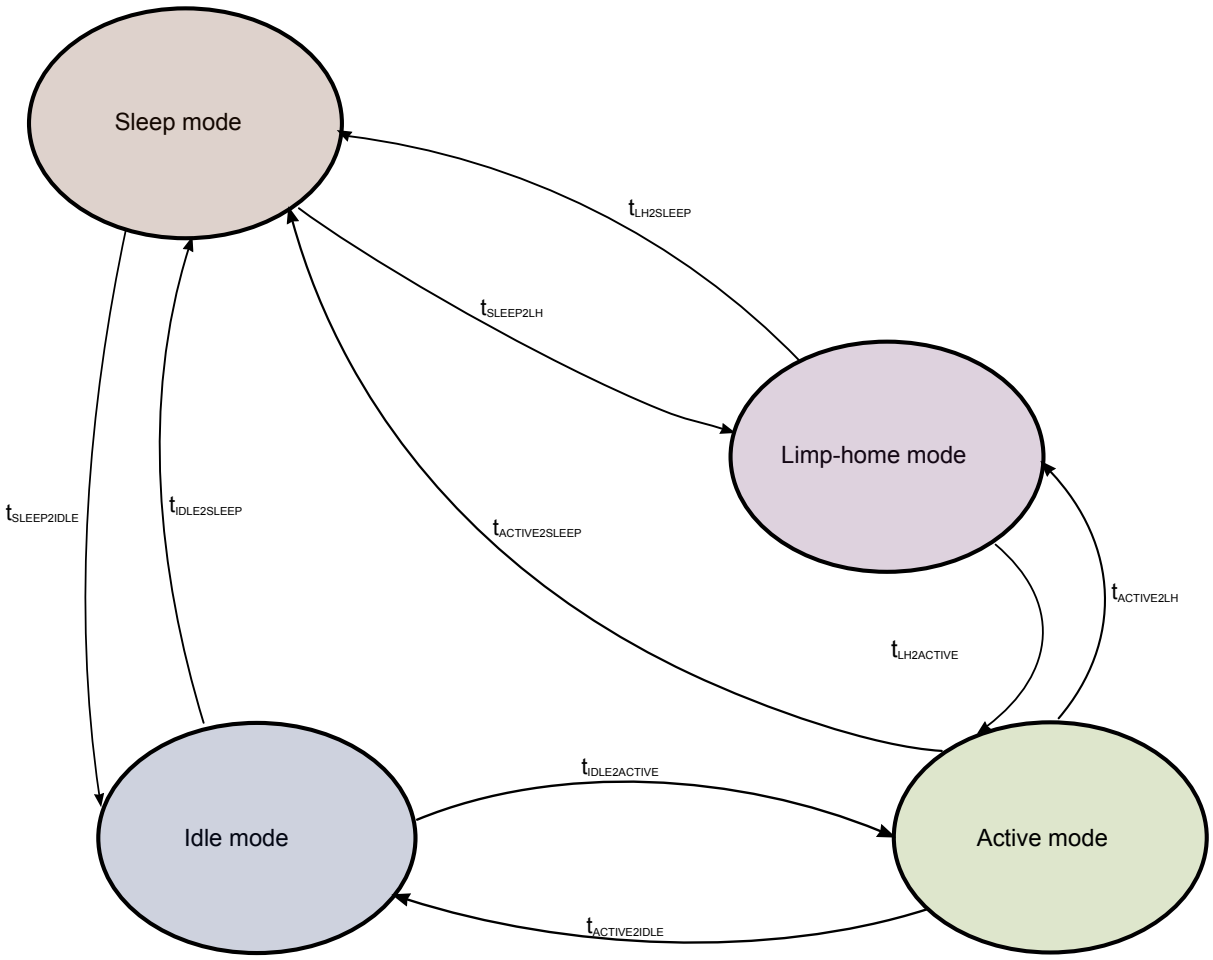
During the transition from limp-home mode to sleep, the complete set of L9800 registers is not accessible for writing until it remains in the limp-home state and is set to their default values.

Refer to Section 6.1: Operating modes for a detailed description of supply voltage conditions required to switch on channels 2 and 3 during limp-home, the other channels are kept off.

6.1.6 Power supply transition

The time to turn on a channel is defined as t_{ON} both in active and limp-home mode. In all other cases, the transition time is reported as shown in Figure 13.

Figure 13. **Transition time diagram**



6.1.7 Reset

The following four conditions reset the SPI register (r/w) to the default value:

1. VDDIO is not present or below the minimum value of $VDDIO_{(UV)}$
2. IDLE pin is set to “low” with both INn “low"
3. A reset command (CFG_1.RST set to “1”) is executed
4. NRES pin asserted

DIAG_OVC_OVT bits are not cleared by a reset command (for functional safety).

STA_1.VDDIO_UV and STA_1.VBATT_UV bits are not cleared by a reset command (for functional safety).

In particular, all channels are switched OFF (if there are no input pin set to “high”) and the input mapping configuration is reset.

6.1.8 Undervoltage on VBATT

If the device is operative and the supply voltage drops below $VBATT_{(UV_L)}$, the logic sets the bit STA_1.VBATT_UV to “1”. As soon as the supply voltage VBATT is above $VBATT_{(UV_H)}$, the bit STA_1.VBATT_UV is set back to “0” after the first clear on read.

Undervoltage condition on VBATT may influence the status of the channels according to VS_UV_MASK bit status, as described in the Table 18.

6.1.9 Low operating power-on VDDIO

When the VDDIO supply voltage drops in the range indicated by $VDDIO_{(UV)}$, the bit STA_1.VDDIO_UV is set to “1”. This is valid if the digital NPOR is ‘1’. For all conditions that generate an NPOR = 0, a dedicated clear on read STA_1. NPOR bit is set. As soon as VDDIO overcomes the minimum of the voltage operative threshold $VDDIO_{(UV_RECOVERY)}$ the bit STA_1.VDDIO_UV is set to “0” after the first clear on read.

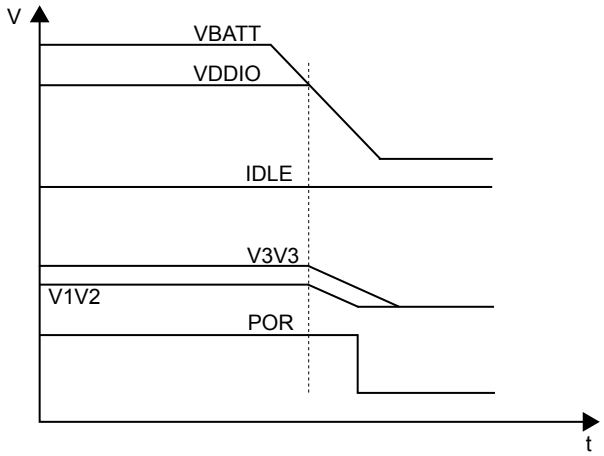
One of the following conditions generates the NPOR condition (reset of the whole internal logic):

1. General internal supply failure (internal 3.3 V supply in UV or bandgap reference not correct)
2. VDDIO < $VDDIO_{(UV)}$ AND IN1 = 0 AND IN0 = 0

6.1.10 Power-down

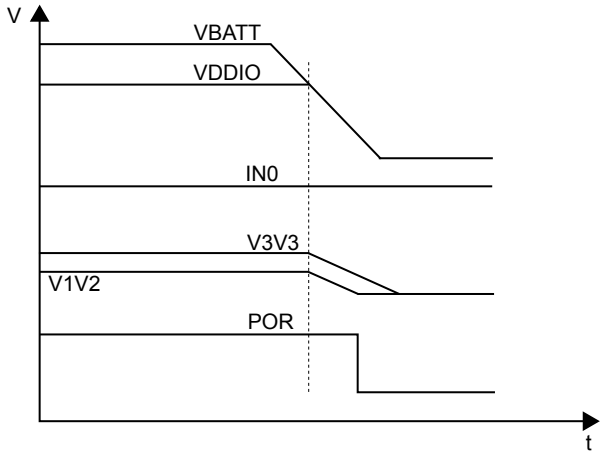
The power-down condition is satisfied if both supply voltages undergo 3 V or, if at least one of them is applied to the device in its operative range, the INn and IDLE pins are all set to “low”. If one or more channels are switched on before power-down, it is necessary to assert a reset to ensure a correct turn-off timing. All possible power-down scenarios are described here below:

Figure 14. Scenario 1 power-down



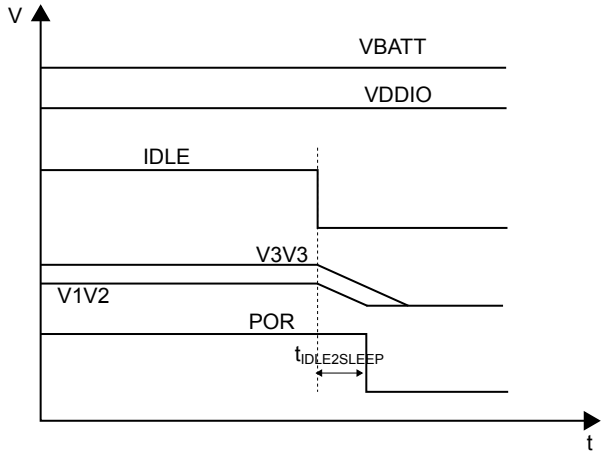
Scenario 1: power-down with both supplies dropping together under 3 V. Although IDLE is high internal supply reference and v_{bg} drop; POR is set to zero. IN0 = IN1 = 0 V.

Figure 15. Scenario 2 power-down



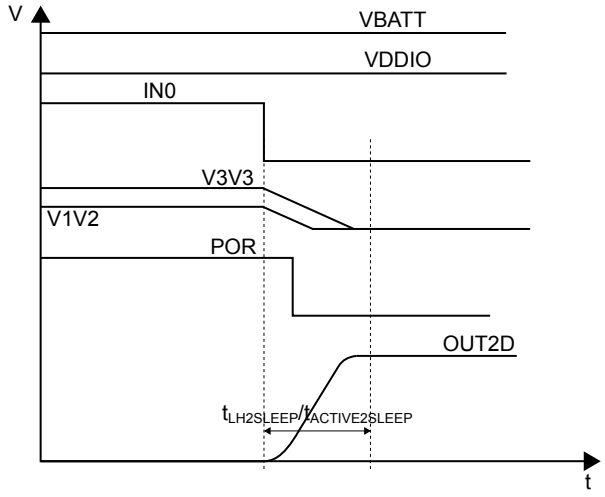
Scenario 2: power-down with both supplies dropping together under 3 V. Although IN0 is high internal supply reference and v_{bg} drop; POR is set to zero. IDLE = IN1 = 0 V.

Figure 16. Scenario 3 power-down



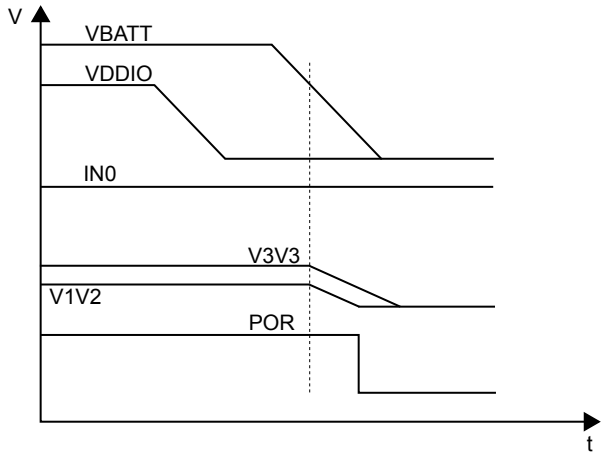
Scenario 3: idle to sleep transition with VDDIO and VBATT in their operative range (at least one of them). IDLE is set to low, V3V3 supply reference and v_{bg} drop, and POR is set to zero by $t_{IDLE2SLEEP}$ of about 10 µs. IN0 = IN1 = 0 V.

Figure 17. Scenario 4 power-down



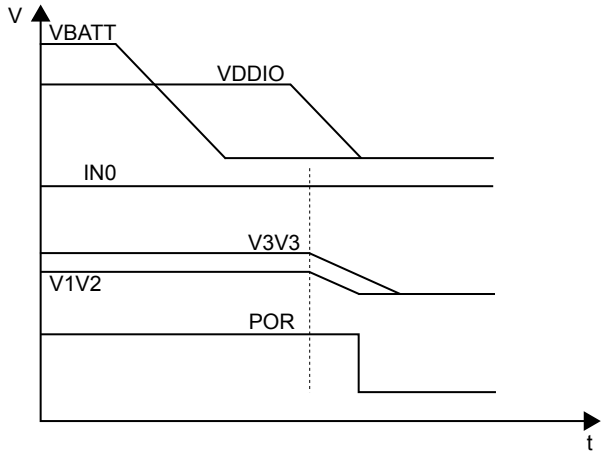
Scenario 4: limp to sleep transition (IDLE=0) and active to sleep transition (IDLE = 1 → 0) with VDDIO and VBATT in their operative range (at least one of them). IN0 is set to low, V3V3 supply reference and v_{bg} , POR goes down to zero and the corresponding channel is switched off within 150 µs, IN1 can be already 0 or can follow IN0 behavior.

Figure 18. **Scenario 5 power-down**



Scenario 5: power-down with VBATT ping down after VDDIO. When even VBATT undergoes 2 V, although IN0 is still high, internal supply reference and v_{bg} ; POR is set to zero. IDLE = IN1 = 0 V.

Figure 19. **Scenario 6 power-down**



Scenario 6: power-down with VDDIO ping down after VBATT. When even VDDIO undergoes 3 V, although IN0 is still high, internal supply reference and v_{bg} ; POR is set to zero, IDLE = IN1 = 0 V. As for scenario 5, the same condition happens if, instead of IN0, one of the other pins is high or two of them or all of them.

6.2 Electrical parameters

3 V < VBATT < 18 V, 3 V < VDDIO < 5.5 V, T_J = -40 °C to 150 °C, unless otherwise noticed.

Table 11. Power supply

Symbol	Description	Comment	Min.	Nom.	Max.	Unit
VBATT pin						
$VBATT_{(UV_L)}$	Analog supply undervoltage low threshold		2.65	2.8	3	V
$VBATT_{(UV_H)}$	Analog supply undervoltage high threshold		2.7	2.85	3.1	V
$dVBATT/dt_{pwrup}$	Battery slew rate during power-up (VBATT from 10% to 90%)		0.5			V/µs
$I_{VBATT(SLEEP)}$	Current consumption from VBATT in sleep mode	V_{IDLE} = 0 V, V_{INn} = 0 V, VDDIO = 5 V, $T_J \leq 85$ °C			1	µA
		V_{IDLE} =0 V, V_{INn} = 0 V, VDDIO = 5 V, 85 °C ≤ T_J ≤ 150 °C			14	µA
$I_{VBATT(IDLE)}$	Analog supply current consumption in idle mode	V_{IDLE} = 5 V, V_{INn} = 0 V, VDDIO = 5 V, f_{SCLK} = 0 MHz, CFG_1.ACT = 0_B, PWM_SPI.OUTn = 0_B, DIAG_OFF_EN.OUTn = 0_B			2.2	mA
$I_{VBATT(IDLE)\ T_J\ high}$	Analog supply current consumption in idle mode for T_J high	V_{IDLE} = 5 V, V_{INn} = 0 V, VDDIO = 5 V, f_{SCLK} = 0 MHz, CFG_1.ACT = 0_B, PWM_SPI.OUTn = 0_B, DIAG_OFF_EN.OUTn = 0_B, T_J > 100 °C			2.3	mA
$I_{VBATT(IDLE_COR)}$	Analog supply current consumption in idle mode from VBATT pin when VBATT is lower than VDDIO (the device is supplied by VDDIO)	V_{IDLE} = 5V, V_{INn} = 0 V, VDDIO = 5 V, f_{SCLK} = 0 MHz, CFG_1.ACT = 0_B, PWM_SPI.OUTn = 0_B, DIAG_OFF_EN.OUTn = 0_B, VBATT = VDDIO-1 V	-0.1		0.1	mA
$I_{VBATT(ACTIVE)}$	Analog supply current consumption in active mode - channels OFF	V_{IDLE} = 5 V, V_{INn} = 0 V, VDDIO = 5 V, f_{SCLK} = 0 MHz, CFG_1.ACT = 1_B, PWM_SPI.OUTn = 0_B, DIAG_OFF_EN.OUTn = 0_B			4.3	mA
$I_{VBATT(ACTIVE_COR)}$	Analog supply current consumption in active mode - channels OFF from VBATT pin when VBATT is lower than VDDIO (the device is supplied by VDDIO)	V_{IDLE} = 5 V, V_{INn} =0 V, VDDIO = 5 V, f_{SCLK} = 0 MHz, CFG_1.ACT = 1_B, PWM_SPI.OUTn = 0_B,	-0.1		0.1	mA

Symbol	Description	Comment	Min.	Nom.	Max.	Unit
		DIAG_OFF_EN.OUTn = 0_B, VBATT=VDDIO - 1 V				
$T_{VBATTUVFLT}$	VBATT undervoltage filter	Covered by SCAN	9	14	19	µs
VDDIO pin						
$VDDIO_{(OP)}$	VDDIO supply operating voltage range	f_{SCLK} = 8 MHz, design info	3.0		5.5	V
$VDDIO_{(UV)}$	Undervoltage shut down threshold	MISO from “low” to high-Z	2.65	2.8	3	V
$VDDIO_{(UV_RECOVERY)}$	Analog supply threshold for recovery after VDDIO undervoltage	MISO from “low” to high-Z	2.7	2.85	3.1	V
$dVDDIO/dt_{pwrup}$	Supply slew rate during power-up (VDDIO from 10% to 90%)					V/µs
$I_{VDDIO(SLEEP)}$	VDDIO supply current in sleep mode	V_{IDLE} = 0 V, V_{INn} = 0 V, VDDIO = 5 V, $T_J \leq 85$ °C			1	µA
		V_{IDLE} = 0 V, V_{INn} = 0 V, VDDIO = 5 V, T_J = 150 °C			2	
$I_{VDDIO(IDLE)}$	VDDIO supply current in idle mode	V_{IDLE} = 5 V, V_{INn} = 0 V, VDDIO = 5 V, f_{SCLK} = 0 MHz, CFG_1.ACT = 0_B, PWM_SPI.OUTn = 0_B, DIAG_OFF_EN.OUTn = 0_B			1.2	mA
$I_{VDDIO(IDLE)\ T_J\ high}$	VDDIO supply current in idle mode for T_J high	V_{IDLE} = 5 V, V_{INn} = 0 V, VDDIO = 5 V, f_{SCLK} = 0 MHz, CFG_1.ACT = 0_B, PWM_SPI.OUTn = 0_B, DIAG_OFF_EN.OUTn = 0_B				
$I_{VDDIO(IDLE)}$	VDDIO supply current in idle mode from VDDIO pin when VBATT is lower than VDDIO (the device is supplied by VDDIO)	V_{IDLE} = 5 V, V_{INn} = 0 V, VDDIO = 5 V, f_{SCLK} = 0 MHz, CFG_1.ACT = 0_B, PWM_SPI.OUTn = 0_B, DIAG_OFF_EN.OUTn = 0_B, VBATT = VDDIO - 1 V			2.2	mA
$I_{VDDIO(ACTIVE)}$	VDDIO supply current in active mode– channels OFF from VDDIO pin when VBATT is lower than VDDIO (the device is supplied by VDDIO)	V_{IDLE} = 5 V, V_{INn} = 0 V, VDDIO = 5 V, f_{SCLK} = 0 MHz, CFG_1.ACT = 1_B, PWM_SPI.OUTn = 0_B, DIAG_OFF_EN.OUTn = 0_B, VBATT = VDDIO - 1 V			4.2	mA

Symbol	Description	Comment	Min.	Nom.	Max.	Unit
$I_{VDDIO(ACTIVE_COR)}$	Logic supply current in active mode–channels OFF from VDDIO pin when VBATT is higher than VDDIO (the device is supplied by VDDIO)	V_{IDLE} = 5 V, V_{INn} = 0 V, VDDIO = 5 V, f_{SCLK} = 0 MHz, CFG_1.ACT = 1_B, PWM_SPI.OUTn = 0_B, DIAG_OFF_EN.OUTn = 0_B			1.2	mA
$T_{VDDIOUVFLT}$	VDDIO undervoltage filter	Covered by SCAN	9	14	19	µs
Timings						
$t_{IDLEFLT}$	Idle filter time	Covered by SCAN	4.9	7	10	µs
$t_{SLEEP2IDLE}$	Sleep to idle delay	Covered by SCAN			120	µs
$t_{IDLE2SLEEP}$	Idle to sleep delay	From IDLE pin to sleep external pull-down MISO to GND required covered by SCAN			10	µs
$t_{IDLE2ACTIVE}$	Idle to active delay	From INn or NCS pins to MODE = 11_B, covered by SCAN			1	µs
$t_{ACTIVE2IDLE}$	Active to idle delay	From INn or NCS pins to MODE = 10_B, covered by SCAN			150	µs
$t_{SLEEP2LH}$	Sleep to limp-home delay	From INn pins to V_{DS} = 10% VBATT, covered by SCAN			120 + t_{ON}	µs
$t_{LH2SLEEP}$	Limp-home to sleep delay	From INn pins to MODE = 00_B, external pull-down MISO to GND required, covered by SCAN			t_{OFF_POR}	µs
$t_{LH2ACTIVE}$	Limp-home to active delay	From IDLE pin to MODE = 11_B covered by SCAN			20	µs
$t_{ACTIVE2LH}$	Active to limp-home delay	From IDLE pin to MODE = 01_B, covered by SCAN			20	µs
$t_{ACTIVE2SLEEP}$	Active to sleep delay	From IDLE pin to MODE = 00_B, External pull-down MISO to GND required, Covered by SCAN			t_{OFF_POR}	µs
t_{OFF_POR}	Channel switch off time with passive pull-down (NPOR=0)	From NPOR = 0 V to V_{DS} = 90% VBATT			150	µs

Note: All the digital filtering times reported in Table 11 are to be considered without spread spectrum.

7 Power stages

The device is an 8-channel low-side relay switch. The power stages are made by N-channel Power MOSFET transistors.

The source of the power transistors must be directly connected to the GND pin potential. An unwanted OV detection may happen when a different voltage is applied.

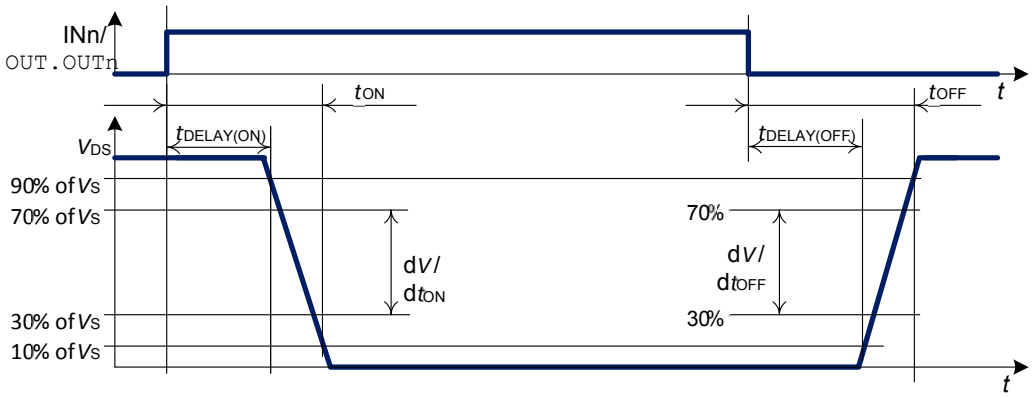
7.1 Operating modes

The $R_{DS(ON)}$ (on-state resistance) depends on the T_J (junction temperature) and on the supply voltage.

7.1.1 Switching resistive loads

In the case of resistive loads switching, refer to the following switching times and slew rates.

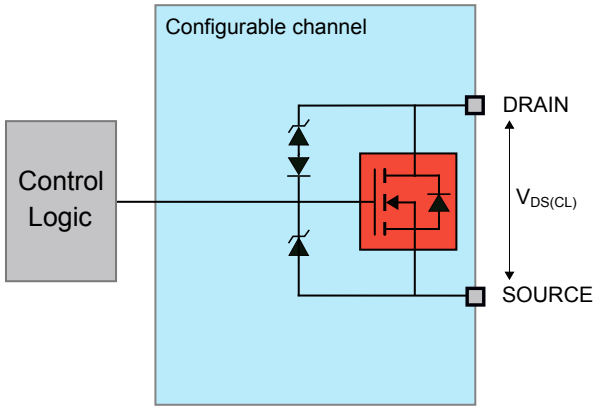
Figure 20. Switching resistive load



7.1.2 Inductive output clamp

The inductance still drives the current the voltage across the power switch increases until reaching $V_{DS(CL)}$ in case of switching off inductive loads. The voltage clamping is necessary to prevent device destruction and protects the device in all operative modes. The maximum allowed load inductance is limited by the max energy. The clamping structure preserves the device in all the operating states: sleep, idle, active, and limp-home (see the Figure 21).

Figure 21. Output clamp concept



7.1.3 Maximum load inductance

The maximum energy, which is converted into heat, is limited by the thermal design of the component. The E_{AR} value provided in Features assumes that all channels can dissipate the same energy when the inductances connected to the outputs are demagnetized at the same time.

7.2 Bulb inrush mode

Although the device is optimized for relays and LED, it may be necessary to use one or more of the outputs to drive small lamps (typically 2 W) or electronic loads with a high input capacitor. In such operative conditions at the switch on, an inrush current may appear, reaching the overload current threshold, which latches the channel off.

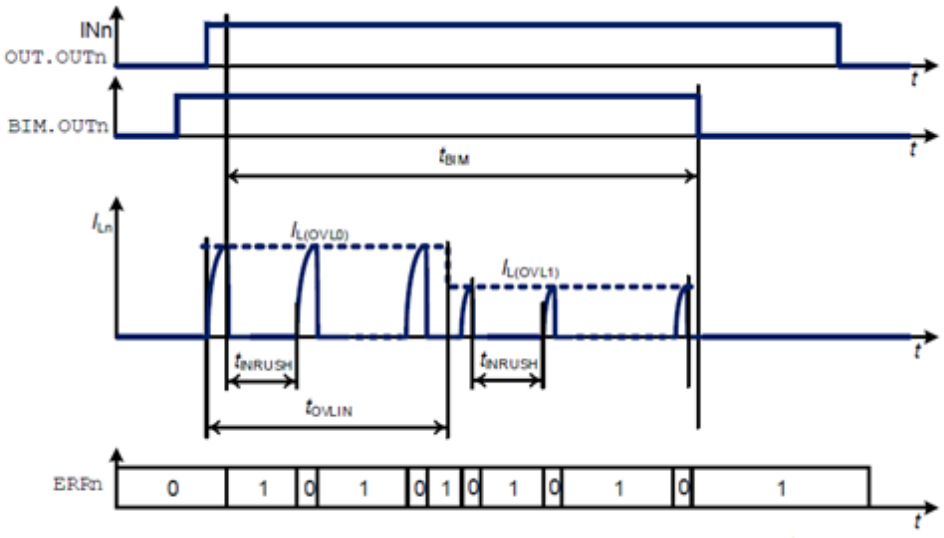
In normal operation the device waits until the microcontroller sends an SPI command to clear the latches (register DIAG_OVC_OVT) allowing the channel to turn on again. Usually this delay is too long to transfer enough energy to the load. If the corresponding bit BIM.OUTn is set to “1”, in case the channel reaches the overload current threshold and latches off, it restarts automatically after a time t_{INRUSH}, allowing the load to go out of the inrush phase. A time diagram is shown in the Figure 22.

The channel configured with the BIM option can be either driven by an SPI command, PWM command (internal generator) or INn parallel input. Once programmed to “1” via SPI, the BIM.OUTn bits are set back to “0” at the end of BIM time(t_{BIM}), unless a reset condition occurs ($VDDIO_{(UV)}$, hardware, or software reset): an eventual switch off of the channel commanded by the user has no impact on BIM.OUTn configuration.

When BIM.OUTn are set to “1”, eventual overcurrent conditions flag DIAG_OVC_OVT.OUTn bit, but the affected channels will not be permanently switched OFF (automatic restart after T_{INRUSH}). Once asserted, the eventual SPI attempt to clear DIAG_OVC_OVT.OUTn is ignored, until the BIM counter is expired. To resume the normal behavior when the BIM counter is expired, the DIAG_OVC_OVT.OUTn should be cleared. If OVT condition happens before OVC condition, the flag is set and the channel is turned off but it could be turned on again by clearing register DIAG_OVC_OVT.OUTn

An internal timer set the bit BIM.OUTn back to “0” after 40 ms (parameter t_{BIM}) starting from the first OVC event latched to prevent an excessive thermal stress to the channel, especially in case of short circuit at the output. Another countermeasure against overheating is that, in case the load current is higher than $I_{L(OVL0)}$ or $I_{L(OVL1)}$, the overloaded channel is immediately switched OFF, without waiting for digital filter time $t_{OFF(OVL)}$ expiration. The overload threshold is $I_{L(OVL0)}$ between first channel switch on and t_{OVLIN} (in BIM mode t_{OVLIN} is not reset every time the channel is switched off by overcurrent); $I_{L(OVL1)}$ from t_{OVLIN} expiration to the end of bulb inrush mode. The device allows a per-channel selection of bulb inrush mode (BIM) in order to be fully flexible without any additional reliability risk.

Figure 22. Bulb mode



7.3 PWM generator

The device has two independent PWM generators, which are defined as “PWM GEN” and “PWM LED” below. The two PWM generators can be associated to one or more channels. It is possible to configure it with various frequencies and duty cycle. For both refer to the same base frequency f_{INT} (8 MHz typ.) even if two separate pre-scalers can be defined.

7.3.1 Automatic PWM generator

The device has one independent automatic PWM generator that can be assigned to one or more channels and can be programmed with different duty cycle and frequency. The PWM frequency is obtained by dividing the internal clock base frequency f_{INT} and can be set using CFG_1.PWM_DIV_GEN bits and adjusted through CFG_2.FR_ADJ bits as described in the Table 12.

Table 12. Coefficient overview

CFG_2.FR_ADJ	Absolute delta to f_{INT} divider
00_B	0%
01_B	-13%
10_B	+18%
11_B	0%

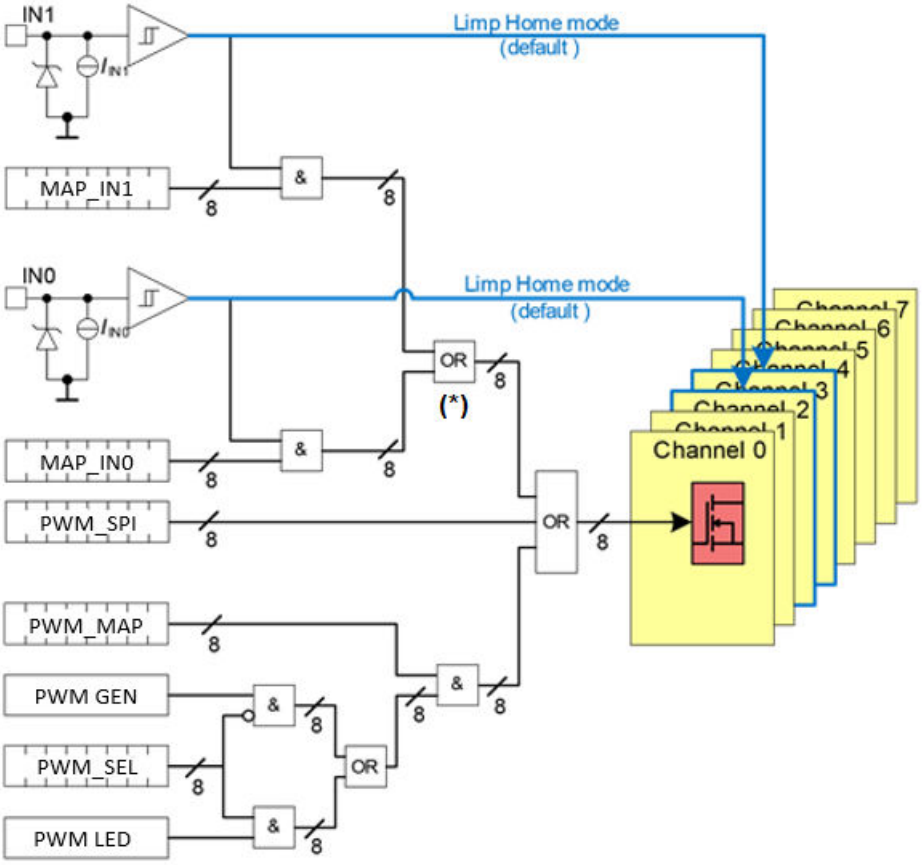
To configure the PWM generator, the user can set the following parameters:

1. Duty cycle (bits PWM_GEN_DC.DUTY_CYCLE)
   8 bits are available to achieve 0.39% duty cycle resolution.
   When the microcontroller programs a new duty cycle, the PWM generator waits until the previous cycle is completed before using the new duty cycle (this happens also when the duty cycle is 100%) - the new duty cycle is taken with the next PWM cycle, while the new duty cycle is immediately taken if the previous DC was 0%)
   The maximum duty cycle achievable is 100% (PWM_GEN_DC.DUTY_CYCLE set to “11111111B”).
2. Frequency (bits CFG_1.PWM_DIV_GEN)
   Using 2 bits it is possible to select the divider for f_{INT} to achieve the needed duty cycle:
   - 00B = PWM frequency is 122.5 Hz
   - 01B = PWM frequency is 245.1 Hz
   - 10B = PWM frequency is 490.2 Hz
   - 11B = PWM frequency is 980.4 Hz
3. Mapping registers (PWM_SEL and PWM_MAP)

To correctly use the PWM generator:

- Configure the channel output control and mapping register (PWM_SEL and PWM_MAP).
- Write the duty cycle control register (PWM_GEN_DC) to enable the PWM generation.

Figure 23. **PWM generator**



(*) In case IN0 and IN1 are mapped to the same channel, IN0 has a higher priority with respect to IN1.

7.3.2 Automatic PWM LED generator

Device has one independent automatic PWM LED generator. This can be assigned to one or more channels, and can be programmed with a different duty cycle and frequency. The PWM frequency is obtained by dividing the internal clock base frequency f_{INT} and can be set using CFG_2.PWM_DIV_LED bits and adjusted through CFG_2.FR_ADJ bits as described in the Table 13.

Table 13. **Coefficient overview**

CFG_2.FR_ADJ	Absolute delta to f_{INT} divider
00_B	0%
01_B	-13%
10_B	+18%
11_B	0%

Four parameters can be set:

1. Duty cycle (bits PWM_LED_DC.DUTY_CYCLE)
   8 bits are available to achieve 0.39% duty cycle resolution.
   When the microcontroller programs a new duty cycle, the PWM LED generator waits until the previous cycle is completed before using the new duty cycle (this happens also when the duty cycle is 100%) - the new duty cycle is taken with the next PWM cycle, while the new duty cycle is immediately taken if the previous DC was 0%).
   Maximum duty cycle achievable is 100% (PWM_LED_DC.DUTY_CYCLE set to “11111111B”)
2. Frequency (bits CFG_2.PWM_DIV_LED)
   Using 2 bits it is possible to select the divider for f_{INT} to achieve the needed duty cycle:
   – 00B = PWM frequency is 122.5 Hz
   – 01B = PWM frequency is 245.1 Hz
   – 10B = PWM frequency is 490.2 Hz
   – 11B = PWM frequency is 980.4 Hz
3. Mapping registers (PWM_SEL and PWM_MAP)

To correctly use the PWM LED generator:

- Configure the channel output control and mapping register (PWM_SEL and PWM_MAP).
- Write the duty cycle control register (PWM_LED_DC) to enable the PWM LED generation.

7.4 Electrical parameters

3 V < VBATT < 18 V, 3 V < VDDIO < 5.5 V, T_J = -40 °C to 150 °C, unless otherwise noticed.

Table 14. Power stages electrical parameters

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit
Power stage						
$R_{DS(ON)}$	On-state resistance	T_J = 25 °C		0.77		Ω
		T_J = 150 °C, I_L= 100 mA			1.7	Ω
$I_{L(NOM)}$	Nominal load current (all channels active)	T_J ≤ 150 °C, design info		260	500	mA
$I_{L(EAR)}$	Load current for maximum energy dissipation–repetitive (all channels active)	T_J ≤ 150°C, design info		220		mA
$V_{LS_DS(CL)}$	Drain to source output clamping voltage	I_L = 10mA	45	47	49	V
$I_{L(OFF)_LS}$	Output leakage current (each channel) T_J = 150 °C	V_{BATT} = 0 V, V_{DDIO} = 0 V, V_{SOURCE}= 0 V, V_{DS} = 28 V (with at least another channel’s V_{DS}= 29 V), T_J up to 150°C	-4	0	4	µA
E_{AR}	Maximum energy dissipation repetitive pulses - 2*$I_{L(EAR)}$ (two channels in parallel)	$T_{J(0)}$ = 85 °C, $I_{L(0)}$ = 2*$I_{L(EAR)}$, 2*10^6 cycles			15	mJ
E_{AS}	Maximum energy dissipation single pulse	T = 25 °C, I_L = 2 * 200 mA			50	mJ
	Maximum energy dissipation single pulse	T = 150 °C, I_L = 400 mA			25	mJ
E_{AR}	Maximum energy dissipation repetitive pulses - $I_{L(EAR)}$	T = 85 °C, 2*10^6 cycles			10	mJ
Timings						
$t_{DELAY(ON)}$	Turn-ON delay (from INn pin or bit to V_{OUT} = 90% VBATT)	R_L = 50 Ω, VBATT = 14 V, Active or limp-home mode	1.5		4	µs
$t_{DELAY(OFF)}$	Turn-OFF delay (from INn pin or bit to V_{OUT} = 10% VBATT)	R_L = 50 Ω, VBATT = 14 V, Active or limp-home mode	2.5	10	21	µs

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit
t_{ON}	Turn on time (from INn pin or bit to V_{OUT} = 10% VBATT)	R_L = 50 Ω, VBATT = 14 V, Active or limp-home mode	7	15	35	µs
t_{OFF}	Turn off time (from INn pin or bit to V_{OUT} = 90% VBATT)	R_L = 50 Ω, VBATT = 14 V, Active or limp-home mode	4		40	µs
dV/dt_{ON}	Turn on slew rate V_{DS} = 70% to 30% VBATT	R_L = 50 Ω, VBATT = 14 V, Active or limp-home mode	0.35	1	2.2	V/µs
dV/dt_{OFF}	Turn off slew rate V_{DS} = 30% to 70% VBATT	R_L = 50 Ω, VBATT = 14 V, Active or limp-home mode	0.15	1.3	3.4	V/µs
dV/dt_{OFF}	Turn off slew rate V_{DS} = 30% to 70% VBATT gate kill condition	R_L = 50 Ω, VBATT = 14 V, Active or limp-home mode	12		35	V/µs
t_{INRUSH}	Bulb inrush mode restart time	Active mode covered by SCAN	29	40	51	µs
t_{BIM}	Bulb inrush mode reset time	Active mode covered by SCAN	29	41	55	ms
PWM generator						
f_{INT}	Internal reference frequency			8		MHz
$f_{INT(VAR)}$	Internal reference frequency variation		-15		15	%
$f_{INT(VAR_3V)}$	Internal reference frequency variation when VBATT=VDDIO=3V		-15		22	%

Note: All the digital filtering times reported in Table 14 are to be considered without spread spectrum.

8 Protection functions

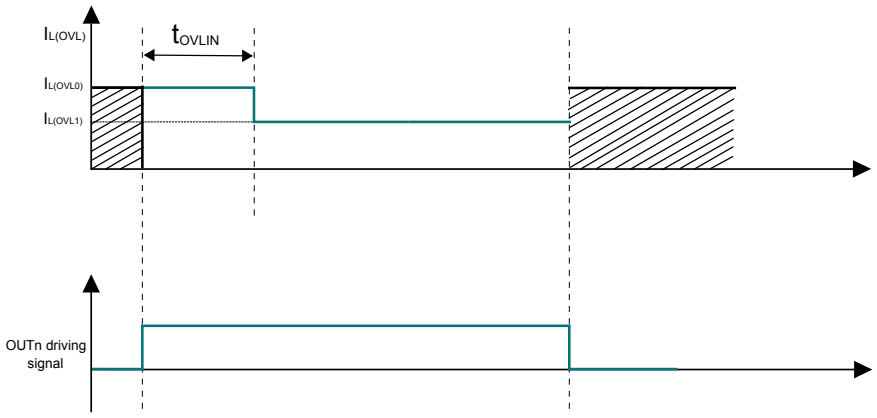
8.1 Overload protection

The L9800 has two different overload current thresholds that preserve itself in case of overload or short-circuit of the load (see Figure 24):

- $I_{L(OVL0)}$ between channel switch on and t_{OVLIN}
- $I_{L(OVL1)}$ after t_{OVLIN}

Every time the channel is switched off the over load current threshold is set back to $I_{L(OVL0)}$.

Figure 24. Overload thresholds



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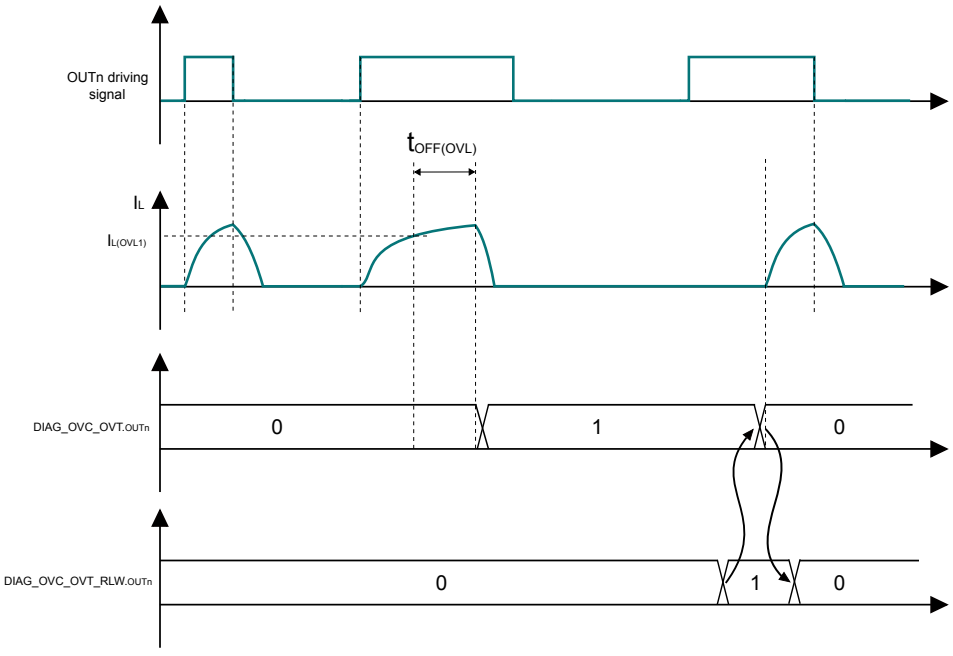
In case the load current is higher than $I_{L(OVL0)}$ or $I_{L(OVL1)}$, after time $t_{OFF(OVL)}$ the over loaded channel is switched off and the corresponding diagnosis bit DIAG_OVC_OVT.OUTn is set to “1”. The channel can be switched on after clearing the protection latch by setting the corresponding DIAG_OVC_OVT_RLW.OUTn bit to “1”. This bit is set back to “0” internally after de-latching the channel. Please refer to Figure 25 for details.

Figure 25. Latch-off overload



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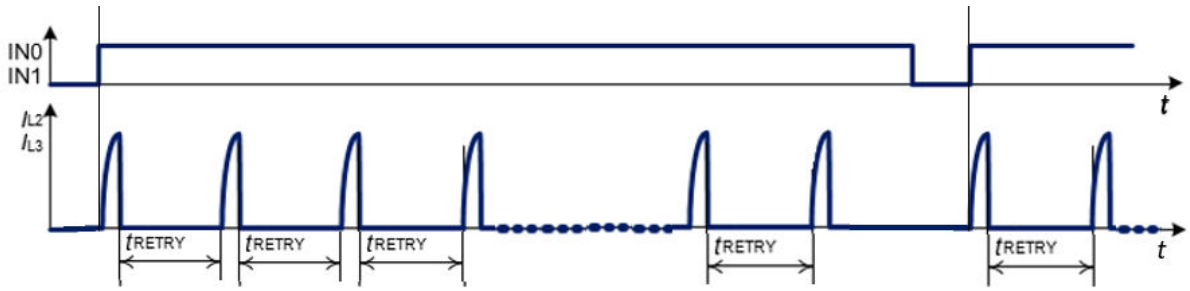
8.2 Overtemperature protection

A temperature sensor is integrated for each channel. Eight temperature sensors are present, causing any overheated channel to switch off to prevent destruction. The thermal protection is disabled (masked) when the channel is in the off state. The thermal protection is enabled when the channel is in on state only. The diagnosis bit DIAG_OVC_OVT is set accordingly (combined with overload protection). The channel can be switched on after clearing the protection latch by setting the corresponding DIAG_OVC_OVT_RLW.OUTn bit to “1”. This bit is set back to “0” internally after de-latching the channel.

8.3 Overtemperature and overload in limp-home mode

In limp-home mode, through the input pin IN0 and IN1, the channels 2 and 3 can be switched on. In case of overload, short-circuit or overtemperature the channels are switched off. If IN0 and IN1 remain “high”, the channel remains on, in case of overload the channels restart at every t_{RETRY}.

Figure 26. Restarter in limp-home mode



8.4 Electrical parameters

3 V < VBATT < 18 V, 3 V < VDDIO < 5.5 V, T_J = -40 °C to 150 °C, unless otherwise noticed.

Table 15. Overtemperature and overload electrical parameters

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit
Overload						
$I_{L(OVL0_LS)}$	High overload detection current	T_J = -40 °C	1		1.9	A
$I_{L(OVL0_LS)}$	High overload detection current	T_J = 25 °C	1		1.7	A
$I_{L(OVL0_LS)}$	High overload detection current	T_J = 150 °C	1		1.7	A
$I_{L(OVL1_LS)}$	Low overload detection current	T_J = -40 °C	0.6		1	A
$I_{L(OVL1_LS)}$	Low overload detection current	T_J = 25 °C	0.6		1	A
$I_{L(OVL1_LS)}$	Low overload detection current	T_J = 150 °C	0.6		1	A
t_{OVLIN}	Overload threshold switch delay time	Covered by SCAN	110	170	260	µs
$t_{OFF(OVL)}$	Overload shut down deglitch filter	BIM.OUTn=0_B, Covered by SCAN	4	5.5	6.5	µs
OVT						
$T_{J(SC)}$	Thermal shut-down temperature		182	192	202	°C
Timings						
t_{RETRY}	Restart time in limp-home mode	Covered by SCAN	29	41	52	ms
t_{OVT}	Overtemperature switch off time	Design info			50	µs

Note: All the digital filtering times reported in the Table 15 are to be considered without spread spectrum.

9 Diagnosis

The SPI communication provides diagnosis information about the device and the load status. Diagnosis information of each channel is independent from other channels. An error condition on one channel has no influence on the diagnostic of the others.

9.1 Overload and overtemperature

When either an overload or an overtemperature occurs on one channel, the diagnosis bit DIAG_OVC_OVT.OUTn is set accordingly. The channel latches OFF and must be reactivated setting the corresponding DIAG_OVC_OVT_RLW.OUTn bit to “1”. The writing operation is necessary to remove the fault as a result of the DIAG_OVC_OVT.OUTn register is clear on write.

9.2 Off diagnosis

This diagnosis is available only in active mode. The device is able to detect two kinds of fault in off, open-load and short to ground.

This diagnosis is available after sending an SPI request. It is performed through two different phases: the first one distinguishes between fault and no fault condition; the second one, completed only if a fault has been found, is intended to investigate the type of the fault.

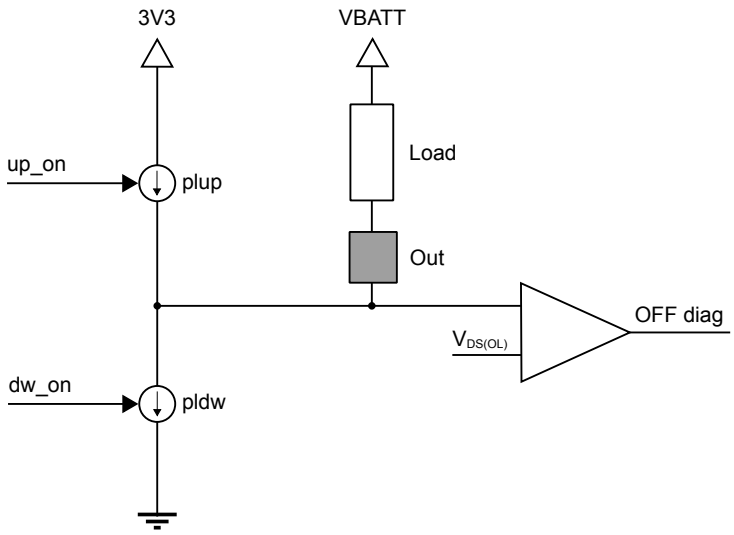
The first phase lasts for t_{OFF1LS}. The current generator showed in the Figure 27, marked with ‘pldw’, and driven by dw_on, is active, and the current generator ‘plup’ is off. In this phase, if the drain voltage remains above the prefixed threshold, the comparator output is low and it means that a load is present; otherwise, if the drain voltages decrease below threshold, the comparator output makes a transition to “1” and sets the presence of a fault.

After the first diagnosis interval, if a fault happened the current generator indicated with ‘plup’ and driven by the signal up_on is activated and the other one is switched off for a time t_{OFF2LS}.

After the pull-up activation, if the drain voltage rises and overcomes the comparator threshold again, an open-load fault is reported. On the other hand, if the voltage remains constant and equal to zero for the whole diagnosis time a short to ground fault is detected. If DIS pin is high an off state diagnosis request is ignored and ongoing diagnosis is reset

The diagnosis can be requested on one or more channels in parallel. Once the diagnosis has been started, a new diagnosis should not be sent until the ongoing diagnostic cycle is finished. Once the diagnosis is completed DIAG_OFF_EN register is automatically cleared.

Figure 27. OFF diagnosis circuit



9.3 Electrical parameters

6 V < VBATT < 18 V, 3 V < VDDIO < 5.5 V, T_J = -40 °C to 150 °C, unless otherwise noticed.

Table 16. Output status and open-load on

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit
Output status monitor						
$V_{DS(OL)}$	Output status monitor threshold voltage	VBATT = 14 V, Active	1.7	1.95	2.2	V
I_{OLD_LS}	Output diagnosis pull-down current	V_{DRAIN} = 14 V	290		550	µA
I_{OLU_LS}	Output diagnosis pull-up current	V_{DRAIN} = 0 V	-260		-140	µA
Open-load at ON						
t_{OFF1LS}	Diag OFF first window	Covered by SCAN	0.89	1.03	1.29	ms
t_{OFF2LS}	Diag OFF second window	Covered by SCAN	200	250	290	µs

Note: All the digital filtering times reported in Table 16 are to be considered without spread spectrum.

10 Limp-home mode

The limp is intended to handle limited functionality of the device in critical faulty situations.

A typical application scenario is reported in the Figure 28, with a system, which is reconfigured during the limp-home as shown in the Figure 29. If the microcontroller that controls the device fails, an external safety microcontroller takes over controlling parallel inputs IN0 and IN1. The SBC forces the IDLE signal low, which brings the device in limp home. Once the switching activity on IN0, IN1 is over, being the IDLE pin still de-asserted, the device reaches sleep mode.

During this mode active, the L9800 is only capable of driving two outputs that is, OUT2 through IN0 and OUT3 through IN1; such a mapping is fixed and overcomes an eventual different mapping programmed via SPI once the limp-home is reached.

Figure 28. Possible system configuration during normal operating conditions

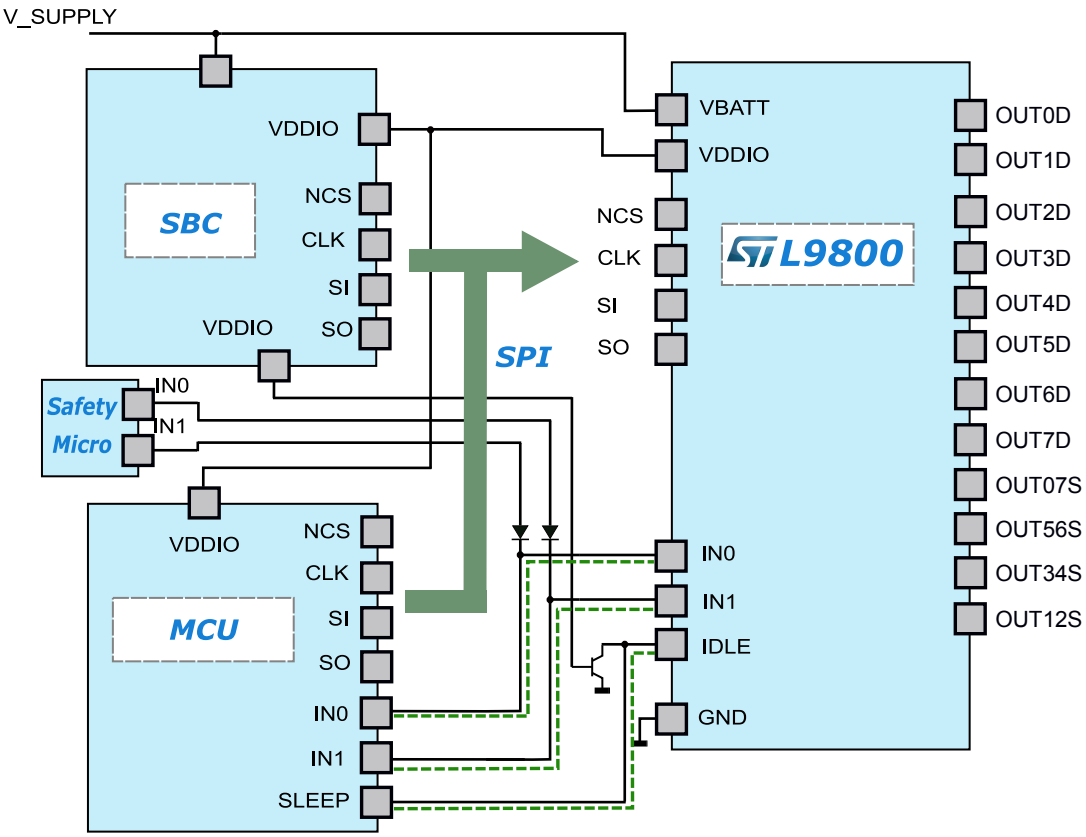
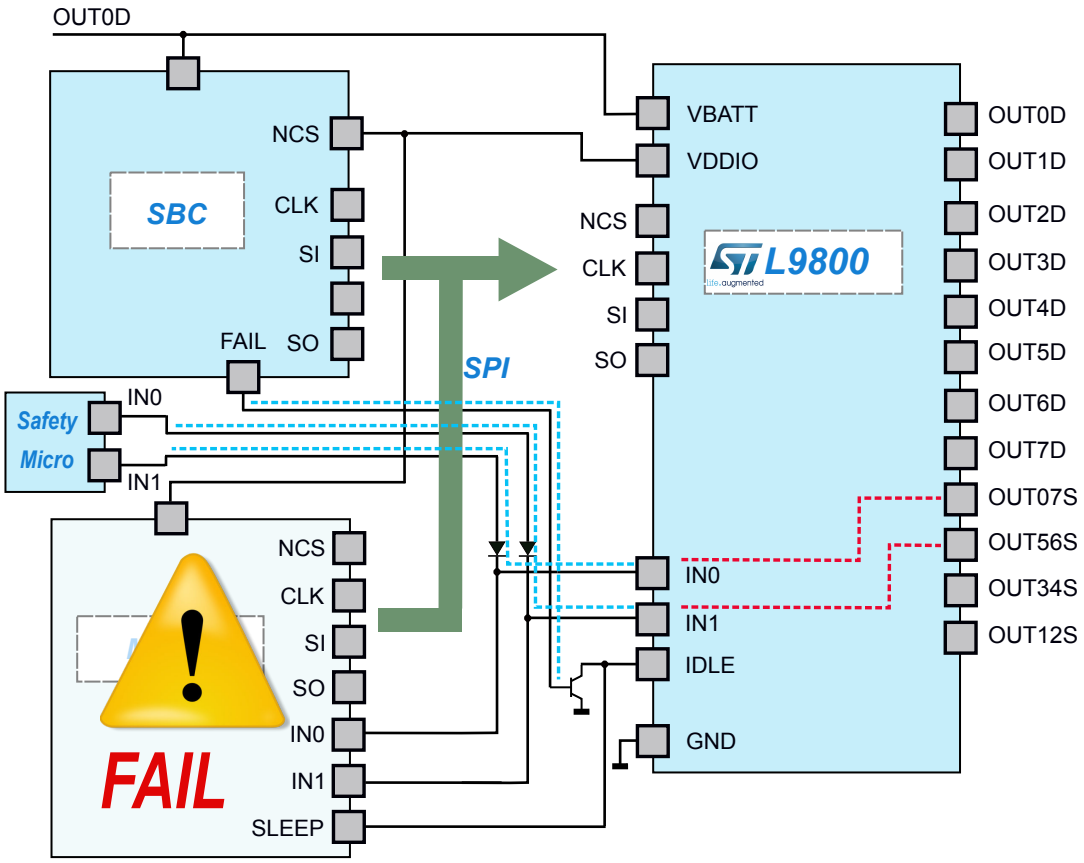


Figure 29. **Possible system configuration during limp-mode**



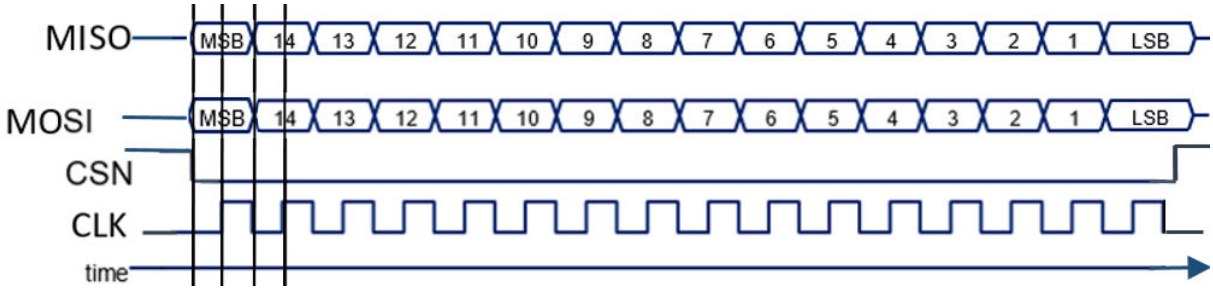
In the Figure 28 the dotted green lines mark the signals path when the device is operating in normal node, IDLE, IN0, IN1 are provided by the main MCU. The Figure 29 shows a possible limp home configuration where the dotted blue lines mark the signals path.

11 Serial peripheral interface (SPI)

The SPI (serial peripheral interface) is a full duplex serial out of frame slave interface made of four lines SO, SI, CLK and NCS. MOSI and MISO are the lines through which the data is transferred. Considering the out-of-frame protocol implemented, it is important to ignore the first MISO received at the start of communication because it is meaningless. The falling edge of NCS defines the start of the SPI frames. The L9800 samples the MOSI line (SI) at the rising edge of CLK while the output data is shifted out on line MISO (SO) at the falling edge of CLK (CPOL='0', CPHA = '0'). End of SPI access is defined by a rising edge of NCS.

The L9800 implements feature to guarantee that SPI frame is considered valid when at least 16 bits have been transferred: in case of transaction with less than 16 bits is received, the frame will be discarded and ERR bit is asserted in the next SPI frame. An SPI access with frame longer than 16 bits will not be discarded to allow daisy chain operation.

Figure 30. SPI



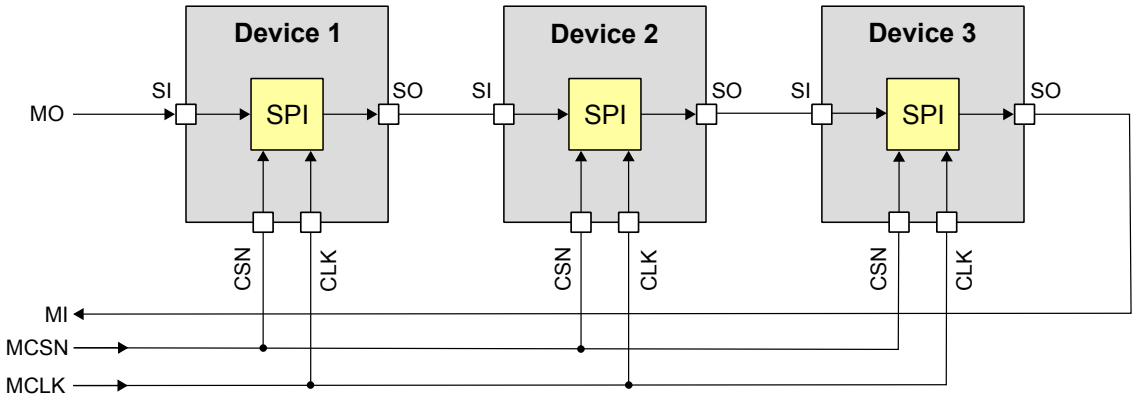
11.1 SPI signal description

- **NCS-chip select**
  The system microcontroller selects the device by means of the NCS pin. Whenever the pin is in "low" state, data transfer can take place. When NCS is in "high" state, any signals at the CLK and MOSI pins are ignored and MISO is forced into a high-Z state.
- **NCS "high" to "low" transition**
  The requested information is transferred into the shift register.
  If the device is in sleep mode, the MISO pin remains in high-Z state and no SPI transmission occurs.
- **NCS "low" to "high" transition**
  Data from the shift register is transferred into the addressed register.
- **CLK-serial clock**
  This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the rising edge of CLK while the serial output (SO) shifts diagnostic information out on the falling edge of the serial clock. It is essential that the CLK pin is in "low" state whenever chip select NCS makes any transition, otherwise the command is not accepted.
- **SI-serial input**
  Serial input data bits are shift-in at this pin, the most significant bit first. MOSI information is read on the rising edge of SCLK. The input data consists of two parts, control bits and data bits.
- **SO-serial output**
  Data is shifted out serially at this pin, the most significant bit first. MISO is in high-Z state until the NCS pin goes to "low" state. New data appears at the MISO pin following the falling edge of SCLK.

11.2 Daisy chain capability

L9800 implements SPI with daisy chain capability where a single master can address multiple slaves by driving a single NCS and MOSI lines, getting back data from a single MISO line as reported in the Figure 31, in order to build a chain. The end of the chain is connected to the output and input of the master device, MO, and MI respectively. The master device provides the master clock MCLK, which is connected to the CLK line of each device in the chain.

Figure 31. **Daisy chain**



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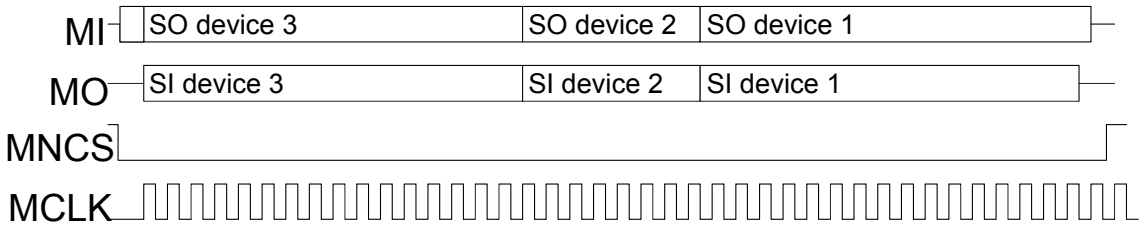
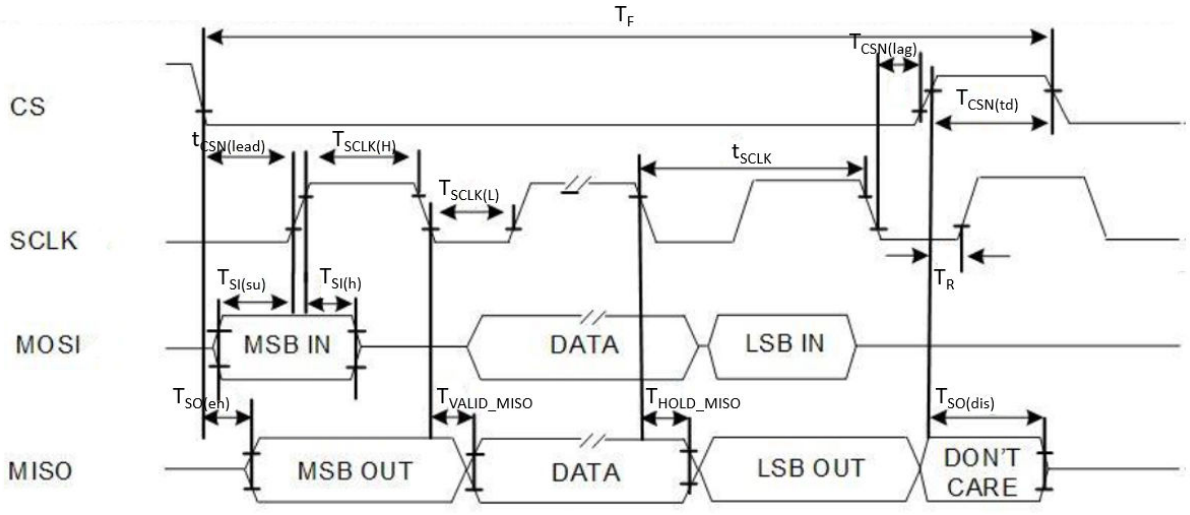
In the SPI block of each device, there is one shift register where each bit from the MOSI line is shifted in each CLK. The bit shifted out occurs at the MISO pin. After 16 CLK cycles, the data transfer for one device is finished. In single chip configuration, the NCS line must turn “high” to make the device acknowledge the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted into device 2. When using three devices in daisy chain, more than 16 bits have to be shifted through the devices (depending on how many devices are connected and how many SPI bits they have). After that, the MNCS line must turn “high” (see the Figure 32).

Figure 32. **Data transfer in daisy chain**



11.3 Timing diagrams

Figure 33. **Timing diagram**



11.4 Electrical parameters

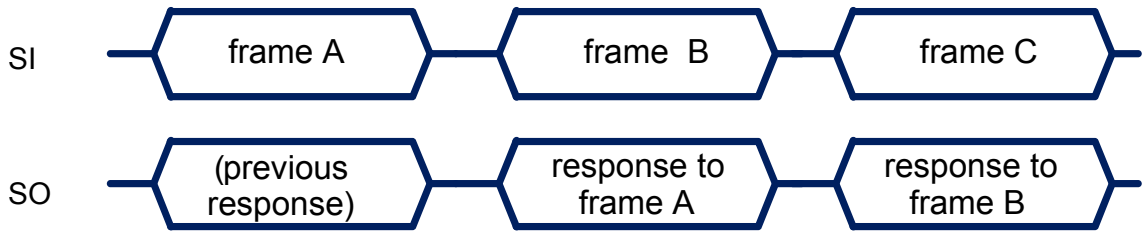
Table 17. **SPI electrical parameters**

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit
Input SPI pin characteristics–low level						
$V_{NCS(L)}$	NCS			-	0.8	V
$V_{SCLK(L)}$	CLK			-	0.8	V
$V_{SI(L)}$	SI			-	0.8	V
Input SPI pin characteristics–high level						
$V_{NCS(H)}$	NCS		2	-		V
$V_{SCLK(H)}$	SCLK		2	-		V
$V_{SI(H)}$	SI		2	-		V
Input pull-up resistor at NCS pin						
R_{NCS}	Input pull-up resistor at NCS pin	NCS = 0.8V	35	-	100	kΩ
Input pull-down resistor at pin SCLK, SI						
R_{SCLK}	Input pull-down resistor on SCLK	V_{SCLK} = 2 V	50	-	180	kΩ
R_{SI}	Input pull-down resistor on SI	V_{SI} = 2 V	50	-	180	kΩ
Output characteristic						
$V_{SO(L)}$	L level output voltage	I_{SO} = -1.5 mA	0	-	0.4	V
$V_{SO(H)}$	H level output voltage	I_{SO} = 1.5 mA	*VDDIO* - 0.4	-	VDDIO	V
$I_{SO(OFF)}$	Output tristate leakage current	VNCS = VDDIO, $VBATT_O$ = 0 V	-1	-	1	µA
$I_{SO(OFF)}$	Output tristate leakage current	VNCS = VDDIO, $VBATT_O$ = VDDIO	-1	-	1	µA
Timings						
$t_{NCS(lead)}$	Enable lead time (falling NCS to rising CLK)	VDDIO = 4.5 V or VBATT > 7 V	200	-		ns
$t_{NCS(lag)}$	Enable lag time (falling CLK to rising NCS)	VDDIO = 4.5 V or VBATT > 7 V	200	-		ns
$t_{NCS(td)}$	Transfer delay time (rising NCS to falling NCS)	VDDIO = 4.5 V or VBATT > 7 V	650	-		ns
$t_{SO(en)}$	Output enable time (falling NCS to SO valid)	VDDIO = 4.5 V or VBATT > 7 V, C_L = 20 pF at MISO pin		-	200	ns
$t_{SO(dis)}$	Output disable time (rising NCS to SO tristate)	VDDIO = 4.5 V or VBATT > 7 V, C_L = 20 pF at MISO pin		-	200	ns
f_{SCLK}	Serial clock frequency	VDDIO = 4.5 V or VBATT > 7 V		-	8	MHz
$t_{SCLK(H)}$	Serial clock “high” time	VDDIO = 4.5 V or VBATT > 7 V	45	-		ns
$t_{SCLK(L)}$	Serial clock “low” time	VDDIO = 4.5 V or VBATT > 7 V	45	-		ns
$t_{SI(su)}$	Data setup time (required time MOSI to rising CLK)	VDDIO = 4.5 V or VBATT > 7 V	30	-		ns
$t_{SI(h)}$	Data hold time (rising CLK to SI)	VDDIO = 4.5 V or VBATT > 7 V	30	-		ns

11.5 SPI protocol

The content of MOSI and MISO during SPI communication is shown in the Figure 34. MOSI line represents the frame sent from the MCU and the MISO line is the answer provided by the device.

Figure 34. Relation between MOSI and MISO



The SPI protocol provides the answer to a command frame only with the next transmission triggered by the MCU.

11.6 SPI frame structure

11.6.1 MOSI frame structure

Each MOSI frame has 16 bits with the following structure:

- A command bit R/W, ‘1’ for write, ‘0’ for read
- 5 ADDRESS bits
- 8 DATA bits
- A PARITY bit, odd parity
- A FR_CNT frame counter bit

The frame count bit (FR_CNT) is toggled at each reception of the SPI data frame. For each frame, the microcontroller has to toggle this bit into the serial IN coherently with the internal device frame counter. If the device frame counter is not consistent with the one from the microcontroller, an SPI error is generated and the frame is rejected. The same behavior is expected for serial OUT.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W[15]	ADDRESS[14:10]					DATA[9:2]								PAR[1]	FR_CNT[0]

11.6.2 MISO frame structure

Each MISO frame has 16 bits with the following structure:

- An ERR error bit, ‘1’ if an error happened in the previous transmission, ‘0’ otherwise
- 5 ADDRESS bits, for address feedback function
- 8 DATA bits
- A PARITY bit, odd parity
- A FR_CNT frame counter bit

The frame count bit (FR_CNT) is toggled at each reception of the SPI data frame. For each frame the microcontroller has to toggle this bit into the serial IN coherently with the internal device frame counter. If the device frame counter is not consistent with the one from the microcontroller, an SPI error is generated and the frame is rejected. The same behavior is expected for serial OUT.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR[15]	ADDRESS[14:10]					DATA[9:2]								PAR[1]	FR_CNT[0]

11.7 SPI registers

The register banks are composed of 8-bit registers.

Table 18. **Register addressing space**

Field name	Type	Bit offset	Bit width	Reset value	Reset source	Description
CHIP_ID, 0x00						
CHIP_ID	RO	0	8	00100010	X	8-bit chip identifier
CFG_0, 0x01						
NU	RO	6	2	0x00	X	Not used
NRES_N_EN	RW	5	1		NPOR, CFG_1.RST, VDD_UV	0 (default): NRES pin masked 1: NRES pin NOT masked (not cleared after an NRES reset)
ACTIVE TO SLEEP DIS SWR	RW	4	1	0x00	NPOR, NRES pin, CFG_1.RST, VDD_UV	0 (default): SW reset required for transition ACTIVE to SLEEP 1: SW reset NOT required for transition ACTIVE to SLEEP
RESERVED	RW	3	1	0x00	NPOR, NRES pin, CFG_1.RST, VDD_UV	Reserved
VS_UV_MASK	RW	2	1	0x00	NPOR, NRES pin, CFG_1.RST, VDD_UV	0 (default): VBATT UV not masked 1: VBATT UV masked but STA_1 diag bit still working
DIS_EN	RW	1	1	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	0: (default) DIS pin masked 1: DIS pin not masked
NRES_EN	RW	0	1	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	0 (default): NRES pin masked 1: NRES pin not masked
CFG_1, 0x02						
RST	WO	7	1	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	Reset: 0: (default) normal operation 1: Execute reset command (self-clearing)
ACT	RW	6	1	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	Active mode: 0: (default) normal operation or device leaves active mode 1: device enters active mode
NU	RO	2	4	0x00	X	
PWM_DIV_LED	RW	0	2	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	Clock division factor for PWM LED generator PWM frequency: 00 (default): PWM_FRQ = 122 Hz 01: PWM_FRQ = 244 Hz 10: PWM_FRQ = 488 Hz 11: PWM_FRQ = 976 Hz
CFG_2, 0x03						
NU	RO	6	2	0x00	X	
RESERVED	RW	4	2	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	Reserved
FR_ADJ	RW	2	2	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	PWM generator and LED frequency adjustment bit (15% of selected frequency): 00: no frequency adjustment 01: -15% on selected frequency 10: +15% on selected frequency 11: no frequency adjustment

Field name	Type	Bit offset	Bit width	Reset value	Reset source	Description
PWM_DIV_GEN	RW	0	2	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	Clock division factor for PWM GEN generator PWM frequency: 00 (default): PWM_FRQ = 122 Hz 01: PWM_FRQ = 244 Hz 10: PWM_FRQ = 488 Hz 11: PWM_FRQ = 976 Hz
BIM, 0x04						
OUTn	RW	0	8	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	Driver bulb inrush mode for n = 0 to 7: 0 (default): output latches OFF in case of overcurrent or overtemperature 1: output restarts automatically in case of overcurrent or overtemperature BIM.OUTn bits are set back to “0” at the end of BIM time(t_{BIM})
RESERVED_1, 0x05						
UNUSED	RO	0	8	0x00	X	
PWM_SPI, 0x06						
OUTn	RW	0	8	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	Power output control register for n = 0 to 7: 0 (default): output is OFF 1: Output is ON
MAP_IN0, 0x07						
OUTn	RW	0	8	0x04	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	0: OUTn not driven by IN0 1: OUTn driver by IN0 (by default OUT2 connected to IN0)
MAP_IN1, 0x08						
OUTn	RW	0	8	0x08	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	0: OUTn not driven by IN1 1: OUTn driver by IN1 (by default OUT3 connected to IN1)
MAP_PWM, 0x09						
OUTn	RW	0	8	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	0 (default): OUTn not driven by PWM generators 1: OUTn driven by PWM generators
PWM_SEL, 0x0A						
OUTn	RW	0	8	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	0 (default): OUTn driven by PWM_GEN 1: OUTn driven by PWM_LED
PWM_GEN_DC, 0x0B						
DUTY_CYCLE	RW	0	8	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	PWM_GEN duty cycle setting: b00000000: PWM generator is OFF b11111111: PWM generator is ON (100% duty cycle)
PWM_LED_DC, 0x0C						
DUTY_CYCLE	RW	0	8	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	PWM_LED duty cycle setting: b00000000: PWM generator is OFF b11111111: PWM generator is ON (100% duty cycle)

Field name	Type	Bit offset	Bit width	Reset value	Reset source	Description
DIAG_OFF_EN, 0x0D						
OUTn	RW	0	8	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	Activation of driver load diagnosis in off state for n = 0 to 7: 0 (default): diagnosis not active 1: diagnosis active, DIAG_OFF_EN.OUTn bits are set back to ”0” at the end of the diagnosis cycle
RESERVED_2, 0x0E						
UNUSED	RO	0	8	0x00	X	
DIAG_OVC_OVT_RLW, 0x0F						
OUTn	WO	0	8	0x00	NPOR, NRES pin, CFG_1.RST bit, VDD_UV	Clear on write for overcurrent and overtemperature error for n = 0 to 7: 0 (default): not active 1: active
STA_0, 0x010						
NU	RO	7	1	0x00	X	
DIS	RO	6	1	0x00	NPOR	Status of DIS input (if properly configured)
NRES_N	RO	5	1	0x00	NPOR	Status of NRES input (if properly configured)
IDLE	RO	4	1	0x00	NPOR	Status of IDLE input
IN1	RO	3	1	0x00	NPOR	Status of IN1 input
IN0	RO	2	1	0x00	NPOR	Status of IN0 input
OUT_ON_ERR	RLR	1	1	0x00	NPOR	0: normal load 1: overcurrent or overtemperature detected
OUT_OFF_ERR	RLR	0	1	0x00	NPOR	0: normal load 1: open load in off state or short load detected
STA_1, 0x11						
NU	RO	5	3	0x00	X	
POR	RLR	4	1	0x01	NPOR	0: NPOR condition not detected 1: NPOR condition detected
VDDIO_UV	RLR	3	1	0x00	NPOR	0: battery undervoltage not detected 1: battery undervoltage detected
VBATT_UV	RLR	2	1	0x00	NPOR	0: battery undervoltage not detected 1: battery undervoltage detected
MODE	RO	0	2	0x00	NPOR	Status of operating mode: 00: Sleep mode 01: Limp-home mode 10: Idle mode 11: Active mode
DIAG_OVC_OVT, 0x12						
OUTn	RLW	0	8	0x00	NPOR	Driver overcurrent or overtemperature detection n = 0 to 7: 0 (default): normal load 1: overcurrent or overtemperature detected

Field name	Type	Bit offset	Bit width	Reset value	Reset source	Description
DIAG_OPL_OFF, 0x13						
OUTn	RLR	0	8	0x00	NPOR	Driver open-load detection in off state n = 0 to 7: 0 (default): normal load 1: open-load detected
RESERVED_3, 0x14						
UNUSED	RO	0	8	0x00	X	
DIAG_SHG, 0x15						
OUTn	RLR	0	8	0x00	NPOR	Driver short load detection in off state n = 0 to 7: 0 (default): normal load 1: short load detected
RESERVED_4, 0x16						
UNUSED	RO	0	8	0x00	X	
RESERVED_5, 0x17						
UNUSED	RO	0	8	0x00	X	

12 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

12.1 TFQFN24 4x4x0.9 wettable flanks package information

Figure 35. TFQFN24 4x4x0.9 wettable flanks package dimension

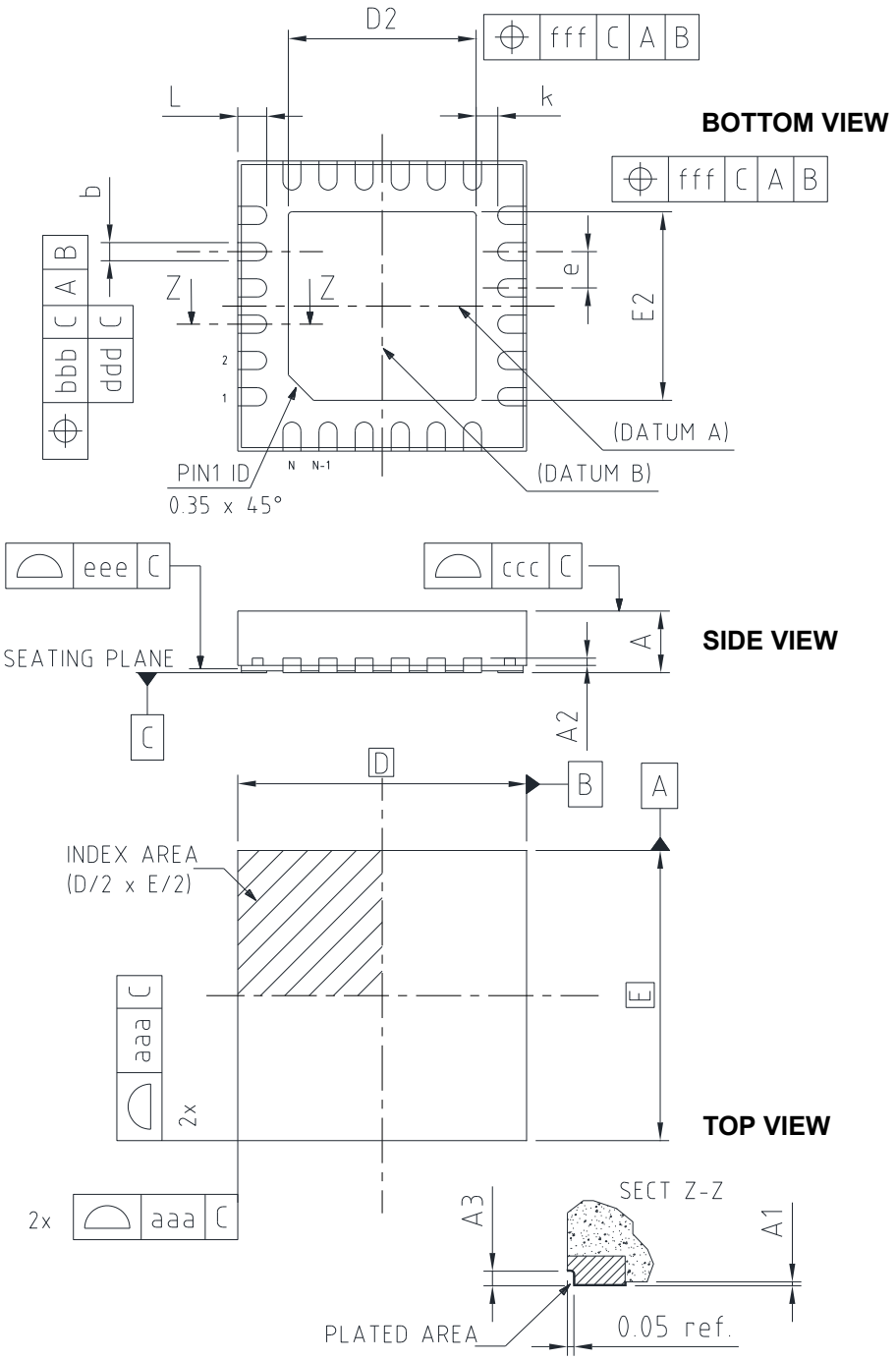


Table 19. TFQFN24 4x4x0.9 wettable flanks mechanical data

Symbol	Dimensions		
	Min.	Typ.	Max.
A(1)	0.80	0.90	1.00
A1(2)	0.00	0.02	0.05
A2		0.20 REF	
A3	0.1		
b(1)(3)	0.20	0.25	0.30
D(1)		4.00	
D2	2.75	2.80	2.85
e(1)		0.50	
E(1)		4.00	
E2	2.75	2.80	2.85
L(1)	0.35	0.40	0.45
k	0.25		
N(4)		24	
Form and position tolerances			
aaa(1)(5)		0.15	
bbb(1)(5)		0.10	
ccc(1)(5)		0.08	
ddd(1)(5)		0.05	
eee(1)(5)		0.10	

1. *To be determined at setting datum plane C.*
2. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
3. *Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.*
4. *“N” is the maximum number of terminal positions for the specified body size.*
5. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*

Revision history

Table 20. **Document revision history**

Date	Revision	Changes
08-Jan-2024	1	Initial release.

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