F1485

High Gain RF Amplifier 2.3GHz to 5.0GHz

The F1485 is a high-gain RF amplifier designed to operate within the 2.3GHz to 5.0GHz frequency range. Using a 5V power supply, the F1485 provides 36.5dB gain, 3.8dB of noise figure, and 27dBm OP1dB at 3.6GHz.

The F1485 is packaged in a 3 × 3 mm, 16-VFQFPN package, with matched 50Ω input and output impedances for ease of integration into the signal path.

Competitive Advantage

- Superior gain flatness
- High linearity
- Combines a multi-stage RF amplifier in a single, compact 3 × 3 mm package
- Excellent performance over exceptionally wide bandwidths
- Excellent ACLR performance

Applications

- 5G sub-6GHz massive MIMO
- Wireless infrastructure base stations
- FDD or TDD systems
- Public safety infrastructure
- Military handhelds
- Repeaters and DAS
- General-purpose RF

Features

- Frequency range: 2.3GHz to 5.0GHz
- 36.5dB typical gain at 3.6GHz
- 3.8dB typical NF at 3.6GHz
- 27dBm typical OP1dB at 3.6GHz
- -41dBc ACLR with LTE-TDD 20MHz signal at Pout = 15dBm average, 8dB PAR at 0.01% probability at 3.6GHz
- 50Ω single-ended input and output impedances
- 5V power supply
- 110mA typical quiescent current consumption
- 1.8V logic compatible Standby Mode for power savings
- Operating temperature (T_{EPAD}) range: -40°C to +115°C
- 3 × 3 mm 16-VFQFPN package

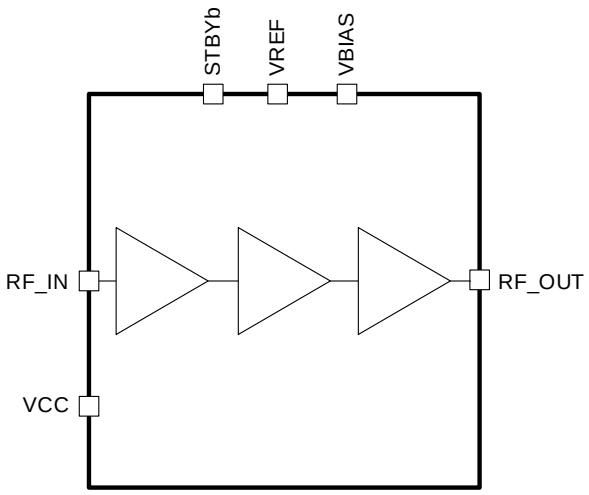

Figure 1. Block Diagram

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1. Pin Information

1.1 Pin Assignments

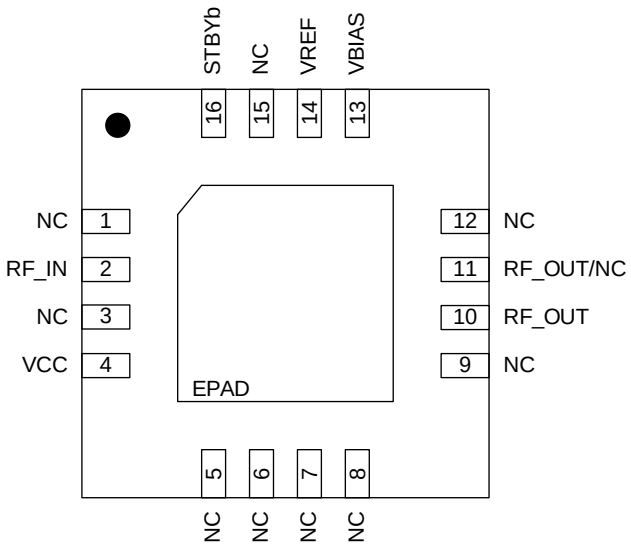


Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Number	Name	Description
1, 3, 5, 6, 7, 8, 9, 12, 15	NC	No internal connection. These pins can be left unconnected or connected to ground, but it is ideal that all NC pins be grounded similar to the F1485 EVK design to ensure optimal RF performance (for grounding recommendations and Application information for layout guidelines, see “Evaluation Kit Circuit” section).
2	RF_IN	RF input internally matched to 50Ω. Must use an external DC block.
4	VCC	Connect pin directly to VCC. Renesas recommends placing a decoupling capacitor as close to this pin as possible.
10	RF_OUT	RF output. Pull up to VCC through an inductor. Must use an external DC block.
11	RF_OUT/NC	No internal connection, but can be connected to RF_OUT for specific product layout compatibility.
13	VBIAS	Connect pin directly to VCC. Renesas recommends placing a decoupling capacitor as close to this pin as possible.
14	VREF	Connect using a resistor to a common VCC and use a bypass capacitor. Place network as close to the pin as possible.
16	STBYb	Standby pin. With Logic LOW applied to this pin, the amplifier is powered off. With Logic HIGH or no connect (NC) applied to this pin, the part is in full operation mode. If standby functionality is not required, it is recommended that this pin be tied to logic HIGH.
-	EPAD	Exposed Pad. Internally connected to ground. Solder this exposed pad to a PCB pad. Maximize the number of ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the noted RF performance.

2. Specifications

2.1 Absolute Maximum Ratings

Stresses above those listed below can cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Parameter	Symbol	Minimum	Maximum	Unit
V_{CC} to GND	V_{CC}	-0.3	6.0	V
STBYb	V_{STBYb}	-0.3	V_{CC}	V
RFIN Externally applied DC Voltage	V_{RFIN}	-	2.0	V
RFOUT Externally applied DC Voltage	V_{RFOUT}	-	6.0	V
Maximum CW Input Power applied for 24 hours. V_{CC} = 5V, T_{EPAD} = 115°C, input/output VSWR < 2:1 based on a 50Ω system. Standby = logic HIGH: ON state. [1]	$P_{MAX\_IN\_ON}$	-	+10	dBm
Maximum CW Input Power applied for 24 hours. V_{CC} = 5V, T_{EPAD} = 115°C, input/output VSWR < 2:1 based on a 50Ω system. Standby = logic LOW: OFF state. [1]	$P_{MAX\_IN\_OFF}$	-	+10	dBm

1. Exposure to these maximum RF levels can result in significant I_{CC} current draw because of overdriving the amplifier stages.

2.2 ESD Ratings

ESD Model/Test	Value	Unit
Human Body Model (Tested per JS-001)	1500	V
Charged Device Model (Tested per JESD22-C101)	750	V

2.3 Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Voltage	V_{CC}	-	4.75	5	5.25	V
Operating Temperature Range	T_{EPAD}	Exposed paddle	-40	-	+115	°C
RF Frequency Range [1]	f_{RF}	2.5GHz tuning set	2.3	-	2.7	GHz
		3.8GHz tuning set	3.3	-	4.2	GHz
		4.7GHz tuning set	4.4	-	5.0	GHz
RFIN Port Impedance	Z_{RFI}	Single-ended	-	50	-	Ω
RFOUT Port Impedance	Z_{RFO}	Single-ended	-	50	-	Ω

1. Using external matching, RF performance is optimized from 2.3GHz to 2.7GHz (2.5GHz Tuning Set), 3.3GHz to 4.2GHz (3.8GHz Tuning Set), and 4.4GHz to 5.0GHz (4.7GHz Tuning Set).

2.4 Thermal Specifications

Thermal Resistance (Typical)	θ_{JA} (°C/W) [1]	θ_{JC} (°C/W) [1]
16-VFQFPN Package, 3 × 3 mm	87.9	29.4

1. Case is defined as the exposed paddle.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-	180	°C
Maximum Storage Temperature Range	-65	+150	°C
Lead Temperature (soldering, 10s)	-	+260	°C

2.5 Electrical Specifications

2.5.1. General

Specifications apply when operated as an amplifier with V_{CC} = V_{BIAS} = V_{REF} = +5.0V, T_{EPAD} = +25°C, STBYb = HIGH, Z_S = Z_L = 50Ω, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
DC Characteristics						
Logic Input High	V_{IH}	-	***1.07*** [1]	-	Vcc	V
Logic Input Low	V_{IL}	-	-0.3	-	***0.67***	V
Logic Current	I_{IH}, I_{IL}	STBYb pin. V_{STBYb} = 1.8V	***-150***	-	***150***	µA
Quiescent Current [2]	I_{CCQ}	3.8GHz tuning set	-	110	***140***	mA
Standby Current	I_{CC_STBY}	STBYb = LOW	-	3.7	-	mA
Transient Characteristics						
Standby Switching Time [3]	t_{ON}	50% STBYb control to within 0.2dB of the on-state final gain value	-	-	800	ns
	t_{OFF}	50% STBYb control to -25dB below the on-state final gain value	-	-	800	ns

1. Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.
2. I_{CCQ} refers to the nominal small signal bias current.
3. Assumes the control signal is clean and no external RC circuitry is required on the pin. Adding RC circuitry increases switching time. Timing tests performed with a control logic signal level high of +1.8V and a rise and fall time ≤ 30ns.

2.5.2. 2300MHz to 2700MHz Tune

Specifications apply when operated as an amplifier with tuning optimized for 2300MHz – 2700MHz band, $V_{CC} = V_{BIAS} = V_{REF} = +5.0V$, f_{RF} = 2600MHz, T_{EPAD} = +25°C, STBYb = HIGH, $Z_S = Z_L = 50\Omega$, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	-	-	36.5	-	dB
Gain Flatness	G_{FLAT}	f_{RF} = 2300MHz to 2700MHz	-	0.25	-	dB
Gain Variation Over Temperature	G_{TEMP}	T_{EPAD} = -40°C to +115°C, referenced to T_{EPAD} = 25°C	-	+1/-1.7	-	dB
STBY Mode Gain	G_{STBY}	STBYb = logic LOW $P_{IN} \leq$ -15dBm f_{RF} = 2300MHz to 2700MHz	-	-50	-	dB
RF Input Return Loss	RL_{RFIN}	f_{RF} = 2300MHz to 2700MHz	10	-	-	dB
RF Output Return Loss	RL_{RFOUT}	f_{RF} = 2300MHz to 2700MHz	11	-	-	dB
Reverse Isolation	ISO_{REV}	f_{RF} = 2300MHz to 2700MHz	-	57	-	dB
Noise Figure	NF	-	-	4.5	-	dB
Output Third Order Intercept Point	OIP3	Pout = 12dBm/tone 1MHz tone separation	-	33	-	dBm
Output 1dB Compression Point	OP1dB	-	-	29	-	dBm
ACLR [2]	$ACLR_{5G\text{-}NR}$	5G NR 100MHz	-	-42	-	dBc
	$ACLR_{LTE}$	LTE-TDD 20MHz	-	-44	-	dBc
Stability K-Factor	K_{FACT}	f_{RF} = Up to 20GHz Vcc = +4.75V to +5.25V $V_{CC} = V_{BIAS} = V_{REF}$ T_{EPAD} = -40°C to +115°C	1	-	-	-

1. Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.
2. Pout = 15dBm, 8dB PAR, Probability = 0.01%.

2.5.3. 3300MHz to 3800MHz Tune

Specifications apply when operated as an amplifier with tuning optimized for 3300MHz – 3800MHz band, $V_{CC} = V_{BIAS} = V_{REF} = +5.0V$, $f_{RF} = 3600MHz$, $T_{EPAD} = +25°C$, STBYb = HIGH, $Z_S = Z_L = 50\Omega$, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	-	-	36.5	-	dB
		V_{CC} = 4.75V to 5.25V $V_{CC} = V_{BIAS} = V_{REF}$ T_{EPAD} = -40°C to +115°C f_{RF} = 3300MHz – 3800MHz	33	-	-	dB
Gain Flatness	G_{FLAT}	f_{RF} = 3300MHz – 3800MHz	-	0.1	-	dB
Gain Variation Over Temperature	G_{TEMP}	T_{EPAD} = -40°C to +115°C, referenced to T_{EPAD} = 25°C f_{RF} = 3300MHz – 3800MHz	-	+0.8/-1.6	-	dB
STBYb Mode Gain	G_{STBY}	STBYb = logic LOW $P_{IN} \leq$ -15dBm f_{RF} = 3300MHz – 3800MHz	-	-42	-	dB
RF Input Return Loss	RL_{RFIN}	f_{RF} = 3300MHz – 3800MHz	15	-	-	dB
RF Output Return Loss	RL_{RFOUT}	f_{RF} = 3300MHz – 3800MHz	14	-	-	dB
Reverse Isolation	ISO_{REV}	f_{RF} = 3300MHz – 3800MHz	-	54	-	dB
Noise Figure	NF	-	-	3.8	-	dB
Output Third Order Intercept Point	OIP3	Pout = 12dBm/tone 1MHz tone separation	-	32	-	dBm
		Pout = 12dBm/tone 1MHz tone separation V_{CC} = 4.75V to 5.25V $V_{CC} = V_{BIAS} = V_{REF}$ T_{EPAD} = -40°C to +115°C f_{RF} = 3300MHz – 3800MHz	28	-	-	dBm
Output 1dB Compression Point	OP1dB	-	-	27	-	dBm
		V_{CC} = 4.75V to 5.25V $V_{CC} = V_{BIAS} = V_{REF}$ T_{EPAD} = -40°C to +115°C f_{RF} = 3300MHz – 3800MHz	24.8	-	-	dBm
ACLR [2]	$ACLR_{5G-NR}$	5G NR 100MHz	-	-40	-	dBc
	$ACLR_{LTE}$	LTE-TDD 20MHz	-	-41	-	dBc
Stability K-Factor	K_{FACT}	f_{RF} = Up to 20GHz Vcc = +4.75V to + 5.25V $V_{CC} = V_{BIAS} = V_{REF}$ T_{EPAD} = -40°C to +115°C	1	-	-	-

1. Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.
2. Pout = 15dBm, 8dB PAR, Probability = 0.01%.

2.5.4. 3800MHz to 4200MHz Tune

Specifications apply when operated as an amplifier with tuning optimized for 3800MHz – 4200MHz band, V_{CC} = V_{BIAS} = V_{REF} = +5.0V, f_{RF} = 4000MHz, T_{EPAD} = +25°C, STBYb = HIGH, Z_S = Z_L = 50Ω, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	-	-	36.5	-	dB
Gain Flatness	G_{FLAT}	f_{RF} = 3800MHz – 4200MHz	-	0.4	-	dB
Gain Variation Over Temperature	G_{TEMP}	T_{EPAD} = -40°C to +115°C, referenced to T_{EPAD} = 25°C f_{RF} = 3800MHz – 4200MHz	-	+1/-2.1	-	dB
STBYb Mode Gain	G_{STBY}	STBYb = logic LOW P_{IN} ≤ -15dBm f_{RF} = 3800MHz – 4200MHz	-	-41	-	dB
RF Input Return Loss	RL_{RFIN}	f_{RF} = 3800MHz – 4200MHz	12	-	-	dB
RF Output Return Loss	RL_{RFOUT}	f_{RF} = 3800MHz – 4200MHz	11	-	-	dB
Reverse Isolation	ISO_{REV}	f_{RF} = 3800MHz – 4200MHz	-	53	-	dB
Noise Figure	NF	-	-	3.8	-	dB
Output Third Order Intercept Point	OIP3	Pout = 12dBm/tone 1MHz tone separation	-	31	-	dBm
Output 1dB Compression Point	OP1dB	-	-	26.5	-	dBm
ACLR [2]	$ACLR_{5G-NR}$	5G NR 100MHz	-	-38	-	dBc
	$ACLR_{LTE}$	LTE-TDD 20MHz	-	-40	-	dBc
Stability K-Factor	K_{FACT}	f_{RF} = Up to 20GHz Vcc = +4.75V to + 5.25V V_{CC} = V_{BIAS} = V_{REF} T_{EPAD} = -40°C to +115°C	1	-	-	-

1. Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.
2. Pout = 15dBm, 8dB PAR, Probability = 0.01%.

2.5.5. 4400MHz to 5000MHz Tune

Specifications apply when operated as an amplifier with tuning optimized for 4400MHz – 5000MHz band, $V_{CC} = V_{BIAS} = V_{REF} = +5.0V$, $f_{RF} = 4900MHz$, $T_{EPAD} = +25°C$, STBYb = HIGH, $Z_S = Z_L = 50\Omega$, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	-	-	35.5	-	dB
Gain Flatness	G_{FLAT}	f_{RF} = 4400MHz – 5000MHz	-	2.8 [2]	-	dB
Gain Variation Over Temperature	G_{TEMP}	T_{EPAD} = -40°C to +115°C, referenced to T_{EPAD} = 25°C 4400MHz – 5000MHz	-	+1.6/-3.1	-	dB
STBYb Mode Gain	G_{STBY}	STBYb = logic LOW $P_{IN} \le$ -15dBm f_{RF} = 4400MHz – 5000MHz	-	-42	-	dB
RF Input Return Loss	RL_{RFIN}	f_{RF} = 4400MHz – 5000MHz	10	-	-	dB
RF Output Return Loss	RL_{RFOUT}	f_{RF} = 4400MHz – 5000MHz	8	-	-	dB
Reverse Isolation	ISO_{REV}	f_{RF} = 4400MHz – 5000MHz	-	49	-	dB
Noise Figure	NF	-	-	3.7	-	dB
Output Third Order Intercept Point	OIP3	Pout = 12dBm/tone 1MHz tone separation	-	33	-	dBm
Output 1dB Compression Point	OP1dB	-	-	27.5	-	dBm
ACLR [3]	$ACLR_{5G-NR}$	5G NR 100MHz	-	-40	-	dBc
	$ACLR_{LTE}$	LTE-TDD 20MHz	-	-42	-	dBc
Stability K-Factor	K_{FACT}	f_{RF} = Up to 20GHz Vcc = +4.75V to + 5.25V $V_{CC} = V_{BIAS} = V_{REF}$ T_{EPAD} = -40°C to +115°C	1	-	-	-

1. Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.
2. Gain Flatness can be improved in the 4.6GHz to 5GHz frequency range with a different tuning set.
3. Pout = 15dBm, 8dB PAR, Probability = 0.01%.

3. Typical Operating Conditions

Unless otherwise stated, the typical operating graphs were measured under the following conditions:

- $V_{CC} = V_{BIAS} = V_{REF} = +5.0V$
- STBYb = HIGH
- $T_{EPAD} = +25°C$
- $f_{RF} = 2.6GHz$
- $f_{RF} = 3.6GHz$
- $f_{RF} = 4.0GHz$
- $f_{RF} = 4.9GHz$
- $Z_S = Z_L = 50\Omega$ Single-ended
- Pout = 12dBm/tone and 1MHz Tone Spacing for OIP3
- Pout = 15dBm, 8dB PAR, Probability = 0.01% for ACLR

4. Typical Performance Characteristics

4.1 2300MHz to 2700MHz Low-Band Performance

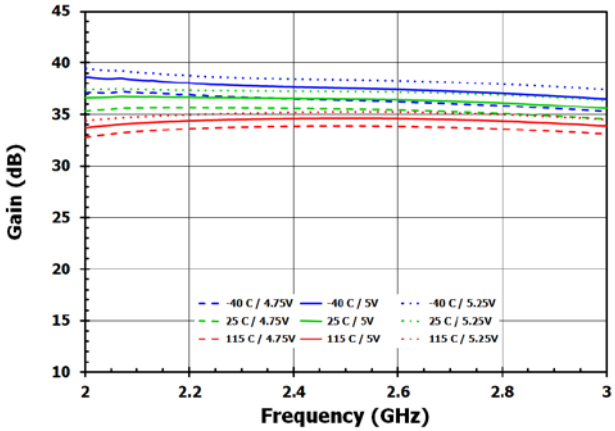


Figure 3. Gain

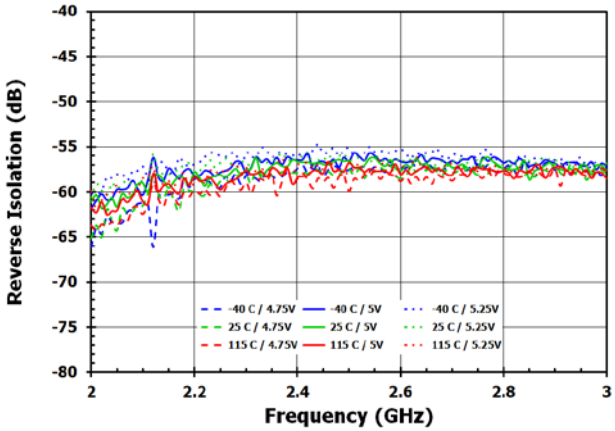


Figure 4. Reverse Isolation

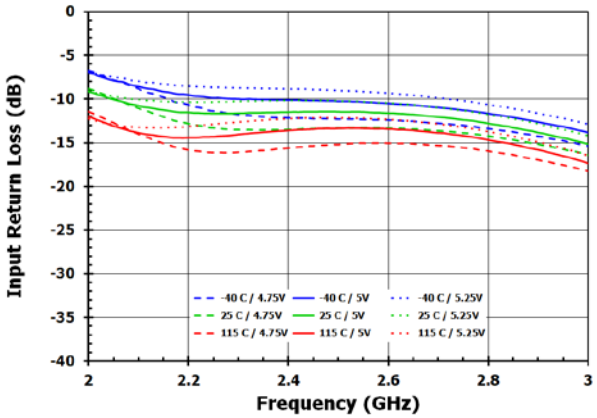


Figure 5. Input Return Loss

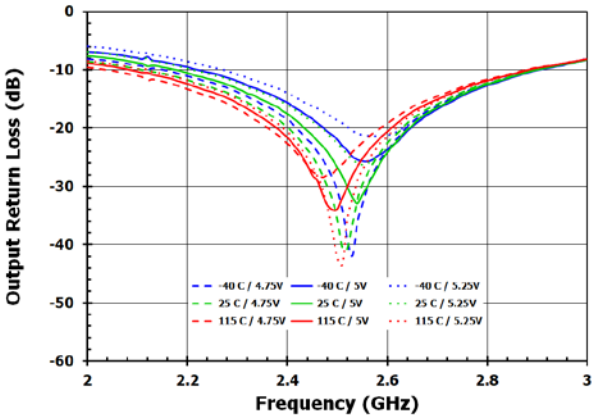


Figure 6. Output Return Loss

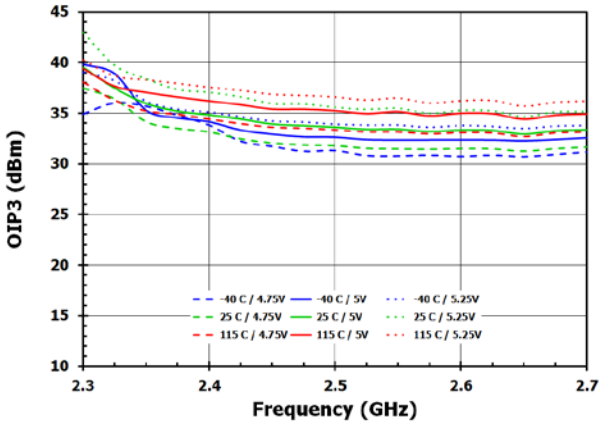


Figure 7. OIP3

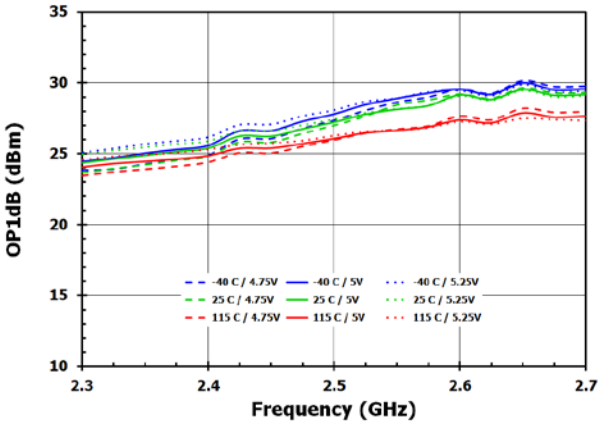


Figure 8. OP1dB

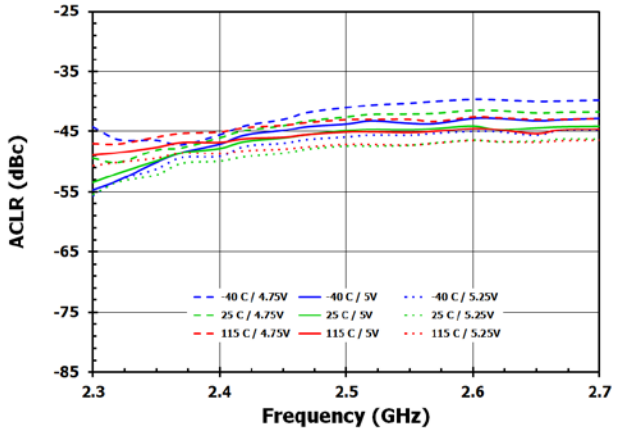


Figure 9. ACLR – LTE (20MHz)

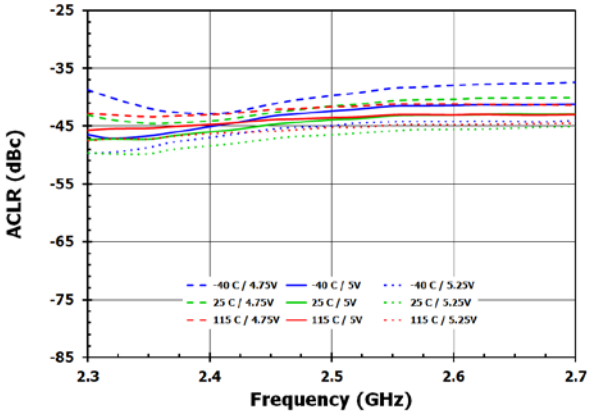


Figure 10. ACLR – 5G NR (100MHz)

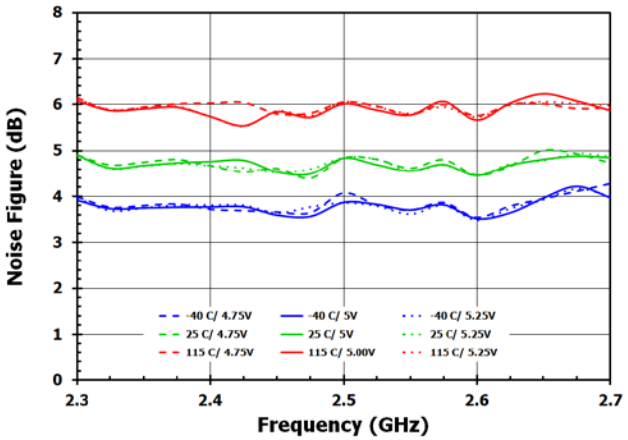


Figure 11. Noise Figure

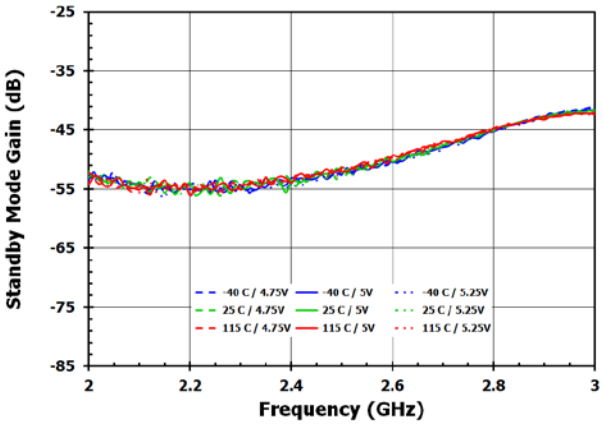


Figure 12. STBYb Gain

4.2 3300MHz to 3800MHz Mid-Band Performance

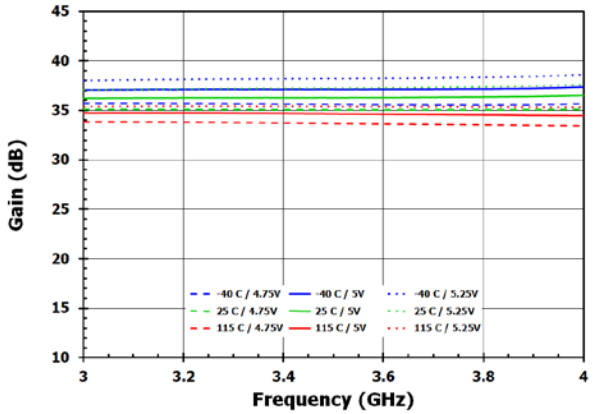


Figure 13. Gain

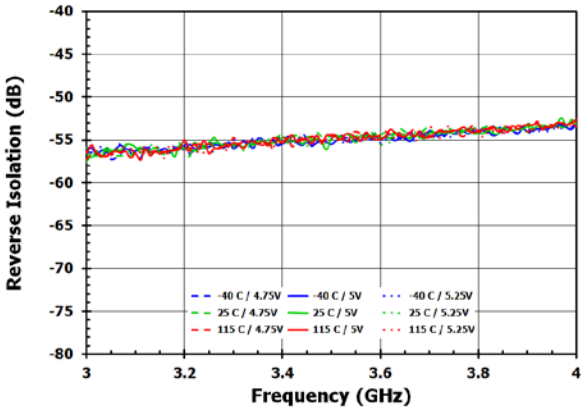


Figure 14. Reverse Isolation

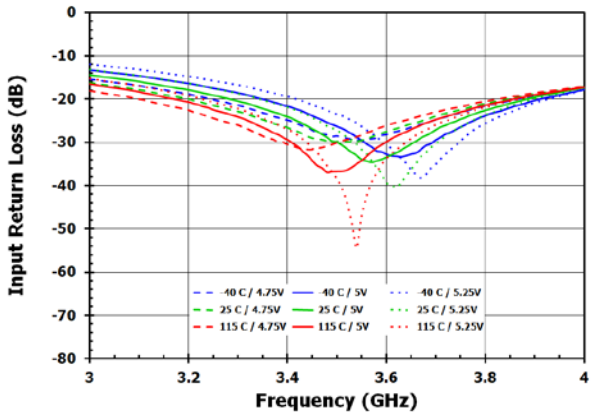


Figure 15. Input Return Loss

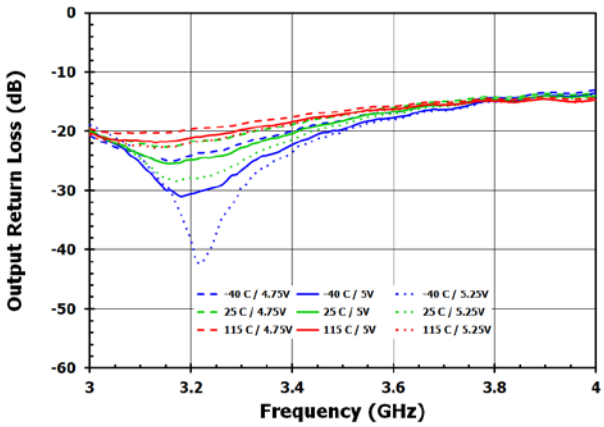


Figure 16. Output Return Loss

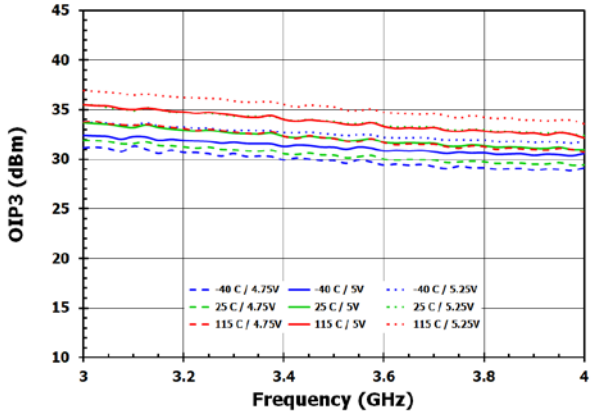


Figure 17. OIP3

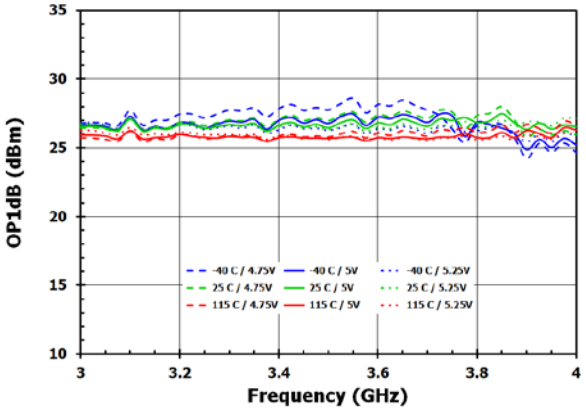


Figure 18. OP1dB

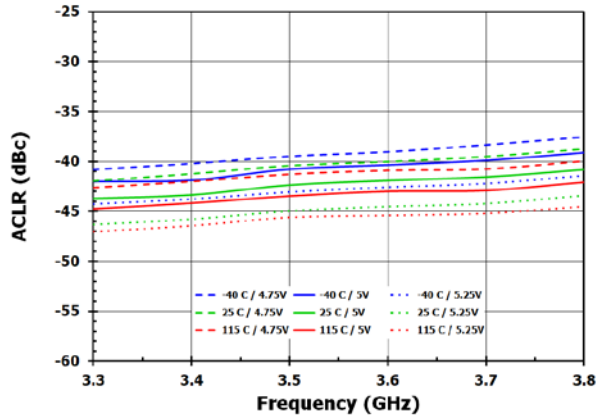


Figure 19. ACLR – LTE (20MHz)

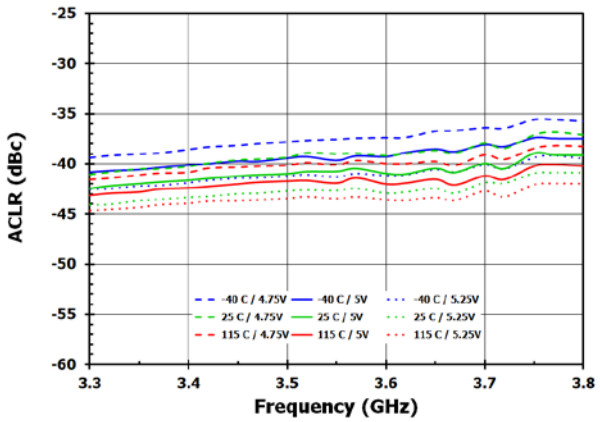


Figure 20. ACLR – 5G NR (100MHz)

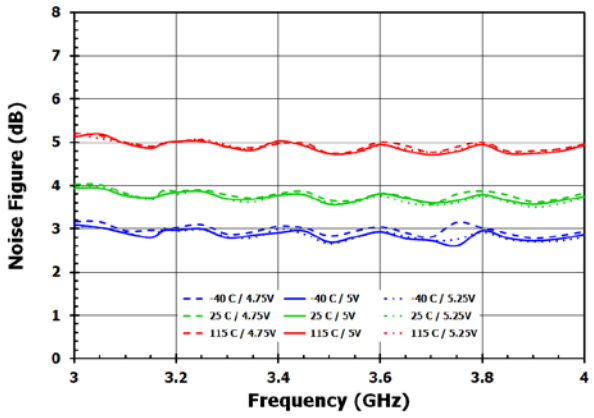


Figure 21. Noise Figure

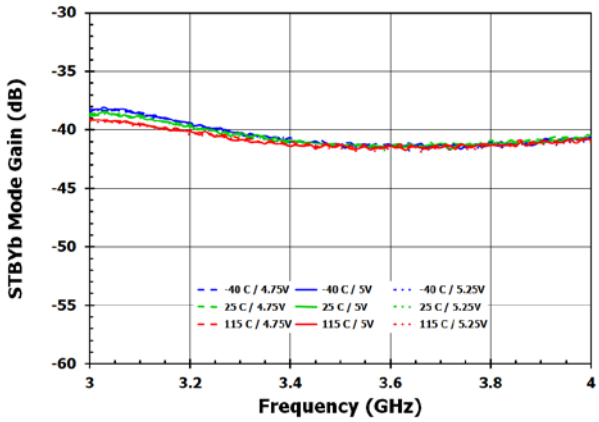


Figure 22. STBYb Gain

4.3 3800MHz to 4200MHz Mid-Band Performance

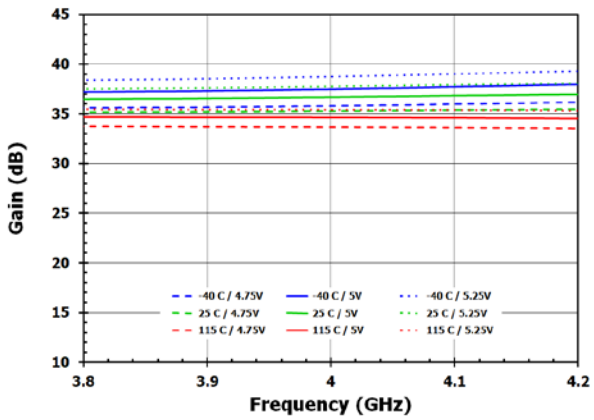


Figure 23. Gain

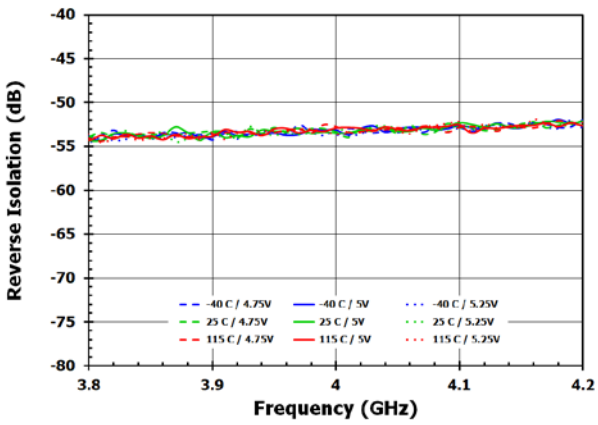


Figure 24. Reverse Isolation

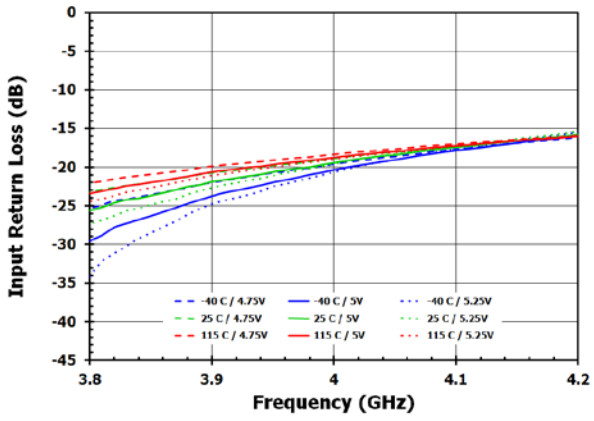


Figure 25. Input Return Loss

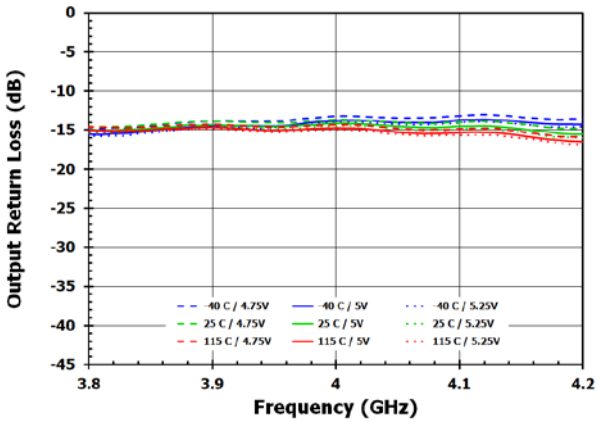


Figure 26. Output Return Loss

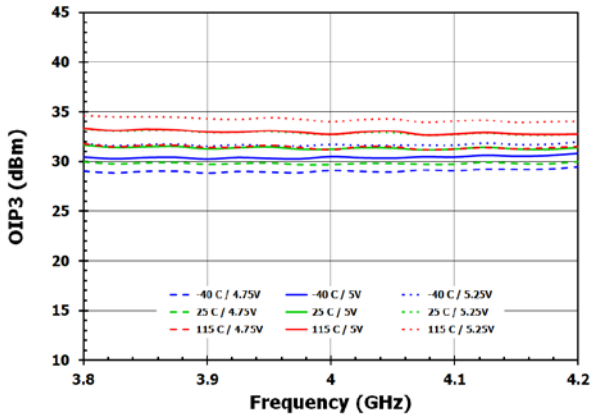


Figure 27. OIP3

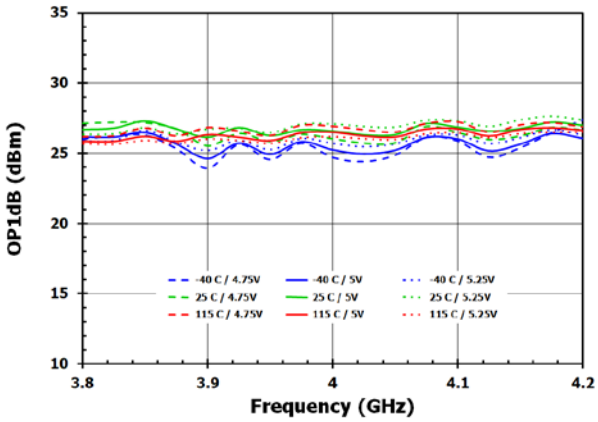


Figure 28. OP1dB

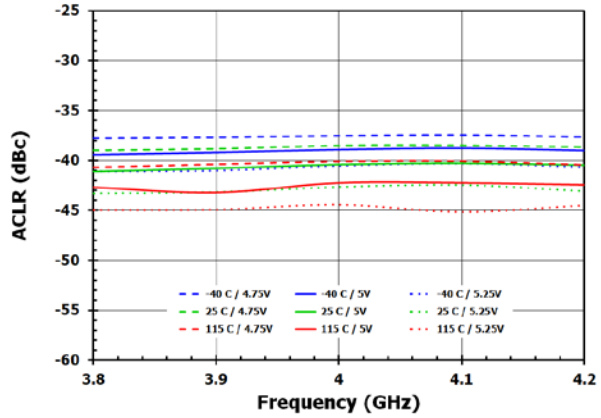


Figure 29. ACLR – LTE (20MHz)

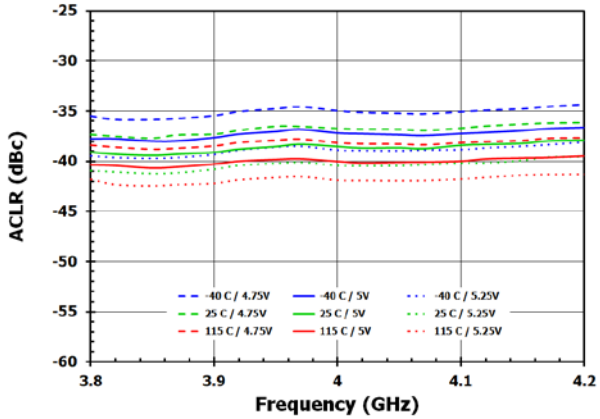


Figure 30. ACLR – 5G NR (100MHz)

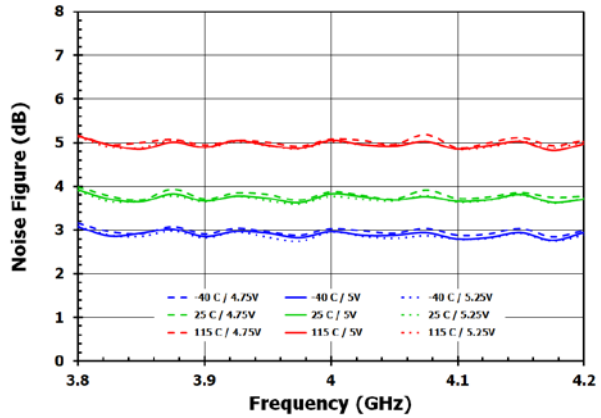


Figure 31. Noise Figure

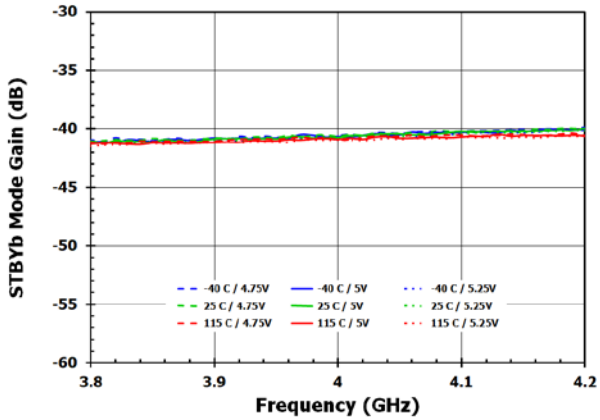


Figure 32. STBYb Gain

4.4 4400MHz to 5000MHz High-Band Performance

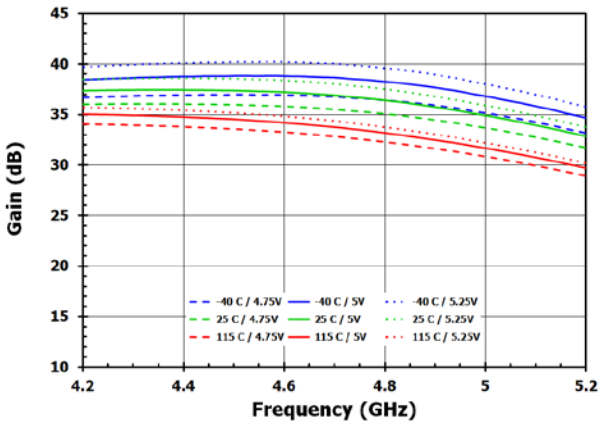


Figure 33. Gain

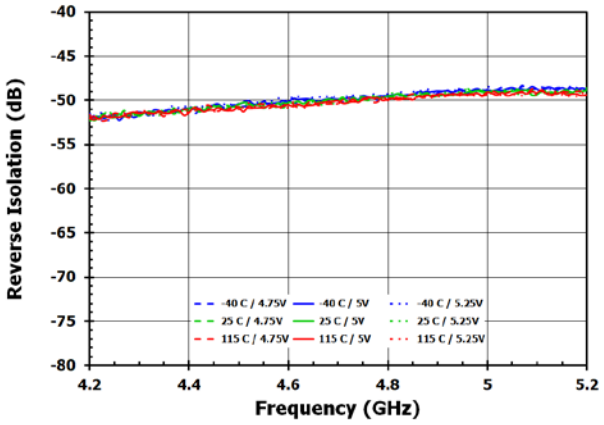


Figure 34. Reverse Isolation

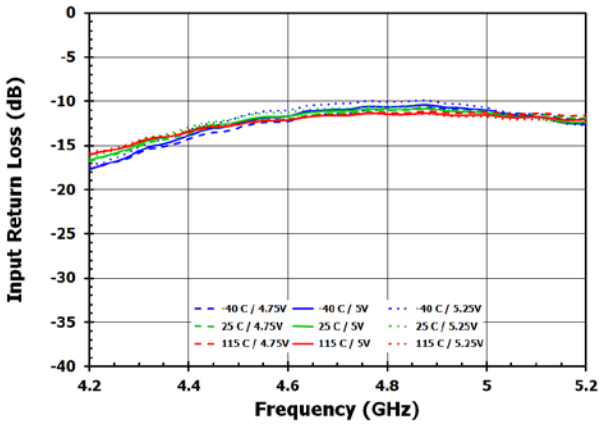


Figure 35. Input Return Loss

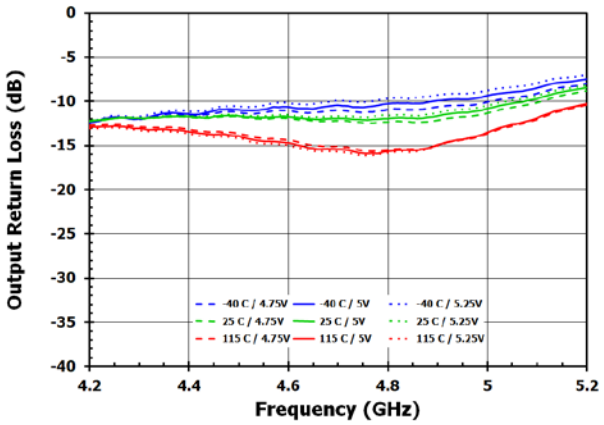


Figure 36. Output Return Loss

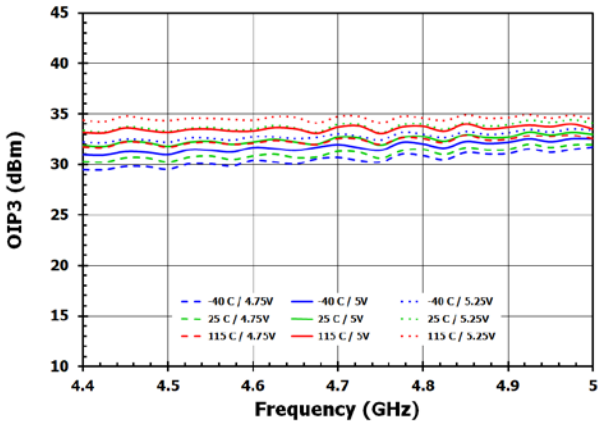


Figure 37. OIP3

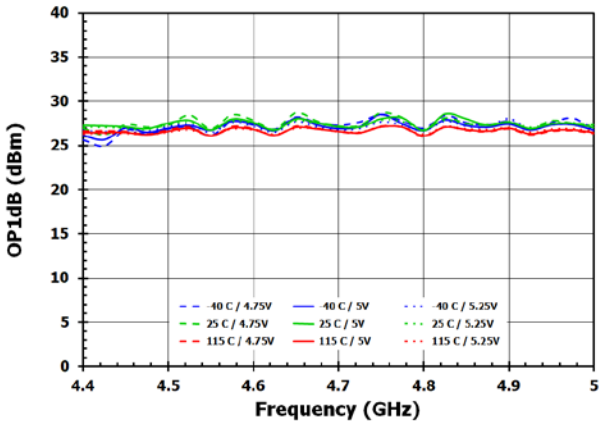


Figure 38. OP1dB

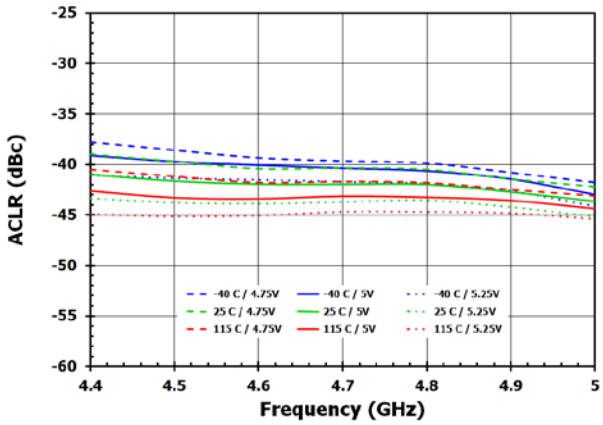


Figure 39. ACLR – LTE (20MHz)

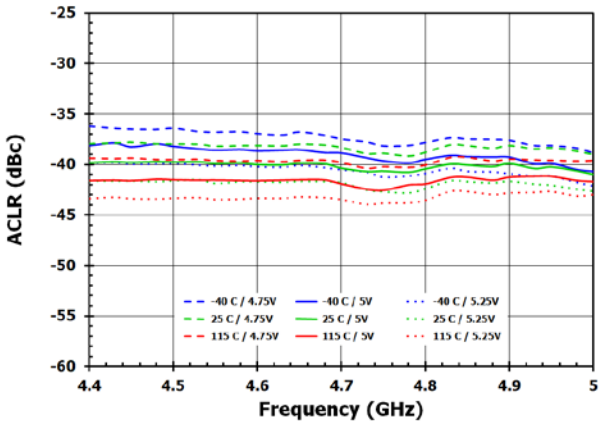


Figure 40. ACLR – 5G NR (100MHz)

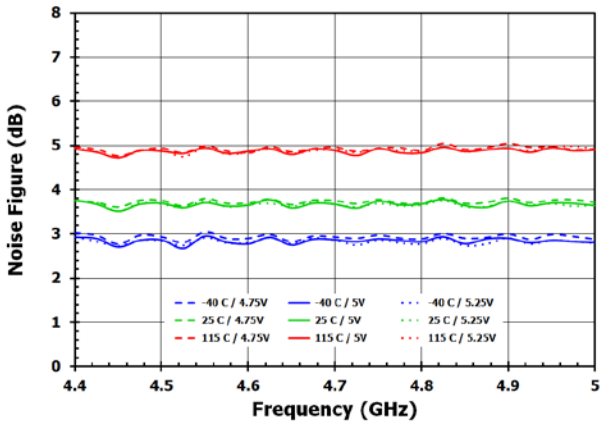


Figure 41. Noise Figure

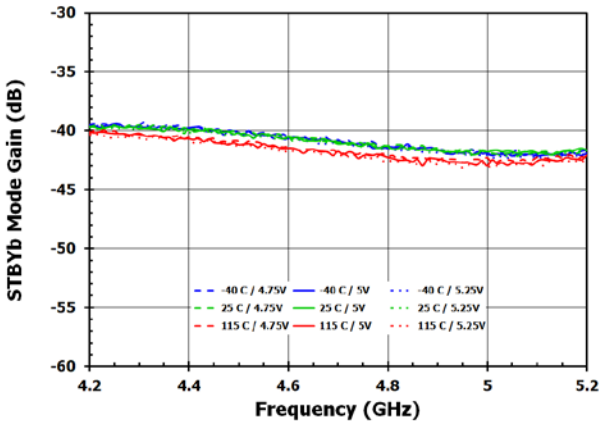


Figure 42. STBYb Gain

5. Functional Description

The F1485 can be turned off for low current consumption by applying a logic voltage to pin 16 using Table 1.

Table 1. Standby Truth Table

STBYb	Condition
Logic HIGH/NC	Full operation
Logic LOW	Amplifier OFF

6. Evaluation Kit Information

6.1 Evaluation Board (Front)

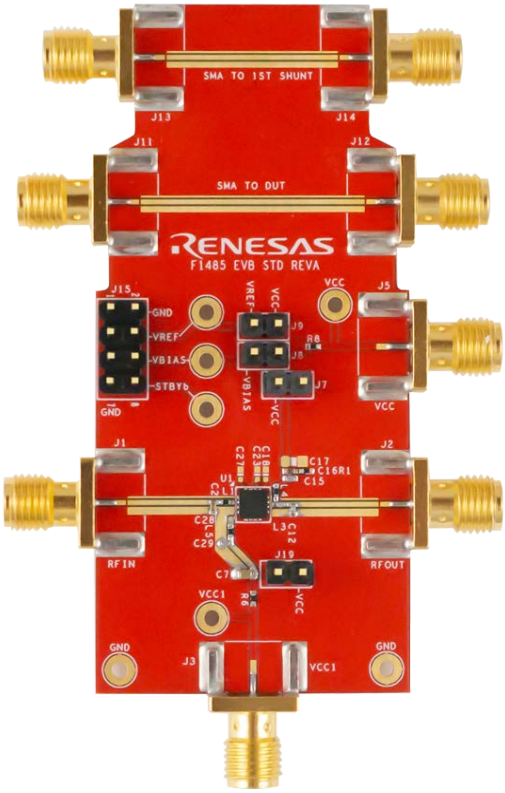


Figure 43. Evaluation Board (Front)

6.2 Evaluation Board (Back)

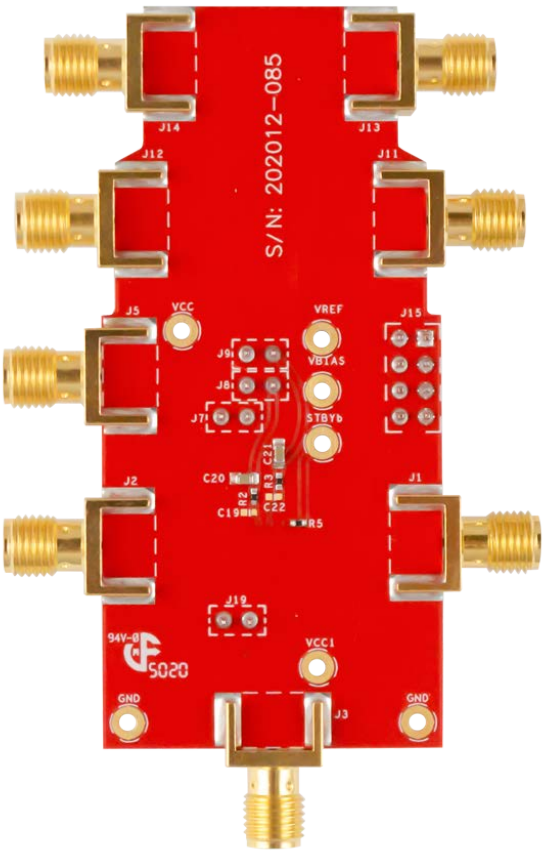


Figure 44. Evaluation Board (Back)

6.3 Evaluation Kit Circuit Schematic

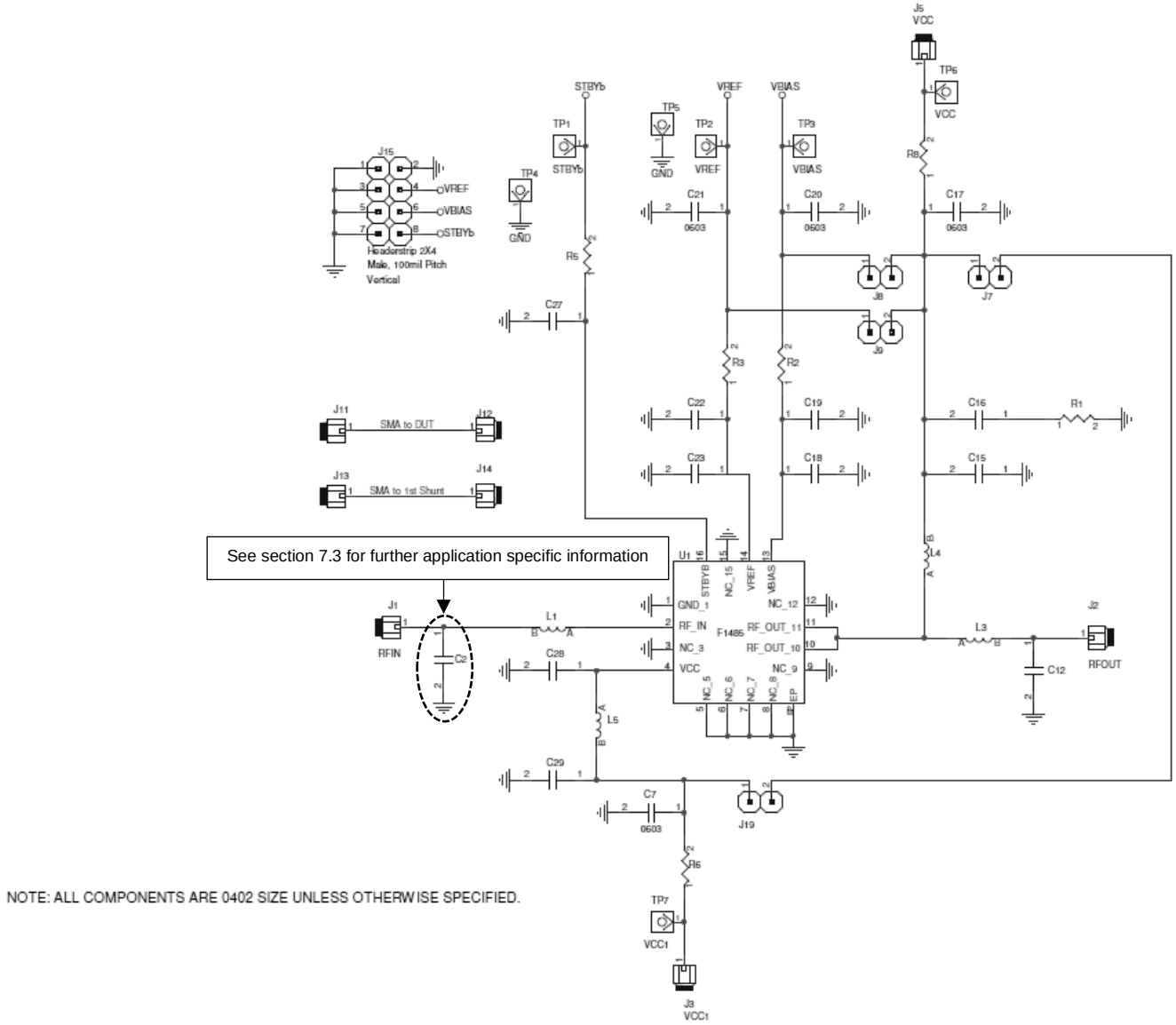


Figure 45. Evaluation Kit Circuit Schematic

6.4 Bill of Materials

Table 2. Evaluation Kit Bill of Material (BOM) – 2300MHz to 2700MHz Tune

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C7,C20,C21	3	47uF ±20%, 6.3V, X5R Ceramic Capacitor (0603)	GRM188R60J476ME15D	MURATA
C15,C29	2	1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	MURATA
C16	1	1uF ±10%, 16V, X6S Ceramic Capacitor (0402)	EMK105C6105MV-F	MURATA
C18, C19, C22, C23, C27, C28, C17	7	DNP	-	-
C2	1	82nH ±2%, 760mA wirewound Chip Inductor (0402)	0402HPH-82NXGRW	COILCRAFT
C12	1	1.6pF ±0.1pF, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H1R6WA	MURATA
L1	1	2.2 Ω ±1% Resistors 1/16watt (0402)	RMCF0401FT2R2CT	PANASONIC
L3	1	56pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H560JA	MURATA
L4	1	6.2nH ±2%, 760mA wirewound Chip Inductor (0402)	0402CS-6N2XGL	COILCRAFT
L5, R1, R2, R5, R6, R8	6	0Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
R3	1	56.2Ω ±1%, 1/10W, Resistor (0402)	ERA-2AEB56R2X	PANASONIC
J1, J2, J3, J5	4	Edge Launch SMA (0.375 inch pitch ground, tab) 50Ω	142-0701-851	Emerson Johnson
J15	1	CONN HEADER VERT DBL 4x2 POS GOLD	67997-108HLF	AMPHENOL FCI
J7, J8, J9, J19	4	CONN HEADER VERT SGL 2x1 POS GOLD	961102-6404-AR	3M
EVB	1	F1485 EVB STD REVA	-	Renesas
Module	1	F1485 ZZZG	-	Renesas

Table 3. Evaluation Kit Bill of Material (BOM) – 3300MHz to 4200MHz Tune

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C7,C20,C21	3	47uF ±20%, 6.3V, X5R Ceramic Capacitor (0603)	GRM188R60J476ME15D	MURATA
C15,C29	2	1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	MURATA
C16	1	1uF ±10%, 16V, X6S Ceramic Capacitor (0402)	EMK105C6105MV-F	MURATA
C18, C19, C22, C23, C27, C28, C17	7	DNP	-	-
C2	1	18nH Chip Inductor (0402)	LQP15MN18NG02D	MURATA
C12	1	0.8pF ±0.05pF, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1HR80W	MURATA
L3	1	56pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H560JA	MURATA
L4	1	18nH ±2%, 760mA wirewound Chip Inductor (0402)	0402CS-18NXGRW	COILCRAFT
L1 ,L5, R1, R2, R5, R6, R8	7	0Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
R3	1	69.8Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF69R8X	PANASONIC
J1, J2, J3, J5	4	Edge Launch SMA (0.375 inch pitch ground, tab) 50Ω	142-0701-851	Emerson Johnson
J15	1	CONN HEADER VERT DBL 4x2 POS GOLD	67997-108HLF	AMPHENOL FCI
J7, J8, J9, J19	4	CONN HEADER VERT SGL 2x1 POS GOLD	961102-6404-AR	3M
EVB	1	F1485 EVB STD REVA	-	Renesas
Module	1	F1485 ZZZG	-	Renesas

Table 4. Evaluation Kit Bill of Material (BOM) – 4400MHz to 5000MHz Tune

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C7,C20,C21	3	47uF ±20%, 6.3V, X5R Ceramic Capacitor (0603)	GRM188R60J476ME15D	MURATA
C15,C29	2	1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	MURATA
C16	1	1uF ±10%, 16V, X6S Ceramic Capacitor (0402)	EMK105C6105MV-F	MURATA
C18, C19, C22, C23, C27, C28, C17	7	DNP	-	-
C2	1	18nH Chip Inductor (0402)	LQP15MN18NG02D	MURATA
C12	1	0.6pF ±0.05pF, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1HR60W	MURATA
L3	1	56pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H560JA	MURATA
L4	1	10nH ±2%, 760mA wirewound Chip Inductor (0402)	0402CS-10NXGRW	COILCRAFT
L1, L5, R1, R2, R5, R6, R8	7	0Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
R3	1	51Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF51R0X	PANASONIC
J1, J2, J3, J5	4	Edge Launch SMA (0.375 inch pitch ground, tab) 50Ω	142-0701-851	Emerson Johnson
J15	1	CONN HEADER VERT DBL 4x2 POS GOLD	67997-108HLF	AMPHENOL FCI
J7, J8, J9, J19	4	CONN HEADER VERT SGL 2x1 POS GOLD	961102-6404-AR	3M
EVB	1	F1485 EVB STD REVA	-	Renesas
Module	1	F1485 ZZZG	-	Renesas

7. Application Information

7.1 Power Supplies

A common V_{CC} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients.

7.2 Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., an RC filter circuit at the input of the STBYb control pin is recommended (see Figure 46).

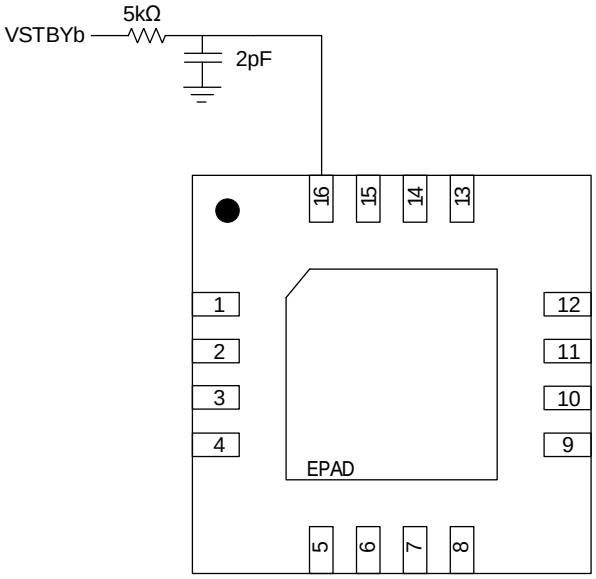


Figure 46. Control Pin Interface for Signal Integrity

7.3 Large-Signal Linearity Optimization

For optimized large-signal linearity when operating near and above compression levels in the 3600MHz – 4200MHz frequency range, it is recommended to implement the RF input circuit as shown in Figure 47. See F1485 Application Note for more information.

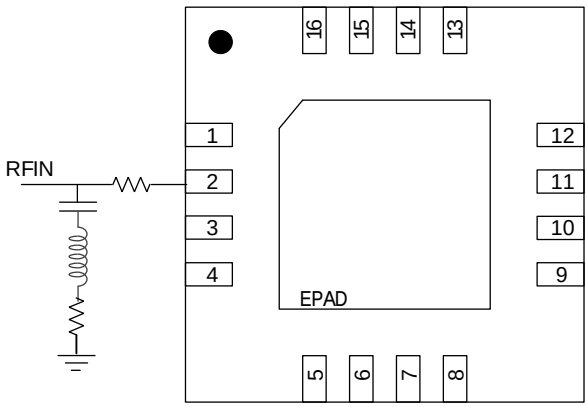


Figure 47. Recommended RF Input Circuit Implementation for Large-Signal Linearity Optimization – 3600MHz to 4200MHz Range

7.4 Evaluation Kit Operation

7.4.1. External Supply Setup

1. Set up a V_{CC} power supply in the voltage range of 4.75V to 5.25V with the power supply output disabled or turned off.
2. Set up a V_{STBYb} power supply in the voltage range of 1.8V to V_{CC} with the power supply output disabled or turned off.

7.4.2. Jumper Setup

Place jumpers J7, J8, J9, and J19 to connect all pins requiring DC power directly to V_{CC} using a single power supply connection through either the J3 or J5 SMA connector.

7.4.3. Logic Control Setup

Using the evaluation board to manually set the Standby control logic:

Standby functionality can be accessed through header J15 of the Evaluation Board. An external V_{STBYb} power supply controls the logic level of the STBYb pin. Alternatively, the pin can be left connected to a logic HIGH to keep the amplifier in full operation mode (for more information, see Table 1. Standby Truth Table).

7.4.4. Turn On Procedure

1. Set up the voltage supplies and F1485 Evaluation Board as described in the “External Supply Setup” and “Jumper Setup” sections.
2. Enable V_{CC} supply.
3. Enable V_{STBYb} supply.

7.4.5. Turn Off Procedure

1. Disable the V_{STBYb} power supply.
2. Disable the V_{CC} power supply.

7.5 Layout Guidelines

PCB layout is critical to achieving the specified performance of the F1485. This section discusses multiple topics to consider when designing the PCB for the F1485. These topics reinforce basic RF layout techniques as well as certain topics specific to the F1485 with the goal of optimizing the device performance.

7.5.1. Grounding

The exposed paddle is the most important grounding point of the F1485. It is recommended to have as many vias with a drill size of 6 mil and 14 mil pad under the device at the top layer as the board fabrication technology permits. The F1485 Evaluation Board has a total of 25 vias (5 × 5) to the ground plane for the device’s exposed paddle (see Figure 48). The vias are critical for both grounding and thermal performance.

The ground should be solid ground planes. The ground paddle should be connected to other ground planes adjacent to the bottom and corners of the device on the top layer and it is recommended to have it connected to all the NC pins on the top layer as well to ensure optimal performance. Place more vias around the part where possible. Figure 47 shows additional recommended placement of ground vias:

- Place as many ground vias that will fit under the package between pins 2 and 4.
- Flood the area with ground vias between RF_IN and VCC traces (Area 1 in Figure 47).
- Place as many ground vias that will fit under the package between pins 4 and 9.
- Flood the area with ground vias between RF_OUT and Vcc traces (Area 2 in Figure 47).
- Place as many ground vias that will fit under the package between pins 12 and 13.

- Flood the area with ground vias between RF_OUT and V_{BIAS} traces (Area 3 in Figure 47).

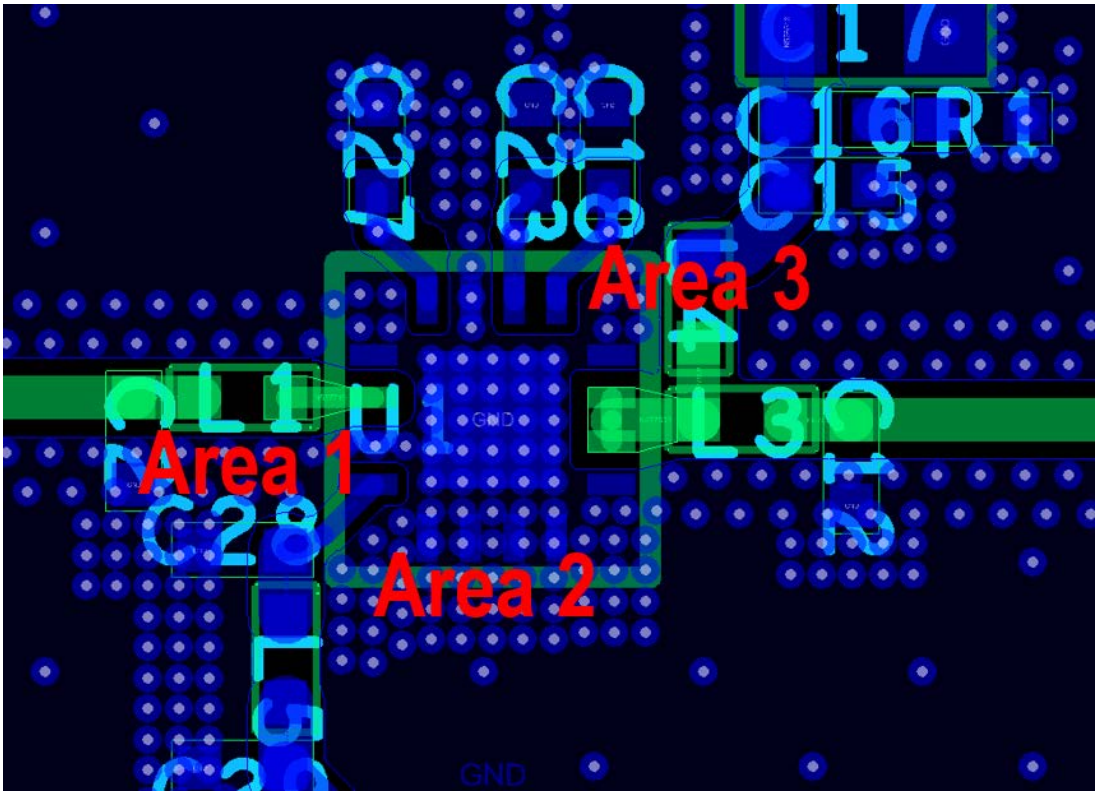


Figure 48. Layout Example

7.5.2. RF Traces and Component Placement

All RF traces should be lines with a characteristic impedance of 50Ω. It is recommended to route the traces on a layer that maximizes the isolation between the RF, DC, and control signals. In the example shown, the RF traces are routed on the top layer while the DC and control signals are routed in different layers. Component placement for the bias networks and matching components are critical to achieve specified performance. Ground vias are used extensively in this design due to the high gain of this amplifier. Isolation of the RF input trace and associated matching network from the bias networks is critical. Isolation of the RF output pins to the bias networks must also be taken into consideration during layout.

- Place decoupling capacitors as close as possible to the IC.
- Place RF matching components as close as possible to the IC.
- Flood the perimeter of the RF traces with ground vias to improve isolation.

8. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

9. Marking Diagram

- Line 1: “XXX” represents the last three digits of the lot number.
- Line 2: “YWW” has one digit for the year and two digits for the work week that the part was assembled; “$” denotes the assembly site.
- Line 3: truncated part number.

10. Ordering Information

Part Number	Package Description	MSL Rating	Carrier Type	Temperature Range
RA81F1485STGNM#BD0	3.0 × 3.0 mm 16-VFQFPN	1	Tray	-40°C to +115°C
RA81F1485STGNM#KD0		1	Reel	-40°C to +115°C
RTKA81F14852P500RU	Evaluation Board 2300MHz – 2700MHz Tune			
RTKA81F14853P800RU	Evaluation Board 3300MHz – 4200MHz Tune			
RTKA81F14854P700RU	Evaluation Board 4200MHz – 5000MHz Tune			

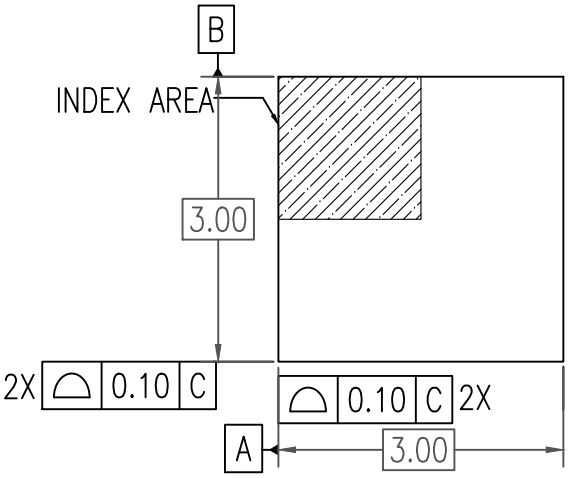
11. Revision History

Revision	Date	Description
1.03	Jul 12, 2023	Updated missing information in title.
1.02	Mar 31, 2023	Updated Human Body Model ESD rating in section 2.2.
1.01	Dec 22, 2022	Updated Human Body Model ESD rating in section 2.2.
1.00	Sep 14, 2022	Initial release.

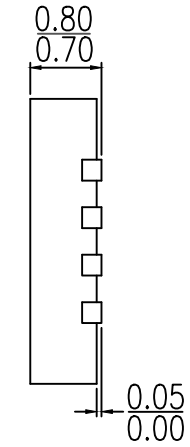
16-VFQFPN, Package Outline Drawing

3.0x 3.0 x 0.75 mm Body,0.50mm Pitch,Epad 1.60 x 1.60 mm

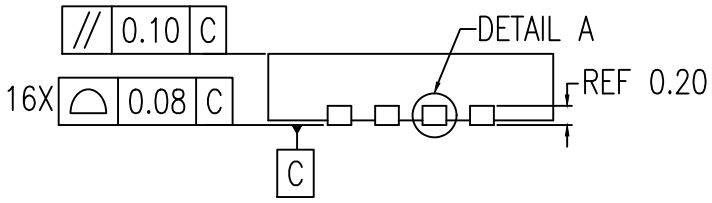
NTG16T1, PSC-4296-03, Rev 03, Page 1



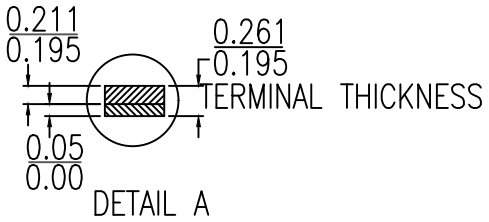
TOP VIEW



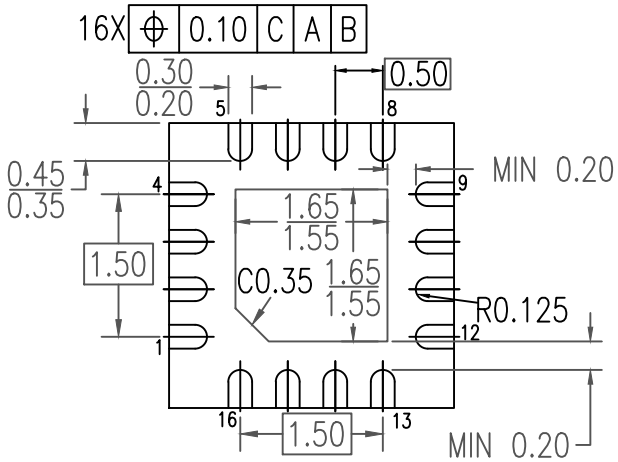
SIDE VIEW



SIDE VIEW



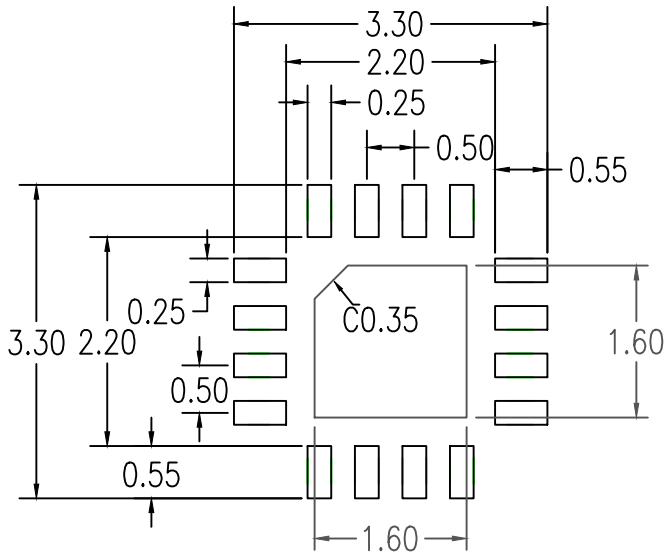
DETAIL A



BOTTOM VIEW

NOTE :

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.05 MM.
3. WARPAGE SHALL NOT EXCEED 0.05 MM.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. REFER JEDEC MO-220.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
July 8, 2019	Rev 03	Correct Typo Error Minimum
Sept 5, 2018	Rev 02	Add "K" Value 0.20 Minimum

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