

Evaluation Board User Manual



EvalAg5700 Evaluation Board User Manual

Version 2.0 - May 2024

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Evaluation Board

1 Kit Contents

- > EvalAg5700 Evaluation Board
- Ag57xxLPB Module Soldered to Evaluation Board

2 Board Layout

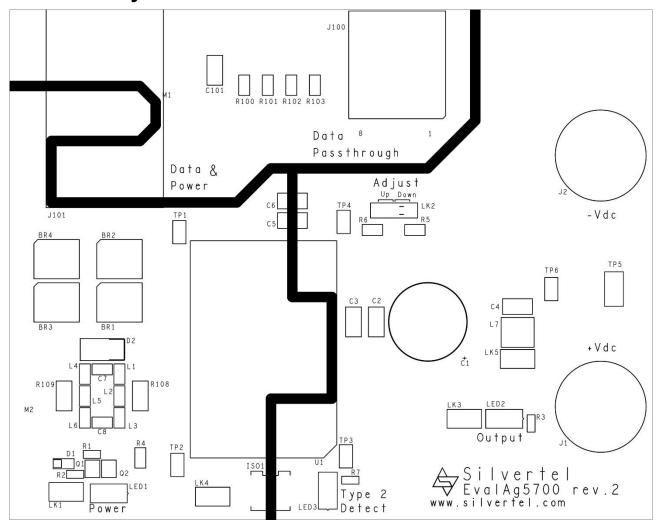


Figure 1: EvalAg7010 Board Layout

2.1 Link Settings

LK1 - Input Power LED Enable

LK2 - Output voltage Adjust

LK3 - Output Power LED Enable

LK4 - Type 2 Detect LED Enable

2.2 Input Output Connections

J1 & J2 – Load Output Binding Posts

J101 – PoE Enabled RJ45

J100 – Data Passthrough RJ45



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3 Introduction

This Manual is a guide to using the EvalAg5700 evaluation board fitted with a Silvertel Ag5712LPB or Ag5724LPB miniaturised Class 4 surface mount power over ethernet module.

This board has been designed to assist with evaluating the use of Silvertel's module in an application; as such it has been designed to pass through Ethernet data signals (10/100/1000BASE-T) from the Midspan PSE (Power Sourcing Equipment) or PoE enabled switch connected to J101, onto the system connected to J100.

While this evaluation board has been designed following Silvertel's recommendations, it should not be considered as a reference design as it features circuity included solely for the purposes of evaluation that are not be required for proper operation.

4 Input

The EvalAg5700 board will extract the power from the data pairsets using the RJ45 connector with integrated magnetics, J101. The data is passively passed on to any peripheral equipment via J100, while the power is provided to the Ag5700LPB module in the correct polarity via the bridge rectifiers BR1-BR4.

4.1 Operation

To ensure that the PSE does not apply power to a non-PoE enabled device the output port first checks for a valid PoE signature. If the PSE does not see a valid signature, then it will disconnect, wait approximately 2 seconds then try again.

Once a valid signature has been detected the PSE may then perform classification to determine the power requirement of the PD, only after this has occurred will the PSE supply power to the powered device.

The module will provide the 25K signature followed by a class 4 power level request to be powered by an IEEE compliant PSE.

If PSE is not capable of suppling the Class four power level requested by the Ag5700LPB, if using an IEEE802.3af PSE for example, it should supply the highest power level it is capable of supplying.

4.2 Input Power LED

LED1 illuminates when the module is being supplied with greater than 36V. This can be disabled by removing the jumper link LK1, removing this link does not affect the power being delivered to the Ag5700LPB.

4.3 **PSE Detect**

When the Ag5700LPB module fitted has detected it is being powered by an IEEE802.3 type 2 or greater PSE, the 'TYP2-DET' pin will be pulled low, and this will cause LED3 to become illuminated on the EvalAg5700 board.

5 Output

The Ag5700LPB output voltage will be present on the two binding post terminations J1 and J2. These can be connected to with 4mm Banana connectors, bare wire, or fork connectors.

5.1 Output Power LED

LED2 illuminates when the module is outputting. This can be disabled by removing the jumper link LK3, removing this link does not affect the power being supplied by the Ag5700LPB.

5.2 Output Voltage Adjust

The output voltage of the Ag5700LPB module can be adjusted by changing the location of the jumper LK2. The EvalAg5700 is fitted with two adjust resistors. The down adjust resistor R5, is fitted with a $68k\Omega$ resistor. And the up adjust resistor R6, which is fitted with a 0Ω resistor to allow for the maximum adjust change of the Ag5700LPB module.

To increase the output voltage, insert the jumper to LK2 in the left position, so that the link is between the middle and leftmost pin.

To reduce the output voltage, insert a jumper to LK2 in the right position, so that the link is between the middle and rightmost pin.

If the output voltage needs to be set to a different value (within the adjustment range) then connect different value resistors in place of R5 (68K) or R6 (0 Ω) and connect the jumper into the corresponding link setting.

Note: ensure that the down adjust resistor is not shorted when connecting a module that has a higher stated resistance in the datasheet, as this could cause damage to the module.

5.1 Data Output

Any data that is provided over the PI (Ethernet cable) connected to the Data & Power port, J100 will be transposed onto the Data output port, J101 via the data transformer.

The data traces on the evaluation board have been designed to pass through 10/100/1000BASE-T Ethernet data signals. No processing or amplification of this signal will be performed on the evaluation board.

6 EMI

The EvalAg5700 contains the recommended components for EMI filtering, see ANX-POE-EMI for more details.

The board is fitted with ferrite beads, L1-6; if these are not required, they can be effectively removed from the circuit by fitting R108 and R109 with 0Ω resistors.

7 Test Setup

Figure 2 shows the basic set up using the EvalAg5700 evaluation board powered by Silvertel's EvalAg6120 PSE.

The equipment required: -

- > EvalAg5700 fitted with Silvertel's Ag5712LPB or Ag5724LPB PD Module.
- EvalAg6120 or other IEEE802.3 compliant PSE
- ➤ Power supply unit, +50-57V output e.g. 60V bench power supply
- CAT5e or greater cables
- > Application Circuit

Optional equipment: -Data source e.g. PC

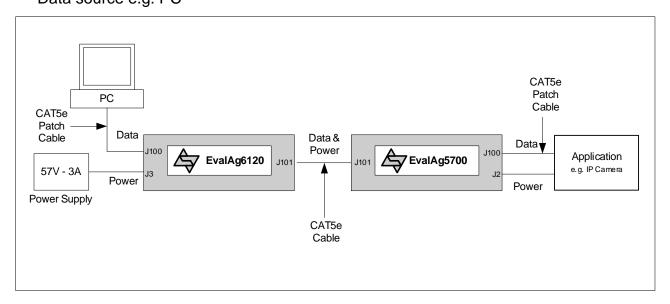


Figure 2: Basic Test Setup

8 Additional information

Full operating conditions and feature set can be found in the Ag5700 product datasheet, available from www.silvertel.com.

9 Schematic

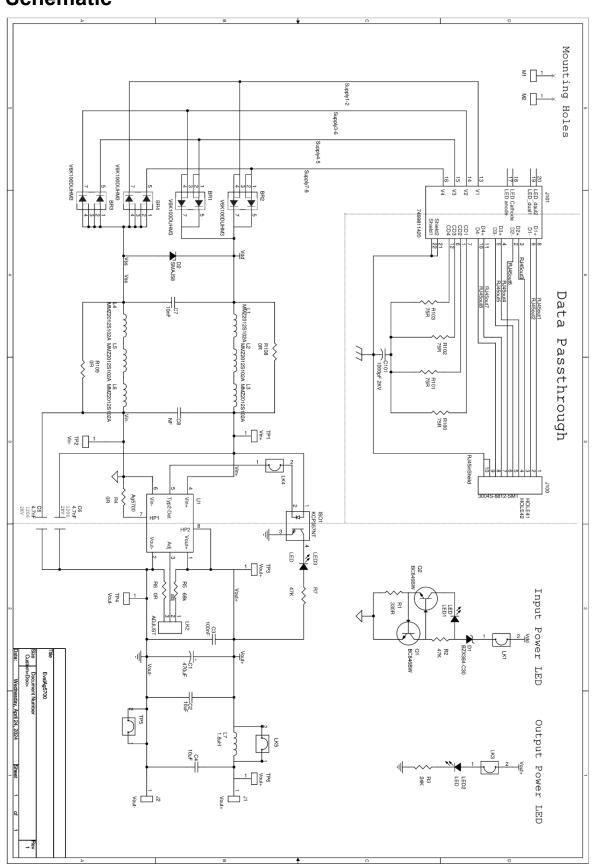


Figure 3: Schematic

Evaluation Board

10 Bill of Materials

					59	Total			
					5	LK1-5,	Links	Jumper Links	
					1		Rev.2.0 - 104.14mm x 82.55mmmm	PCB	
	Toby LHCS-03S-R-060-034, Wurth 61300311121			Through Hole		LK3	3 Way	Link	
	Toby LHCS-02S-R-060-034, Wurth 61300211121			Through Hole	51	LK1, LK3-5, TP5	2Way	Link	
	Wurth - 7499811420			SMT		J101	7499811420	Magnetics	
	Toby 3004S-8821-SMT			SMT	_	J100	RJ45	Ethernet Connector	
	Mac 8			SMT	5	TP1-4, TP6	HK-1-G	Test Point	
	Switch Electronics 354146			Screw Mount	_	J4	Binding Post	Black Connector	
	Switch Electronics 354147			Screw Mount	_	J3	Binding Post	Red Connecor	
	Royal Ohm, Eurohm & Yageo	1%	250mW	1206	0	R108, R109	0R	Resistor - 1206	
	Royal Ohm, Eurohm & Yageo	1%	125mW	0805	4	R100-103	75R	Resistor - 0805	
	Royal Ohm, Eurohm & Yageo	1%	63mW	0805	_	R5	68K	Resistor - 0805	
	Royal Ohm, Eurohm & Yageo	1%	63mW	0805	2	R4, R6	0R	Resistor - 0805	
	Royal Ohm, Eurohm & Yageo	1%	63mW	0603	_	R3	24K	Resistor - 0603	
	Royal Ohm, Eurohm & Yageo	1%	63mW	0603	2	R2, R7	47K	Resistor - 0603	
	Royal Ohm, Eurohm & Yageo	1%	63mW	0603	1	R1	330R	Resistor - 0603	
	Samsung, NIC, TDK, Murata, Kemet & AVX, Wurth-885342208024	20%	2KV	1206	1	C108	1000pF 2KV	Ceramic multi-layer	
		20%	100V	0805	0	C7, C8	No Fit	Ceramic multi-layer	
		20%	150	1206	2	C5, C6	4.7nF	Ceramic multi-layer	
		20%	25V	1206	_	C3	100nF	Ceramic multi-layer	
	TDK, Murata, Kemet, Multicomp, Wurth 885012208069	20%	25V	1206	2	C2,C4	10µF	Ceramic multi-layer	
	Kemet A750MS477M1EAAE015, Wurth 860040475008	20%	25V	Through Hole	1	C1	470µF	Capacitor Electolytic	
	Wurth, Cosmo Electronics Corp	-		SMT	1	ISO1	140356145200, KPC357NT	Opto-Isolator	
	Infineon, ON-Semi , NXP , Diodes Inc.	-	60V	SOT323	2	Q1, Q2	BC846BW	NPN Transistor	
	NPI43C1R8MTRF/OWI0403-1R8M-R-T1-LF/Wurth-74438356018	20%	3A	SMD	1	L7	1.8µH	Inductor	
	TDK MPZ2012S102A, Wurth 742792096	25%	≥ 1A	0805	6	L1-6	≥1000Ω@100MHz	Ferrite Chip	
	Wurth - 150 141 RS7 310 0			SMT	3	LED1-LED3	RED LED	SMD LED	
	Vishay			FlatPAK_5x6	4	BR1-BR4	V6K100DUHM3	Bridge Rectifiers	
	Wurth- 824 500 581, Vishay, ST Micro, Diodes Inc			SMA	_	D2	SMAJ58A	Protection Diode	
	Vishay			SOD323	1	D1	BZX384-C30	Zener Diode	
	Silver Telecom Part	-		Custom	1	U1	Ag5700	PD Module	
Comments:	Supplier Pt NO:	Tol:	Rating:	Package:	Qtv:	Location:	<u>Value</u>	<u>Description</u>	Silver Part No.
	Date: 5th February, 2024			Q - KeV.Z	Boa	EvalAgo/00 Eval Board - Rev.2			
	D-4 F41- F-1 0001					F 14 E 700 F			

Figure 4: Bill of Materials

11 Layer Routing

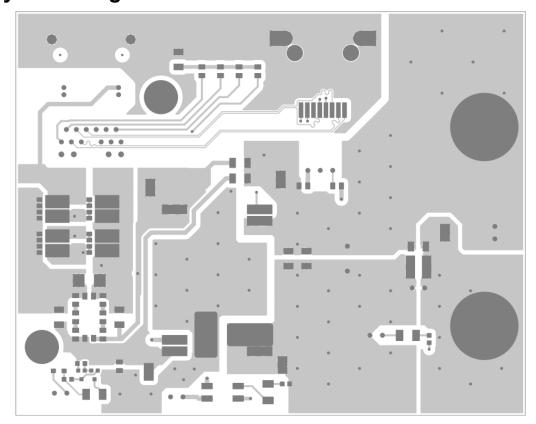


Figure 5: Top Layer Routing

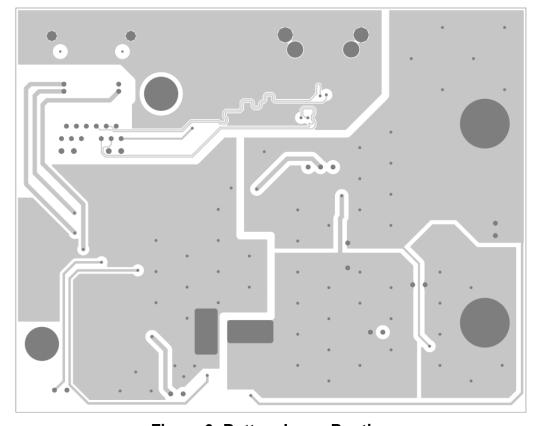


Figure 6: Bottom Layer Routing