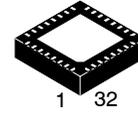


# Hot Swap, Smart Fuse

## 18 V, 0.65 mΩ, 50 A, LQFN32

### NCP81428



LQFN32 5x5, 0.5P  
CASE 487AA

#### General Description

The NCP81428 is a PMBus® enabled, 12 V, 50 A resettable in-line fuse designed for comprehensive protection against over current events, over voltage events, short circuit events, and excessive inrush current. The NCP81428 consists of a 0.65 mΩ NMOS FET, a high performance Hot-Swap Controller, and a Non-Volatile Memory (NVM) all co-packaged into a LQFN32 package. The NCP81428 can be configured as a single-phase solution, or in multi-phase as a Master or a Slave to support higher current applications.

#### Power Features

- Up to 80 A Peak Output Current, 50 A Continuous
- VIN Operating Range: 5 to 18 V
- Up to 30 V Standby (PowerFet Off) Operation
- 0.65 mΩ Path Resistance

#### Control Features

- Enabled by Pin Assertion and/or Through PMBus
- Output Pulldown Selection Via PMBus
- External Soft-Start Programming
- Programmable VIN Under Voltage Warning and Overvoltage Fault
- Programmable OCP Levels and Timers
- Soft Start Current Balancing between Parallel Units

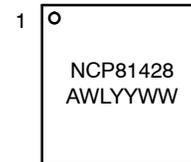
#### Other Features

- Co-packaged Power Switch, Hotswap Controller and NVM
- (TWI) Two Wire Interface between Master and Slave(s)
- PMBus 1.4 Compliant for Telemetry
- ±2% IMON Accuracy at 30 A and Higher
- 10-bit ADC for I<sub>OUT</sub>, V<sub>IN</sub>, I<sub>OUT\_pk</sub>, V<sub>OUT</sub>, V<sub>TEMP</sub>
- Parallel Operation for High Current Applications
- Excellent Current Balancing in Parallel Operations
- Over-temperature Shutdown
- FAULT#\_C & FAULT#\_D Multi-purpose Pins
- Internal FET Health Diagnostics
- Soft-start Current Limiting For SOA Protection
- Excessive Soft-start Duration Protection
- Fault Event and Peak Current Recording
- Programmable Auto Retry/Latch off Options
- 5 mm x 5 mm LQFN32 Package
- Operating Temperature: -40°C to +125°C

#### Applications

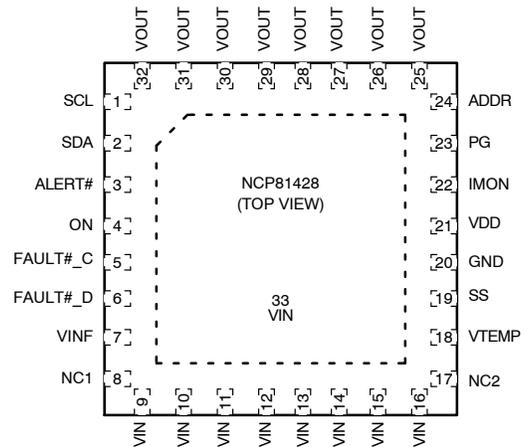
- Servers
- Data Storage
- Base Stations
- Industrial Applications

#### MARKING DIAGRAM



NCP81428 = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

#### PIN CONNECTIONS



#### ORDERING INFORMATION

See detailed ordering and shipping information on page 59 of this data sheet.

# NCP81428

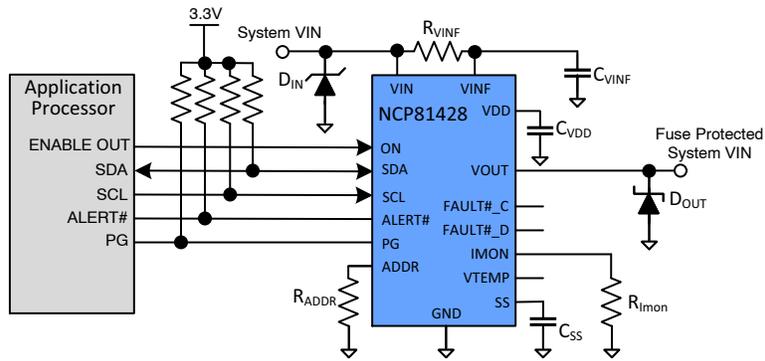


Figure 1. Application Schematic

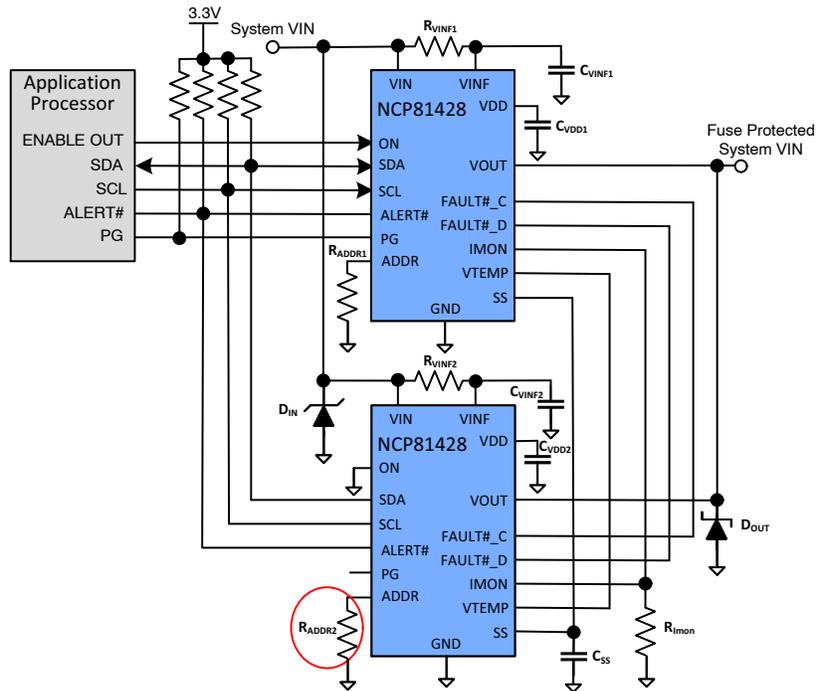


Figure 2. Application Schematic Parallel Configuration with Master and Slave Connected to PMBus

# NCP81428

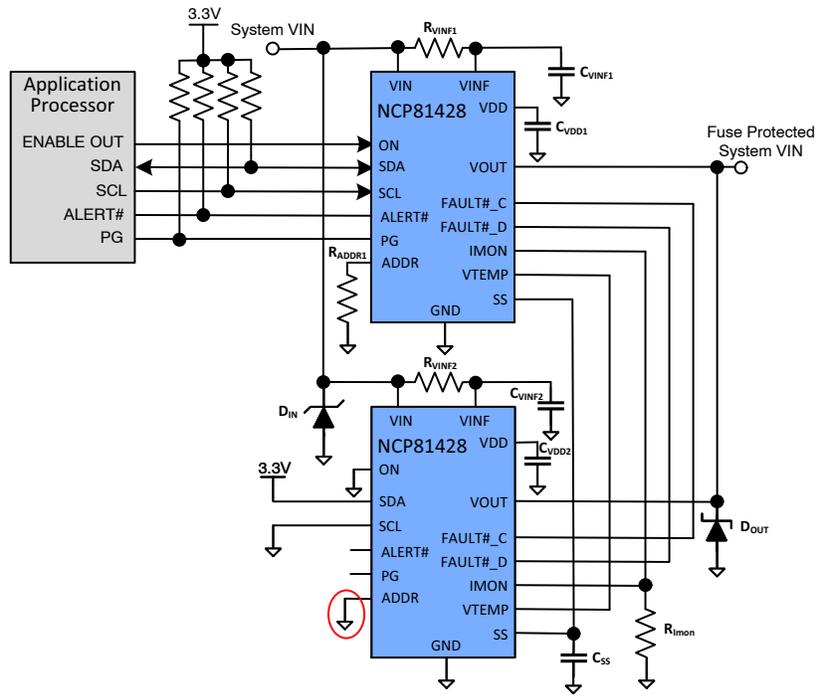


Figure 3. Application Schematic – Parallel Configuration, No PMBus on Slaves and with Master / Slave Communication

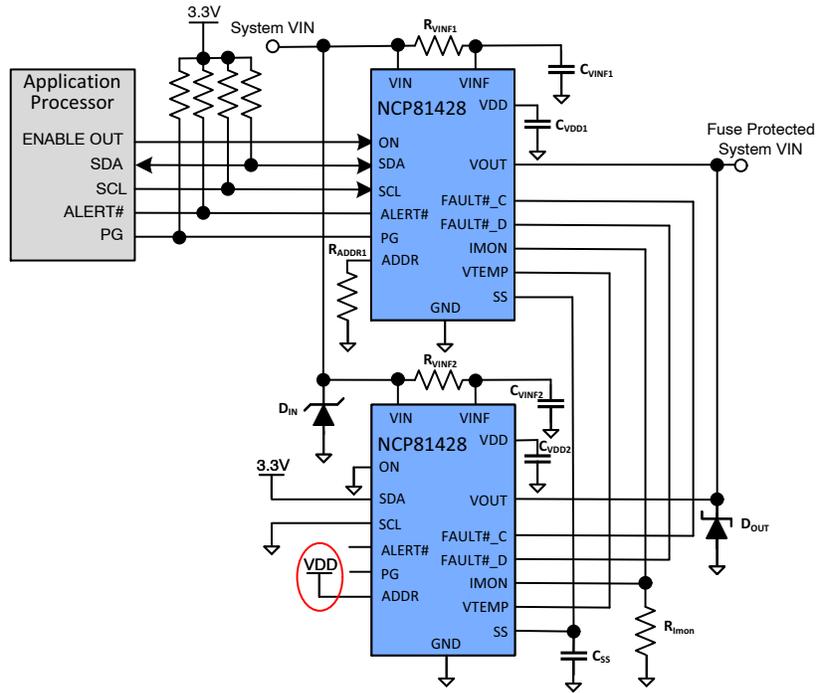


Figure 4. Application Schematic – Parallel Configuration, No PMBus on Slaves and without Master / Slave Communication

# NCP81428

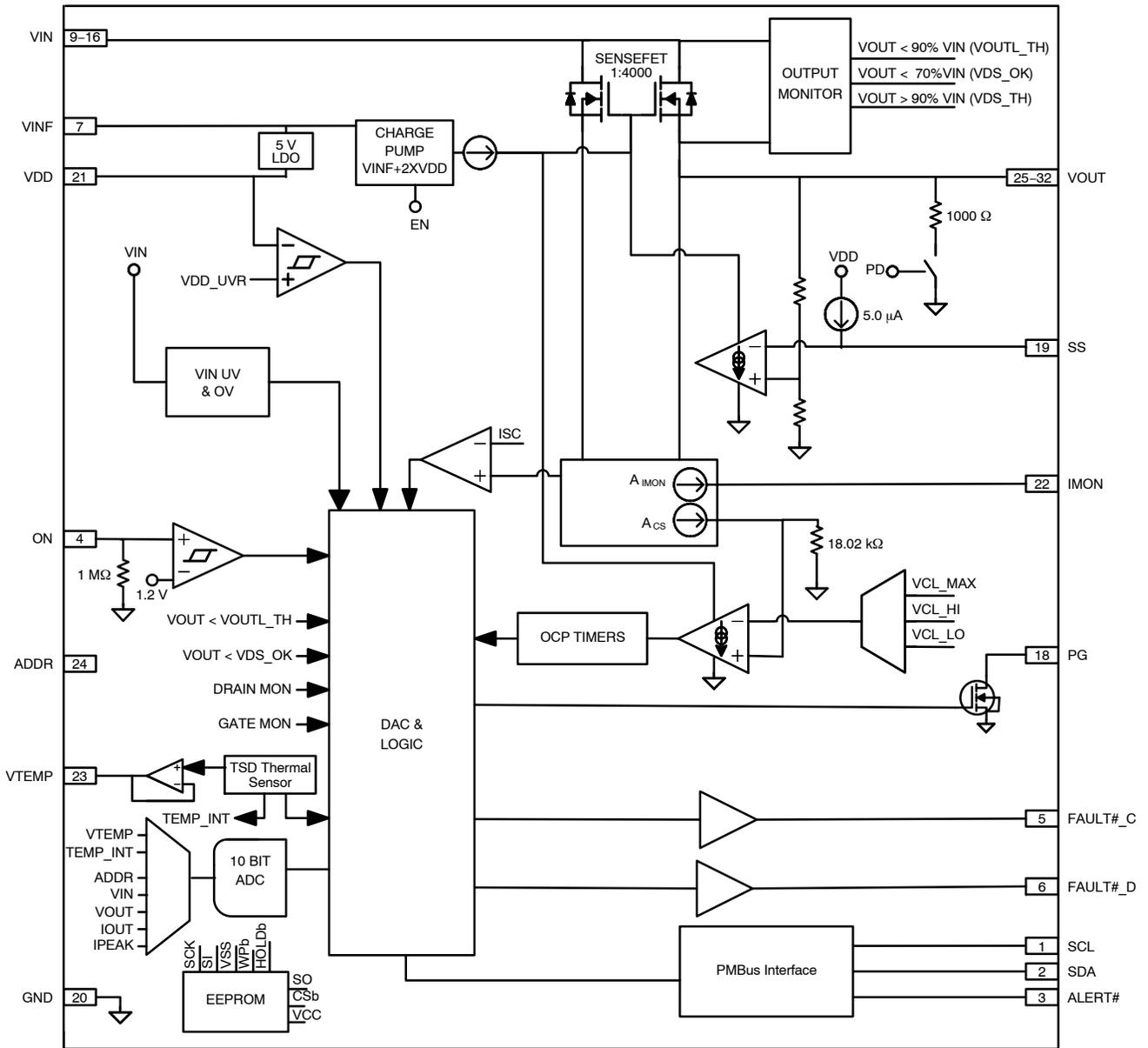


Figure 5. Simplified Block Diagram

# NCP81428

## Pin Connections

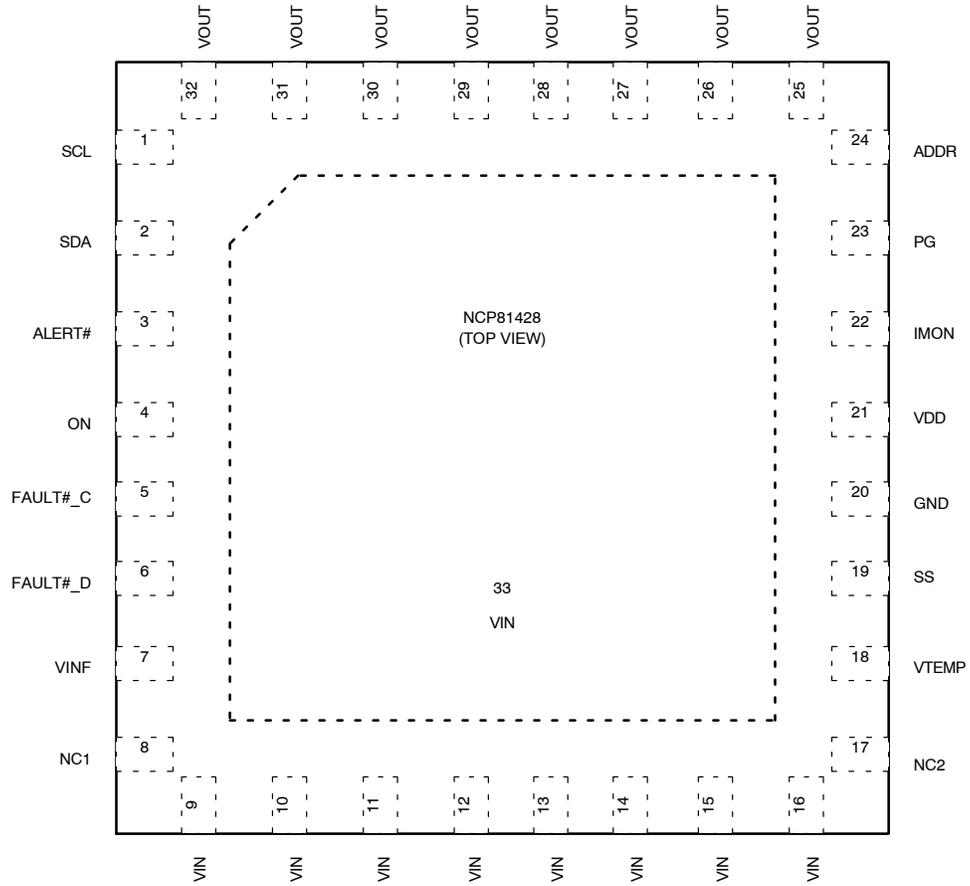


Figure 6. Pin Connections

# NCP81428

## PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	SCL	PMBus serial clock. Short to GND if not used.
2	SDA	PMBus serial data input/output. Pull-up to 3.3 V if not used.
3	ALERT#	ALERT# pin is an Open drain output. A logic low alert signal of the PMBus interface.
4	ON	Active high, enable input.
5	FAULT#_C	Active low Fault communication pin in parallel application between master and slave devices. Connect FAULT#_C pins together in parallel applications. This pin is an output on the master and an input on the slave.
6	FAULT#_D	Active low Fault communication pin in parallel application between master and slave devices. Connect FAULT#_D pins together in parallel application.
7	VINF	Control circuit power supply input. Connect to VIN pins through an RC filter.
8	NC1	Do not connect to this pin. Leave floating.
9	VIN09	Input of high current output switch (MOSFET drain connection).
10	VIN10	Input of high current output switch (MOSFET drain connection).
11	VIN11	Input of high current output switch (MOSFET drain connection).
12	VIN12	Input of high current output switch (MOSFET drain connection).
13	VIN13	Input of high current output switch (MOSFET drain connection).
14	VIN14	Input of high current output switch (MOSFET drain connection).
15	VIN15	Input of high current output switch (MOSFET drain connection).
16	VIN16	Input of high current output switch (MOSFET drain connection).
17	NC2	Do not connect to this pin. Leave floating.
18	VTEMP	Analog temperature monitoring. Connect all VTEMP pins together in parallel applications.
19	SS	Soft-start time programming pin. Connect a capacitor to this pin to set the soft-start time. The internal circuit controls the slew rate of the output voltage at turn-on. Connect all SS pins together in parallel applications.
20	GND	Ground
21	VDD	Internal linear regulated supply output. Place a capacitor with a value of 4.7 $\mu$ F or greater on this pin to maintain accuracy.
22	IMON	Analog current monitor output, Connect a 2 k $\Omega$ resistor between pin and ground. A proportional current to the output current develops a voltage across the resistor. Connect all IMON pins together in parallel applications.
23	PG	Power Good, Open Drain output pin. Can be connected to VDD with a 100 k $\Omega$ pull-up resistor.
24	ADDR	PMBus address-setting pin. Connect a resistor from this pin to GND to set the device address.
25	VOUT25	Output of high current output switch (MOSFET source connection).
26	VOUT26	Output of high current output switch (MOSFET source connection).
27	VOUT27	Output of high current output switch (MOSFET source connection).
28	VOUT28	Output of high current output switch (MOSFET source connection).
29	VOUT29	Output of high current output switch (MOSFET source connection).
30	VOUT30	Output of high current output switch (MOSFET source connection).
31	VOUT31	Output of high current output switch (MOSFET source connection).
32	VOUT32	Output of high current output switch (MOSFET source connection).
33	VIN33	Input of high current output switch (MOSFET drain connection).

# NCP81428

## MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIN, VIN <sub>F</sub>	Input Voltage (Notes 1, 3)		-0.3	-	20.0	V
	Input Voltage (Notes 1, 2)		-0.3	-	30	
VOUT	VOUT Pin Voltage Range (Note 1)		-0.3, -1.0 V (<500 ms)	-	20	V
VDD	LDO Output (Note 1)		-0.3	-	6.0	V
All Other Pins	Pin Voltage Range (Note 4)		-0.3	-	VDD + 0.3	V
T <sub>J(MAX)</sub>	Operating Junction Temperature		-	-	+150	°C
T <sub>STG</sub>	Storage Temperature Range		-55	-	+150	°C
T <sub>SLD</sub>	Lead Temperature Soldering Reflow (SMD Styles Only) Pb- Free Versions (Note 5)		-	-	+260	°C
ESD <sub>CDM</sub>	Electrostatic Discharge – Charged Device Model	Charged Device Model	-	-	2.0	kV
ESD <sub>HBM</sub>	Electrostatic Discharge – Human Body Model	Human Body Model	-	-	3.0	kV
C <sub>FAULT#_C</sub> , C <sub>FAULT#_D</sub>	PCB Capacitance on FAULT#_C and FAULT#_D Pins		-	-	200	pF

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All signals referenced to ground unless noted otherwise.
2. Vout disabled is when the internal Power FET has turned off by disabling the device or after triggering a fault event.
3. Vout enabled is when the internal Power FET has turned on either by enabling the device or after restart fault event.
4. The ratings of Pins referenced to VDD, only apply when VDD is within the recommended Voltage Range.
5. For information, please refer to **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>θJA</sub>	Junction-to-Ambient Thermal Resistance (Note 6)		-	30	-	°C/W
R <sub>θJCT</sub>	Junction-to-Top-Case Thermal Resistance		-	50	-	°C/W
R <sub>θJCB</sub>	Junction-to-Bottom-Case Thermal Resistance		-	1.5	-	°C/W
R <sub>θJB</sub>	Junction-to-Board Thermal Resistance (Note 7)		-	1.5	-	°C/W
R <sub>θJAC</sub>	Junction-to-Case Thermal Resistance (Note 8)		-	1.5	-	°C/W

6. Theta JA is obtained by simulating the device mounted on a 500 mm<sup>2</sup>, 1-oz Cu pad on a 80 mm x 80 mm, 1.6 mm 8 layer FR4 board.
7. Theta JB value based on hottest board temperature within 1 mm of the package.
8. Theta JC ~ = Theta JCT // Theta JCB (Two-Resistor Compact Thermal Model, JESD15-3).

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	VIN, VIN <sub>F</sub> Pin Voltage Range		5	-	18	V
I <sub>AVE</sub>	Minimum Continuous Output Current		-	-	50	A
I <sub>PEAK</sub>	Peak Output Current		-	-	80	A
C <sub>VDD</sub>	VDD Output Load Capacitance Range		4.7	-	10	μF
C <sub>OUT</sub>	Output Capacitance Range		100	-	10000	μF
T <sub>SS</sub>	Soft Start Duration		10	-	110	ms
R <sub>IMON</sub>	IMON Resistor		1.98	2	2.02	kΩ
T <sub>J(OP)</sub>	Junction Temperature		-40	-	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# NCP81428

**ELECTRICAL CHARACTERISTICS** (Typical values are at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{INF} = 12.0\text{ V}$ ,  $V_{ON} = 3.3\text{ V}$ ,  $C_{VIN} = 0.1\ \mu\text{F}$ ,  $C_{VDD} = 4.7\ \mu\text{F}$ ,  $C_{SS} = 100\ \text{nF}$ . Min/Max values are valid for  $6\text{ V} \leq V_{IN} \leq 18\text{ V}$ ,  $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ , unless otherwise noted.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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## VINF INPUT

$I_{q\_OP}$	Operating Current	$V_{ON} > 1.3\text{ V}$ , No Load	-	9.5	14	mA
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## VDD REGULATOR

$V_{DD\_NL}$	VDD Output Voltage	$1\text{ mA} < I_{VIN} < 10\text{ mA}$ , $6\text{ V} < V_{INF} < 18\text{ V}$	4.7	5.0	5.3	V
$V_{DD\_UVR}$	UVLO Threshold – Rising		4.1	4.3	4.5	V
$V_{DD\_UVF}$	UVLO Threshold – Falling		3.5	3.7	3.9	V
$I_{DD\_CL}$	VDD Current Limit	$6\text{ V} < V_{INF} < 18\text{ V}$ , $V_{DD} = 100\text{ mV}$	20	25	50	mA
$I_{DD\_FLD}$	VDD Short Circuit Current Limit	$6\text{ V} < V_{INF} < 18\text{ V}$ , $V_{DD} = 0\text{ V}$	5	13	25	mA

## ON INPUT

$V_{SWON}$	Rising Switch ON Threshold		1.10	1.20	1.30	V
$V_{ON\_HYS}$	ON Comparator Hysteresis		-	100	-	mV
$t_{ON}$	Switch ON Delay Timer	From ON transitioning above $V_{SWON}$ to SS start.	0.6	1.0	1.4	ms
$t_{OFF}$	Switch OFF Delay Timer	From ON transitioning below $V_{ONhys}$ to PowerFET OFF, No Load	-	-	2	$\mu\text{s}$
$R_{ON\_PD}$	Input Pulldown Resistance	$V_{IN} = 12\text{ V}$	0.7	1.0	1.3	$M\Omega$

## SS PIN

$I_{SS}$	Bias Current	Force $V_{SS} = 0\text{ V}$	4.5	5.0	5.5	$\mu\text{A}$
$A_{VSS}$	Gain at $V_{OUT}$	$V_{SS} = 1.0\text{ V}$	9.7	10	10.3	V/V
$V_{OL\_SS}$	SS PullDown Voltage	0.1 mA into pin during ON delay	-	3.5	7.5	mV

## IMON OUTPUT

$TOL_{IMON}$	Accuracy (Single eFuse)	$I_{OUT} = 8\text{ A}$ , $V_{IN} = 12\text{ V}$ , $T_J = 25^\circ\text{C}$	-4	-	+4	%
		$I_{OUT} = 15\text{ A}$ (Note 9), $V_{IN} = 12\text{ V}$ , $T_J = 25^\circ\text{C}$	-2.5	-	+2.5	
		$I_{OUT} = 30\text{ A}$ (Note 9), $V_{IN} = 12\text{ V}$ , $T_J = 25^\circ\text{C}$	-2	-	+2	
		$I_{OUT} = 50\text{ A}$ (Note 9), $V_{IN} = 12\text{ V}$ , $T_J = 25^\circ\text{C}$	-2	-	+2	
$V_{IMON\_CLMP}$	IMON Current Source Clamp Voltage	Max pullup voltage of current source	2.4	3.0	-	V

## CURRENT LIMIT at SOFTSTART

VIN < 13.2 V						
$I_{CS\_LO}$	Current Limit Clamp Voltage, Low VIN (Note 9)	$V_{OUT} < 0.4 \times V_{IN}$ , $V_{IN} < 13.2\text{ V}$	6	7.5	9	A
$I_{CS\_HI}$	Current Limit Clamp Voltage, Low VIN (Note 9)	$0.4 \times V_{IN} < V_{OUT} < 0.8 \times V_{IN}$ , $V_{IN} < 13.2\text{ V}$	12	15	18	
$I_{CS\_MAX}$	Current Limit Max Clamp Voltage, Low VIN (Note 9)	$0.8 \times V_{IN} < V_{OUT}$ , $V_t < V_{GS}$ , $V_{IN} < 13.2\text{ V}$	24	30	36	A
$t_{CL\_REG}$	CL Duration before SD (Note 9)		200	250	300	$\mu\text{s}$
VIN > 13.2 V						
$I_{CS\_LO}$	Current Limit Clamp Voltage, High VIN (Note 9)	$V_{OUT} < 0.4 \times V_{IN}$ , $V_{IN} > 13.2\text{ V}$	4	5	6	A
$I_{CS\_HI}$	Current Limit Clamp Voltage, High VIN (Note 9)	$0.4 \times V_{IN} < V_{OUT} < 0.8 \times V_{IN}$ , $V_{IN} > 13.2\text{ V}$	8	10	12	
$I_{CS\_MAX}$	Current Limit Max Clamp Voltage, High VIN (Note 9)	$0.8 \times V_{IN} < V_{OUT}$ , $V_t < V_{GS}$ , $V_{IN} > 13.2\text{ V}$	16	20	24	A
$t_{CL\_REG}$	CL Duration before SD (Note 9)		200	250	300	$\mu\text{s}$

# NCP81428

**ELECTRICAL CHARACTERISTICS** (Typical values are at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{INF} = 12.0\text{ V}$ ,  $V_{ON} = 3.3\text{ V}$ ,  $C_{VIN} = 0.1\ \mu\text{F}$ ,  $C_{VDD} = 4.7\ \mu\text{F}$ ,  $C_{SS} = 100\ \text{nF}$ . Min/Max values are valid for  $6\text{ V} \leq V_{IN} \leq 18\text{ V}$ ,  $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ , unless otherwise noted.) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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## OCP PROTECTION

OCP Threshold						
$I_{OCP}$	Over Current Detection Programmable Range		10	–	80	A
$I_{OCP\_HYS}$	Over Current Hysteresis – Percentage of Threshold		75	80	85	%
$OCP_{Accuracy}$	Over Current Detection Accuracy	$V_{IN} = 12\text{ V}$ , $OCP_x = 10\text{ A}$	–10	–	+12	%
		$V_{IN} = 12\text{ V}$ , $OCP_x = 15\text{ to }80\text{ A}$	–10	–	+10	
Timeout Delay						
$OCP_{Timer}$	Over Current Debounce Timer Range		0.25	–	50	ms
$OCP_{Accuracy}$	Over Current Debounce Timer Accuracy		–10	–	+10	%
$OCP_{Reset-Timer}$	Over Current Debounce Timer Reset		90	100	110	$\mu\text{s}$

## SHORT CIRCUIT PROTECTION

$I_{SC}$	Short Circuit Current Threshold (Note 9)		135	150	165	A
$t_{SC}$	Response Time (Note 9)	From $I_{OUT} > I_{LIMSC}$ until gate pulldown	–	–	2000	ns

## THERMAL PROTECTION

$T_{OT\_F}$	Programmable Over-Temperature Fault Threshold Range		80	–	150	$^\circ\text{C}$
	Resolution		–	0.5	–	
	Default Setting		–	140	–	
$T_{OT\_W}$	Programmable Over-Temperature Warning Threshold Range		70	–	150	$^\circ\text{C}$
	Resolution		–	0.5	–	
	Default Setting		–	120	–	

## OUTPUT SWITCH (FET)

$R_{DS\_ON}$	Rdson Resistance	$V_{IN} = 6\text{ V to }18\text{ V}$ , $I_{LOAD} = 8\text{ A}$	–	0.65	1.3	$\text{m}\Omega$
$I_{ds\_OFF}$	Off-state leakage current	$V_{IN} = 18\text{ V}$ , $V_{ON} < 1.0\text{ V}$ , $T_J = 25^\circ\text{C}$	–	–	1	$\mu\text{A}$

## FAULT DETECTION

$V_{G\_TH}$	VG Low Threshold	Latch/Restart if $V_{GS} < V_{G\_TH}$ after $t_{SS\_FLT}$ , $V_{IN} = 12\text{ V}$	5.2	5.5	5.8	V
$V_{DS\_TH}$	VDS Short Threshold	Startup postpones if $V_{OUT} > V_{DS\_TH}$ at $V_{ON} > V_{SWON}$ transition, $V_{IN} = 12\text{ V}$	85	90	95	% $V_{IN}$
$V_{DS\_OK}$	VDS Short OK Threshold	Startup resumes if $V_{OUT} < V_{DS\_OK}$ Threshold, $V_{IN} = 12\text{ V}$	65	70	75	% $V_{IN}$
$V_{DG\_TH}$	VGD Short Threshold	Startup postpones if $V_G > V_{DG\_TH}$ at $V_{ON} > V_{SWON}$ transition, $V_{IN} = 12\text{ V}$	2.5	3.0	3.6	V
$V_{DG\_OK}$	VGD Short OK Threshold	Startup resumes if $V_G < V_{DG\_OK}$ , $V_{IN} = 12\text{ V}$	2.1	2.6	3.2	V
$V_{OUTL\_TH}$	VOU Low Threshold	Latch/Restart if $V_{OUT} < V_{OUTL\_TH}$ after $t_{SS\_FLT}$ , $V_{IN} = 12\text{ V}$	85	90	95	% $V_{IN}$
$t_{SS\_FLT}$	Startup Timer Failsafe (Note 9)	$V_{IN} = 12\text{ V}$	180	200	220	ms

## AUTO\_RETRY

$t_{DLY\_RETRY}$	Auto-Retry Delay (Note 9)	$V_{IN} = 12\text{ V}$ , $I_{OUT} = 1\text{ A}$	700	1000	1300	ms
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## VIN OVP

$V_{IN\_OVP\_LO}$	Programmable Over Voltage Range	$V_{ON} = 2\text{ V}$ , $I_{OUT} = 1\text{ A}$	6	–	8	V
$V_{IN\_OVP\_HI}$			14	–	19	V

# NCP81428

**ELECTRICAL CHARACTERISTICS** (Typical values are at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{INF} = 12.0\text{ V}$ ,  $V_{ON} = 3.3\text{ V}$ ,  $C_{VIN} = 0.1\ \mu\text{F}$ ,  $C_{VDD} = 4.7\ \mu\text{F}$ ,  $C_{SS} = 100\ \text{nF}$ . Min/Max values are valid for  $6\text{ V} \leq V_{IN} \leq 18\text{ V}$ ,  $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ , unless otherwise noted.) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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## VIN OVP

VIN_OVP_ACC	VIN OVP Accuracy	6–8 V	-5	-	+5	%
		14–19 V	-3	-	+3	%
VIN_OVP_DFLT	Default VIN OVP Setting		-	14.0	-	V

## VIN UVLO

VIN_UVLO_ThF	VIN Under Voltage Lock-out Falling Threshold	No Load	4.40	4.55	4.70	V
VIN_UVLO_Hys	VIN Under Voltage Lock-out Hysteresis		75	100	125	mV

## VTEMP

V_VTEMP25	VTEMP Pin Voltage at 25°C	$T_J = 25^\circ\text{C}$	410	420	430	mV
A_VTEMP	VTEMP Pin Gain Per °C (Note 9)	$25^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$	7.0	7.8	8.6	mV/°C

## PMBus TIMING AND PERFORMANCE

F_SCL	Clock Frequency Range		10	-	400	kHz
V_IH	SDA and SCL Logic High threshold		1.35	-	-	V
V_IL	SDA and SCL Logic Low threshold		-	-	0.8	V
V_HYS	Logic Input Hysteresis threshold		80	-	-	mV
I_Bias	Logic Input Bias Current		-1	-	+1	μA
V_OL	SDA Output Logic Low Voltage	ISDA = 6 mA (Sink)	-	-	0.4	V
C_i	SDA and SCL Input Capacitance		-	-	10	pF
t_R	SDA and SCL Rise Time		120	-	-	ns
t_F	SDA and SCL Fall Time		100	-	300	ns
t_SU;DAT	Data Setup Time		100	-	-	ns
t_VD;DAT	Data Valid Time		0	-	-	ns
t_HIGH	SCL HIGH Time		0.6	-	50	μs
t_LOW	SCL LOW Period		1.3	-	-	μs
t_TIMEOUT	Detect Low Time-Out		25	-	35	ms
t_BUF	Bus-Free Time between STOP and START Conditions		-	1.3	-	μs
t_SU;STA	Repeated START Setup Time		-	0.6	-	μs
t_HD;STA	START or Repeated START Hold Time		-	0.6	-	μs
t_LOW;MEXT	Cumulative Clock Low Extended Time (Master Device)		-	-	10	ms
t_LOW;SEXT	Cumulative Low Extended Time (Slave Device)		-	-	25	ms

## MASTER/SLAVE FAULTS (FAULT#\_C, FAULT#\_D PINS)

V_FLT_IL	FAULT#_x Active Low Input		-	-	0.4	V
V_FLT_IH	FAULT#_x Active High Input		3.2	-	-	
R_FLT_Rup	Pull-up Resistance on FAULT#_x		300	450	700	Ω
R_FLT_Rdwn	Pull-down Resistance on FAULT#_x		5.0	10	15	

## ALERT#

I_ALT_HI	Leakage Current into ALERT# Pin	ALERT# state is "High" and tied to, $V_{IN} = 12\text{ V}$	-	-	1	μA
V_AL_LO	Low Output Voltage	$I_{\_ALERT\#} = -1\ \text{mA}$ , $V_{IN} = 12\text{ V}$	-	-	0.3	V

## POWERGOOD

I_LKG_PG	Leakage Current into PG Pin	PG state is "High" and tied to VDD, $V_{IN} = 12\text{ V}$	-	-	1	μA
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# NCP81428

**ELECTRICAL CHARACTERISTICS** (Typical values are at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{INF} = 12.0\text{ V}$ ,  $V_{ON} = 3.3\text{ V}$ ,  $C_{VIN} = 0.1\ \mu\text{F}$ ,  $C_{VDD} = 4.7\ \mu\text{F}$ ,  $C_{SS} = 100\ \text{nF}$ . Min/Max values are valid for  $6\text{ V} \leq V_{IN} \leq 18\text{ V}$ ,  $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ , unless otherwise noted.) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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## POWERGOOD

$V_{PG\_LO}$	Low Output Voltage	$I_{PG} = -1\ \text{mA}$ , $V_{IN} = 12\text{ V}$	-	-	0.3	V
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## TELEMETRY

$T_{TLMR}$	Period for all ADC Input Channels to be Measured		-	120	132	$\mu\text{s}$
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## VIN

$V_{IN\_MON}$	VIN Measurement Range	No Load, MOSFET Enabled	6.0	-	19	V
	Accuracy	$V_{IN} = 6\text{ V}$ , No Load, $T_J = 25^\circ\text{C}$ (Note 10)	-2.5	-	+2.5	%
		$12\text{ V} \leq V_{IN} \leq 18\text{ V}$ , No Load, $T_J = 25^\circ\text{C}$ (Note 10)	-1.25	-	+1.25	
	Resolution	$6\text{ V} \leq V_{IN} \leq 19\text{ V}$ , No Load	-	31.25	-	mV

## VOUT

$V_{OUT\_MON}$	VOUT Measurement Range	No Load, MOSFET Enabled	6.0	-	19	V
	Accuracy	$V_{OUT} = 6\text{ V}$ , No Load, MOSFET ON, $T_J = 25^\circ\text{C}$ (Note 10)	-2.5	-	+2.5	%
		$12\text{ V} \leq V_{OUT} \leq 18\text{ V}$ , No Load, MOSFET ON, $T_J = 25^\circ\text{C}$ (Note 10)	-1.25	-	+1.25	
	Resolution	$6\text{ V} \leq V_{OUT} \leq 19\text{ V}$ , No Load	-	31.25	-	mV

## IOUT

$I_{OUT\_MON}$	Output Current Measurement Range		0	-	127.87 5	A
	Accuracy	$I_{OUT} = 8\text{ A}$ , $V_{IN} = 12\text{ V}$ , $T_J = 25^\circ\text{C}$ (Note 10)	-14	-	+6.5	%
		$15\text{ A} \leq I_{OUT} \leq 80\text{ A}$ , $V_{IN} = 12\text{ V}$ , $T_J = 25^\circ\text{C}$ (Notes 9, 10)	-7.5	-	+3.5	
	Resolution		-	125		mA

## INTERNAL TEMP

$V_{TEMP\_MON}$	Temperature Monitoring Range		-20	-	160	$^\circ\text{C}$
	Accuracy	$-20 < T_J < 125^\circ\text{C}$ (Note 10)	-3	-	+3	$^\circ\text{C}$
	High Temp Accuracy	$125 \leq T_J \leq 160^\circ\text{C}$ (Note 10)	-3	-	+3	$^\circ\text{C}$
	Resolution		-	0.5	-	$^\circ\text{C}$

## SYSTEM TEMP (VTEMP)

$V_{TEMP\_SYS\_MON}$	Temperature Monitoring Range		-20	-	160	$^\circ\text{C}$
	Accuracy	$-20 < T_J < 125^\circ\text{C}$ (Note 10)	-3	-	+3	$^\circ\text{C}$
	High Temp Accuracy	$125 \leq T_J \leq 160^\circ\text{C}$ (Note 10)	-3	-	+3	$^\circ\text{C}$
	Resolution		-	0.5	-	

## OUTPUT PULLDOWN

$R_{OUT\_PD}$	Output Pulldown Resistance	$V_{OUT} = 12\text{ V}$ , PD mode = 1	600	1000	2200	$\Omega$
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Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. Guaranteed by design or characterization data. Not tested in production.

10. Min/Max Telemetry values are the combined errors of sense circuitry and ADC conversion errors.

TYPICAL CHARACTERISTICS

(VIN = VINFINF = 12 V, CVINFINF = 0.1 μF, CVDD = 4.7 μF, CSS = 220 nF, COUT = 100 μF, TA = 25°C, UNLESS OTHERWISE SPECIFIED)

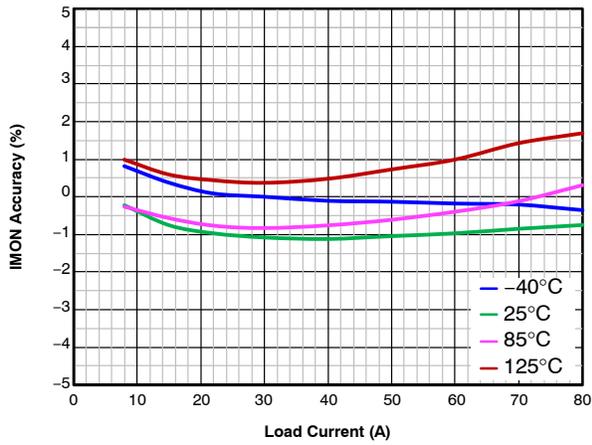


Figure 7. IMON Accuracy vs. Load Current and Temperature

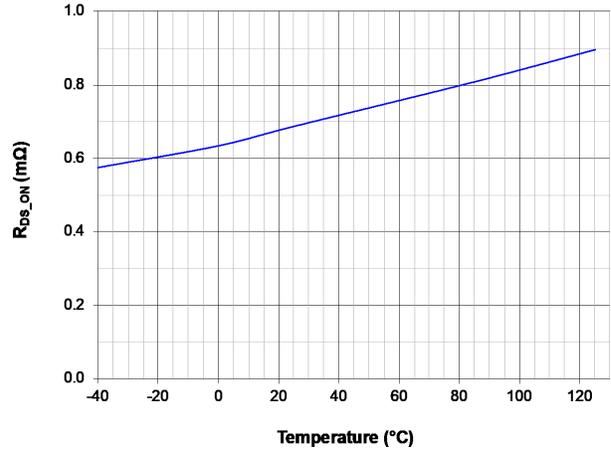


Figure 8. Switch RDS\_ON @ 8 A vs. Temperature

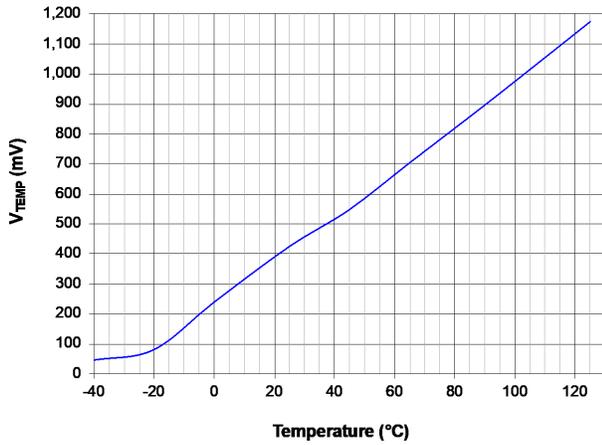


Figure 9. VTEMP vs. Temperature

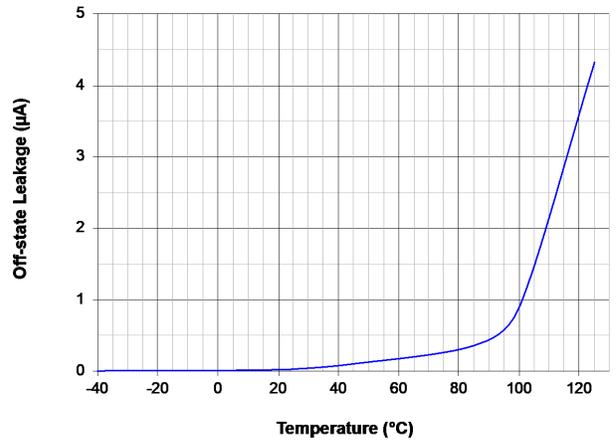


Figure 10. Switch Off-State Leakage vs. Temperature

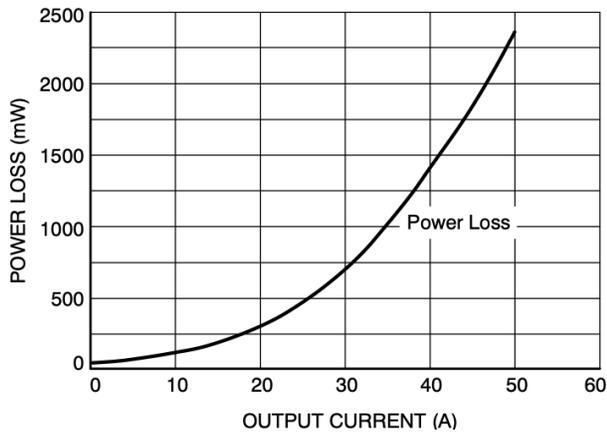


Figure 11. Power Loss vs. Current

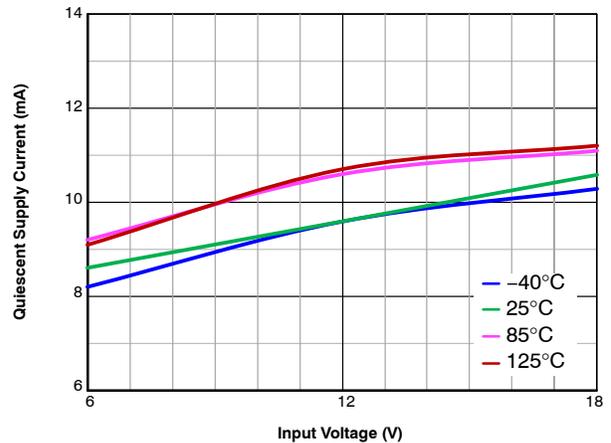


Figure 12. Quiescent Current vs. Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

(VIN = VINFINF = 12 V, CVINFINF = 0.1 μF, CVDD = 4.7 μF, CSS = 220 nF, COUT = 100 μF, TA = 25°C, UNLESS OTHERWISE SPECIFIED)

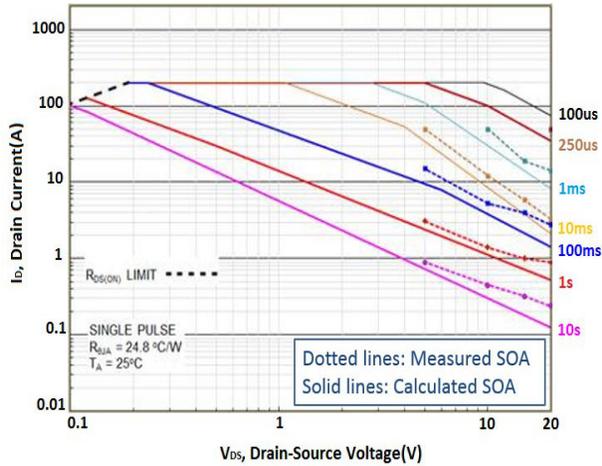


Figure 13. Power FETs Safe Operating Area

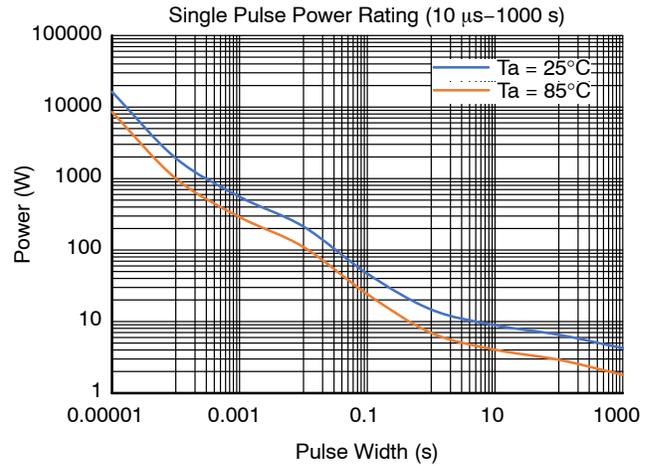


Figure 14. Single Pulse Power Rating (10 μs to 1000 s, Junction to Ambient, Note 6)

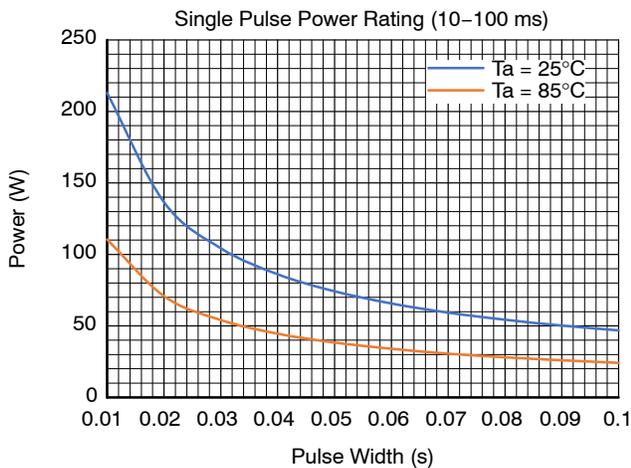


Figure 15. Single Pulse Power Rating (10 ms to 100 ms, Junction to Ambient, Note 6)

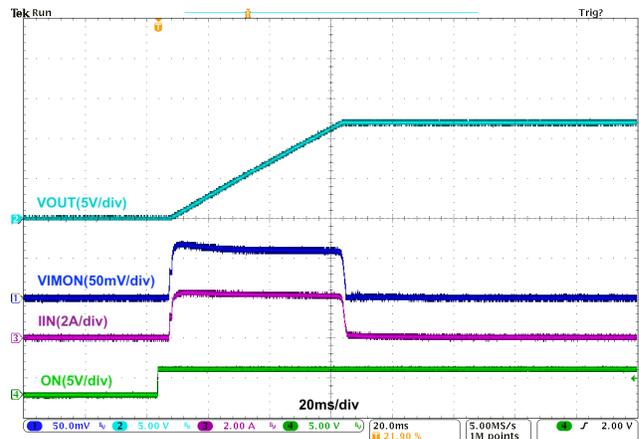


Figure 16. Start-up by ON, IOU = 0 A, COUT = 10 mF

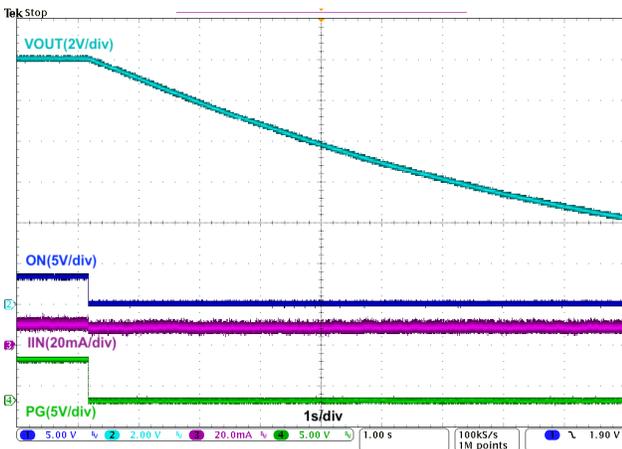


Figure 17. Shutdown by ON, IOU = 0 A, COUT = 10 mF, Output Pulldown Enabled

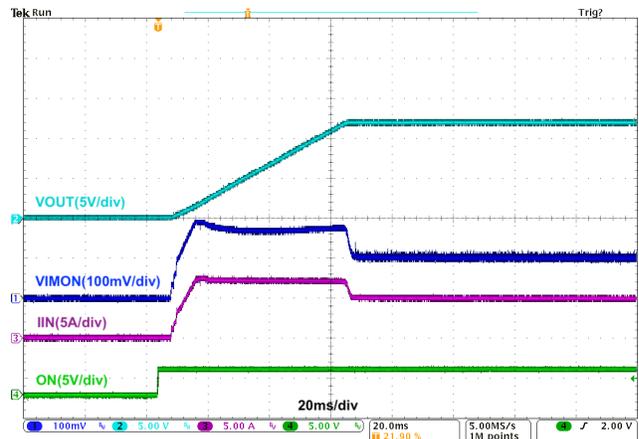


Figure 18. Start-up by ON, IOU = 5 A, COUT = 10 mF

TYPICAL CHARACTERISTICS (CONTINUED)

(VIN = VINF = 12 V, CVINF = 0.1  $\mu$ F, CVDD = 4.7  $\mu$ F, CSS = 220 nF, COUT = 100  $\mu$ F, TA = 25°C, UNLESS OTHERWISE SPECIFIED)

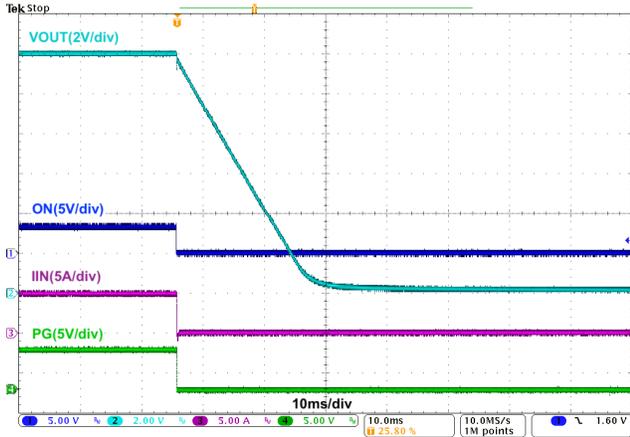


Figure 19. Shutdown by ON, IOU<sub>T</sub> = 5 A, COUT = 10 mF

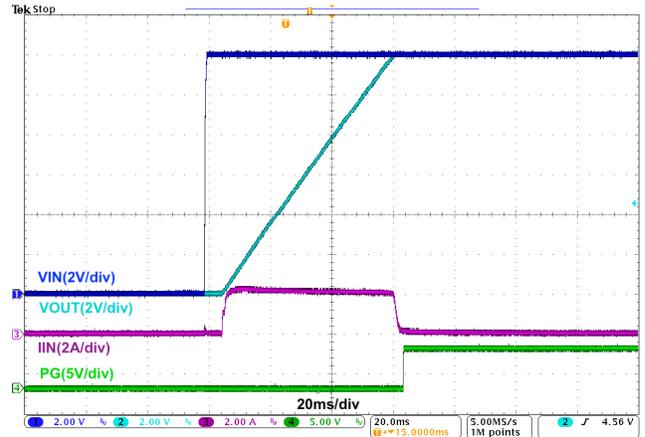


Figure 20. Start-up by VIN, IOU<sub>T</sub> = 0 A, COUT = 10 mF

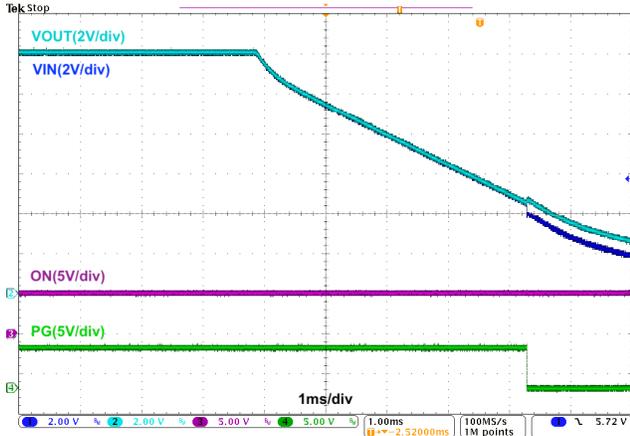


Figure 21. Shut-down by VIN, IOU<sub>T</sub> = 0 A, COUT = 10 mF

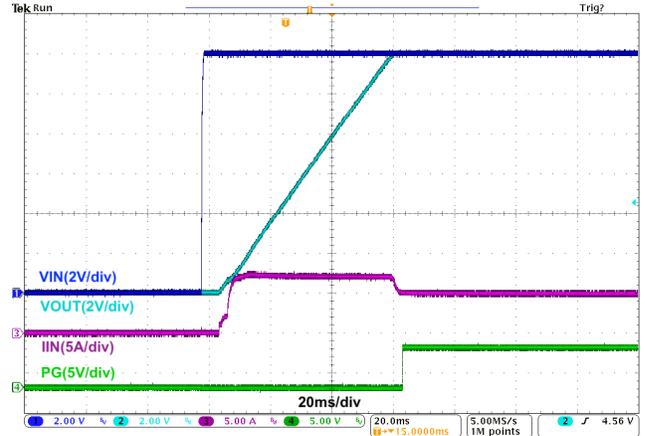


Figure 22. Start-up by VIN, IOU<sub>T</sub> = 5 A, COUT = 10 mF

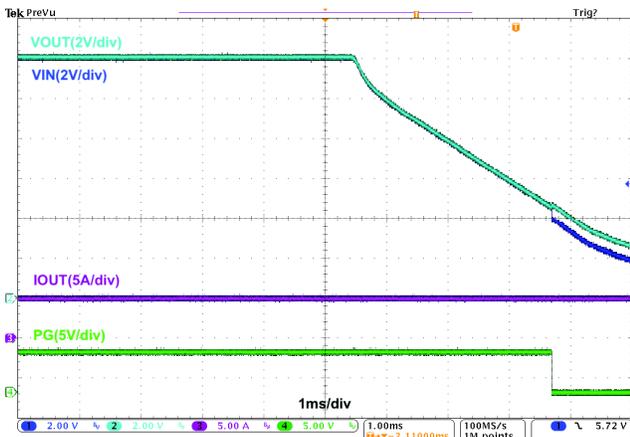


Figure 23. Shut-down by VIN, IOU<sub>T</sub> = 5 A, COUT = 10 mF

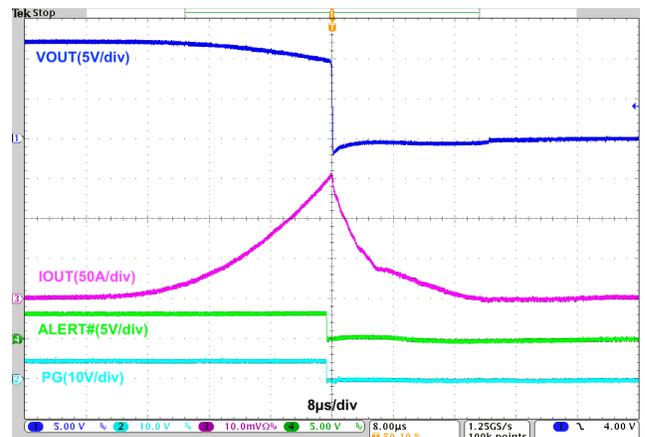


Figure 24. Short Circuit During Normal Operation, Initial IOU<sub>T</sub> = 0 A

TYPICAL CHARACTERISTICS (CONTINUED)

(VIN = VINFINF = 12 V, CVINFINF = 0.1  $\mu$ F, CVDD = 4.7  $\mu$ F, CSS = 220 nF, COUT = 100  $\mu$ F, TA = 25°C, UNLESS OTHERWISE SPECIFIED)

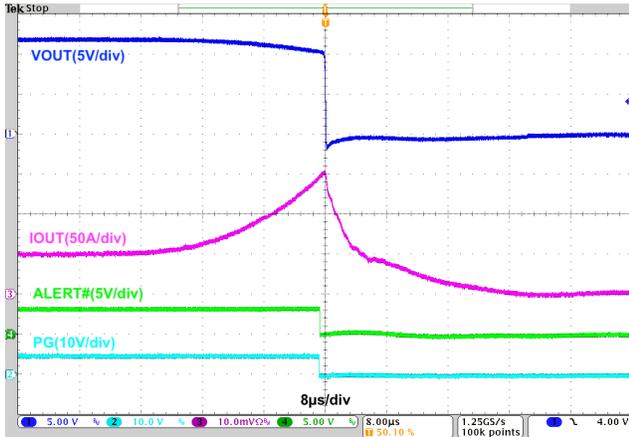


Figure 25. Short Circuit During Normal Operation, Initial IOU = 50 A

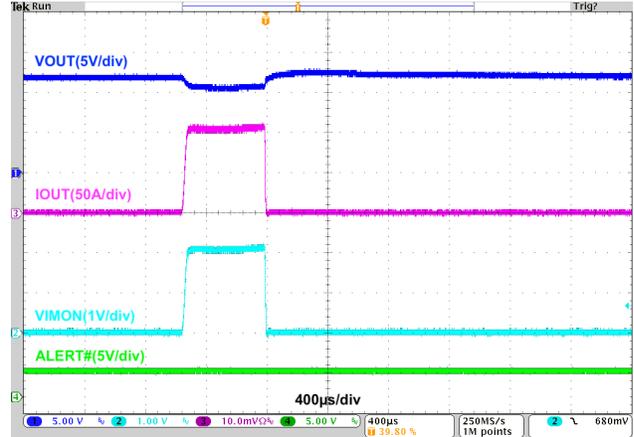


Figure 26. Over Current Protection During Normal Operation, OCP3 Level = 80 A, OCP3 Debounce Timer = 1 ms, Load Pulse Width = 500  $\mu$ s

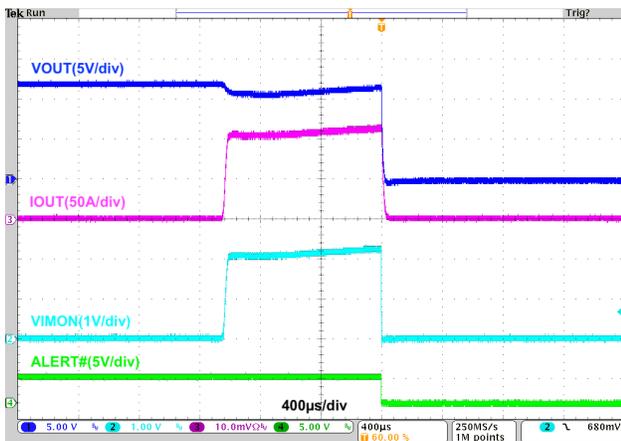


Figure 27. Over Current Protection During Normal Operation, OCP3 Level = 80 A, OCP3 Debounce Timer = 1 ms, Load Pulse Width = 1.5 ms

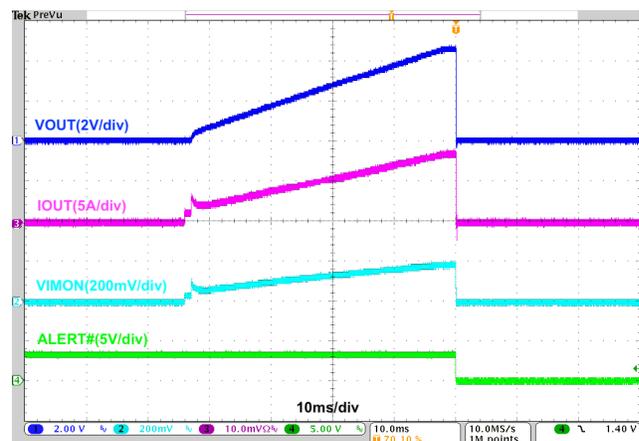


Figure 28. Over Current Protection During Softstart

## DEFINITIONS

### Definitions

The NCP81428 uses “Host”, “Master” and “Slave” terminology when referring to the operation of the NCP81428’s function in the application:

- A Host is the device which controls the PMBus
- A Master is an NCP81428 device that is a Slave to the Host, controls the NCP81428 Slaves’ On/Off Operation and/or the Two Wire Interface (TWI) via FAULT#\_C and FAULT#\_D.
- A device referred to as a Slave is controlled by the NCP81428 Master for enablement, TWI communication and fault reporting.

Please refer to the Master/Slave configuration and the TWI sections for further information.

### General Information

The NCP81428 is an electronically re-settable, fuse for use in server-based, high current 12 V hot-swap applications. The NCP81428 consists of a very low RDSon

NMOS pass device for minimal power dissipation and in using a copper clip leadframe improves heat transfer away from the power FET.

The device also contains a 10 bit ADC for accurate current, voltage and temperature measurements and the data is stored in user interface registers through the PMBus interface. The device also has two pins dedicated (Fault#\_C and Fault#\_D) for controlled start-up and shutdown between devices in parallel.

Additionally, the NCP81428 contains Non-Volatile Memory for storing user defined values for setting the Over-Current-Protection levels, the Over-temperature Fault Level and other parameters.

### Initialization

#### Master and Slave Initialization

The diagram below is the State Machine for the operation of the Master and Slave Device.

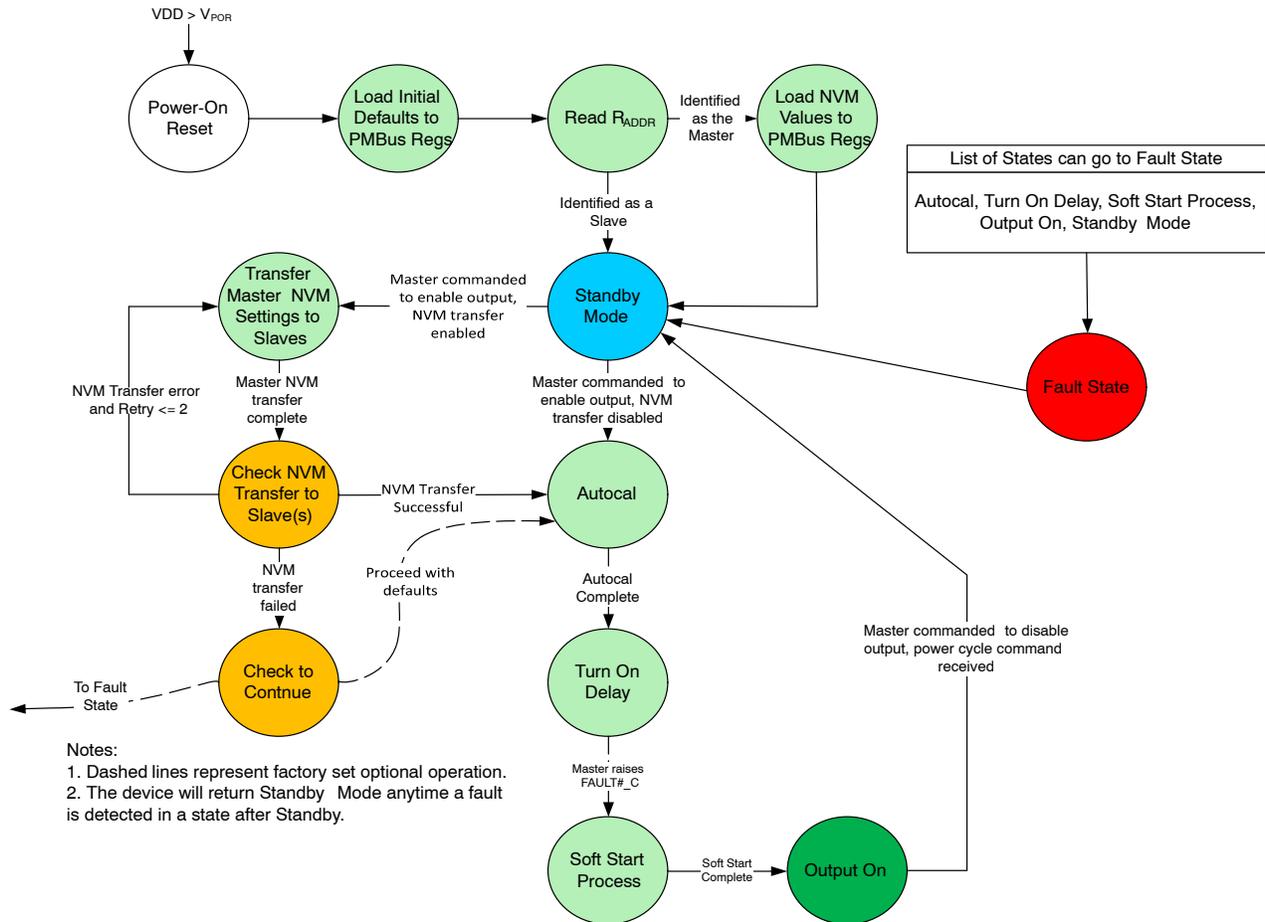


Figure 29. Master/Slave State Diagram

*Master/Slave State Machine Simplified Breakdown*

Upon applying power to the device, as the LDO output crosses the VDD UVLO threshold, the device's default values are transferred to the operating registers. Once the default values are loaded into the operating registers, the device reads the address resistor (R<sub>ADDR</sub>). During the read of R<sub>ADDR</sub>, the device determines whether it is connected to the PMBus, if it is a master (or single device) or a slave, and whether data transfer over the Two Wire Interface (TWI) will be utilized in parallel configurations.

Only masters will respond to its ON pin being driven high and/or the command through the PMBus to be enabled. Once in standby mode and the master is enabled, the devices can either proceed to Auto-Cal or start data transfer based on the ADDR resistor programmed configuration. If the master and slaves have data transfer enabled, FAULT#\_C and FAULT#\_D become CLK and SDA outputs from the master and inputs to the slaves only during data transfer. Once data is transferred, the slaves regain control over the FAULT#\_D pin and notify the master if there is data mismatch by asserting FAULT#\_D low. In the event there is an error in the data transfer, the master will attempt to transfer the data 3 times. If after three failures to transfer, there is a factory setting to either proceed with the default values or shutdown. Once in Auto-Cal, a t<sub>ON</sub> delay is built into the process to ensure the devices are ready before the Master simultaneously enables soft-start in itself and the slaves by asserting FAULT#\_C high. Note that there are four 8 $\mu$ s consecutive FAULT#\_C pulses that occur during the initial soft-start stage for gate pre-charge and synchronization between master and slaves to ensure a current balanced soft-start.

With the exception of during data transfer, in all modes starting at standby, FAULT#\_C is used for enabling all devices in parallel and signaling that the master has a fault and FAULT#\_D is used for any slave to signal that it has a fault.

The user is highly recommended to send a STORE\_USER\_ALL command when the device is in stand-by mode and not during normal operation just as PMBus protocol suggests as this may result in unpredictable and even catastrophic results. Once the user is satisfied with their custom settings and a STORE\_USER\_ALL command is sent, the second time the device gets powered-up (VDD recycle) the user settings get stored in the operating memory replacing the manufacturer's PMBus default values.

*Power-Up with VIN Release*

Once the voltage at VDD rises above VDD UVLO threshold, the device's LDO is always on irrespective of output enable status (ON pin or enable via PMBus). The device will then proceed to reading the ADDR configuration

resistor and load the factory set default values to the operating registers. Note that during the power up sequence, the NCP81428 forces a current out the ADDR pin to produce a voltage across the address resistor connected to the pin. By measuring the voltage with the internal ADC, the device is able to determine whether the device is to behave as a master or slave; whether it is to communicate across the PMBus and if data transfer from the master and slave(s) are enabled (Refer to Master/Slave Configuration sections for details).

For the first 2 ms after the VDD UVLO is reached, PMBus commands to the device are blocked to prevent writing to registers before the default values are loaded. If commands to the device are sent during the 2 ms blanking period, the device will respond by setting the busy bit in registers 0x78 and 0x79 and assert ALERT# low. For this reason, it is recommended that any changes to control registers be performed 2 ms or more after the VDD UVLO occurs and prior to enabling the device. Additionally, in parallel configurations where data transfer is enabled, the device will blank PMBus commands for approximately 2 ms after the master is enabled. During this period, the master will attempt to transfer stored settings in the Non-Volatile Memory to the slaves.

In parallel configurations, after the first 2 ms blanking, if there are no faults present, the slaves release FAULT#\_D to high. If the system is configured for data transfer, this indicates to the master that the slaves are ready for the data transfer. Then when the master is enabled, FAULT#\_C goes high, and data transfer begins. During data transfer, FAULT#\_D and FAULT#\_C are configured as output signals (DATA, CLK) respectively from the master device and input signals to the slave. The masters sends a series of high frequency pulses on FAULT#\_D to initiate the data transfer while FAULT#\_C is held high until the transfer begins. Once data transmission is complete, FAULT#\_C and FAULT#\_D pins on the master and slaves revert back to being Master and Slave fault indicators respectively. Then the master drives FAULT#\_C high signaling the slaves to begin soft-start simultaneously with the master.

The plot below showcases a simplified parallel eFuse application power-up event with data transfer enabled. The master device detects a VIN Over-Voltage fault at the end of soft-start and asserts FAULT#\_C to disable itself and the slaves. If a slave fault would have occurred instead, FAULT#\_D asserts low alerting the Master device which in turn asserts FAULT#\_C low, disabling all the NCP81428 devices simultaneously. Note that for a single device application, FAULT#\_C and FAULT#\_D are floating pins and data transfer is not applicable in such a case.

# NCP81428

Master and Slave(s) Device Data Transfer Enabled  
Power-up Event Followed by VIN OV Fault Event

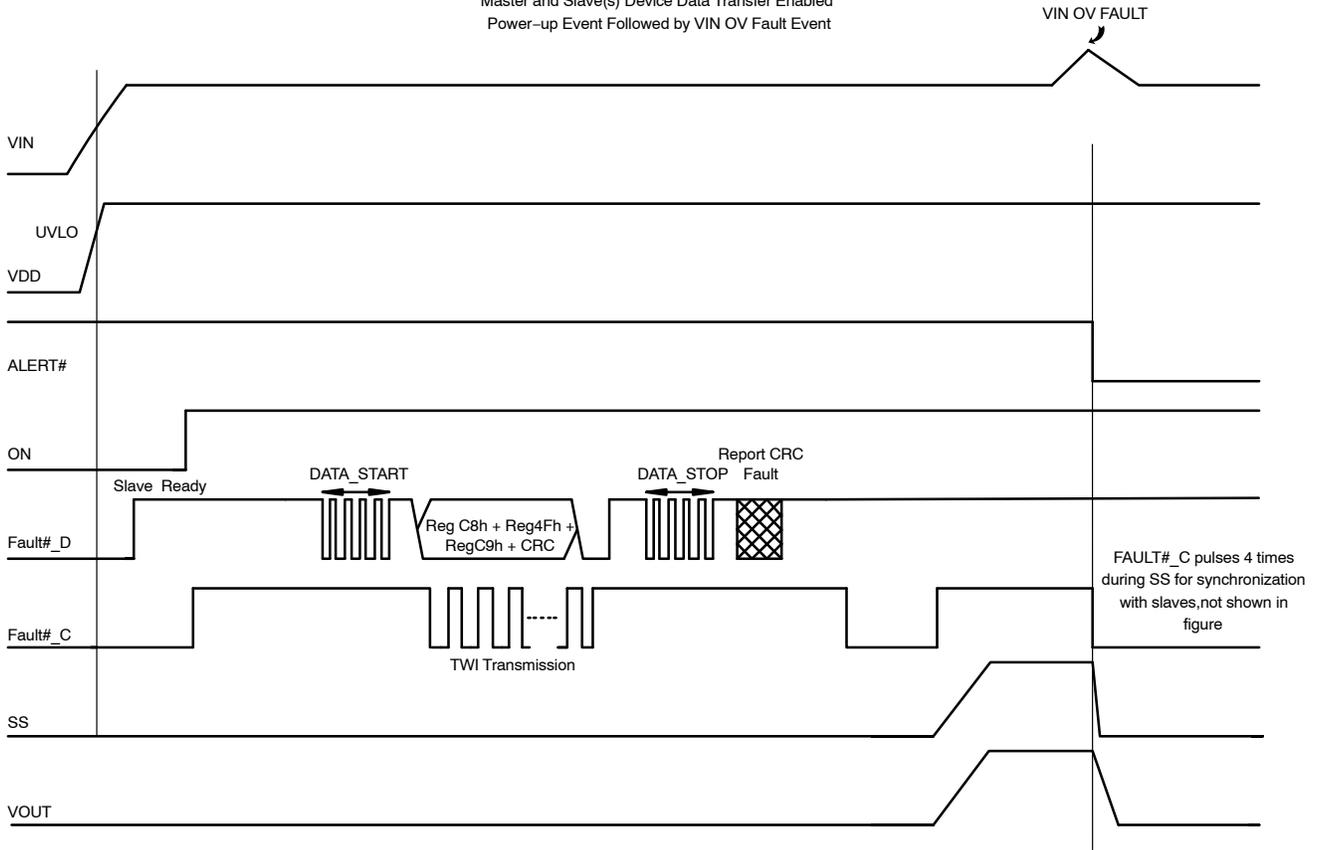


Figure 30. Data Transfer Sequence and VIN OV Fault

## Simplified System Block Diagram

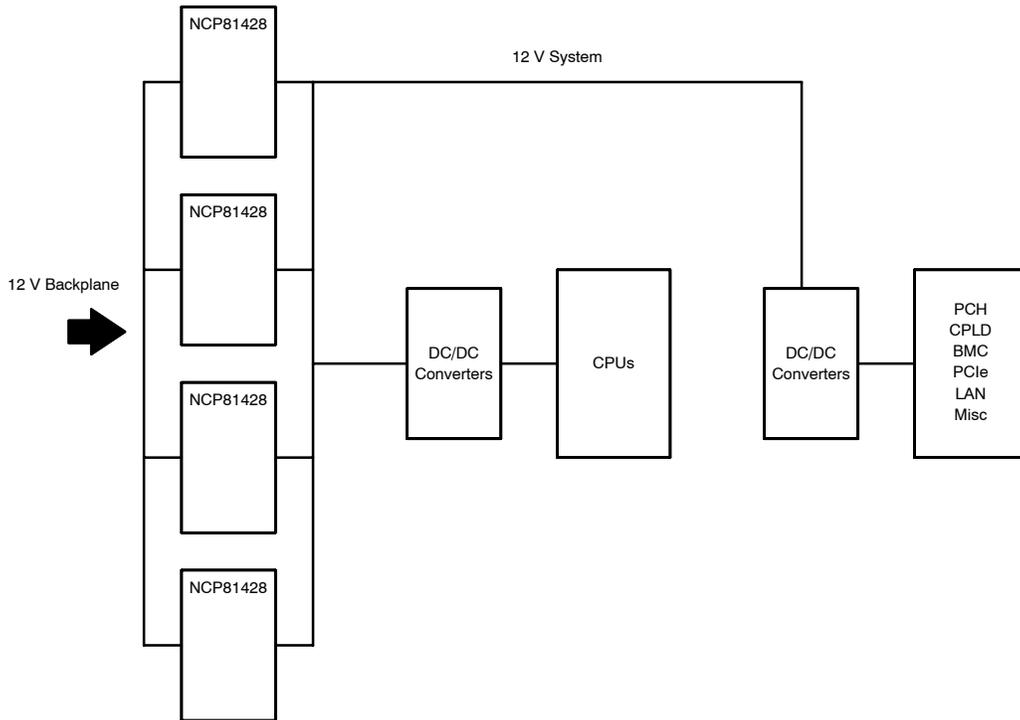


Figure 31. Simplified System Block Diagram

# NCP81428

## Configurations

### eFuse System Configuration

The four system configurations below represent ways the NCP81428 can be configured. In the three Master/Slave

configurations (Sub Figures B, C and D), only one slave is represented, but up to six slaves can be connected with the master.

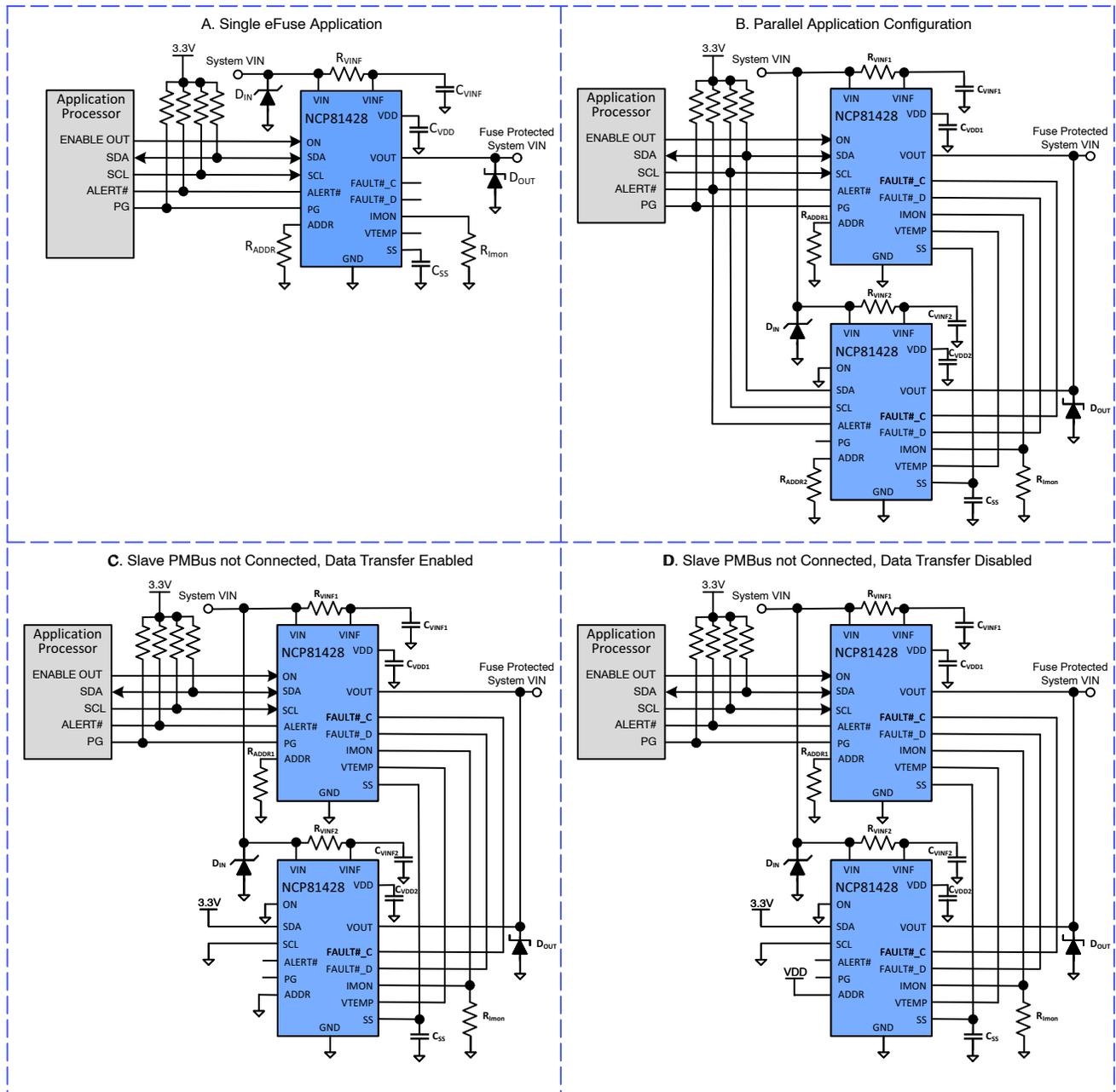


Figure 32. Four Possible PMBus and Data Transfer Configurations

**Table 1. MASTER/SLAVE CONFIGURATIONS** (Master enable Method: HW by asserting the ON pin high; SW by Software command)

	Description	Enable Method	PMBus	TWI	ADDR Pin Resistor
1	Single Device	ON and/or SW	Yes	No	20.0K NVM Data Transfer Disabled
2	Master	ON and/or SW	Yes	Only for Fault Communication	9.31K,14.3K NVM Data Transfer Enabled 20.0K NVM Data Transfer Disabled
	Single or Multiple Slaves	FAULT#_C pulled up by Master	Yes		26.7K to 73.2K NVM Data Transfer Enabled 86.6K to 182K NVM Data Transfer Disabled (Refer to ADDR pin Configuration for details)
	Single or Multiple Slaves		No		Pulled to VDD (NVM Data Transfer Disabled) Shorted to GND (NVM Data Transfer Enabled)

11. NVM will be blank the very first time the device turns on. The device will populate the manufacturer’s default settings the first time it powers-up. Once the user programs and sends a STORE\_USER\_ALL Command, all the user programmable PMBus registers will be stored in the NVM so that on the next power-up event the user settings will be loaded onto the operating memory. Once that procedure is complete, it is imperative not to alter the operating memory’s data prior to enabling the device as that will lead to discrepancies between what was stored in the NVM and what will be transferred during TWI if any of the transferable bits get changed. Refer to the simplified State Machine Diagram for details.

*Slave w/o PMBus Configuration*

The NCP81428 provides the capability to designate one device as the master with up to 6 other devices designated as slaves in parallel. With the NCP81428 having its own TWI communication, the Master can provide over-current, over-temperature protection and base address settings to the slaves from the Master’s on-board, non-volatile memory (NVM). Additionally, if any slave in the system identifies a fault, the slave will alert the Master device by pulling FAULT#\_D low. Upon capturing a FAULT#\_D logic low the master forces FAULT#\_C low to turn itself and all the slaves off. Utilizing the TWI bus features, communication and control can be entirely between the system’s application processor and the Master eFuse. This reduces the complexity and host activity for parallel eFuse applications.

Please refer to Figure 32C, PMBus Not Connected, Data Transfer Enabled. Tying the slave’s ADDR pin to ground disables PMBus communications and enables the NVM data transfer. When power is applied to the Slave and no LDO faults are detected on either master or slave(s) and the LDO outputs have settled, POR is generated, manufacturer’s default register values are populated. As the device gets enabled, the Master’s NVM registers C8h, C9h, 4Fh registers get transferred to all the slaves simultaneously via the FAULT#\_C and FAULT#\_D pins. Note that copying the Master’s NVM register data to the slaves is repeated every time the devices recover from a fault or power is removed and reapplied. The user must not alter the operating memory prior to enabling the device as that would cause a mismatch between what was written in the NVM and what gets transferred during the TWI process. Once the data transfer is complete, both the Master and the Slaves reconfigure their TWI bus pins to be a 2-wire fault notification system.

Please refer to Figure 32D, PMBus Not Connected, Data Transfer Disabled. Tying the slave’s ADDR pin to VDD disables both PMBus communications and the NVM data transfer. Once the master is enabled, the devices progress straight to Auto-Cal. And after the t<sub>ON</sub> delay, the master drives the FAULT#\_C high and soft-start begins.

Note that in configurations where the slave(s) are not connected to the PMBus, the ALERT# pin driver is disabled on the slave(s). However a fault event among a slave will be relayed to the master via FAULT#\_D which in turn asserts ALERT# to notify the host and FAULT#\_C low to disable all of the eFuses simultaneously.

*Slave w/ PMBus Configuration*

Please refer to Figure 32B, PMBus Connected W/ and W/O Data Transfer.

In parallel applications, a master/slave that are on the PMBus have to be configured as shown in the ADDR pin configurations table (Table 6) in order to enable or disable TWI data transfer.

The ALERT# pins of the master and each slave are tied together and to the system’s application processor (Host). This way, any master or slave warning or fault will result in the device pulling the ALERT# low to notify the Host per PMBus standards. Additionally, any condition which results in the Master or a Slave to shut off its output, will result in the Master pulling down on the PG pin. An example of both ALERT# and PG being pulled down is an OCP condition. As soon as the Master recognizes an over current condition, it starts the debounce timer defined in register C9h. If the Over-Current still exists at the end of the timer, ALERT# goes low (if not masked) and FAULT#\_C asserts low disabling the master and slave device(s) simultaneously, PG asserts low and Vout discharges.

When the master’s 0xC9 register has been configured for Retry and a Slave has faulted, in order to identify the fault, the Slave’s Status registers need to be polled within 125 ms of the Alert# going low in order to capture the source of the fault before the slave registers are reset upon the Master re-enabling the devices by asserting FAULT#\_C high.

Another possible configuration is enabling TWI data transfer while a slave is on the PMBus.

Refer to the ADDR pin configurations table (Table 6) for selecting the proper resistor values for both master and slave devices. In order to alleviate PMBus write transactions

among multiple devices on the board, the TWI interface allows the master constants in regC8h, 4Fh and C9h to be transferred to the slaves. The user simply stores the Master’s operating memory in the master device’s NVM using the Store\_User\_All command and on the next power cycle, the master transfers the aforementioned registers to the slaves. Then the slaves only need to be addressed for telemetry readback and cases of a faults or warnings.

**Inputs/Outputs**

*VDD Output (Auxiliary Regulated Supply)*

An internal linear regulator draws current from the VIN pin to produce and regulate the voltage at the VDD pin. This auxiliary output supply is current limited to I<sub>DD\_CL</sub>. A 4.7 μF ceramic capacitor must be placed between the VDD and GND pins and as close as possible to the NCP81428. The voltage difference between the VIN and VIN pin voltage should be within 0.4 V for adequate IMON performance. A small time constant R/C filter such as 1 Ω/0.1 μF on the VIN pin is recommended. The VDD pin is intended to power internal circuitry in the NCP81428. Do not connect any load to the VDD pin. Doing so, may result in erratic behavior.

*Single Device Sequence*

When the ON pin voltage is higher than V<sub>SWON</sub> and no Under-voltage (UVLO) or output switch faults are present, SS begins after the t<sub>ON</sub> timer set by the device. To ensure consistent behavior, a weak internal 1 MΩ pull down resistor holds the pin low if the pin is left floating and 100 mV of hysteresis reduces the likelihood of chatter.

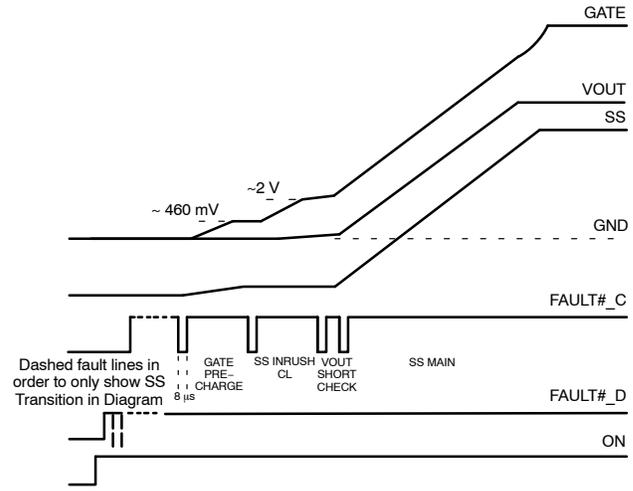
*Simplified Parallel Configuration Enabling and Soft-Start Synchronization Diagram*

When the V<sub>ON</sub> > V<sub>SWON</sub>, no UVLO or output switch faults are present and FAULT#\_D is driven high, depending on ADDR configuration, TWI data transfer will or will not occur. Once the t<sub>ON</sub> timer elapses, the master device initiates the SS sequence by enabling itself and the slaves with three 8 μs FAULT#\_C logic high pulses which pre-charge the gate, synchronize the devices to current share adequately, check for output short conditions and gear up for the main soft-start with a fourth logic high on FAULT#\_C. The Figure 33 showcases how the slave releases FAULT#\_D line to indicate readiness for the master and upon receiving a logic high on the ON pin the master pulls up the FAULT#\_C. Various state machine transitions were skipped as depicted by the dashed lines since this plot concentrates on enablement and soft-start sequencing.

*SS Output (Soft Start)*

When the power switch first turns on, it does so in a controlled manner. The output voltage (VOUT) follows the voltage at the SS pin, produced by current I<sub>SS</sub> into a capacitor (C<sub>SS</sub>). In parallel eFuse applications, the SS pins of all fuses should be shorted together to one shared SS capacitor, note that only the master device will source out the 5 μA current to initiate soft-start. The internal soft-start load

balancing circuitry will ensure the soft-start currents are evened out among the NCP81428 devices so that it doesn’t put stress on one device over another or cause a soft start-current limiting event.



**Figure 33. Soft Start Signals**

The soft-start capacitor value can be calculated by the following equation:  $C_{SS} = (t_{SS} \times I_{SS} \times AV_{SS}) / V_{IN}$  (where t<sub>SS</sub> is the target soft-start time and the recommended range is 10–110 ms).

The typical C<sub>SS</sub> values for different t<sub>SS</sub> are approximated below for 12 V VIN.

The calculated soft-start times in Table 2 reflect the time when VOUT begins charging up from ground level to VIN. This does not include the gate pre-charge and synchronization delays before the main soft-start event.

**Table 2. SOFT START PROGRAMMING CAPACITOR**

T <sub>SS</sub> (ms)	C <sub>SS</sub> (nF)
12	47
20	82
29	120
43	180
52	220
64	270
78	330
110	470

The maximum load capacitor value NCP81428 can power up depends on the device soft-start time.

*IMON Output (Current Monitor)*

The IMON pin sources a current that is A<sub>IMON</sub> (10 μA/A) times the VOUT output current. A 2 kΩ resistor connected from the IMON pin to ground must be used to monitor current information as a voltage up to V<sub>IMON\_CLMP</sub>. A 100 nF capacitor can be used to low-pass filter the IMON

signal without affecting the internal operation of the device. In parallel applications, the IMON pins of all eFuses should be tied together. Connect a 2 kΩ resistor from the IMON pin of each eFuse to the ground. The total equivalent IMON resistance would be 2 kΩ/#D, where #D is the number of eFuses in parallel. In order to simplify the BOM, one single R<sub>IMON</sub> resistor with the value of 2 kΩ/#D can be used across all IMON pins and the ground.

**VTEMP Pin**

The VTEMP pin is a voltage output proportional to the device’s temperature, with an offset voltage (420 mV at 25°C). The VTEMP output can source much more current than it can sink, so that if multiple VTEMP pins are connected together, the voltage of all VTEMP outputs will be driven to the voltage produced by the hottest NCP81428 device in the application. Note that in parallel of the device applications, register 0x8D represents the temperature being addressed through the PMBus, whereas register 0x6C represents the hottest device among the paralleled eFuses. In most cases when appropriate layout and proper component placement is followed, the eFuse die temperatures should be relatively close amongst the parallel devices. But if the die temperature indicated in register 0x6C becomes 20°C greater than that in the master’s 0x8D register, the master’s ALERT# signal will assert to notify the host that an eFuse is operating at a higher die temperature compared with the master and the dev\_temp\_warn bit will set.

**Auto Retry and Latch-Off through PMBus**

When the Retry\_Latchoff bit in register C9(h) is set to 1, the NCP81428 enters auto-retry mode. In this mode under

certain fault conditions, the FET is turned off and a new soft-start procedure takes place. Between the fault and the new soft-start, there is a delay of t<sub>DLY\_RETRY</sub>. The protection features that cause an auto-retry event are:

- Over-Current Protection
- Soft-Start Current Limiting Fault
- Short-Circuit Detection
- Over-Temperature Fault
- Excessive Soft-Start Duration Violation
- VIN OV and VIN UV Faults
- VIN to GATE Short

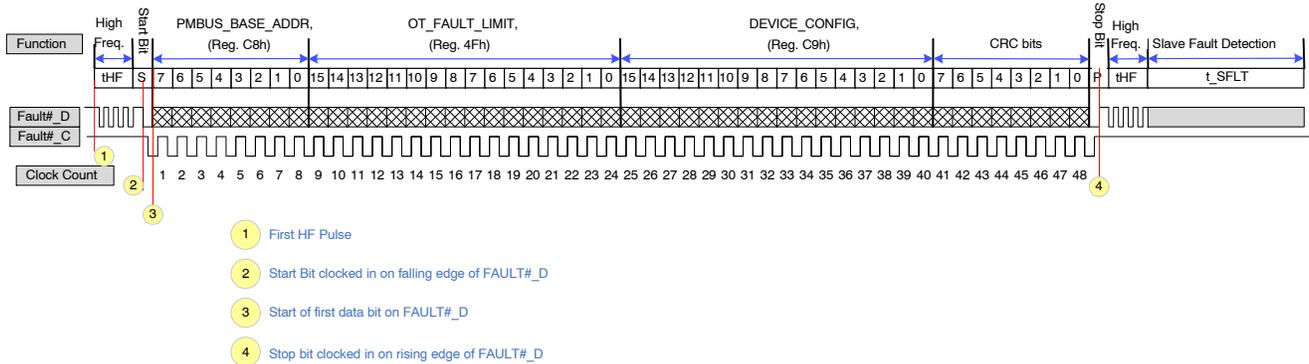
A VIN to VOUT short condition is non-latching/non-auto-retry. If the device is disabled and VOUT > VDS\_TH the device is prevented from powering up. The device is allowed to power up once VOUT < VDS\_OK.

When the Retry\_Latchoff bit is set to 0, the NCP81428 is in latch-off mode. If a fault occurs, the device remains off until either the ON pin is toggled or when VDD is recycled.

Note that the Retry\_Latchoff bit is ignored in a slave device as the decision to restart is controlled solely by the master.

**Data Transfer Sequencing**

Figure 34 below represents the sequence of starting, transferring, checking, stopping and validation of the data transfer from the Master’s NVM values to the slaves. During data transfer, the clock frequency will be a typical 400 kHz and the entire process will take approximately 120 μs.



**Figure 34. Master to Slave NVM Content Transfer Sequence**

Warnings

Table 3. WARNINGS SUMMARY

Warning Type	Master/Slave	ALERT#	FAULT#_C	FAULT#_D
VIN_OV	Master	H	H	H
VIN_UV			H	H
Over_Temperature	Master	H	H	H
	Slave			

In a Master/Slave Configuration, only the Master reports a VIN\_OV or VIN\_UV warning condition. If the user wishes to communicate with a slave device, then a valid resistor value should be selected to program the slave address. If no communication is necessary with the slaves, then connect the address pin(s) to ground. Note that in the case of no communication with PMBus on the slave, the alert pin driver gets disabled and ALERT# stays high all the time.

FAULT#\_C and FAULT#\_D Operation

FAULT#\_C and FAULT#\_D are used for initiating soft-start and proper sequencing but also for fault communication between master and slave devices. Under normal operating conditions FAULT#\_C and FAULT#\_D are set in the high state. The tables below summarize the master / slaves actions upon a fault condition.

Table 4. MASTER FAULT#\_C AND FAULT#\_D FAULT BEHAVIOR

Master Faults	FAULT#_C	FAULT#_D	Notes
SS Current Limit, VDD UVLO, FET Health, OCP, SCP, VIN UV/OV, OT	H to L	H	Master FET health includes (VGS/ VDS/VGD and SS timer faults)
TWI Fault	*H to L	H to L	Three consecutive data transmission failures / CRC mismatch and Device configured to not continue when TWI fails

NOTE: In a Master/Slave system, only the master monitors VIN and VOUT related faults. As for a TWI related fault, only the master will set the twi\_fault bit 2 in reg 0x80, STATUS\_MFG\_SPECIFIC register. Any fault can have ALERT# masked as described in register (1Bh) SMBALERT\_MASK.

Table 5. SLAVE FAULT#\_C AND FAULT#\_D FAULT BEHAVIOR

Slave Faults	FAULT#_C	FAULT#_D	Notes
SS Current Limit, VDD UVLO, FET Health, OCP, SCP, OT**	*H to L	H to L	Slave FET health includes (VGS and VGD faults)

\*Represents a delayed signal on the master upon receiving a FAULT#\_D low from the slave

\*\*Represents that a Slaves OT Fault range is from 120.5°C to 150°C. The Master is responsible for OT faults outside of this range. 12.A typical FAULT#\_D to FAULT#\_C delay is 500 ns.

ADDR Pin Configuration

The NCP81428 offers various types of parallel configurations to select from based on the application’s needs. In a master/slave configuration, the NCP81428 allows the user to choose to communicate with the slaves or not. The purpose of this is to reduce host activity by communicating with just the master device.

Table 6. ADDR PIN DEFINED CONFIGURATIONS

Device	R_ADDR (kΩ)	PMBus	Address	TWI Data Transfer	
Master	9.31	YES	Base + 00h	Enabled	
	14.3		Base + 01h	Enabled	
	20.0		Base + 02h	Disabled	
Slave	26.7	YES	Base + 03h	Enabled	
	34.0		Base + 04h	Enabled	
	42.2		Base + 05h	Enabled	
	51.1		Base + 06h	Enabled	
	61.9		Base + 07h	Enabled	
	73.2		Base + 08h	Enabled	
	86.6		Base + 09h	Disabled	
	102.0		Base + 0Ah	Disabled	
	118.0		Base + 0Bh	Disabled	
	137.0		Base + 0Ch	Disabled	
	158.0		Base + 0Dh	Disabled	
	182.0		Base + 0Eh	Disabled	
	Ground		NO	N/A	Enabled
	VDD				Disabled

PowerGood

The NCP81428 provides a dedicated PG pin to indicate that output voltage is within a range relative to the input voltage. The PG pin is an open drain signal that is held low during soft-start until the output voltage reaches approximately Vin and VGS > 6.3 V. Once those conditions are met, the PG pin will be released, the PG\_STATUS# bit will clear as full load can be applied across the device. PG pin will assert low during fault events or when the NCP81428 is commanded by the host to be disabled (PG\_STATUS# bit will set), but will remain high during warning events. During a thermal shutdown event, if the device is programmed for auto retry mode, the PG pin will be held low until the die temperature drops below the OT\_WARN\_LIMIT and tDLY\_RETRY elapses, which prompts a new soft-start sequence.

PG can go high again upon meeting the conditions described above for VGS and VOUT.

Since PG is an open drain signal, it requires an external pull-up resistor (see Applications Diagrams).

**IMON Peak**

The IMON Peak detection circuit samples and holds the IMON voltage to represent the peak current value upon entering an OCP event. The peak current can be read in register 0xC4 which is a READ/CLEAR register. Once the register is read, it is automatically cleared. If not read and the device encounters a peak that is higher than the previous peak current captured by the device, then the later peak will be populated in the register replacing this former value. Toggling the ON pin does not clear this 0xC4 register, the device instead, holds the peak value until the register is read.

**Protection Features**

*Current Limiting During Start-up*

During startup, the NCP81428 current limits are dependent on a number of factors such as VIN and VOUT levels relative to VIN.

**Table 7. FOR VIN < 13.2 V**

VOUT/VIN	IcsLO
0 < VOUT < 0.4 x VIN	7.5 A (Typ)
0.4 x VIN < VOUT < 0.8 x VIN	15 A (Typ)
0.8 x VIN < VOUT < VOUT-VIN	30 A (Typ)

**Table 8. FOR VIN > 13.2 V**

VOUT/VIN	IcsHI
0 < VOUT < 0.4 x VIN	5 A (Typ)
0.4 x VIN < VOUT < 0.8 x VIN	10 A (Typ)
0.8 x VIN < VOUT < VOUT-VIN	20 A (Typ)

As VOUT is approximately equal to VIN and PowerGood goes high the device stops current limiting and Over Current Protection becomes active.

If a current limiting condition exists anytime for a continuous duration > tCL\_REG, then the device latches off. If the NCP81428 is programmed for auto-retry mode, then the device will try to softstart after the tDLY\_RETRY elapses.

*Soft Start Duration*

If VOUT < VOUTL\_TH when tSS\_FLT expires, the NMOS FET latches-off or restarts based on the Retry\_Latchoff bit setting. Note that a VGS fault (VGS < VG\_TH) can also cause an excessive soft-start duration fault. Both conditions have to be met at tSS\_FLT, otherwise a fault will occur.

*Short Circuit Detection*

The NCP81428 contains a high-bandwidth current sense SCP amplifier monitoring and rapidly responding to severe shorts which may cause irreparable damage. The fast current loop circuit allows the device to start pulling the gate low within the tSC limit from the time it senses the fault. Once the Power FET turns off, it either is restarted or remains latched off depending on the bit setting set in the Retry\_Latchoff

Register under Device Configuration. The short-circuit current threshold is fixed and not user programmable.

*Over Current Protection*

The NCP81428 provides three programmable levels of over current protection (OCP) in register 0xC9. OCP1 provides the lowest current range while OCP3 allows up to 80 A before the device determines an overcurrent condition.

OCP1 and OCP2 settings can work in parallel to provide a case where a longer timer can be used for OCP1 and a shorter timer for OCP2 such that the energy during a fault remains similar and below the SOA of the device for the application. If the current levels in OCP1 are not a concern for the application, set ocp1\_level to 00b (None).

OCP3 is reserved for higher operating current applications. In order for the OCP3 level to work properly, both ocp1\_level and ocp2\_level should be set to 00b (None).

Each OCP level can be programmed for a debounce time of 0.25 to 50 ms to determine if the fault is valid. Reg. 0xC9 contains the debounce timers (ocp1\_delay, ocp2\_delay, ocp3\_delay). A reset timer is also implemented such that if the current level exceeds the OCP setting, but returns to a value below the hysteresis of the OCP threshold for a minimum of 100 μs before the debounce timer expires, the debounce timer will reset. Expiration of the OCP debounce timer in a single device configuration will result in the device disabling the output. In a Master/Slave configuration, if an OCP debounce timer expires on a Slave, the Slave will pull FAULT#\_D low to signal the Master of a fault. In the case of the Master determining an OCP fault, it will pull FAULT#\_C low to disable the Slaves and itself.

*Over Temperature Shutdown*

The NCP81428 employs an internal thermal sensor for monitoring the die temperature. If the junction temperature surpasses the thermal warning threshold set in register OT\_WARN\_LIMIT (51h), the bit in the STATUS BYTE register sets. Upon surpassing the warning limit, the Host is notified to take the appropriate actions. If the Host does not respond to the temperature warning event, as the junction temperature continues to rise when it exceeds the thermal shutdown fault threshold set in OT\_FAULT\_LIMIT (4Fh) the device will shut off. After thermal shutdown, the NCP81428 recovery mode depends on the Retry\_Latchoff bit setting in Device Config. If retry mode is selected, when the die temperature falls below the OT\_WARN\_LIMIT, the device restarts. If programmed in latch-off mode, the device has to be re-enabled for a restart and will only restart after the temperature falls below OT\_WARN\_LIMIT. Note that if the OT\_FAULT\_LIMIT is set lower than or equal to the OT\_WARN\_LIMIT threshold, an invalid data fault sets.

*FET Fault Detection (FET Health)*

The device contains various FET monitoring circuits:

## NCP81428

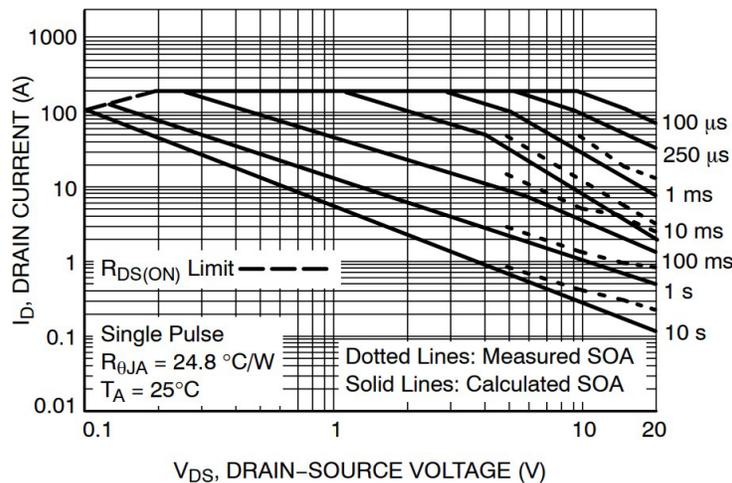
- VIN to VOUT short, non-latching/non-auto-retry condition. If the device is disabled and  $V_{OUT} > V_{DS\_TH}$ , then ALERT# is pulled low and the device is prevented from powering up. The device is allowed to power up once  $V_{OUT} < V_{DS\_OK}$ .
- GATE to VIN short, latching/auto-retry condition. If the device is disabled and  $V_{GATE}$  (Pin 8)  $> V_{DG\_TH}$ , then ALERT# is pulled low and device latches/auto-retries.
- GATE leakage, If  $(V_{GATE} - V_{INF}) < V_{G\_TH}$  after  $t_{SS\_FLT}$ , then ALERT# is pulled low and the device latches/auto-retries.

Note that only the master monitors a VIN to VOUT short. Whereas the other two faults mentioned above are monitored across both master and slave. FAULT#\_C and FAULT#\_D will pull low depending on the offending

device. For instance, a slave device experiences a gate leakage at  $t_{SS\_FLT}$  then it will assert FAULT#\_D alerting the master which in turn asserts FAULT#\_C to disable itself and the slave(s) simultaneously.

### FET SOA Limits

The NCP81428 has built-in current limits and fault-monitoring circuits to ensure that the co-packaged NFET is always kept within SOA limits. The startup current limiting conditions adjust based on the input voltage levels as described in the electrical specifications table to ensure constant power across the device throughout the soft-start transition. Refer to the internal current sensing section for more details. Note that the NCP81428 does not limit the current during an OCP event, the powerFET is always in the linear region.



Internal FET's Safe Operating Area (SOA)

Figure 35. Power FET Safe Operating Curves

### VIN OVP and UVP

The NCP81428 has a programmable VIN Over-Voltage Protection feature that allows the user to set the input over voltage fault threshold. The VIN\_OV\_FAULT\_LIMIT in register (55h) has two data bytes encoded in linear11 format with 5 bits unsigned exponent and 11 bits mantissa. Refer to register 55h for range, resolution and programmability. The VIN\_OV\_FAULT thresholds are comparator based in order to respond swiftly to a fault whereas the VIN\_OV\_WARN thresholds are ADC based. The device also has a VIN under voltage protection feature that is fixed to 4.55 V (typ) rising with 0.10 V (typ) hysteresis.

### GOK Bit

The GOK bit in the STATUS\_MFR\_SPECIFIC Register is meant to report faults under the following conditions:

- V\_ON disabled and V\_DS\_OK is false (indicates a VIN to VOUT short) – the device is allowed to power-up when the short is cleared
- V\_ON disabled and V\_GD\_OK is false (indicates a VIN to GATE short) – device latches off or auto-retries depending on latch\_off\_auto\_retry\_bit
- V\_ON enabled and V\_SS\_OK is false at  $t_{SS\_END}$  (indicates either  $V_{OUT} < 90\%V_{IN}$  or  $V_{GS}$  below  $V_{G\_TH}$  at the end of soft-start) – device latches off or auto-retries depending on latch\_off\_auto\_retry\_bit

**PMBus Address**

*PMBus Addressing*

The NCP81428's PMBus Default Base Address is 0x64.

**Table 9.**

Binary Address							
7	6	5	4	3	2	1	0
1	1	0	0	1	0	0	R/W

READ = 1

WRITE = 0

Refer to register (0xC8) for reprogramming the PMBus Base address selection. Note, care should be taken in parallel configurations to ensure no values are used which are not permitted by the SMBus standards.

*Commands w/o PEC*

The Send Byte transaction is used to send a simple command to the device. A send byte transaction transfers a command with no data. The CLEAR\_FAULTS command is one example of a Send Byte command.

A start bit followed by the 7 bit slave address with a 0 (write) appended comprises the first stage of the transaction. If the slave ACKs the address, then the host sends the 8 bit command followed by a stop condition. A format example is shown below:

1	7	1	1	8	1	1
S	Slave Address	W	A	Command Code	A	P

Send Byte

**Figure 36. Send Byte**

The Read Byte starts like a typical I<sup>2</sup>C write transaction by sending the slave address, plus write bit, followed by a 2<sup>nd</sup> byte containing the command code. Then repeated start (SR) is sent, followed by the slave address with read bit (1), requesting the slave device to return the data for the specified command code. The slave responds by transmitting the byte value requested.

1	7	1	1	8	1	1	7	1	1	8	1	1	
S	Slave Address	W	A	Command Code	A	S	R	Slave Address	R	A	Data Byte	N	P

Read Byte

**Figure 37. Read Byte**

The Read Word transaction also starts like a typical I<sup>2</sup>C write by sending the slave address, plus write bit. The 2nd byte contains the command code. Then repeated start is sent, followed by the slave address with read bit, signaling the device to return data for the specified command code. The slave responds by transmitting the value requested, low data byte first, followed by the high data byte, as illustrated below:

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1	
S	Slave Address	W	A	Command Code	A	S	R	Slave Address	R	A	Data Byte Low	N	Data Byte High	N	P

Read Word

**Figure 38. Read Word**

The Write Byte transaction is used by the host to send a single byte of data to the device. The OPERATION command, used to configure the device operation, is an example of this type of transaction.

The transaction begins with a start bit followed by the 7 bit slave address with a 0 (write) appended as the 8th bit, the command byte followed by the data byte, as illustrated below:

1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Byte	A	P

Write Byte

**Figure 39. Write Byte**

The Write Word transaction is used by the host to send a single word of data (2 bytes) to the device. The SMBALERT\_MASK command is an example of this type of transaction.

Similar to the write command, the only difference is that after the low data byte's ACK (3<sup>rd</sup> ACK), the high data byte is sent in addition.

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

Write Word

**Figure 40. Write Word**

*Packing Error Checking (PEC)*

PEC is an optional implementation in the PMBUS devices, but is highly recommended due to the critical nature of the data validity in power management systems. Packet Error Code bytes are generated using CRC-8 algorithm that is based on performing XOR operations on the input bit streams with a fixed CRC polynomial. The PEC byte is calculated on all bytes in the I<sup>2</sup>C transaction, including device address and read/write. PEC does not include start, stop, ACK/NACK or repeated state bits. Below are shown the Read and Write functions with the PEC byte included.

1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	PEC Byte	A	P

Send Byte with PEC

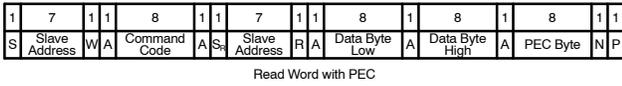
**Figure 41. PEC Send Byte**

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1	
S	Slave Address	W	A	Command Code	A	S	R	Slave Address	R	A	Data Byte	A	PEC Byte	N	P

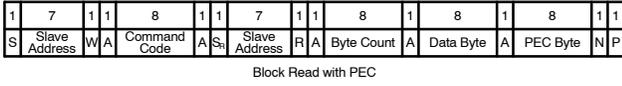
Read Byte with PEC

**Figure 42. PEC Read Byte**

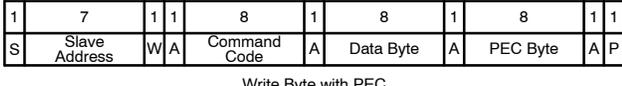
# NCP81428



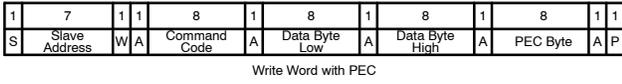
**Figure 43. PEC Read Word**



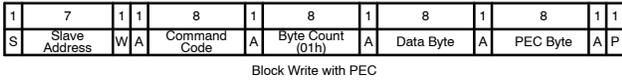
**Figure 44. PEC Block Read**



**Figure 45. PEC Write Byte**



**Figure 46. PEC Write Word**



**Figure 47. PEC Block Write**

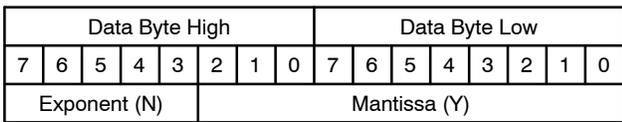
### Data Byte Format

Various NCP81428 commands utilize different data byte encoding to accommodate negative numeric values, step size, and range supporting DAC and ADC values.

The type used is designated individually for each register of the PMBus COMMAND DETAILS section of this document.

### Linear11 format

The Linear11 format consists of 5-bit, 2's complement integer exponent and 11 bit linear mantissa, shown below:



LINEAR11 Format

**Figure 48. Linear11 Format**

The exponent value is a fixed binary value, positive or negative, which typically determines step size or resolution for a given command. The mantissa is an 11-bit 2's complement integer typically establishing the range and be selective limited to discrete values.

The integer (1) of the data byte in LINEAR11 format can be calculated using:

$$I = Y \times 2^N \quad (\text{eq. 1})$$

where: Y is a 2's complement integer from the mantissa and N is the 2's complement integer of the exponent

### ULinear16 Format

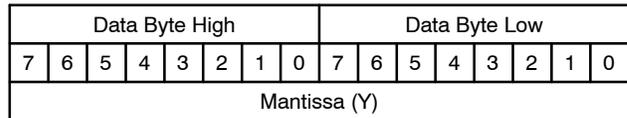
In the NCP81428 only the linear mode is supported. The VOUT\_MODE bits are set to X00b. VOUT\_MODE DATA BYTE:



Linear Mode

**Figure 49. VOUT\_MODE Linear Format**

This establishes the 5-bit 2's complement exponent for the 16 bit mantissa delivered as data bytes for an output voltage related command.



ULINEAR16 Format

**Figure 50. ULinear16 Format**

The integer (V) of the full data byte in ULINEAR16 format can be calculated using:

$$V = Y \times 2^N \quad (\text{eq. 2})$$

where: Y is a 16-bit unsigned binary integer from the mantissa and N is the 2's complement integer of the exponent

PMBus Commands

Commands

Table 10. PMBus COMMANDS LIST

Command Code	Command Name	SMBus Transaction Type: Writing Data	SMBus Transaction Type: Reading Data	Number of Data Bytes	NVM	TWI	Description
01h	OPERATION	Write Byte	Read Byte	1	YES	NO	See Registers Specifications Section
02h	ON_OFF_CONFIG	Write Byte	Read Byte	1	YES	NO	See Registers Specifications Section
03h	CLEAR_FAULTS	Send Byte	N/A	0	NO	NO	<p>This command is used to clear all fault bits that have been set in the status register simultaneously and releases the ALERT#.</p> <p>CLEAR_FAULTS will not restart a device that has latched-off due to a fault condition. A latched-off device will remain off until:</p> <ul style="list-style-type: none"> <li>• Removing and then restoring VDD bias power. Device will restart in its default state. Fault bits are cleared when <math>VDD &lt; V_{DD\_UVF}</math> threshold.</li> <li>• Faults are also cleared based on the turn on settings established by the ON_OFF_CONFIG:                     <ul style="list-style-type: none"> <li>If ON is used for turn on, the faults are cleared when ON goes low.</li> <li>If soft enable is used for turn on, faults are cleared when OPERATION [7] is set to 0.</li> <li>If soft enable and the EN pin are both used for turn on, faults are cleared when OPERATION [7] and ON are both low.</li> </ul> </li> </ul> <p>If fault conditions persists after the fault bit is cleared, the fault bit shall immediately be set again with the host notified via the ALERT# signal.</p> <p>NOTE: Any or all fault bits in any register except STATUS_BYTE and STATUS_WORD can be directly cleared by issuing the status command with 1 binary data byte. The binary data byte bits align with the corresponding status register bits. To clear fault bits, write a 1 to the corresponding bit in the binary data byte.</p>
0Ch	ARA	Send Byte	N/A	0	NO	NO	<p>The host sends an Alert Response Address (ARA) command to determine which device on the PMBus generated the alert signal.</p> <p>If more than one device pulls SMBALERT# low, the highest priority (lowest address) device will win communication rights via standard arbitration during the slave address transfer.</p>
10h	WRITE_PROTECT	Write Byte	Read Byte	1	YES	NO	See Registers Specifications Section
15h	STORE_USER_ALL	Send Byte	N/A	0	NO	NO	<p>The STORE_USER_ALL command instructs the PMBus device to copy the entire contents of the Operating Memory to the matching locations in the non-volatile User Store memory. Any items in Operating Memory that do not have matching locations in the User Store are ignored.</p>

Table 10. PMBus COMMANDS LIST (continued)

Command Code	Command Name	SMBus Transaction Type: Writing Data	SMBus Transaction Type: Reading Data	Number of Data Bytes	NVM	TWI	Description
16h	RESTORE_USER_ALL	Send Byte	N/A	0	NO	NO	The RESTORE_USER_ALL command instructs the PMBus device to copy the entire contents of the non-volatile User Store memory to the matching locations in the Operating Memory. Any items in Non-Volatile Memory that do not have matching locations in the operating memory are ignored. It is recommended to wait at least 10 ms after STORE_USER_ALL command is sent before a RESTORE_USER_ALL or a second STORE_USER_ALL is sent.
19h	CAPABILITY	N/A	Read Byte	1	NO	NO	See Registers Specifications Section
1Bh	SMBALERT_MASK	Write Word	Read Byte	2	NO	NO	See Registers Specifications Section
20h	VOUT_MODE	N/A	Read Word	1	NO	NO	See Registers Specifications Section
39h	IOUT_CAL_OFFSET	Write Word	Read Word	2	YES	NO	See Registers Specifications Section
4Fh	OT_FAULT_LIMIT	Write Word	Read Word	2	YES	YES	See Registers Specifications Section
51h	OT_WARN_LIMIT	Write Word	Read Word	2	YES	NO	See Registers Specifications Section
55h	VIN_OV_FAULT_LIMIT	Write Word	Read Word	2	YES	NO	See Registers Specifications Section
57h	VIN_OV_WARN_LIMIT	Write Word	Read Word	2	YES	NO	See Registers Specifications Section
58h	VIN_UV_WARN_LIMIT	Write Word	Read Word	2	YES	NO	See Registers Specifications Section
78h	STATUS_BYTE	Write Byte	Read Byte	1	NO	NO	See Registers Specifications Section
79h	STATUS_WORD	Write Word	Read Word	2	NO	NO	See Registers Specifications Section
7Bh	STATUS_IOUT	Write Byte	Read Byte	1	NO	NO	See Registers Specifications Section
7Ch	STATUS_INPUT	Write Byte	Read Byte	1	NO	NO	See Registers Specifications Section
7Dh	STATUS_TEMPERATURE	Write Byte	Read Byte	1	NO	NO	See Registers Specifications Section
7Eh	STATUS_CML	Write Byte	Read Byte	1	NO	NO	See Registers Specifications Section
88h	READ_VIN	N/A	Read Word	2	NO	NO	See Registers Specifications Section
8Bh	READ_VOUT	N/A	Read Word	2	NO	NO	See Registers Specifications Section
8Ch	READ_IOUT	N/A	Read Word	2	NO	NO	See Registers Specifications Section
8Dh	READ_TEMPERATURE	N/A	Read Word	2	NO	NO	See Registers Specifications Section
98h	PMBUS_REVISION	N/A	Read Byte	1	NO	NO	See Registers Specifications Section
ADh	IC_DEVICE_ID	N/A	Read Word	2	NO	NO	See Registers Specifications Section
A Eh	IC_DEVICE_REV	N/A	Read Word	2	NO	NO	See Registers Specifications Section
C4h	PEAK_IOUT	N/A	Read Word	2	NO	NO	See Registers Specifications Section
C6h	READ_HOT_DEVICE	N/A	Read Word	2	NO	NO	See Registers Specifications Section
C7h	POWER_CYCLE	Send Byte	N/A	0	NO	NO	This command is to allow the processor to request the device to turn off and turn back on again approximately 10 seconds after shutting down. This command does not require any data.  Note that once the 10 second timer elapses, the ON signal has to be high and the VIN voltage above UVLO in order for the device to restart otherwise if either condition is not met the device remains off until both signals are above their respected thresholds.
C8h	PMBUS_BASE_ADDR	Write Byte	Read Byte	1	YES	YES	See Registers Specifications Section
C9h	DEVICE_CONFIG	Write Word	Read Word	2	YES	YES	See Registers Specifications Section

**Clearing Warning or Fault Bits**

Almost all of the warning or fault bits set in the status registers remain set, even if the fault or warning condition is removed or corrected, until one of the following occurs:

- The bit is individually cleared
- The device receives a CLEAR\_FAULTS command
- A RESET signal (if one exists) is asserted
- The output is commanded through the ON pin, the OPERATION command, or the combined action of the ON pin and OPERATION command, to turn off and then to turn back on, or
- Bias power is removed from the PMBus device.

Removing the bias power usually means that the input power has been removed long enough that the voltage to the control circuit has decayed to zero. However, in some devices, the input power and the power to the control circuitry are separate. In this case, removing the bias power means removing the input power to the control circuitry.

The two exceptions to the rule that status bits remain set are the OFF and PG\_STATUS# bits. These bits always reflect the current state of the device and the POWER\_GOOD signal (if present).

*Device Busy*

If the NCP81428 is communicated to during power-up before reaching stand-by mode (refer to master/slave initialization) the device will set the busy bit and pull down on the ALERT#. Setting the busy will not cause a fault condition, however the device will respond as mentioned by the PMBus protocol.

If the device is too busy to accept and process a command being sent to it over the bus, it will respond as follows:

- ACK the address byte as all SMBus devices must ACK their own address
- If possible, NACK the command byte and data bytes as they are received
- If the host is attempting to read from the device, the device will send all ones (FFh) as long as the host keeps clocking and acknowledging
- Set the BUSY bit in the STATUS\_BYTE, and
- Notify the host by asserting the ALERT# (if not masked)

As mentioned in prior sections, the user is recommended to wait 2 ms after VDD crosses the rising UVLO threshold in order to avoid setting the busy bit and asserting the ALERT#.

*Response to Invalid Data or Command Faulty*

If the NCP81428 receives unsupported data, the device shall:

- If possible, NACK the unsupported data bytes received before the next STOP condition,

- Flush or ignore the received command code and any received data,
- Set the CML bit in the STATUS\_BYTE,
- Set the Invalid Or Unsupported Data Received bit in the STATUS\_CML register, and
- Notify the host by asserting ALERT# low

**Unsupported Command Code**

If the device receives a command that it does not support, including those command codes identified as Reserved, the device will respond as follows:

- If possible, NACK the unsupported command code and all data bytes received before the next STOP condition,
- Flush or ignore the received command code and any received data,
- Set the CML bit in the STATUS\_BYTE register,
- Set the Invalid Or Unsupported Command Received bit in the STATUS\_CML register, and
- Notify the host by asserting ALERT# low

**Alert Response Address (ARA)**

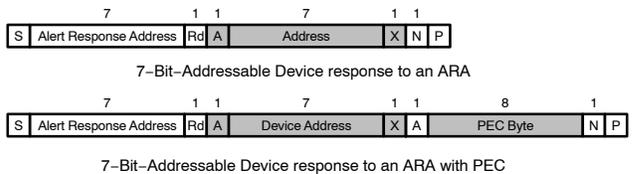
A slave-only device can signal the host through SMBALERT# that it wants to talk. The host processes the interrupt and simultaneously accesses all SMBALERT# devices through the Alert Response Address. Only the device(s) which pulled SMBALERT# low will acknowledge the Alert Response Address. The host performs a modified Receive Byte operation. The 7 bit device address provided by the slave transmit device is placed in the 7 most significant bits of the byte. The eighth bit can be a zero or one.

If more than one device pulls SMBALERT# low, the highest priority (lowest address) device will win communication rights via standard arbitration during the slave address transfer.

After receiving an acknowledge (ACK) from the master in response to its address, that device must stop pulling down on the SMBALERT# signal. If the host still sees SMBALERT# low when the message transfer is complete, it knows to read the ARA again.

A host which does not implement the SMBALERT# signal may periodically access the ARA.

The SMBus Alert Response Address is (0001 100b) and that is the one case when the R/W# bit should be set to 1.



**Figure 51. 7 bit-Addressable ARA Command Strings**

# NCP81428

## Register Mapping

**Table 11. REGISTER MAPPING**

Address	Name	Write / Clear								Read / Clear		Read / Write		Write Only		Read Only		
		B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
<b>Control Registers</b>																		
0x01	OPERATION									op_cntl	off_beh_avior	0						
0x02	ON_OFF_CONFIG											en_vcc_mode	en_op	en_cntl	en_pol	en_toff_dly		
0x10	WRITE_PROTECT									write_pro		0						
0x1B	SMBALERT_MASK	mask_byte								status_x								
0x39	IOUT_CAL_OFFSET	iout_cal_off																
0x4F	OT_FAULT_LIMIT	ot_fit_lmt																
0x51	OT_WARN_LIMIT	ot_warn_lmt																
0x55	VIN_OV_FAULT_LIMIT	vin_ov_fit_lmt																
0x57	VIN_OV_WARN_LIMIT	vin_ov_warn_lmt																
0x58	VIN_UV_WARN_LIMIT	vin_uv_warn_lmt																
0xC8	PMBUS_BASE_ADDR									mst_addr_set								unused_bit
0xC9	DEVICE_CONFIG	unused_bits	ocp3_level	ocp2_level	ocp1_level	ocp3_delay		ocp2_delay		ocp1_delay		output_pd	retry_latchoff					
<b>Status Registers</b>																		
0x78	STATUS_BYTE									busy	off	vout_ov_fault	iout_oc_fault	vin_uv_fault	temperature	cml	none_of_the_above	
0x79	STATUS_WORD	vout	iout_pout	input	mfr_specific	pg_stat_us#	fans	other	unknown	busy	off	vout_ov_fault	iout_oc_fault	vin_uv_fault	temperature	cml	none_of_the_above	
0x7B	STATUS_IOUT									iout_oc_fault	iout_oc_lv_fault	iout_oc_warning	iout_uc_fault	iout_share_fault	iin_pwr_lmt	pout_op_fault	pout_warn	
0x7C	STATUS_INPUT									vin_ov_fault	vin_ov_warn	vin_uv_warn	vin_uv_fault	unit_off	iin_oc_fault	iin_oc_warn	pin_op_warn	
0x7D	STATUS_TEMP									ot_fault	ot_warning	ut_warning	ut_fault	0				
0x7E	STATUS_CML									inv_command	inv_data	packet_error	mem_fault	proc_fault	0	comm_other	Other	
0x80	STATUS_MFR_SPECIFIC									gok_fault	scp_fault	mst_fault	slv_fault	reserved	twi_fault	ss_fault	dev_temp_warn	
<b>Read Registers</b>																		
0x19	CAPABILITY									pec_cap	pmbus_spd	alert#_cap	num_format	avsbussup	0			
0x20	VOUT_MODE	vout_mode																
0x88	READ_VIN	read_vin																
0x8B	READ_VOUT	read_vout																
0x8C	READ_IOUT	read_iout																
0x8D	READ_TEMPERATURE	read_temp																
0x98	PMBUS REVISION									rev_part_I				rev_part_II				
0xAD	IC_DEVICE_ID	ic_device_id																
0xC4	PEAK_IOUT	read_peak_iout																
0xC6	READ_HOT_DEVICE	read_hot_dev																

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## Register Details

### Control Registers

**Table 12. DETAILS FOR 0x01 – OPERATION**

0x01	OPERATION		Default = 0x00		
Bit(s)	Name	R/W	Default	Details	
7	op_cntl	R/W	0	The OPERATION ON command is used to control the power MOSFET switch which provides another way to control the hotswap on/off function. Upon turning on the device clears status bits for any faults or warnings that are not active.	
				<b>Value</b>	<b>Description</b>
				0	Output Off
				1	Output On
6	off_behavior	Read	0	Bit[6] is always '0' meaning the device will power down immediately when Bit[7] = 0.	
5:0	UNUSED		0		

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**Table 13. DETAILS FOR 0x02 – ON\_OFF\_CONFIG**

0x02	ON_OFF_CONFIG		Default = 0x17						
Bit(s)	Name	R/W	Default	Details					
7:5	UNUSED		000						
4	en_vcc_mode	Read	1	<p>This bit always returns a 1 meaning the unit does not power up until commanded by the ON pin and/or OPERATION command.</p> <p>NOTE: Writing a “0” to bit [4] the device shall respond by:</p> <ul style="list-style-type: none"> <li>• Flushing or ignoring the received write.</li> <li>• Set the CML bit in the STATUS_BYTE,</li> <li>• Set the Invalid Or Unsupported Data Received bit in the STATUS_CML register</li> <li>• Assert the ALERT#</li> </ul>					
3	en_op	R/W	0	The table below sets the conditions for the device to be enabled with the use of OPERATIONAL register, bit [7] along with ON_OFF_CONFIG reg. bits [3:2].					
				<b>Reg 0x01h, bit[7]</b>	<b>Reg 0x02h, bit[4]</b>	<b>Reg 0x02h, bit[3]</b>	<b>Reg 0x02h, bit[2]</b>	<b>ENABLE Pin</b>	<b>On/Off</b>
				X	1	0	1	1	On
				1	1	1	0	X	On
1	1	1	1	1	On				
<p>If bit [3] is cleared, and bit [2] is set, then the unit is turned on and off only by the ON pin.</p> <p>If bit [3] is set, and bit [2] is cleared, then the unit is turned on and off only by commands received over the serial bus (reg1h bit 7)</p> <p>If bit [3] is set, and bit [2] is set, then the unit is turned on and off only when both the commands received over the serial bus AND the ON pin are commanding the device to be on. If either a command from the serial bus OR the ON pin commands the unit to be off, the unit turns off.</p> <p>The en_toff_dly, bit 0 is related to the programmable turn off delay and is not applicable to this device.</p>									
2	en_cntl	R/W	1	See table bit en_op for description.					
1	en_pol	Read	1	<p>This bit always returns a 1 meaning the ON pin is active high (pull high to start the unit).</p> <p>NOTE: Writing a “0” to this bit the device shall respond by:</p> <ul style="list-style-type: none"> <li>• Flushing or ignoring the received write.</li> <li>• Set the CML bit in the STATUS_BYTE,</li> <li>• Set the Invalid Or Unsupported Data Received bit in the STATUS_CML register</li> <li>• Assert ALERT# low.</li> </ul>					
0	en_toff_dly	Read	1	<p>This bit always returns a 1 meaning the unit turns off immediately when the ON pin turns off the device.</p> <p>NOTE: Writing a “0” to this bit the device shall respond by:</p> <ul style="list-style-type: none"> <li>• Flushing or ignoring the received write.</li> <li>• Set the CML bit in the STATUS_BYTE,</li> <li>• Set the Invalid Or Unsupported Data Received bit in the STATUS_CML register</li> <li>• Assert ALERT# low.</li> </ul>					

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**Table 14. DETAILS FOR 0x10 – WRITE\_PROTECT**

0x10	WRITE_PROTECT		Default = 0x00		
Bit(s)	Name	R/W	Default	Details	
7:5	write_pro	R/W	000	Three bits [7:5] are used to set the write protection level.	
				<b>Bits [7:5]</b>	<b>Description</b>
				000	Enables writes to all commands (Default)
				001	Disables writes to all commands except for WRITE PROTECT OPERATION and ON_OFF_CONFIG commands
				010	Disables writes to all commands except for WRITE PROTECT and OPERATION commands
				100	Disables write to all commands except for WRITE PROTECT
				<p>The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a device's configuration or operation. All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.</p> <p>If a device receives a data byte that is not listed in the table, then the device shall treat this as invalid data, declare a communications fault. If the NCP81428 receives unsupported data, the response is that the device shall:</p> <ul style="list-style-type: none"> <li>• Flush or ignore the received command code and any received data,</li> <li>• Set the CML bit in the STATUS_BYTE,</li> <li>• Set the Invalid Or Unsupported Data Received bit in the STATUS_CML register</li> <li>• Set ALERT# low to alert the host</li> </ul>	
4:0	UNUSED		00000		

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**Table 15. DETAILS FOR 0x1B – SMBALERT\_MASK**

0x1B	SMBALERT_MASK	Default = 0x0000																																																																																																			
Bit(s)	Name	R/W	Default	Details																																																																																																	
15:8	mask_byte	R/W	00000000	<p>Only the write function is support for this bit in the NCP81428. The SMBALERT_MASK register utilizes two bytes. STATUS_MASK, first or lowest Byte, provides the Fault/Warning register address to be masked. The MASK_BYTE, second or highest byte is the data byte bits to be masked. The SMBALERT_MASK write protocol is shown below:</p> <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <tr> <td style="width: 10%; text-align: center;">1</td> <td style="width: 10%; text-align: center;">7</td> <td style="width: 10%; text-align: center;">1</td> <td style="width: 10%; text-align: center;">1</td> <td style="width: 10%; text-align: center;">8</td> <td style="width: 10%; text-align: center;">1</td> <td style="width: 10%; text-align: center;">8</td> <td style="width: 10%; text-align: center;">1</td> <td style="width: 10%; text-align: center;">8</td> <td style="width: 10%; text-align: center;">1</td> <td style="width: 10%; text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">S</td> <td style="text-align: center;">Slave Address</td> <td style="text-align: center;">W</td> <td style="text-align: center;">A</td> <td style="text-align: center;">SMBALERT_MASK Command Code</td> <td style="text-align: center;">A</td> <td style="text-align: center;">Status_X Command Code</td> <td style="text-align: center;">A</td> <td style="text-align: center;">Mask_Byte</td> <td style="text-align: center;">A</td> <td style="text-align: center;">P</td> </tr> </table> <p style="text-align: center;">SMBALERT_MASK</p> <p style="text-align: center;"><b>Figure 52. SMBALERT_MASK Command Sequence</b></p> <p>This does not mask the FAULT#_C or FAULT#_D pins, nor does it prevent the device from shutting down do to the fault.</p> <table border="1" style="margin: 10px auto; border-collapse: collapse; width: 100%;"> <thead> <tr> <th style="width: 5%;">Bit</th> <th style="width: 10%;">STATUS_BYTE</th> <th style="width: 10%;">STATUS_WORD</th> <th style="width: 10%;">STATUS_IOUT</th> <th style="width: 10%;">STATUS_INPUT</th> <th style="width: 10%;">STATUS_TEMP</th> <th style="width: 10%;">STATUS_CML</th> <th style="width: 10%;">STATUS_MFR_SPECIFIC</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">7</td> <td style="text-align: center;">busy</td> <td style="text-align: center;">vout*</td> <td style="text-align: center;">iout_oc_fault</td> <td style="text-align: center;">vin_ov_fault</td> <td style="text-align: center;">ot_fault</td> <td style="text-align: center;">inv_command</td> <td style="text-align: center;">gok_fault</td> </tr> <tr> <td style="text-align: center;">6</td> <td style="text-align: center;">off</td> <td style="text-align: center;">iout_pout</td> <td style="text-align: center;">iout_oc_lv_fault*</td> <td style="text-align: center;">vin_ov_warn</td> <td style="text-align: center;">ot_warning</td> <td style="text-align: center;">inv_data</td> <td style="text-align: center;">scp_fault</td> </tr> <tr> <td style="text-align: center;">5</td> <td style="text-align: center;">vout_ov_fault*</td> <td style="text-align: center;">input</td> <td style="text-align: center;">iout_oc_warning*</td> <td style="text-align: center;">vin_uv_warn</td> <td style="text-align: center;">ut_warning*</td> <td style="text-align: center;">packet_error</td> <td style="text-align: center;">mst_fault</td> </tr> <tr> <td style="text-align: center;">4</td> <td style="text-align: center;">iout_oc_fault</td> <td style="text-align: center;">mfr_specific</td> <td style="text-align: center;">iout_uc_fault*</td> <td style="text-align: center;">vin_uv_fault</td> <td style="text-align: center;">ut_fault*</td> <td style="text-align: center;">mem_fault*</td> <td style="text-align: center;">slv_fault</td> </tr> <tr> <td style="text-align: center;">3</td> <td style="text-align: center;">vin_uv_fault</td> <td style="text-align: center;">pg_status#</td> <td style="text-align: center;">iout_share_fault*</td> <td style="text-align: center;">unit_off*</td> <td style="text-align: center;">unused*</td> <td style="text-align: center;">proc_fault*</td> <td style="text-align: center;">unused*</td> </tr> <tr> <td style="text-align: center;">2</td> <td style="text-align: center;">temperature</td> <td style="text-align: center;">fans*</td> <td style="text-align: center;">iin_pwr_lmt*</td> <td style="text-align: center;">iin_oc_fault*</td> <td style="text-align: center;">unused*</td> <td style="text-align: center;">unused*</td> <td style="text-align: center;">twi_fault</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">cml</td> <td style="text-align: center;">other*</td> <td style="text-align: center;">pout_op_fault*</td> <td style="text-align: center;">iin_oc_warn*</td> <td style="text-align: center;">unused*</td> <td style="text-align: center;">comm_other*</td> <td style="text-align: center;">ss_fault</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">none_of_the_above</td> <td style="text-align: center;">unknown*</td> <td style="text-align: center;">pout_warn*</td> <td style="text-align: center;">pin_op_warn*</td> <td style="text-align: center;">unused*</td> <td style="text-align: center;">other*</td> <td style="text-align: center;">dev_temp_warn</td> </tr> </tbody> </table> <p>Note that the 'off' and 'pg_status#' bits provide live status and are not maskable bits as they don't have any effect on the ALERT#. There will be no effect if they are written to. To mask the lower byte of STATUS_WORD apply SMBALERT_MASK to STATUS_BYTE.</p> <p>* Means a function that is not supported by the NCP81428 An attempt to write "Not supported" data given in the table above will flag an invalid data fault.</p> <ul style="list-style-type: none"> <li>Ignores/flushes the command code and received data</li> <li>Sets the CML bit in STATUS_BYTE</li> <li>Sets the Invalid or Unsupported Data bit 6 in the STATUS_CML register</li> <li>Assert ALERT# to alert the host (if not masked)</li> </ul>				1	7	1	1	8	1	8	1	8	1	1	S	Slave Address	W	A	SMBALERT_MASK Command Code	A	Status_X Command Code	A	Mask_Byte	A	P	Bit	STATUS_BYTE	STATUS_WORD	STATUS_IOUT	STATUS_INPUT	STATUS_TEMP	STATUS_CML	STATUS_MFR_SPECIFIC	7	busy	vout*	iout_oc_fault	vin_ov_fault	ot_fault	inv_command	gok_fault	6	off	iout_pout	iout_oc_lv_fault*	vin_ov_warn	ot_warning	inv_data	scp_fault	5	vout_ov_fault*	input	iout_oc_warning*	vin_uv_warn	ut_warning*	packet_error	mst_fault	4	iout_oc_fault	mfr_specific	iout_uc_fault*	vin_uv_fault	ut_fault*	mem_fault*	slv_fault	3	vin_uv_fault	pg_status#	iout_share_fault*	unit_off*	unused*	proc_fault*	unused*	2	temperature	fans*	iin_pwr_lmt*	iin_oc_fault*	unused*	unused*	twi_fault	1	cml	other*	pout_op_fault*	iin_oc_warn*	unused*	comm_other*	ss_fault	0	none_of_the_above	unknown*	pout_warn*	pin_op_warn*	unused*	other*	dev_temp_warn
1	7	1	1	8	1	8	1	8	1	1																																																																																											
S	Slave Address	W	A	SMBALERT_MASK Command Code	A	Status_X Command Code	A	Mask_Byte	A	P																																																																																											
Bit	STATUS_BYTE	STATUS_WORD	STATUS_IOUT	STATUS_INPUT	STATUS_TEMP	STATUS_CML	STATUS_MFR_SPECIFIC																																																																																														
7	busy	vout*	iout_oc_fault	vin_ov_fault	ot_fault	inv_command	gok_fault																																																																																														
6	off	iout_pout	iout_oc_lv_fault*	vin_ov_warn	ot_warning	inv_data	scp_fault																																																																																														
5	vout_ov_fault*	input	iout_oc_warning*	vin_uv_warn	ut_warning*	packet_error	mst_fault																																																																																														
4	iout_oc_fault	mfr_specific	iout_uc_fault*	vin_uv_fault	ut_fault*	mem_fault*	slv_fault																																																																																														
3	vin_uv_fault	pg_status#	iout_share_fault*	unit_off*	unused*	proc_fault*	unused*																																																																																														
2	temperature	fans*	iin_pwr_lmt*	iin_oc_fault*	unused*	unused*	twi_fault																																																																																														
1	cml	other*	pout_op_fault*	iin_oc_warn*	unused*	comm_other*	ss_fault																																																																																														
0	none_of_the_above	unknown*	pout_warn*	pin_op_warn*	unused*	other*	dev_temp_warn																																																																																														

# NCP81428

**Table 15. DETAILS FOR 0x1B – SMBALERT\_MASK (continued)**

0x1B	SMBALERT_MASK	Default = 0x0000																																																								
Bit(s)	Name	R/W	Default	Details																																																						
7:0	status_x	R/W	00000000	<p>Only the write function is support for this bit in the NCP81428. The SMBALERT_MASK register utilizes two bytes. STATUS_MASK, first or lowest Byte, provides the Fault/Warning register address to be masked. The MASK_BYTE, second or highest byte is the data byte bits to be masked. The SMBALERT_MASK write protocol is shown below:</p> <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <tr> <td style="width: 10px; text-align: center;">1</td> <td style="width: 40px; text-align: center;">7</td> <td style="width: 10px; text-align: center;">1</td> <td style="width: 10px; text-align: center;">1</td> <td style="width: 40px; text-align: center;">8</td> <td style="width: 10px; text-align: center;">1</td> <td style="width: 40px; text-align: center;">8</td> <td style="width: 10px; text-align: center;">1</td> <td style="width: 40px; text-align: center;">8</td> <td style="width: 10px; text-align: center;">1</td> <td style="width: 10px; text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">S</td> <td style="text-align: center;">Slave Address</td> <td style="text-align: center;">W</td> <td style="text-align: center;">A</td> <td style="text-align: center;">SMBALERT_MASK Command Code</td> <td style="text-align: center;">A</td> <td style="text-align: center;">Status_X Command Code</td> <td style="text-align: center;">A</td> <td style="text-align: center;">Mask_Byte</td> <td style="text-align: center;">A</td> <td style="text-align: center;">P</td> </tr> </table> <p style="text-align: center;">SMBALERT_MASK</p> <p style="text-align: center;"><b>Figure 53. SMBALERT_MASK Command String</b></p> <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th style="width: 40%;">Register Name</th> <th style="width: 10%;">Hex</th> <th style="width: 20%;">Binary</th> <th style="width: 30%;">Description</th> </tr> </thead> <tbody> <tr> <td>STATUS_BYTE</td> <td>78</td> <td>0111 1000</td> <td></td> </tr> <tr> <td>STATUS_WORD</td> <td>79</td> <td>0111 1001</td> <td></td> </tr> <tr> <td>STATUS_IOUT</td> <td>7B</td> <td>0111 1011</td> <td></td> </tr> <tr> <td>STATUS_INPUT</td> <td>7C</td> <td>0111 1100</td> <td></td> </tr> <tr> <td>STATUS_TEMP</td> <td>7D</td> <td>0111 1101</td> <td></td> </tr> <tr> <td>STATUS_CML</td> <td>7E</td> <td>0111 1110</td> <td></td> </tr> <tr> <td>STATUS_MFG_SPECIAL</td> <td>80</td> <td>1000 0000</td> <td></td> </tr> </tbody> </table>	1	7	1	1	8	1	8	1	8	1	1	S	Slave Address	W	A	SMBALERT_MASK Command Code	A	Status_X Command Code	A	Mask_Byte	A	P	Register Name	Hex	Binary	Description	STATUS_BYTE	78	0111 1000		STATUS_WORD	79	0111 1001		STATUS_IOUT	7B	0111 1011		STATUS_INPUT	7C	0111 1100		STATUS_TEMP	7D	0111 1101		STATUS_CML	7E	0111 1110		STATUS_MFG_SPECIAL	80	1000 0000	
1	7	1	1	8	1	8	1	8	1	1																																																
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STATUS_CML	7E	0111 1110																																																								
STATUS_MFG_SPECIAL	80	1000 0000																																																								

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**Table 16. DETAILS FOR 0x39 – IOUT\_CAL\_OFFSET**

0x39	IOUT_CAL_OFFSET		Default = 0xE800																																																																					
Bit(s)	Name	R/W	Default	Details																																																																				
15:0	iout_cal_off	R/W	1110100000000000	<p>This command is used to null out any offsets in the current sensing circuit. The two data bytes are encoded LINEAR11 format. Exponent is in 2's compliment format and mantissa is signed binary. The default contents of the register are fuse programmable. The format supported range and resolution are given in the below table. Exponent: Fixed -3 (11101b)</p> <p>If a device receives a data byte that is not listed in the table, then the device shall treat this as invalid data, declare a communications fault. If the NCP81428 receives unsupported data, the response is that the device shall:</p> <ul style="list-style-type: none"> <li>• Flush or ignore the received command code and any received data,</li> <li>• Set the CML bit in the STATUS_BYTE,</li> <li>• Set the Invalid Or Unsupported Data Received bit in the STATUS_CML register</li> <li>• Set ALERT# low to alert the host</li> </ul> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">IOUT_CAL_OFFSET (A)</th> </tr> </thead> <tbody> <tr><td>1110 1000 0000 0000</td><td>0.000 (Default)</td></tr> <tr><td>1110 1000 0000 0001</td><td>0.125</td></tr> <tr><td>1110 1000 0000 0010</td><td>0.250</td></tr> <tr><td>1110 1000 0000 0011</td><td>0.375</td></tr> <tr><td>1110 1000 0000 0100</td><td>0.500</td></tr> <tr><td>1110 1000 0000 0101</td><td>0.625</td></tr> <tr><td>1110 1000 0000 0110</td><td>0.750</td></tr> <tr><td>1110 1000 0000 0111</td><td>0.875</td></tr> <tr><td>1110 1000 0000 1000</td><td>1.000</td></tr> <tr><td>1110 1000 0000 1001</td><td>1.125</td></tr> <tr><td>1110 1000 0000 1010</td><td>1.250</td></tr> <tr><td>1110 1000 0000 1011</td><td>1.375</td></tr> <tr><td>1110 1000 0000 1100</td><td>1.500</td></tr> <tr><td>1110 1000 0000 1101</td><td>1.625</td></tr> <tr><td>1110 1000 0000 1110</td><td>1.750</td></tr> <tr><td>1110 1000 0000 1111</td><td>1.875</td></tr> <tr><td>1110 1000 0001 0000</td><td>2.000</td></tr> <tr><td>1110 1111 1111 1111</td><td>-0.125</td></tr> <tr><td>1110 1111 1111 1110</td><td>-0.250</td></tr> <tr><td>1110 1111 1111 1101</td><td>-0.375</td></tr> <tr><td>1110 1111 1111 1100</td><td>-0.500</td></tr> <tr><td>1110 1111 1111 1011</td><td>-0.625</td></tr> <tr><td>1110 1111 1111 1010</td><td>-0.750</td></tr> <tr><td>1110 1111 1111 1001</td><td>-0.875</td></tr> <tr><td>1110 1111 1111 1000</td><td>-1.000</td></tr> <tr><td>1110 1111 1111 0111</td><td>-1.125</td></tr> <tr><td>1110 1111 1111 0110</td><td>-1.250</td></tr> <tr><td>1110 1111 1111 0101</td><td>-1.375</td></tr> <tr><td>1110 1111 1111 0100</td><td>-1.500</td></tr> <tr><td>1110 1111 1111 0011</td><td>-1.625</td></tr> <tr><td>1110 1111 1111 0010</td><td>-1.750</td></tr> <tr><td>1110 1111 1111 0001</td><td>-1.875</td></tr> <tr><td>1110 1111 1111 0000</td><td>-2.000</td></tr> </tbody> </table>	Value	IOUT_CAL_OFFSET (A)	1110 1000 0000 0000	0.000 (Default)	1110 1000 0000 0001	0.125	1110 1000 0000 0010	0.250	1110 1000 0000 0011	0.375	1110 1000 0000 0100	0.500	1110 1000 0000 0101	0.625	1110 1000 0000 0110	0.750	1110 1000 0000 0111	0.875	1110 1000 0000 1000	1.000	1110 1000 0000 1001	1.125	1110 1000 0000 1010	1.250	1110 1000 0000 1011	1.375	1110 1000 0000 1100	1.500	1110 1000 0000 1101	1.625	1110 1000 0000 1110	1.750	1110 1000 0000 1111	1.875	1110 1000 0001 0000	2.000	1110 1111 1111 1111	-0.125	1110 1111 1111 1110	-0.250	1110 1111 1111 1101	-0.375	1110 1111 1111 1100	-0.500	1110 1111 1111 1011	-0.625	1110 1111 1111 1010	-0.750	1110 1111 1111 1001	-0.875	1110 1111 1111 1000	-1.000	1110 1111 1111 0111	-1.125	1110 1111 1111 0110	-1.250	1110 1111 1111 0101	-1.375	1110 1111 1111 0100	-1.500	1110 1111 1111 0011	-1.625	1110 1111 1111 0010	-1.750	1110 1111 1111 0001	-1.875	1110 1111 1111 0000	-2.000
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**Table 17. DETAILS FOR 0x4F – OT\_FAULT\_LIMIT**

0x4F	OT_FAULT_LIMIT		Default = 0xF918																																																																																																								
Bit(s)	Name	R/W	Default	Details																																																																																																							
15:0	ot_ft_lmt	R/W	1111100100011000	<p>This command sets the temperature in degrees Celsius at which the chip should indicate an over temperature fault and shutdown.            The OT_FAULT_LIMIT command has two data bytes encoded LINEAR11 format with 5 bits signed exponent and 11 bits mantissa.            The exponent is read only and if an exponent other -1 (11111b) is written, an invalid data fault is flagged.            The temperature can be set in 0.5C increments and the table below gives examples of every two degree steps.            Note that an over temperature fault limit has to be set at least 0.5°C higher than an over temperature warning limit otherwise the command will be rejected and an invalid data fault sets.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">ot_fault_limit (Degrees °C)</th> <th style="text-align: center;">Data (b)</th> <th style="text-align: center;">Data (h)</th> </tr> </thead> <tbody> <tr><td style="text-align: center;">80.0</td><td style="text-align: center;">1111 1000 1010 0000</td><td style="text-align: center;">F8A0</td></tr> <tr><td style="text-align: center;">82.0</td><td style="text-align: center;">1111 1000 1010 0100</td><td style="text-align: center;">F8A4</td></tr> <tr><td style="text-align: center;">84.0</td><td style="text-align: center;">1111 1000 1010 1000</td><td style="text-align: center;">F8A8</td></tr> <tr><td style="text-align: center;">86.0</td><td style="text-align: center;">1111 1000 1010 1100</td><td style="text-align: center;">F8AC</td></tr> <tr><td style="text-align: center;">88.0</td><td style="text-align: center;">1111 1000 1011 0000</td><td style="text-align: center;">F8B0</td></tr> <tr><td style="text-align: center;">90.0</td><td style="text-align: center;">1111 1000 1011 0100</td><td style="text-align: center;">F8B4</td></tr> <tr><td style="text-align: center;">92.0</td><td style="text-align: center;">1111 1000 1011 1000</td><td style="text-align: center;">F8B8</td></tr> <tr><td style="text-align: center;">94.0</td><td style="text-align: center;">1111 1000 1011 1100</td><td style="text-align: center;">F8BC</td></tr> <tr><td style="text-align: center;">96.0</td><td style="text-align: center;">1111 1000 1100 0000</td><td style="text-align: center;">F8C0</td></tr> <tr><td style="text-align: center;">98.0</td><td style="text-align: center;">1111 1000 1100 0100</td><td style="text-align: center;">F8C4</td></tr> <tr><td style="text-align: center;">100.0</td><td style="text-align: center;">1111 1000 1100 1000</td><td style="text-align: center;">F8C8</td></tr> <tr><td style="text-align: center;">102.0</td><td style="text-align: center;">1111 1000 1100 1100</td><td style="text-align: center;">F8CC</td></tr> <tr><td style="text-align: center;">104.0</td><td style="text-align: center;">1111 1000 1101 0000</td><td style="text-align: center;">F8D0</td></tr> <tr><td style="text-align: center;">106.0</td><td style="text-align: center;">1111 1000 1101 0100</td><td style="text-align: center;">F8D4</td></tr> <tr><td style="text-align: center;">108.0</td><td style="text-align: center;">1111 1000 1101 1000</td><td style="text-align: center;">F8D8</td></tr> <tr><td style="text-align: center;">110.0</td><td style="text-align: center;">1111 1000 1101 1100</td><td style="text-align: center;">F8DC</td></tr> <tr><td style="text-align: center;">112.0</td><td style="text-align: center;">1111 1000 1110 0000</td><td style="text-align: center;">F8E0</td></tr> <tr><td style="text-align: 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center;">1111 1001 0001 1000</td><td style="text-align: center;">F918</td></tr> <tr><td style="text-align: center;">142.0</td><td style="text-align: center;">1111 1001 0001 1100</td><td style="text-align: center;">F91C</td></tr> <tr><td style="text-align: center;">144.0</td><td style="text-align: center;">1111 1001 0010 0000</td><td style="text-align: center;">F920</td></tr> </tbody> </table>		ot_fault_limit (Degrees °C)	Data (b)	Data (h)	80.0	1111 1000 1010 0000	F8A0	82.0	1111 1000 1010 0100	F8A4	84.0	1111 1000 1010 1000	F8A8	86.0	1111 1000 1010 1100	F8AC	88.0	1111 1000 1011 0000	F8B0	90.0	1111 1000 1011 0100	F8B4	92.0	1111 1000 1011 1000	F8B8	94.0	1111 1000 1011 1100	F8BC	96.0	1111 1000 1100 0000	F8C0	98.0	1111 1000 1100 0100	F8C4	100.0	1111 1000 1100 1000	F8C8	102.0	1111 1000 1100 1100	F8CC	104.0	1111 1000 1101 0000	F8D0	106.0	1111 1000 1101 0100	F8D4	108.0	1111 1000 1101 1000	F8D8	110.0	1111 1000 1101 1100	F8DC	112.0	1111 1000 1110 0000	F8E0	114.0	1111 1000 1110 0100	F8E4	116.0	1111 1000 1110 1000	F8E8	118.0	1111 1000 1110 1100	F8EC	120.0	1111 1000 1111 0000	F8F0	122.0	1111 1000 1111 0100	F8F4	124.0	1111 1000 1111 1000	F8F8	126.0	1111 1000 1111 1100	F8FC	128.0	1111 1001 0000 0000	F900	130.0	1111 1001 0000 0100	F904	132.0	1111 1001 0000 1000	F908	134.0	1111 1001 0000 1100	F90C	136.0	1111 1001 0001 0000	F910	138.0	1111 1001 0001 0100	F914	140.0 (Default)	1111 1001 0001 1000	F918	142.0	1111 1001 0001 1100	F91C	144.0	1111 1001 0010 0000	F920
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**Table 17. DETAILS FOR 0x4F – OT\_FAULT\_LIMIT (continued)**

0x4F	OT_FAULT_LIMIT		Default = 0xF918			
Bit(s)	Name	R/W	Default	Details		
				146.0	1111 1001 0010 0100	F924
				148.0	1111 1001 0010 1000	F928
				150.0	1111 1001 0010 1100	F92C
Upon triggering an over-temperature fault, the following actions are taken <ul style="list-style-type: none"> <li>• Set the TEMPERATURE bit in the STATUS_BYTE</li> <li>• Set the OT_FAULT bit in the STATUS_TEMPERATURE register, and</li> <li>• The device notifies the host by asserting ALERT# low if not masked)</li> </ul>						

**Table 18. DETAILS FOR 0x51 – OT\_WARN\_LIMIT**

0x51	OT_WARN_LIMIT		Default = 0xF8F0			
Bit(s)	Name	R/W	Default	Details		
15:0	ot_warn_lmt	R/W	1111100011110000	This command sets the temperature in degrees Celsius at which the chip should indicate an over temperature warning. The OT_WARN_LIMIT command has two data bytes encoded LINEAR11 format with 5 bits signed exponent and 11 bits mantissa. The default contents of the register are user programmable The exponent is read only and if an exponent other -1 (11111b) is written, an invalid data fault is flagged. The mantissa range is 70°C to 150°C. Any mantissa outside this range will assert invalid data fault. Also if the ot_warn_limit is set higher or equal to ot_fit_limit then an invalid data fault is flagged. The temperature can be set in 0.5°C increments and the table below gives examples of every two degree steps. Note that an over temperature warn limit has to be set at least 0.5°C lower than an over temperature fault limit otherwise the command will be rejected and an invalid data fault sets.		
				<b>ot_warn_limit (Degrees °C)</b>	<b>Data (b)</b>	<b>Data (h)</b>
				70.0	1111 1000 1000 1100	F88C
				72.0	1111 1000 1001 0000	F890
				74.0	1111 1000 1001 0100	F894
				76.0	1111 1000 1001 1000	F898
				78.0	1111 1000 1001 1100	F89C
				80.0	1111 1000 1010 0000	F8A0
				82.0	1111 1000 1010 0100	F8A4
				84.0	1111 1000 1010 1000	F8A8
				86.0	1111 1000 1010 1100	F8AC
				88.0	1111 1000 1011 0000	F8B0
				90.0	1111 1000 1011 0100	F8B4
				92.0	1111 1000 1011 1000	F8B8
				94.0	1111 1000 1011 1100	F8BC
				96.0	1111 1000 1100 0000	F8C0
				98.0	1111 1000 1100 0100	F8C4
				100.0	1111 1000 1100 1000	F8C8
				102.0	1111 1000 1100 1100	F8CC
				104.0	1111 1000 1101 0000	F8D0
				106.0	1111 1000 1101 0100	F8D4
				108.0	1111 1000 1101 1000	F8D8
				110.0	1111 1000 1101 1100	F8DC

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**Table 18. DETAILS FOR 0x51 – OT\_WARN\_LIMIT (continued)**

0x51	OT_WARN_LIMIT		Default = 0xF8F0			
Bit(s)	Name	R/W	Default	Details		
				112.0	1111 1000 1110 0000	F8E0
				114.0	1111 1000 1110 0100	F8E4
				116.0	1111 1000 1110 1000	F8E8
				118.0	1111 1000 1110 1100	F8EC
				120.0 (Default)	1111 1000 1111 0000	F8F0
				122.0	1111 1000 1111 0100	F8F4
				124.0	1111 1000 1111 1000	F8F8
				126.0	1111 1000 1111 1100	F8FC
				128.0	1111 1001 0000 0000	F900
				130.0	1111 1001 0000 0100	F904
				132.0	1111 1001 0000 1000	F908
				134.0	1111 1001 0000 1100	F90C
				136.0	1111 1001 0001 0000	F910
				138.0	1111 1001 0001 0100	F914
				140.0	1111 1001 0001 1000	F918
				142.0	1111 1001 0001 1100	F91C
				144.0	1111 1001 0010 0000	F920
				146.0	1111 1001 0010 0100	F924
				148.0	1111 1001 0010 1000	F928
				150.0	1111 1001 0010 1100	F92C
<p>Upon triggering an over-temperature warn, the following actions are taken:</p> <ul style="list-style-type: none"> <li>• Sets the TEMPERATURE bit in the STATUS_BYTE</li> <li>• Sets the OT Warning bit in the STATUS_TEMPERATURE register, and</li> <li>• The device notifies the host (asserts ALERT# if not masked).</li> </ul>						

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**Table 19. DETAILS FOR 0x55 – VIN\_OV\_FAULT\_LIMIT**

0x55	VIN_OV_FAULT_LIMIT	Default = 0xF81C																																																											
Bit(s)	Name	R/W	Default	Details																																																									
15:0	vin_ov_ft_lmt	R/W	1111100000011100	<p>This command sets the value of the input voltage VIN in volts that causes an input over voltage fault. The VIN_OV_FAULT_LIMIT command has two data bytes encoded in LINEAR11 format with 5bits signed exponent and 11 bits mantissa. The range, resolution and default are shown in the table below:</p> <table border="1" style="width: 100%; margin: 5px 0;"> <thead> <tr> <th>Ranges</th> <th>Resolution</th> <th>Default</th> </tr> </thead> <tbody> <tr> <td>6–8 V, 14–19 V</td> <td>0.5 V</td> <td>14 V</td> </tr> </tbody> </table> <p>The default of this register is user programmable. The exponent is read only and if an exponent other than –1 (11111b) is written, an invalid data fault is flagged. All the options supported are given in the Table below. Any data other than the data given in the table below will flag an invalid data fault.</p> <p>NOTES: 13. An over voltage fault limit has to be set at least 0.5 V higher than an over voltage warn limit, otherwise the command will be rejected and an invalid data fault sets.</p> <table border="1" style="width: 100%; margin: 5px 0;"> <thead> <tr> <th>vin_ov_ft_lmt</th> <th>Data (B)</th> <th>Data (h)</th> </tr> </thead> <tbody> <tr><td>6.0 V</td><td>1111 1000 0000 1100</td><td>F80C</td></tr> <tr><td>6.5 V</td><td>1111 1000 0000 1101</td><td>F80D</td></tr> <tr><td>7.0 V</td><td>1111 1000 0000 1110</td><td>F80E</td></tr> <tr><td>7.5 V</td><td>1111 1000 0000 1111</td><td>F80F</td></tr> <tr><td>8.0 V</td><td>1111 1000 0001 0000</td><td>F810</td></tr> <tr><td>14.0 V (Default)</td><td>1111 1000 0001 1100</td><td>F81C</td></tr> <tr><td>14.5 V</td><td>1111 1000 0001 1101</td><td>F81D</td></tr> <tr><td>15.0 V</td><td>1111 1000 0001 1110</td><td>F81E</td></tr> <tr><td>15.5 V</td><td>1111 1000 0001 1111</td><td>F81F</td></tr> <tr><td>16.0 V</td><td>1111 1000 0010 0000</td><td>F820</td></tr> <tr><td>16.5 V</td><td>1111 1000 0010 0001</td><td>F821</td></tr> <tr><td>17.0 V</td><td>1111 1000 0010 0010</td><td>F822</td></tr> <tr><td>17.5 V</td><td>1111 1000 0010 0011</td><td>F823</td></tr> <tr><td>18.0 V</td><td>1111 1000 0010 0100</td><td>F824</td></tr> <tr><td>18.5 V</td><td>1111 1000 0010 0101</td><td>F825</td></tr> <tr><td>19.0 V</td><td>1111 1000 0010 0110</td><td>F826</td></tr> </tbody> </table> <p>Upon triggering an input over-voltage fault, the following actions are taken:</p> <ul style="list-style-type: none"> <li>• Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE,</li> <li>• Sets the INPUT bit in the upper byte of the STATUS_WORD,</li> <li>• Sets the VIN_OV_FAULT bit in the STATUS_INPUT register, and</li> <li>• The device notifies the host (asserts PG pin low, asserts ALERT# if not masked)</li> </ul>	Ranges	Resolution	Default	6–8 V, 14–19 V	0.5 V	14 V	vin_ov_ft_lmt	Data (B)	Data (h)	6.0 V	1111 1000 0000 1100	F80C	6.5 V	1111 1000 0000 1101	F80D	7.0 V	1111 1000 0000 1110	F80E	7.5 V	1111 1000 0000 1111	F80F	8.0 V	1111 1000 0001 0000	F810	14.0 V (Default)	1111 1000 0001 1100	F81C	14.5 V	1111 1000 0001 1101	F81D	15.0 V	1111 1000 0001 1110	F81E	15.5 V	1111 1000 0001 1111	F81F	16.0 V	1111 1000 0010 0000	F820	16.5 V	1111 1000 0010 0001	F821	17.0 V	1111 1000 0010 0010	F822	17.5 V	1111 1000 0010 0011	F823	18.0 V	1111 1000 0010 0100	F824	18.5 V	1111 1000 0010 0101	F825	19.0 V	1111 1000 0010 0110	F826
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				17.0 V	1111 1000 0010 0010	F822																																																							
				17.5 V	1111 1000 0010 0011	F823																																																							
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19.0 V	1111 1000 0010 0110	F826																																																											

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**Table 20. DETAILS FOR 0x57 – VIN\_OV\_WARN\_LIMIT**

VIN_OV_WARN_LIMIT		Default = 0xD9A7																																																																																										
Bit(s)	Name	R/W	Default	Details																																																																																								
15:0	vin_ov_warn_lmt	R/W	1101100110100111	<p>This command sets the value of the input voltage VIN in volts that causes an input over voltage warning.</p> <p>The VIN_OV_WARN_LIMIT command has two data bytes encoded in LINEAR11 format with 5 bits signed exponent and 11 bits mantissa.</p> <p>The exponent is fixed -5 (11011b).</p> <p>The range, resolution and default are shown in the below table.</p> <p>The default of this register is fuse programmable.</p> <p>The exponent is read only and if an exponent other than -5 (11011b) is written, an invalid data fault is flagged. An example of the supported range is given in the Table below. Any data other than given in the table below will flag an invalid data fault.</p> <p>NOTE: An over voltage warn limit has to be set at least 0.5 V lower than an over voltage fault limit otherwise the command will be rejected and an invalid data fault sets.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th>Range</th> <th>Resolution</th> </tr> </thead> <tbody> <tr> <td>5.0 to 18.5 V</td> <td>31.25 mV</td> </tr> </tbody> </table> <p><i>Example VIN_OV_WARN_LIMIT register values.</i></p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th>vin_ov_warn_lmt</th> <th>Data (b)</th> <th>Data (h)</th> </tr> </thead> <tbody> <tr><td>5.0 V</td><td>1101 1000 1010 0000</td><td>D8A0</td></tr> <tr><td>5.5 V</td><td>1101 1000 1011 0000</td><td>D8B0</td></tr> <tr><td>6.0 V</td><td>1101 1000 1100 0000</td><td>D8C0</td></tr> <tr><td>6.5 V</td><td>1101 1000 1101 0000</td><td>D8D0</td></tr> <tr><td>7.0 V</td><td>1101 1000 1110 0000</td><td>D8E0</td></tr> <tr><td>7.5 V</td><td>1101 1000 1111 0000</td><td>D8F0</td></tr> <tr><td>8.0 V</td><td>1101 1001 0000 0000</td><td>D900</td></tr> <tr><td>8.5 V</td><td>1101 1001 0001 0000</td><td>D910</td></tr> <tr><td>9.0 V</td><td>1101 1001 0010 0000</td><td>D920</td></tr> <tr><td>9.5 V</td><td>1101 1001 0011 0000</td><td>D930</td></tr> <tr><td>10.0 V</td><td>1101 1001 0100 0000</td><td>D940</td></tr> <tr><td>10.5 V</td><td>1101 1001 0101 0000</td><td>D950</td></tr> <tr><td>11.0 V</td><td>1101 1001 0110 0000</td><td>D960</td></tr> <tr><td>11.5 V</td><td>1101 1001 0111 0000</td><td>D970</td></tr> <tr><td>12.0 V</td><td>1101 1001 1000 0000</td><td>D980</td></tr> <tr><td>12.5 V</td><td>1101 1001 1001 0000</td><td>D990</td></tr> <tr><td>13.0 V</td><td>1101 1001 1010 0000</td><td>D9A0</td></tr> <tr><td>13.21875 (DEFAULT)</td><td>1101 1001 1010 0111</td><td>D9A7</td></tr> <tr><td>13.5 V</td><td>1101 1001 1011 0000</td><td>D9B0</td></tr> <tr><td>14.0 V</td><td>1101 1001 1100 0000</td><td>D9C0</td></tr> <tr><td>14.5 V</td><td>1101 1001 1101 0000</td><td>D9D0</td></tr> <tr><td>15.0 V</td><td>1101 1001 1110 0000</td><td>D9E0</td></tr> <tr><td>15.5 V</td><td>1101 1001 1111 0000</td><td>D9F0</td></tr> <tr><td>16.0 V</td><td>1101 1010 0000 0000</td><td>DA00</td></tr> <tr><td>16.5 V</td><td>1101 1010 0001 0000</td><td>DA10</td></tr> <tr><td>17.0 V</td><td>1101 1010 0010 0000</td><td>DA20</td></tr> <tr><td>17.5 V</td><td>1101 1010 0011 0000</td><td>DA30</td></tr> </tbody> </table>	Range	Resolution	5.0 to 18.5 V	31.25 mV	vin_ov_warn_lmt	Data (b)	Data (h)	5.0 V	1101 1000 1010 0000	D8A0	5.5 V	1101 1000 1011 0000	D8B0	6.0 V	1101 1000 1100 0000	D8C0	6.5 V	1101 1000 1101 0000	D8D0	7.0 V	1101 1000 1110 0000	D8E0	7.5 V	1101 1000 1111 0000	D8F0	8.0 V	1101 1001 0000 0000	D900	8.5 V	1101 1001 0001 0000	D910	9.0 V	1101 1001 0010 0000	D920	9.5 V	1101 1001 0011 0000	D930	10.0 V	1101 1001 0100 0000	D940	10.5 V	1101 1001 0101 0000	D950	11.0 V	1101 1001 0110 0000	D960	11.5 V	1101 1001 0111 0000	D970	12.0 V	1101 1001 1000 0000	D980	12.5 V	1101 1001 1001 0000	D990	13.0 V	1101 1001 1010 0000	D9A0	13.21875 (DEFAULT)	1101 1001 1010 0111	D9A7	13.5 V	1101 1001 1011 0000	D9B0	14.0 V	1101 1001 1100 0000	D9C0	14.5 V	1101 1001 1101 0000	D9D0	15.0 V	1101 1001 1110 0000	D9E0	15.5 V	1101 1001 1111 0000	D9F0	16.0 V	1101 1010 0000 0000	DA00	16.5 V	1101 1010 0001 0000	DA10	17.0 V	1101 1010 0010 0000	DA20	17.5 V	1101 1010 0011 0000	DA30
Range	Resolution																																																																																											
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7.0 V	1101 1000 1110 0000	D8E0																																																																																										
7.5 V	1101 1000 1111 0000	D8F0																																																																																										
8.0 V	1101 1001 0000 0000	D900																																																																																										
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9.5 V	1101 1001 0011 0000	D930																																																																																										
10.0 V	1101 1001 0100 0000	D940																																																																																										
10.5 V	1101 1001 0101 0000	D950																																																																																										
11.0 V	1101 1001 0110 0000	D960																																																																																										
11.5 V	1101 1001 0111 0000	D970																																																																																										
12.0 V	1101 1001 1000 0000	D980																																																																																										
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16.0 V	1101 1010 0000 0000	DA00																																																																																										
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17.5 V	1101 1010 0011 0000	DA30																																																																																										

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**Table 20. DETAILS FOR 0x57 – VIN\_OV\_WARN\_LIMIT** (continued)

VIN_OV_WARN_LIMIT		Default = 0xD9A7		
Bit(s)	Name	R/W	Default	Details
				18.0 V      1101 1010 0100 0000      DA40
				18.5 V      1101 1010 0101 0000      DA50
				Upon triggering an input over-voltage warn, the following actions are taken: <ul style="list-style-type: none"> <li>• Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE,</li> <li>• Sets the INPUT bit in the upper byte of the STATUS_WORD,</li> <li>• Sets the VIN_OV_WARN bit in the STATUS_INPUT register, and</li> <li>• The device notifies the host (asserts ALERT# if not masked)</li> </ul>

**Table 21. DETAILS FOR 0x58 – VIN\_UV\_WARN\_LIMIT**

VIN_UV_WARN_LIMIT		Default = 0xD959																																																																											
Bit(s)	Name	R/W	Default	Details																																																																									
15:0	vin_uv_warn_lmt	R/W	1101100101011001	<p>This command sets the value of the input voltage VIN in volts that causes an input under voltage warning. The VIN_UV_WARN_LIMIT command has two data bytes encoded in LINEAR11 format with 5 bits signed exponent and 11 bits mantissa. The exponent is fixed -5 (11011b). The range, resolution and default are shown in the below table. The default of this register is fuse programmable. The exponent is read only and if an exponent other than -5 (11011b) is written, an invalid data fault is flagged. An example of the supported range is given in the Table below. Any data other than the data provided in the table below will flag an invalid data fault.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Range</th> <th style="width: 50%;">Resolution</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">4.75 to 18.0 V</td> <td style="text-align: center;">31.25 mV</td> </tr> </tbody> </table> <p><i>Example VIN_UV_WARN_LIMIT register values.</i></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">vin_uv_warn_lmt</th> <th style="width: 30%;">Data (b)</th> <th style="width: 40%;">Data (h)</th> </tr> </thead> <tbody> <tr><td style="text-align: center;">4.75 V</td><td style="text-align: center;">1101 1000 1001 1000</td><td style="text-align: center;">D898</td></tr> <tr><td style="text-align: center;">5.0 V</td><td style="text-align: center;">1101 1000 1010 0000</td><td style="text-align: center;">D8A0</td></tr> <tr><td style="text-align: center;">5.5 V</td><td style="text-align: center;">1101 1000 1011 0000</td><td style="text-align: center;">D8B0</td></tr> <tr><td style="text-align: center;">6.0 V</td><td style="text-align: center;"><i>1101 1000 1100 0000</i></td><td style="text-align: center;"><i>D8C0</i></td></tr> <tr><td style="text-align: center;">6.5 V</td><td style="text-align: center;">1101 1000 1101 0000</td><td style="text-align: center;">D8D0</td></tr> <tr><td style="text-align: center;">7.0 V</td><td style="text-align: center;">1101 1000 1110 0000</td><td style="text-align: center;">D8E0</td></tr> <tr><td style="text-align: center;">7.5 V</td><td style="text-align: center;">1101 1000 1111 0000</td><td style="text-align: center;">D8F0</td></tr> <tr><td style="text-align: center;">8.0 V</td><td style="text-align: center;">1101 1001 0000 0000</td><td style="text-align: center;">D900</td></tr> <tr><td style="text-align: center;">8.5 V</td><td style="text-align: center;">1101 1001 0001 0000</td><td style="text-align: center;">D910</td></tr> <tr><td style="text-align: center;">9.0 V</td><td style="text-align: center;">1101 1001 0010 0000</td><td style="text-align: center;">D920</td></tr> <tr><td style="text-align: center;">9.5 V</td><td style="text-align: center;">1101 1001 0011 0000</td><td style="text-align: center;">D930</td></tr> <tr><td style="text-align: center;">10.0 V</td><td style="text-align: center;"><i>1101 1001 0100 0000</i></td><td style="text-align: center;"><i>D940</i></td></tr> <tr><td style="text-align: center;">10.5 V</td><td style="text-align: center;">1101 1001 0101 0000</td><td style="text-align: center;">D950</td></tr> <tr><td style="text-align: center;"><i>10.78125 (DEFAULT)</i></td><td style="text-align: center;"><i>1101 1001 0101 1001</i></td><td style="text-align: center;"><i>D959</i></td></tr> <tr><td style="text-align: center;">11.0 V</td><td style="text-align: center;">1101 1001 0110 0000</td><td style="text-align: center;">D960</td></tr> <tr><td style="text-align: center;">11.5 V</td><td style="text-align: center;">1101 1001 0111 0000</td><td style="text-align: center;">D970</td></tr> <tr><td style="text-align: center;">12.0 V</td><td style="text-align: center;">1101 1001 1000 0000</td><td style="text-align: center;">D980</td></tr> <tr><td style="text-align: center;">12.5 V</td><td style="text-align: center;">1101 1001 1001 0000</td><td style="text-align: center;">D990</td></tr> <tr><td style="text-align: center;">13.0 V</td><td style="text-align: center;">1101 1001 1010 0000</td><td style="text-align: center;">D9A0</td></tr> <tr><td style="text-align: center;">13.5 V</td><td style="text-align: center;">1101 1001 1011 0000</td><td style="text-align: center;">D9B0</td></tr> <tr><td style="text-align: center;">14.0 V</td><td style="text-align: center;">1101 1001 1100 0000</td><td style="text-align: center;">D9C0</td></tr> <tr><td style="text-align: center;">14.5 V</td><td style="text-align: center;">1101 1001 1101 0000</td><td style="text-align: center;">D9D0</td></tr> </tbody> </table>	Range	Resolution	4.75 to 18.0 V	31.25 mV	vin_uv_warn_lmt	Data (b)	Data (h)	4.75 V	1101 1000 1001 1000	D898	5.0 V	1101 1000 1010 0000	D8A0	5.5 V	1101 1000 1011 0000	D8B0	6.0 V	<i>1101 1000 1100 0000</i>	<i>D8C0</i>	6.5 V	1101 1000 1101 0000	D8D0	7.0 V	1101 1000 1110 0000	D8E0	7.5 V	1101 1000 1111 0000	D8F0	8.0 V	1101 1001 0000 0000	D900	8.5 V	1101 1001 0001 0000	D910	9.0 V	1101 1001 0010 0000	D920	9.5 V	1101 1001 0011 0000	D930	10.0 V	<i>1101 1001 0100 0000</i>	<i>D940</i>	10.5 V	1101 1001 0101 0000	D950	<i>10.78125 (DEFAULT)</i>	<i>1101 1001 0101 1001</i>	<i>D959</i>	11.0 V	1101 1001 0110 0000	D960	11.5 V	1101 1001 0111 0000	D970	12.0 V	1101 1001 1000 0000	D980	12.5 V	1101 1001 1001 0000	D990	13.0 V	1101 1001 1010 0000	D9A0	13.5 V	1101 1001 1011 0000	D9B0	14.0 V	1101 1001 1100 0000	D9C0	14.5 V	1101 1001 1101 0000	D9D0
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6.5 V	1101 1000 1101 0000	D8D0																																																																											
7.0 V	1101 1000 1110 0000	D8E0																																																																											
7.5 V	1101 1000 1111 0000	D8F0																																																																											
8.0 V	1101 1001 0000 0000	D900																																																																											
8.5 V	1101 1001 0001 0000	D910																																																																											
9.0 V	1101 1001 0010 0000	D920																																																																											
9.5 V	1101 1001 0011 0000	D930																																																																											
10.0 V	<i>1101 1001 0100 0000</i>	<i>D940</i>																																																																											
10.5 V	1101 1001 0101 0000	D950																																																																											
<i>10.78125 (DEFAULT)</i>	<i>1101 1001 0101 1001</i>	<i>D959</i>																																																																											
11.0 V	1101 1001 0110 0000	D960																																																																											
11.5 V	1101 1001 0111 0000	D970																																																																											
12.0 V	1101 1001 1000 0000	D980																																																																											
12.5 V	1101 1001 1001 0000	D990																																																																											
13.0 V	1101 1001 1010 0000	D9A0																																																																											
13.5 V	1101 1001 1011 0000	D9B0																																																																											
14.0 V	1101 1001 1100 0000	D9C0																																																																											
14.5 V	1101 1001 1101 0000	D9D0																																																																											

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**Table 21. DETAILS FOR 0x58 – VIN\_UV\_WARN\_LIMIT** (continued)

VIN_UV_WARN_LIMIT		Default = 0xD959		
Bit(s)	Name	R/W	Default	Details
				15.0 V      1101 1001 1110 0000      D9E0
				15.5 V      1101 1001 1111 0000      D9F0
				16.0 V      1101 1010 0000 0000      DA00
				16.5 V      1101 1010 0001 0000      DA10
				17.0 V      1101 1010 0010 0000      DA20
				17.5 V      1101 1010 0011 0000      DA30
				18.0 V      1101 1010 0100 0000      DA40
				Upon triggering an input under-voltage warn, the following actions are taken: <ul style="list-style-type: none"> <li>• Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE,</li> <li>• Sets the INPUT bit in the upper byte of the STATUS_WORD,</li> <li>• Sets the VIN_UV_WARN bit in the STATUS_INPUT register, and</li> <li>• The device notifies the host (asserts ALERT# if not masked)</li> </ul>

**Table 22. DETAILS FOR 0xC8 – PMBUS\_BASE\_ADDR**

PMBUS_BASE_ADDR		Default = 0xC8																																																								
Bit(s)	Name	R/W	Default	Details																																																						
7:1	mst_addr_set	R/W	1100100	Both master and slaves base address registers should be programmed to the same value. The default base address is 64h, but can be programmed to other addresses as shown below.																																																						
				<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>R_ADDR (kΩ)</th> <th>Address</th> <th>Device</th> </tr> </thead> <tbody> <tr><td>9.31</td><td>Base + 00h</td><td>Master w/ TWI Data Transfer</td></tr> <tr><td>14.3</td><td>Base + 01h</td><td>Master w/ TWI Data Transfer</td></tr> <tr><td>20.0</td><td>Base + 02h</td><td>Master w/o TWI Data Transfer</td></tr> <tr><td>26.7</td><td>Base + 03h</td><td>Slave 1 w/ TWI Data Transfer</td></tr> <tr><td>34.0</td><td>Base + 04h</td><td>Slave 2 w/ TWI Data Transfer</td></tr> <tr><td>42.2</td><td>Base + 05h</td><td>Slave 3 w/ TWI Data Transfer</td></tr> <tr><td>51.1</td><td>Base + 06h</td><td>Slave 4 w/ TWI Data Transfer</td></tr> <tr><td>61.9</td><td>Base + 07h</td><td>Slave 5 w/ TWI Data Transfer</td></tr> <tr><td>73.2</td><td>Base + 08h</td><td>Slave 6 w/ TWI Data Transfer</td></tr> <tr><td>86.6</td><td>Base + 09h</td><td>Slave 1 w/o TWI Data Transfer</td></tr> <tr><td>102.0</td><td>Base + 0Ah</td><td>Slave 2 w/o TWI Data Transfer</td></tr> <tr><td>118.0</td><td>Base + 0Bh</td><td>Slave 3 w/o TWI Data Transfer</td></tr> <tr><td>137.0</td><td>Base + 0Ch</td><td>Slave 4 w/o TWI Data Transfer</td></tr> <tr><td>158.0</td><td>Base + 0Dh</td><td>Slave 5 w/o TWI Data Transfer</td></tr> <tr><td>182.0</td><td>Base + 0Eh</td><td>Slave 6 w/o TWI Data Transfer</td></tr> <tr><td>Ground</td><td>Slave PMBus Disconnect</td><td>Slave w/ TWI Data Transfer</td></tr> <tr><td>VDD</td><td>Slave PMBus Disconnect</td><td>Slave w/o TWI Data Transfer</td></tr> </tbody> </table>	R_ADDR (kΩ)	Address	Device	9.31	Base + 00h	Master w/ TWI Data Transfer	14.3	Base + 01h	Master w/ TWI Data Transfer	20.0	Base + 02h	Master w/o TWI Data Transfer	26.7	Base + 03h	Slave 1 w/ TWI Data Transfer	34.0	Base + 04h	Slave 2 w/ TWI Data Transfer	42.2	Base + 05h	Slave 3 w/ TWI Data Transfer	51.1	Base + 06h	Slave 4 w/ TWI Data Transfer	61.9	Base + 07h	Slave 5 w/ TWI Data Transfer	73.2	Base + 08h	Slave 6 w/ TWI Data Transfer	86.6	Base + 09h	Slave 1 w/o TWI Data Transfer	102.0	Base + 0Ah	Slave 2 w/o TWI Data Transfer	118.0	Base + 0Bh	Slave 3 w/o TWI Data Transfer	137.0	Base + 0Ch	Slave 4 w/o TWI Data Transfer	158.0	Base + 0Dh	Slave 5 w/o TWI Data Transfer	182.0	Base + 0Eh	Slave 6 w/o TWI Data Transfer	Ground	Slave PMBus Disconnect	Slave w/ TWI Data Transfer	VDD	Slave PMBus Disconnect	Slave w/o TWI Data Transfer
R_ADDR (kΩ)	Address	Device																																																								
9.31	Base + 00h	Master w/ TWI Data Transfer																																																								
14.3	Base + 01h	Master w/ TWI Data Transfer																																																								
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Ground	Slave PMBus Disconnect	Slave w/ TWI Data Transfer																																																								
VDD	Slave PMBus Disconnect	Slave w/o TWI Data Transfer																																																								
				<i>Address Options</i>																																																						
				000 0000 to 000 1100      Not Allowed																																																						
				000 1101 to 001 1000      OK																																																						

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**Table 22. DETAILS FOR 0xC8 – PMBUS\_BASE\_ADDR (continued)**

PMBUS_BASE_ADDR		Default = 0xC8			
Bit(s)	Name	R/W	Default	Details	
				010 1001 to 010 0111	Not recommended as Base Addresses
				010 1000	Not Allowed
				010 1001 to 010 1011	Not recommended as Base Addresses
				010 1100 to 010 1101	Not Allowed
				010 1110 to 011 0110	Not recommended as Base Addresses
				011 0111	Not Allowed
				011 1000 to 011 1111	Not recommended as Base Addresses
				100 0000 to 100 0100	Not Allowed
				100 0101 to 100 0111	Not recommended as Base Addresses
				100 1000 to 100 1011	Not Allowed
				100 1101 to 101 0001	OK
				101 0010 to 110 0000	Not recommended as Base Addresses
				110 0001	Not Allowed
				110 0010 to 110 1000	OK
				110 1001 to 111 0111	Not recommended as Base Addresses
				111 1000 to 111 1111	Not Allowed
				Not allowed address are per the SMBus specification. Not recommend address are those that fall within 15 addresses under a “Not Allowed” address. Depending on the number of Slaves, some of these addresses may be used. For instance a base address of 2Eh could be used if 7 or fewer eFuses will be connected to the PMBus. Default addresses other than 64h can be ordered.	
0	unused	Read	0		

**Table 23. DETAILS FOR 0xC9 – DEVICE\_CONFIG**

0xC9		DEVICE_CONFIG		Default = 0x3041		
Bit(s)	Name	R/W	Default	Details		
15:14	unused	Read	00			
13:12	ocp3_level	R/W	11	Sets the Over Current Protection level – 3.		
				<b>Value</b>	<b>Description</b>	
				00	50	
				01	60	
				10	70	
				11	80 (Default)	
			Upon triggering an over-current protection fault the device shall perform the following actions: <ul style="list-style-type: none"> <li>• Set the IOUT_OC_FAULT bit in the STATUS_BYTE</li> <li>• Set the IOUT bit in the STATUS_WORD</li> <li>• Set the IOUT_OC_FAULT bit in the STATUS_IOUT register, and</li> <li>• The device notifies the host (asserts PG pin low, asserts ALERT# if not masked)</li> </ul>			
11:10	ocp2_level	R/W	00	Sets the Over Current Protection level – 2.		
				<b>Value</b>	<b>Description</b>	
				00	None (Default)	
				01	25	
				10	35	
				11	45	

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**Table 23. DETAILS FOR 0xC9 – DEVICE\_CONFIG** (continued)

0xC9	DEVICE_CONFIG		Default = 0x3041		
Bit(s)	Name	R/W	Default	Details	
				<p>Upon triggering an over-current protection fault the device shall perform the following actions:</p> <ul style="list-style-type: none"> <li>• Set the IOUT_OC_FAULT bit in the STATUS_BYTE</li> <li>• Set the IOUT bit in the STATUS_WORD</li> <li>• Set the IOUT_OC_FAULT bit in the STATUS_IOUT register, and</li> <li>• The device notifies the host (asserts PG pin low, asserts ALERT# if not masked)</li> </ul>	
9:8	ocp1_level	R/W	00	Sets the Over Current Protection level – 1.	
				<b>Value</b>	<b>Description</b>
				00	<i>None (Default)</i>
				01	10
				10	15
				11	20
				<p>Upon triggering an over-current protection fault the device shall perform the following actions:</p> <ul style="list-style-type: none"> <li>• Set the IOUT_OC_FAULT bit in the STATUS_BYTE</li> <li>• Set the IOUT bit in the STATUS_WORD</li> <li>• Set the IOUT_OC_FAULT bit in the STATUS_IOUT register, and</li> <li>• The device notifies the host (asserts PG pin low, asserts ALERT# if not masked)</li> </ul>	
7:6	ocp3_delay	R/W	01	Sets the period of time from when the over current condition 3 is detected and when the device shuts down.	
				<b>Value</b>	<b>Delay (ms)</b>
				00	<i>0.25</i>
				01	1 (Default)
				10	10
				11	50
5:4	ocp2_delay	R/W	00	Sets the period of time from when the over current condition 2 is detected and when the device shuts down.	
				<b>Value</b>	<b>Delay (ms)</b>
				00	<i>0.25 (Default)</i>
				01	1
				10	10
				11	50
3:2	ocp1_delay	R/W	00	Sets the period of time from when the over current condition 1 is detected and when the device shuts down.	
				<b>Value</b>	<b>Delay (ms)</b>
				00	<i>0.25 (Default)</i>
				01	1
				10	10
				11	50
1	output_pd	R/W	0	To enable or Disable the internal Pulldown refer to the settings below.	
				<b>Value</b>	<b>Description</b>
				0	Internal Pulldown Disabled (Default)
				1	Internal Pulldown Enabled
0	retry_latchoff	R/W	1	<b>Value</b>	
				<b>Description</b>	
				0	Latch-Off
				1	Auto-Retry (Default)
				NOTE: This bit is ignored in a Slave device as the decision to restart is controlled by the master.	

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## Status Registers

**Table 24. DETAILS FOR 0x78 – STATUS\_BYTE**

0x78	STATUS_BYTE		Default = 0x00		
Bit(s)	Name	R/W	Default	Details	
7	busy	Read	0	This bit indicates if the NCP81428 is ready to communicate on the PMBus.	
				<b>Value</b>	<b>Description</b>
				0	Device is ready to communicate. (Default)
				1	Device is busy and unable to communicate.
6	off	Read	0	Provides status byte read if the device is not supplying power to the output.	
				<b>Value</b>	<b>Description</b>
				0	The MOSFET is "On" (Default)
				1	The MOSFET is "Off" This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	vout_ov_fault	Read	0	This feature is not supported. Read of this bit will always return a "0".	
4	iout_oc_fault	Read	0	Provides status byte read of the Over-Current Protections and Short Circuit faults.	
				<b>Value</b>	<b>Description</b>
				0	None of the over-current levels have been exceeded (Default)
				1	An Over-Current limit has been exceeded
3	vin_uv_fault	Read	0	Provides status byte read of the Vin under voltage faults.	
				<b>Value</b>	<b>Description</b>
				0	No under-voltage faults have occurred (Default)
				1	At least one under-voltage fault has occurred.
2	temperature	Read	0	Provides status byte read of the temperature warnings and faults.	
				<b>Value</b>	<b>Description</b>
				0	There haven't been any over-temperature warnings or over-temperature shutdowns. (Default)
				1	At least one over-temperature warning or over temperature shutdown has occurred.
1	cml	Read	0	Provides status byte read of the communications faults.	
				<b>Value</b>	<b>Description</b>
				0	No communication faults (Default)
				1	Communication fault has been detected
0	none_of_the_above	Read	0	<b>Value</b>	
				<b>Description</b>	
				0	No fault has occurred
				1	A fault or warning not listed in bits [7:1] of this byte has occurred.
				List of faults that can set this bit : VIN_OV_WARN_LIMIT VIN_UV_WARN_LIMIT	

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**Table 25. DETAILS FOR 0x79 – STATUS\_WORD**

0x79	STATUS_WORD		Default = 0x0800		
Bit(s)	Name	R/W	Default	Details	
15	vout	Read	0	This feature is to provide information on:	
				<b>Value</b>	<b>Description</b>
				0	Output Voltage fault or warning has not occurred (Default)
				1	An output voltage fault or warning has occurred
14	iout_pout	Read	0	Provides status of whether the device is.	
				<b>Value</b>	<b>Description</b>
				0	Output is okay (Default)
				1	An output over-current or output power fault or warning has occurred
13	input	Read	0	Provides status of whether the input is good or not.	
				<b>Value</b>	<b>Description</b>
				0	Input is good (Default)
				1	An input voltage, input current or input power fault or warning has occurred
12	mfr_specific	Read	0	This is bit is an OR'd function of all bits in the STATUS_MFR_STATUS register.	
				<b>Value</b>	<b>Description</b>
				0	No faults or warnings are reported in register 0x80, STATUS_MFR_STATUS (Default)
				1	A fault(s) or warning is shown in register 0x80, STATUS_MFR_STATUS
11	pg_status#	Read	1	This bit indicates whether the voltage on the output is a valid level to operate from.	
				<b>Value</b>	<b>Description</b>
				0	Output voltage has risen to a value close to VIN
				1	Either the output voltage has not reached a level close to VIN during soft start or the voltage has fallen to level not recommended for operation (Default)
10	fans	Read	0	This feature is not supported. Read of this bit will always return a "0".	
9	other	Read	0	This feature is not supported. Read of this bit will always return a "0".	
8	unknown	Read	0	This feature is not supported. Read of this bit will always return a "0".	
7	busy	Read	0	This bit indicates if the NCP81428 is ready to communicate on the PMBus.	
				<b>Value</b>	<b>Description</b>
				0	Device is ready to communicate. (Default)
				1	Device is busy and unable to communicate.
6	off	Read	0	Provides status byte read if the device is not supplying power to the output.	
				<b>Value</b>	<b>Description</b>
				0	The MOSFET is "On" (Default)
				1	The MOSFET is "Off"
				This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. This bit cannot be cleared, reflects device status.	
5	vout_ov_fault	Read	0	This feature is not supported. Read of this bit will always return a "0".	

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**Table 25. DETAILS FOR 0x79 – STATUS\_WORD** (continued)

0x79	STATUS_WORD		Default = 0x0800		
Bit(s)	Name	R/W	Default	Details	
4	iout_oc_fault	Read	0	Provides status byte read of the Over-Current Protections and Short Circuit faults.	
				<b>Value</b>	<b>Description</b>
				0	None of the over-current levels have been exceeded and no short circuit fault events have occurred. (Default)
				1	An Over-Current limit fault has been exceeded or Short Circuit event has occurred.
3	vin_uv_fault	Read	0	Provides status byte read of the Vin under voltage faults.	
				<b>Value</b>	<b>Description</b>
				0	No input under-voltage fault has occurred (Default)
				1	Input under-voltage fault has occurred.
2	temperature	Read	0	Provides status byte read of the temperature warnings and faults.	
				<b>Value</b>	<b>Description</b>
				0	There haven't been any over-temperature warnings or over-temperature shutdowns. (Default)
				1	At least one over-temperature warning or over temperature shutdown has occurred.
1	cml	Read	0	Provides status byte read of the communications faults.	
				<b>Value</b>	<b>Description</b>
				0	No communication faults (Default)
				1	Communication (memory or logic) fault has been detected
0	none_of_the_above	Read	0	<b>Value</b>	
				<b>Description</b>	
				0	A fault or warning other than in bits [7:1] did not occur (Default)
				1	A fault or warning other than in bits [7:1] has occurred (TWI data transfer fault)

**Table 26. DETAILS FOR 0x7B – STATUS\_IOUT**

0x7B	STATUS_IOUT		Default = 0x0800		
Bit(s)	Name	R/W	Default	Details	
7	iout_oc_fault	Read	0	Indicates an over current fault has occurred	
				<b>Value</b>	<b>Description</b>
				0	No over current fault has occurred. (Default)
				1	An over current fault has occurred.
6	iout_oc_lv_fault	Read	0	This feature is not supported. Read of this bit will always return a "0".	
5	iout_oc_warning	Read	0	This feature is not supported. Read of this bit will always return a "0".	
4	iout_uc_fault	Read	0	This feature is not supported. Read of this bit will always return a "0".	
3	iout_share_fault	Read	0	This feature is not supported. Read of this bit will always return a "0".	
2	iin_pwr_lmt	Read	0	This feature is not supported. Read of this bit will always return a "0".	
1	pout_op_fault	Read	0	This feature is not supported. Read of this bit will always return a "0".	
0	pout_warn	Read	0	This feature is not supported. Read of this bit will always return a "0".	

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**Table 27. DETAILS FOR 0x7C – STATUS\_INPUT**

0x7C	STATUS_INPUT		Default = 0x00		
Bit(s)	Name	R/W	Default	Details	
7	vin_ov_fault	Read	0	Indicates an over voltage fault has occurred.	
				<b>Value</b>	<b>Description</b>
				0	No over voltage fault on the input has occurred. (Default)
				1	An over voltage fault on the input has occurred.
6	vin_ov_warn	Read	0	Indicates an over voltage warning has occurred.	
				<b>Value</b>	<b>Description</b>
				0	No over voltage warning on the input has occurred. (Default)
				1	An over voltage warning on the input has occurred.
5	vin_uv_warn	Read	0	Indicates an under voltage warning has occurred.	
				<b>Value</b>	<b>Description</b>
				0	No under voltage warning on the input has occurred (Default)
				1	An under voltage warning on the input has occurred.
4	vin_uv_fault	Read	0	Indicates an under voltage fault has occurred.	
				<b>Value</b>	<b>Description</b>
				0	No under voltage fault on the input has occurred. (Default)
				1	An under voltage fault on the input has occurred.
3	iout_share_fault	Read	0	This feature is not supported. Read of this bit will always return a “0”.	
2	iin_pwr_lmt	Read	0	This feature is not supported. Read of this bit will always return a “0”.	
1	pout_op_fault	Read	0	This feature is not supported. Read of this bit will always return a “0”.	
0	pout_warn	Read	0	This feature is not supported. Read of this bit will always return a “0”.	

**Table 28. DETAILS FOR 0x7D – STATUS\_TEMP**

0x7D	STATUS_TEMP		Default = 0x00		
Bit(s)	Name	R/W	Default	Details	
7	ot_fault	Read	0	Indicates an over temperature fault has occurred.	
				<b>Value</b>	<b>Description</b>
				0	No over temperature fault has occurred. (Default)
				1	An over temperature fault has occurred.
6	ot_warning	Read	0	Indicates an over temperature warning has occurred.	
				<b>Value</b>	<b>Description</b>
				0	No over temperature warning has occurred. (Default)
				1	An over temperature warning has occurred.
3	ut_warning	Read	0	This feature is not supported. Read of this bit will always return a “0”.	
2	ut_fault	Read	0	This feature is not supported. Read of this bit will always return a “0”.	
3:0	UNUSED		0000		

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**Table 29. DETAILS FOR 0x7E – STATUS\_CML**

0x7E	STATUS_CML		Default = 0x00		
Bit(s)	Name	R/W	Default	Details	
7	inv_command	Read	0	Indicates an invalid or unsupported command received.	
				<b>Value</b>	<b>Description</b>
				0	All commands received are valid. (Default)
				1	An invalid or unsupported command has been received.
6	inv_data	Read	0	Indicates an invalid or unsupported data received.	
				<b>Value</b>	<b>Description</b>
				0	All data received are valid. (Default)
				1	An invalid or unsupported data has been received.
5	packet_error	Read	0	Indicates a packet error has occurred.	
				<b>Value</b>	<b>Description</b>
				0	No packet error communications (PEC) has occurred. (Default)
				1	A packet error communications (PEC) has occurred.
4	mem_fault	Read	0	This feature is not supported. Read of this bit will always return a “0”.	
3	proc_fault	Read	0	This feature is not supported. Read of this bit will always return a “0”.	
2	UNUSED		0		
1	comm_other	Read	0	This feature is not supported. Read of this bit will always return a “0”.	
0	Other	Read	0	This feature is not supported. Read of this bit will always return a “0”.	

**Table 30. DETAILS FOR 0x80 – STATUS\_MFR\_SPECIFIC**

0x80	STATUS_MFR_SPECIFIC		Default = 0x00		
Bit(s)	Name	R/W	Default	Details	
7	gok_fault	Read	0	<b>Value</b>	<b>Description</b>
				0	No GOK fault has occurred. (Default)
				1	A GOK fault has occurred.
6	scp_fault	Read	0	<b>Value</b>	<b>Description</b>
				0	No SCP fault has occurred. (Default)
				1	An SCP fault has occurred.
5	mst_fault	Read	0	<b>Value</b>	<b>Description</b>
				0	No Master fault has occurred. (Default)
				1	A Master fault has occurred.
4	slv_fault	Read	0	<b>Value</b>	<b>Description</b>
				0	No Slave fault has occurred. (Default)
				1	A Slave fault has occurred.
3	reserved	Read	0	This feature is not supported. Read of this bit will always return a “0”.	
2	twi_fault	Read	0	<b>Value</b>	<b>Description</b>
				0	No failure to transmit Master data to Slave has occurred. (Default)
				1	A failure to transmit Master data to Slave has occurred.
1	ss_fault	Read	0	<b>Value</b>	<b>Description</b>
				0	No soft-start current limiting fault (250us qualified) has occurred. (Default)
				1	A soft-start current limiting fault (250us qualified) has occurred.
0	dev_temp_warn	Read	0	<b>Value</b>	<b>Description</b>
				0	Die temperatures evened out across devices on the board (Default)
				1	Die temperatures are uneven, requires attention.

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## Read Registers

**Table 31. DETAILS FOR 0x19 – CAPABILITY**

0x19	CAPABILITY		Default = 0xB0		
Bit(s)	Name	R/W	Default	Details	
7	pec_cap	Read	1	<b>Value</b>	<b>Description</b>
				0	Packet Error Checking (PEC) is not supported
				1	Packet Error Checking (PEC) enabled (Default)
6:5	pmbus_spd	Read	01	<b>Value</b>	<b>Description</b>
				00	Maximum communication speed is 100 kHz
				01	Maximum communication speed is 400 kHz (Default)
				10	Maximum communication speed is 1 MHz (Not Supported)
				11	Reserved
4	alert#_cap	Read	1	<b>Value</b>	<b>Description</b>
				0	Device does not have Alert# pin and does not support PMBus Alert Response Protocol.
				1	Device provides an Alert# pin and supports PMBus Alert Response protocol (Default)
3	num_format	Read	0	Numeric Format support	
				<b>Value</b>	<b>Description</b>
				0	Numeric data is LINEAR11, ULINEAR 16, SLINEAR 16 or DIRECT FORMAT (Default)
				1	Numeric data is IEEE Half Precision Floating Point.
2	avsbu_sup	Read	0	AVSBus support	
				<b>Value</b>	<b>Description</b>
				0	AVSBus is not supported (Default)
				1	AVSBus is supported
1:0	UNUSED		00		

**Table 32. DETAILS FOR 0x20 – VOUT\_MODE**

0x20	VOUT_MODE		Default = 0xB0							
Bit(s)	Name	R/W	Default	Details						
7:0	vout_mode	Read	00011011	This establishes the 5 bit 2's complement exponent for the 16 bit mantissa delivered as data bytes for the READ Vout command (8Bh).						
				VOUT MODE DATA BYTE:						
				7	6	5	4	3	2	1
			Mode			Exponent (N)				

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**Table 33. DETAILS FOR 0x88 – READ\_VIN**

0x88	READ_VIN		Default = 0xD800			
Bit(s)	Name	R/W	Default	Details		
15:0	read_vin	Read	1101100000000000	<b>Range</b>	<b>Resolution</b>	
				0 to 31.96875 V	31.25 mV	
				The READ_VIN command returns the measured input voltage (V <sub>IN</sub> ), Volts. Two data bytes are encoded in LINEAR11 format with 5 bits signed exponent and 11 bits mantissa. The exponent is fixed –5 (11011b). Example READ_VIN register values.		
				<b>Data (h)</b>	<b>Data (b)</b>	<b>VIN</b>
				D800	1101 1000 0000 0000	0.00
				D8C0	1101 1000 1100 0000	6.00
				D900	1101 1001 0000 0000	8.00
				D940	1101 1001 0100 0000	10.00
				D980	1101 1001 1000 0000	12.00
				D9C0	1101 1001 1100 0000	14.00
				DA00	1101 1010 0000 0000	16.00
				DA40	1101 1010 0100 0000	18.00
				DA80	1101 1010 1000 0000	20.00
				DAC0	1101 1010 1100 0000	22.00
				DB00	1101 1011 0000 0000	24.00
DBFF	1101 1011 1111 1111	31.96875				

**Table 34. DETAILS FOR 0x8B – READ\_VOUT**

0x8B	READ_VOUT		Default = 0x0000			
Bit(s)	Name	R/W	Default	Details		
15:0	read_vout	Read	0000000000000000	<b>Range</b>	<b>Resolution</b>	
				0 to 31.96875 V	31.25 mV	
				The READ_VOUT command returns the measured output voltage (V <sub>OUT</sub> ), Volts. Two data bytes are encoded in ULINEAR16 format as shown below: Example READ_VOUT register values.		
				<b>Data (h)</b>	<b>Data (b)</b>	<b>VOUT</b>
				0000	0000 0000 0000 0000	0.00
				00C0	0000 0000 1100 0000	6.00
				0100	0000 0001 0000 0000	8.00
				0140	0000 0001 0100 0000	10.00
				0180	0000 0001 1000 0000	12.00
				01C0	0000 0001 1100 0000	14.00
				0200	0000 0010 0000 0000	16.00
				0240	0000 0010 0100 0000	18.00
				0280	0000 0010 1000 0000	20.00
				03FF	0000 0011 1111 1111	31.96825

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**Table 35. DETAILS FOR 0x8C – READ\_IOUT**

0x8C	READ_IOUT		Default = 0xE800						
Bit(s)	Name	R/W	Default	Details					
15:0	read_iout	Read	1110100000000000	<b>Range</b>	<b>Resolution</b>				
				0 to +127.875 A	125 mA				
				<p>The IOUT register provides a digitized value of the voltage developed across the equivalent resistance on the IMON pins. In an application where there is a single eFuse, this voltage is representative of the current the device is delivering to the load. In an application where multiple eFuses are in parallel, the digitized voltage value represents the total load current delivered by the eFuse devices, divided by the number of eFuses in parallel. This is based on the equivalent resistance of all R<sub>IMON</sub> resistors of each eFuse being in parallel. For instance: If 5 eFuses are in parallel, the Req = 2 kΩ/5 = 400 Ω.</p> <p>The READ_IOUT command returns the measured output current IOUT, Amps. Two data bytes are encoded in LINEAR11 format with 5 bits signed exponent and 11 bits mantissa. The exponent is fixed –3(11101b). In this application, the current should never be negative and thus bit [10] should always be 0.</p> <p>Example READ_IOUT register values.</p>					
				<b>Data (h)</b>	<b>Data (b)</b>	<b>IOUT (A)</b>	<b>Vimon (V)</b>		
				E800	1110 1000 0000 0000	0.00	0.00		
				E850	1110 1000 0101 0000	10.00	0.20		
				E8A0	1110 1000 1010 0000	20.00	0.40		
				E8F0	1110 1000 1111 0000	30.00	0.60		
				E940	1110 1001 0100 0000	40.00	0.80		
				E990	1110 1001 1001 0000	50.00	1.00		
				E9E0	1110 1001 1110 0000	60.00	1.20		
				EA30	1110 1010 0011 0000	70.00	1.40		
				EA80	1110 1010 1000 0000	80.00	1.60		
				EAD0	1110 1010 1101 0000	90.00	1.80		
EB20	1110 1011 0010 0000	100	2.0						
EBFF	1110 1011 1111 1111	127.875	2.575						
<p>NOTE: R<sub>IMON</sub> is 2 kΩ per eFuse. In parallel configuration, the R<sub>IMON</sub> equivalent resistance will be 2 kΩ/#D, where #D represents the number of eFuses connected in parallel.</p>									

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**Table 36. DETAILS FOR 0x8D – READ\_TEMPERATURE**

0x8D	READ_TEMPERATURE		Default = 0xF828			
Bit(s)	Name	R/W	Default	Details		
15:0	read_temp	Read	1111100000101000	<b>Range</b>	<b>Resolution</b>	
				-20.00°C to +256.00°C	0.5°C	
				The READ_TEMPERATURE command returns the internal device temperature. Two data bytes are encoded in LINEAR11 format with 5 bits signed exponent and 11 bits mantissa. The exponent is fixed -1 (11111b). Example READ_TEMP register values.		
				<b>Data (h)</b>	<b>Data (b)</b>	<b>IC Temp</b>
				FFD8	1111 1111 1101 1000	-20.0
				F800	1111 1000 0000 0000	0.00
				F828	1111 1000 0010 1000	20.0
				F850	1111 1000 0101 0000	40.0
				F878	1111 1000 0111 1000	60.0
				F8A0	1111 1000 1010 0000	80.0
				F8C8	1111 1000 1100 1000	100.0
				F8F0	1111 1000 1111 0000	120.0
				F918	1111 1001 0001 1000	140.0
F92C	1111 1001 0010 1100	150.0				

**Table 37. DETAILS FOR 0x98 – PMBUS REVISION**

0x98	PMBUS REVISION		Default = 0x33		
Bit(s)	Name	R/W	Default	Details	
7:4	rev_part_I	Read	0101	PMBUS_REVISION command Stores or reads the revision of the PMBus to which the device is compliant. The command has one data byte. Bits [7:4] indicate the revision of the PMBus specification Part I to which the device is compliant. Devices may support this as a read only command.	
				<b>Bits [7:4]</b>	<b>Part I Revision</b>
				0000b	1.0
				0001b	1.1
				0010b	1.2
				0011b	1.3
				0100b	1.3.1
				0101b	1.4 (Default)
3:0	rev_part_II	Read	0101	PMBUS_REVISION command Stores or reads the revision of the PMBus to which the device is compliant. The command has one data byte. Bits [3:0] indicate the revision of the PMBus specification Part II to which the devices compliant. Devices may support this as a read only command.	
				<b>Bits [3:0]</b>	<b>Part II Revision</b>
				0000b	1.0
				0001b	1.1
				0010b	1.2
				0011b	1.3
				0100b	1.3.1
				0101b	1.4 (Default)

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**Table 38. DETAILS FOR 0xAD – IC\_DEVICE\_ID**

0xAD	IC_DEVICE_ID		Default = 0x2800				
Bit(s)	Name	R/W	Default	Details			
15:0	ic_device_id	Read	0010100000000000	The read only IC_DEVICE_ID register contains manufacturer specific type or part number information. The Block Read format must be used to access this 2 byte read.			
							UPDATE
				[15:0]	0010, 1000, 0000 00XX	2800 2801 2802 2803	NCP81428 – 64h NCP81428A – 4Ch NCP81428B – 38h NCP81428C – 0Dh

**Table 39. DETAILS FOR 0xC4 – PEAK\_IOUT**

0xC4	PEAK_IOUT		Default = 0xE800				
Bit(s)	Name	R/W	Default	Details			
15:0	read_peak_iout	R/CLR	1110100000000000	Range	Resolution		
				0 to +127.875 A	125 mA		
				The PEAK_IOUT command returns the measured peak output current at an OCP event, Amps. Two data bytes are encoded in LINEAR11 format with 5 bits signed exponent and 11 bits mantissa. The exponent is fixed –3 (11101b). In this application, the current should never be negative and thus bit [10] should always be 0. Note that PEAK_IOUT reporting shares the same accuracy and resolution as IOUT reporting. Example PEAK_IOUT register values.			
				Data (h)	Data (b)	IOUT (A)	Vimon (V)
				E800	1110 1000 0000 0000	0.00	0.00
				E850	1110 1000 0101 0000	10.00	0.20
				E8A0	1110 1000 1010 0000	20.00	0.40
				E8F0	1110 1000 1111 0000	30.00	0.60
				E940	1110 1001 0100 0000	40.00	0.80
				E990	1110 1001 1001 0000	50.00	1.00
				E9E0	1110 1001 1110 0000	60.00	1.20
				EA30	1110 1010 0011 0000	70.00	1.40
				EA80	1110 1010 1000 0000	80.00	1.60
				EAD0	1110 1010 1101 0000	90.00	1.80
EB20	1110 1011 0010 0000	100	2.0				
EBFF	1110 1011 1111 1111	127.875	2.575				
NOTE: R <sub>IMON</sub> is 2 kΩ per eFuse. In parallel configuration, the R <sub>IMON</sub> equivalent resistance will be 2 kΩ/#D, where #D represents the number of eFuses connected in parallel.							

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**Table 40. DETAILS FOR 0xC6 – READ\_HOT\_DEVICE**

0xC6	READ_HOT_DEVICE	Default = 0xF828				
Bit(s)	Name	R/W	Default	Details		
15:0	read_hot_dev	Read	1111100000101000	<b>Range</b>	<b>Resolution</b>	
				-256.00°C to +256.00°C	0.5°C	
				<p>The READ_HOT_DEVICE command returns the hottest measured die in the application. The VTEMP output can source much more current than it can sink, so that if multiple VTEMP outputs are connected together, the voltage of all VTEMP outputs will be driven to the voltage produced by the hottest NCP81428. Two data bytes are encoded in LINEAR11 format with 5 bits signed exponent and 11 bits mantissa. The exponent is fixed -1 (11111b). Example READ_HOT_DEVICE register values.</p>		
				<b>Data (h)</b>	<b>Data (b)</b>	<b>IC Temp</b>
				F800	1111 1000 0000 0000	0.00
				F828	1111 1000 0010 1000	20.0
				F850	1111 1000 0101 0000	40.0
				F878	1111 1000 0111 1000	60.0
				F8A0	1111 1000 1010 0000	80.0
				F8C8	1111 1000 1100 1000	100.0
				F8F0	1111 1000 1111 0000	120.0
				F918	1111 1001 0001 1000	140.0
F92C	1111 1001 0010 1100	150.0				

# NCP81428

## Application Circuit

### Application Circuit Diagram

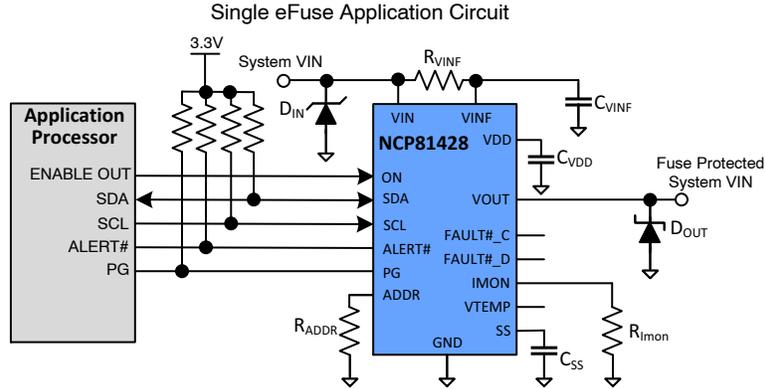


Figure 54. Application Circuit

### Application Circuit Components

Table 41. PRIMARY COMPONENTS

Component	Manufacturer	Part Number	Value	Case Size	Voltage Rating
R <sub>VINF</sub>	Vishay	CRCW06031R00FKEA	1 Ω	0603	75 V
C <sub>VINF</sub>	Murata	0603YC104KAT2A	0.1 μF	0603	16 V
C <sub>VDD</sub>	Murata	GRM188C81E475KE11D	4.7 μF	0603	25 V
R <sub>Imon</sub>	KOA Speer	RK73H1JTTD2001F	2 kΩ	0603	75 V
C <sub>SS</sub>	Murata	0603YC104KAT2A	0.1 μF	0603	16 V
D <sub>IN</sub>	LittleFuse	SMBJ13A	Clamping Voltage = 21.5 V, Peak Current = 28 A	DO- 214AA, 3.30 mm x 4.06 mm	V <sub>r</sub> = 13 V
D <sub>OUT</sub>	onsemi	MBR2045EMFST3G	20 A	8-SOFL, 5 mm x 6 mm	45 V

### Application Component Guidelines

#### Transient Voltage Suppression

Hotswap eFuses are prone to sudden interruption in current flow, input cable inductance creates a positive voltage transient spike on the input of the device. These type of events if not suppressed by an external TVS diode they could easily exceed the AMR of the NCP81428. Similarly,

output inductance creates a negative voltage spike on the output of the device that needs to be clamped by a diode with the cathode connected to ground and the anode to Vout.

Users can roughly estimate the magnitudes of these spike by referring to the Formula below:

$$V_{\text{Spike}} = V_{\text{DC}} + I_{\text{OUT}} \times \sqrt{L / C} \quad (\text{eq. 3})$$

# NCP81428

## ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Shipping†
NCP81428MNTXG	NCP81428	LQFN32 5x5, 0.5P	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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onsemi is licensed by the Philips Corporation to carry the I<sup>2</sup>C bus protocol.

# MECHANICAL CASE OUTLINE

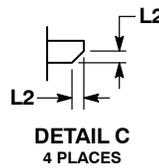
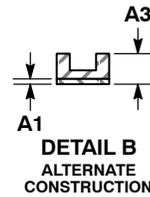
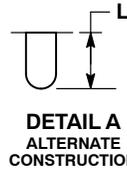
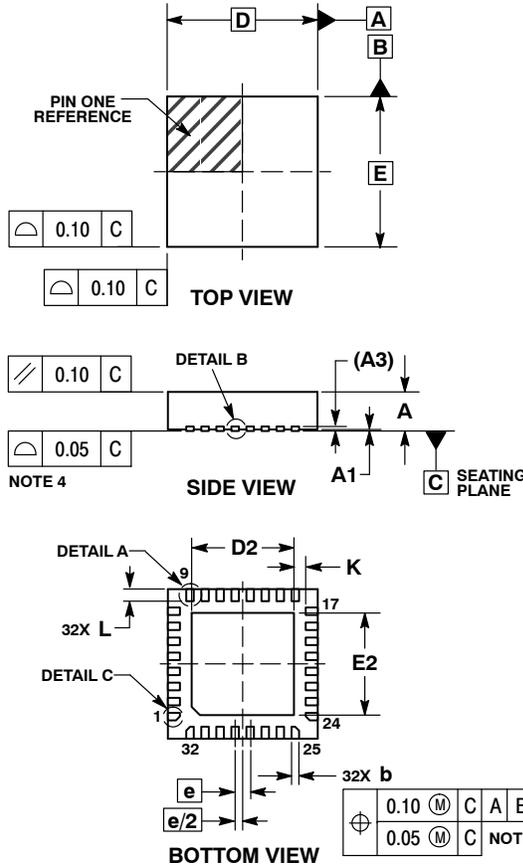
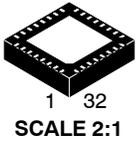
## PACKAGE DIMENSIONS

ON Semiconductor®



LQFN32 5x5, 0.5P  
CASE 487AA  
ISSUE A

DATE 03 OCT 2017

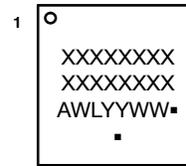


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	1.20	1.40
A1	---	0.05
A3	0.20	REF
b	0.18	0.30
D	5.00	BSC
D2	3.30	3.50
E	5.00	BSC
E2	3.30	3.50
e	0.50	BSC
L	0.30	0.50
L2	0.13	REF

**GENERIC MARKING DIAGRAM\***

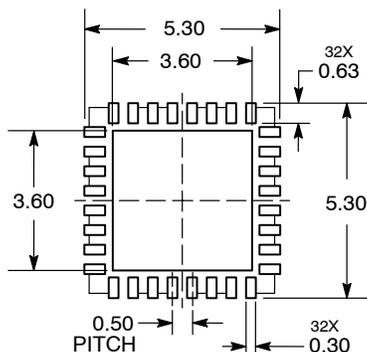


- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**RECOMMENDED SOLDERING FOOTPRINT\***



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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