USRP X300

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USRP X300 (KINTEX7-325T FPGA, 2 CHANNELS, 10GIGE AND PCIE BUS)

The Ettus Research USRP X300 is a high-performance, scalable software-defined radio (SDR) platform for designing and deploying next-generation wireless communications systems.

Overview +

Features +

Additional Resources +

Overview | Features | Additional Resources

Overview

The Ettus Research USRP X300 is a high-performance, scalable software-defined radio (SDR) platform for designing and deploying next-generation wireless communications systems. The hardware architecture combines two extended-bandwidth daughterboard slots covering DC – 6 GHz with up to 160 MHz of baseband bandwidth, multiple high-speed interface options (PCIe, dual 10 GigE, dual 1 GigE), and a large user-programmable Kintex-7 FPGA in a convenient

desktop or rack-mountable half-wide 1U form factor. In addition to providing best-in-class hardware performance, the open source software architecture of X300 provides cross-platform UHD driver support making it compatible with a large number of supported development frameworks, reference architectures, and open source projects.

Operating Systems	Linux Windows
Development Frameworks	GNU Radio Xilinx Vivado 2015.2 Design Suite

Table 1: Operating systems, development frameworks, and reference applications

High-Performance User-Programmable FPGA

At the heart of the USRP X300, the XC7K325T FPGA provides high-speed connectivity between all major components within the device including radio frontends, host interfaces, and DDR3 memory. The default FPGA core provided with UHD provides all of the functional blocks for digital down-conversion and up-conversion, fine-frequency tuning, and other DSP functions allowing it to be interchangeable with other USRP devices using the UHD architecture. The large Kintex-7 FPGA provides additional space for developers to incorporate custom DSP blocks and is compatible with a large number of USRP-supported development frameworks, reference architectures, and open source projects.

	USRP N210	**USRP X300**	**USRP X310**
FPGA	Spartan3 XC3SD3400A	Kintex 7-325T	Kintex 7-410T
Logic Cells	53k	321k	406k
Memory	2,268 Kb	16,020 Kb	28,620 Kb
Multipliers	126	840	1540
Clock Rate	100 MHz	200 MHz	200 MHz

Streaming Bandwidth per Channel (16-bit)	25 MS/s	200 MS/s	200 MS/s

Table 2: FPGA resource comparison

Multiple High-Speed Interface Options

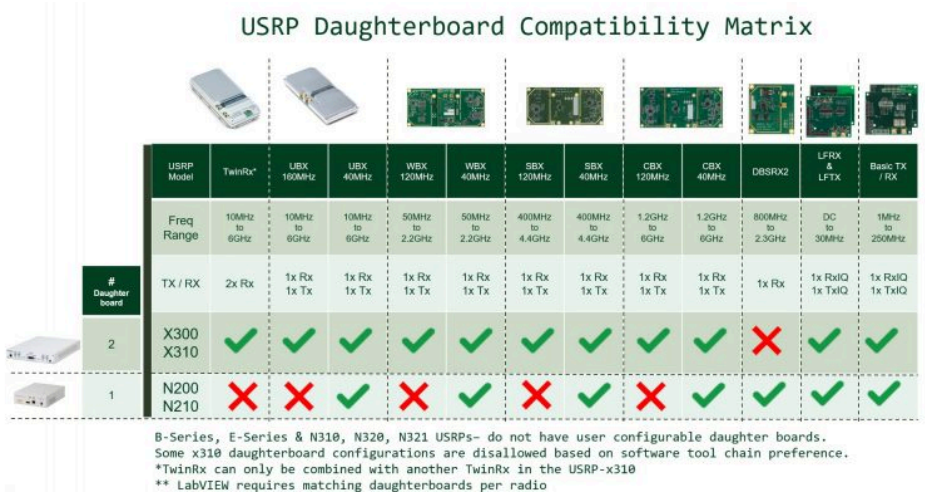
The USRP X300 provides multiple interface options. Out of the box, 1 GigE provides a convenient way to get started. For extended bandwidth and lower latency applications such as PHY/MAC research, PCIe x4 provides an efficient bus for deterministic operation. Applications using network recorders or multiple processing nodes can be best served by the 10 GigE interface option.

Additional Features- GPSDO, GPIO, 1 GB DDR3, Synchronization

The X300 includes many additional features that facilitate wireless system development. On-board 1GB DDR3 with flexible access through the FPGA

reference design supplements the FPGA resources with buffering and data storage memory. An optional internal GPSDO provides a high-accuracy frequency reference, and global timing alignment to within 50 ns when synchronized to the GPS system. The external GPIO connector allows users to control external components such as amplifiers and switches, accept inputs like event triggers, and observe debug signals. The USRP X300 also includes an internal JTAG adapter that allows FPGA developers to easily load and debug new FPGA images.

**USRP X300 RF daughterboards sold separately*
Compatible RF Daughterboards: UBX, CBX, WBX, SBX, LFRX, LFTX, Basic TX/RX)



# Daughter board	USRP Model	TwinRx*	UBX 160MHz	UBX 40MHz	WBX 120MHz	WBX 40MHz	SBX 120MHz	SBX 40MHz	CBX 120MHz	CBX 40MHz	DBSRX2	LFRX & LFTX	Basic TX / RX
	Freq Range	10MHz to 6GHz	10MHz to 6GHz	10MHz to 6GHz	50MHz to 2.2GHz	50MHz to 2.2GHz	400MHz to 4.4GHz	400MHz to 4.4GHz	1.2GHz to 6GHz	1.2GHz to 6GHz	800MHz to 2.3GHz	DC to 30MHz	1MHz to 250MHz
	TX / RX	2x Rx	1x Rx 1x Tx	1x Rx 1x Tx	1x Rx 1x Tx	1x Rx 1x Tx	1x Rx 1x Tx	1x Rx 1x Tx	1x Rx 1x Tx	1x Rx 1x Tx	1x Rx	1x RxIQ 1x TxIQ	1x RxIQ 1x TxIQ
2	X300 X310	✓	✓	✓	✓	✓	✓	✓	✓	✓	✗	✓	✓
1	N200 N210	✗	✗	✓	✗	✓	✗	✓	✗	✓	✓	✓	✓

B-Series, E-Series & N310, N320, N321 USRPs- do not have user configurable daughter boards.
Some x310 daughterboard configurations are disallowed based on software tool chain preference.
*TwinRx can only be combined with another TwinRx in the USRP-x310
** LabVIEW requires matching daughterboards per radio

Download Datasheet

Compatible Products

UBX 10-6000 MHz Rx/Tx (160

The UBX 160 daughterboard is...