2-Channel, 300 mA Current Source Output 16-Bit SoftSpan DAC

FEATURES

- Per channel programmable output ranges: 300 mA, 200 mA, 100 mA, 50 mA, 25 mA, 12.5 mA, 6.25 mA, and 3.125 mA
- Flexible 2.85 V to 33 V supply voltage
- 1 V dropout guaranteed
- Separate voltage supply per output channel
- Internal switches to optional negative supply
- Full 16-bit resolution at all ranges
- Guaranteed operation –40°C to 125°C
- Precision (10 ppm/°C maximum) internal reference or external reference input
- Analog mux monitors, voltages, and currents
- A/B toggle via SPI or dedicated pin
- 1.8 V to 5 V SPI
- 32-lead (5 mm × 5 mm) QFN package

APPLICATIONS

- Tunable lasers
- Semiconductor optical amplifiers
- Resistive heaters
- Current-mode biasing
- Proportional solenoid drive

GENERAL DESCRIPTION

The AD5778R is a 2-channel, 16-bit current source digital-to-analog converter (DAC), providing two high-compliance current source outputs with a guaranteed 1 V dropout at 200 mA. The device supports load voltages of up to 32 V. There are eight current ranges, programmable per channel, with full-scale outputs of up to 300 mA. Additionally, the channels can be paralleled to allow for ultrafine adjustments of large currents or for combined outputs of up to 600 mA.

A dedicated supply pin is provided for every output channel. Each channel can be operated from 2.85 V to 33 V, and internal switches allow any output to be pulled to the optional negative supply.

The AD5778R includes a precision integrated 1.25 V reference (10 ppm/°C maximum), with the option to use an external reference.

The SPI-/Microwire-compatible 3-wire serial interface operates on logic levels as low as 1.71 V at clock rates up to 50 MHz.

FUNCTIONAL BLOCK DIAGRAM

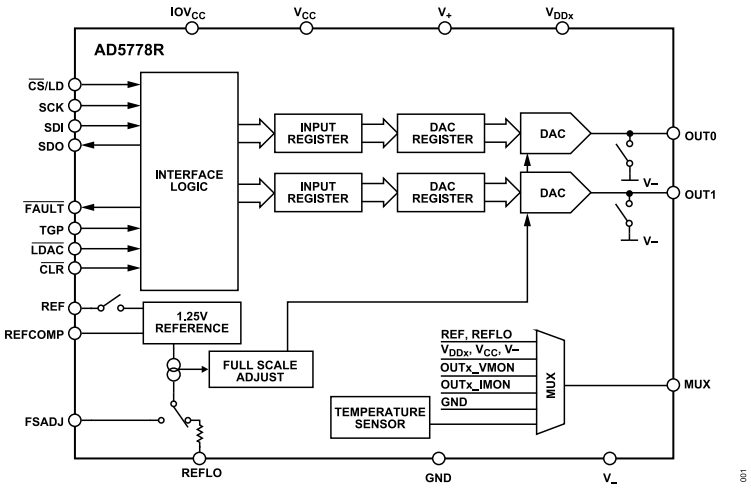


Figure 1. Functional Block Diagram

TABLE OF CONTENTS

REVISION HISTORY

4/2024—Revision 0: Initial Version

SPECIFICATIONS

All specifications applied over the full operating T_J range, unless otherwise noted. Typical values are at T_J = 25°C, V_{CC} = IOV_{CC} = 5 V, V_- = –5 V, V_{DDx} = 5 V, V_+ = 5 V, FSADJ = V_{CC}, and reference output voltage (V_{REF}) = 1.25 V external, unless otherwise specified.

Table 1. Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DC PERFORMANCE, AD5778R						
Resolution			16			Bits
Monotonicity		All current ranges[1]	16			Bits
Differential Nonlinearity	DNL	All current ranges[1]	−1	±0.2	+1	LSB
Integral Nonlinearity	INL	All current ranges[1]	−64	±12	+64	LSB
Current Offset Error	I_{OS}	All current ranges[1]	−0.4	±0.1	+0.4	%FSR
I_{OS} Temperature Coefficient		All current ranges[1]		±10		ppm/°C
Gain Error[2]	GE	300 mA and 200 mA output current ranges	−0.9	±0.3	+0.9	%FSR
		100 mA, 50 mA, and 25 mA output current ranges	−1.2	±0.4	+1.2	%FSR
		12.5 mA, 6.25 mA, and 3.125 mA output current ranges	−1.5	±0.7	+1.5	%FSR
Gain Temperature Coefficient		FSADJ = V_{CC}		30		ppm/°C
Total Unadjusted Error[2]	TUE	300 mA and 200 mA output current ranges	−1.4	±0.4	+1.4	%FSR
		100 mA, 50 mA, and 25 mA output current ranges	−1.7	±0.5	+1.7	%FSR
		12.5 mA, 6.25 mA, and 3.125 mA output current ranges	−2	±0.8	+2	%FSR
Power Supply Rejection Ratio	PSRR	Range = 100 mA, OUTx current (I_{OUTx}) = 50 mA				
		V_{CC} = 4.75 V to 5.25 V		±2.2		LSB
		V_{DDx} = 2.85 V to 3.15 V		±0.6		LSB
		V_{DDx} = 4.75 V to 5.25 V		±3.7		LSB
		V_+ = 4.75 V to 5.25 V		±0.09		LSB
		V_- = −5.25 V to −4.75 V		±0.01		LSB
DC Crosstalk[3]		Result of a 50 mW change in dissipated power		3		LSB
Dropout Voltage (V_{DDx} − V_{OUTx}[4])	$V_{DROPOUT}$	200 mA range, (V_{DDx} − V_-) = 4.75 V		0.72	1	V
		200 mA range, (V_{DDx} – V_-) = 2.85 V		0.85		V
		200 mA range, (V_{DDx} – V_-) = 33 V		0.76	1.1	V
		300 mA range, (V_{DDx} – V_-) = 4.75 V		1.13		V
		300 mA range, (V_{DDx} – V_-) = 2.85 V		1.35	1.95	V
High-Z Output Leakage Current[5]		IOUTx = high-Z, 2.85V ≤ (V_{DDX} – V_-) ≤ 33V	−1	+0.1	+1	µA
OUTx Switch to V_- Resistance to V_- Supply	$R_{PULLDOWN}$	Span code = 1000b, sinking 80 mA		8	12	Ω
OUTx Switch to V_- Current	$I_{PULLDOWN}$	Maximum allowable DC current			80	mA
AC PERFORMANCE		T_A = 25°C for all ac performance specifications				
Settling Time[6, 7]	t_{SETTLE}					
Full-Scale Step 3.125 mA Range		±0.0015% (±1 LSB at 16b)		19.2		µs
145 mA to 155 mA Step 200 mA Range		±0.0015% (±1 LSB at 16b)		7.7		µs
Full-Scale Step 200 mA Range		±0.0015% (±1 LSB at 16b)		8.7		ms
Glitch Impulse		At midscale transition, 200 mA range, and resistive load that connects the DAC output to GND (R_{LOAD}) = 4 Ω		180		pA × s
DAC to DAC Crosstalk[8]		100 mA to 200 mA step, R_{LOAD} = 15 Ω		121		pA × s
Noise Current	I_{NOISE}	Output current noise density internal reference, I_{OUTx} = 150 mA, R_{LOAD} = 4 Ω, load capacitance (C_{LOAD}) = 10 µF				
Frequency (f) = 1 kHz				12		nA/√Hz
f = 10 kHz				5		nA/√Hz
f = 100 kHz				0.5		nA/√Hz
f = 1 MHz				0.05		nA/√Hz
REFERENCE						
Internal Reference Mode						
Reference Output Voltage	V_{REF}		1.248	1.250	1.252	V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
V_{REF} Temperature Coefficient[9]			−10	±3	+10	ppm/°C
V_{REF} Line Regulation		V_{CC} = 5 V ± 10%		50		µV/V
V_{REF} Short-Circuit Current		V_{CC} = 5.5 V, forcing output to GND		2.5		mA
REFCOMP Pin Short-Circuit Current		V_{CC} = 5.5 V, forcing output to GND		65		µA
V_{REF} Load Regulation		V_{CC} = 5 V ± 10%, reference current (I_{REF}) = 100 µA sourcing		140		mV/mA
V_{REF} Output Voltage Noise Density		REFCOMP pin capacitance ($C_{REFCOMP}$) = REF pin capacitance (C_{REF}) = 0.1 µF, at f = 10 kHz		32		nV/√Hz
External Reference Mode						
Reference Input Voltage		REFCOMP pin is tied to GND	1.225		1.275	V
Input Current				0.001	1	µA
Input Capacitance[10]				40		pF
Full-Scale Adjust Resistor	R_{FSADJ}	R_{FSADJ} to GND	19	20	50	kΩ
DIGITAL INPUT AND OUTPUT						
Digital Output High Voltage	V_{OH}	SDO pin, load current = −100 µA	IOV_{CC} − 0.2			V
Digital Output Low Voltage	V_{OL}	SDO pin, load current = 100 µA			0.2	V
		$\overline{FAULT}$ pin, load current = 100 µA			0.2	V
Digital High-Z Output Leakage Current		SDO pin leakage current ($\overline{CS}$/LD high)	−1		+1	µA
		$\overline{FAULT}$ pin leakage current (not asserted)			1	µA
Digital Input Current		Input voltage (V_{IN}) = GND to IOV_{CC}	−1		+1	µA
Digital Input Capacitance[10]	C_{IN}				8	pF
High-Level Input Voltage	V_{IH}	2.85 ≤ IOV_{CC} ≤ V_{CC}	0.8 × IOV_{CC}			V
		1.71 ≤ IOV_{CC} ≤ 2.85	0.8 × IOV_{CC}			V
Low-Level Input Voltage	V_{IL}	2.85 ≤ IOV_{CC} ≤ V_{CC}			0.5	V
		1.71 ≤ IOV_{CC} ≤ 2.85			0.3	V
POWER SUPPLY						
Analog Supply Voltage	V_{CC}	V_{CC} must not exceed V_+	2.85		5.5	V
Digital Input and Output Supply Voltage	IOV_{CC}		1.71		V_{CC}	V
Negative Supply	V_-		−15.75		0	V
Positive Supply	V_+		2.85		V_- + 33	V
Output Supply Voltages	V_{DDx}		2.85		V_+	V
V_{CC} Supply Current		All ranges (code = 0, all channels)		2.6	3.8	mA
IOV_{CC} Supply Current		All ranges (code = 0, all channels)		0.01	1	µA
V_+ Supply Current		All ranges (code = 0, all channels)		385	500	µA
V_- Supply Current		All ranges (code = 0, all channels)		2.3	3.2	mA
V_{DDx} Supply Current		All ranges (code = 0, per channel)		0.7	1.2	mA
		25 mA range (code = full-scale, per channel)[11]		26.5	27.6	mA
		200 mA range (code = full-scale, per channel)		204	207	mA
V_{CC} Shutdown Current[12, 13]	I_{SLEEP}			1	10	µA
IOV_{CC} Shutdown Current				0.01	1	µA
V_+ Shutdown Current				20	36	µA
V_- Shutdown Current				30	59	µA
V_{DDx} Shutdown Current		Per channel		4.2	8.1	µA
MONITOR MULTIPLEXER						
MUX Pin DC Output Impedance				15		kΩ
MUX Pin Leakage Current		Monitor multiplexer disabled (high impedance)	−1	+0.1	+1	µA
MUX Pin Output Voltage Range		Monitor multiplexer selected to OUT0 pin voltage or OUT1 pin voltage	V_-		V_+	V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
MUX Pin Continuous Current[10]		T_A = 25°C (do not exceed)	−1		+1	mA

[1] The current offset error is measured at Code 384 for the AD5778R. Linearity is defined from Code 384 to Code 65535 for the AD5778R.

[2] For the full-scale current (I_{FS}) = 300 mA, R_{LOAD} = 10 Ω. For I_{FS} = 200 mA, R_{LOAD} = 15 Ω. For I_{FS} = 100 mA, R_{LOAD} = 30 Ω. For I_{FS} = 50 mA, R_{LOAD} = 50 Ω. For I_{FS} = 25 mA, R_{LOAD} = 100 Ω. For I_{FS} = 12.5 mA, R_{LOAD} = 200 Ω. For I_{FS} = 6.25 mA, R_{LOAD} = 400 Ω. For I_{FS} = 3.125 mA, R_{LOAD} = 800 Ω.

[3] I_{FS} = 200 mA and R_{LOAD} = 15 Ω. The DC crosstalk is measured with a 100 mA to 200 mA current step on an aggressor channel. The monitor channel is held at 3/4 × I_{FS} or 150 mA.

[4] V_{OUTx} is the channel output (OUTx) voltage.

[5] The loads attached to the OUTx pins must be terminated to GND.

[6] V_{DDx} = 5 V (3.125 mA range), V_{DDx} = 4 V (200 mA range), and V_- = −5 V for all ranges. For large current output steps, the internal thermal effects result in a final settling tail. In most cases, the tail is too small to affect settling to ±0.024%, but several milliseconds can be needed for full settling to the ±0.0015% level. For optimal results, solder or via all GND and REFLO pins, as well as the exposed pad, to a solid GND plane, and set VDDx as low as practicable for each channel to reduce power dissipation in the device.

[7] Internal reference mode. The load is 15 Ω (200 mA range) or 800 Ω (3.125 mA range) in parallel with 100 pF terminated to GND.

[8] DAC to DAC crosstalk is the glitch that appears at the output of one DAC because of a 100 mA to 200 mA step change in an adjacent DAC channel or vice versa. The measured DAC is at midscale (100 mA output current) in the 200 mA span range, with the internal reference, V_{DDx} = 5 V, V_- = −3.3 V.

[9] The temperature coefficient is calculated by first computing the ratio of the maximum change in the output voltage to the nominal output voltage and then dividing the ratio by the specified temperature range.

[10] Guaranteed by design and not production tested.

[11] Single channel at a specified output.

[12] V_{CC} = IOV_{CC} = 5 V, V_{DDx} = 5 V, and V_- = −5 V.

[13] Digital inputs are at 0 V or IOV_{CC}.

SPECIFICATIONS

TIMING CHARACTERISTICS

All specifications apply over the full operating T_J range, unless otherwise noted. Typical values are at T_J = 25°C, unless otherwise specified. Digital input low and high voltages are 0 V and IOV_{CC}, respectively.

Table 2. Timing Characteristics

			$V_+ = V_{DDx} = V_{CC}$ = 2.85 V to 5.5 V, IOV_{CC} = 2.85 V to V_{CC}			$V_+ = V_{DDx} = V_{CC}$ = 2.85 V to 5.5 V, 1.71 V ≤ IOV_{CC} < 2.85 V			
Symbol	**Parameter**	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
t_1	SDI Valid to SCK Setup		6			7			ns
t_2	SDI Valid to SCK Hold		6			7			ns
t_3	SCK HIGH Time		9			30			ns
t_4	SCK LOW Time		9			30			ns
t_5	$\overline{CS}$/LD Pulse Width		10			15			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		19			19			ns
t_7	$\overline{CS}$/LD Low to SCK High		7			7			ns
t_8	SDO Propagation Delay from SCK Falling Edge, C_{LOAD} = 10 pF	4.5 V ≤ IOV_{CC} ≤ V_{CC}			20				ns
		2.85 V ≤ IOV_{CC} < 4.5 V			30				ns
		1.71 V ≤ IOV_{CC} < 2.85 V						60	ns
t_9	$\overline{CLR}$ Pulse Width		20			30			ns
t_{10}	$\overline{CS}$/LD High to SCK Positive Edge		7			7			ns
t_{12}	$\overline{LDAC}$ Pulse Width		15			15			ns
t_{13}	$\overline{CS}$/LD High to $\overline{LDAC}$ High or Low Transition		15			15			ns
	SCK Frequency	50% Duty Cycle			50			15	MHz
t_{14}	TGP High Time[1]		1			1			µs
t_{15}	TGP Low Time[1]		1			1			µs

[1] Guaranteed by design and not production tested.

Timing Diagrams

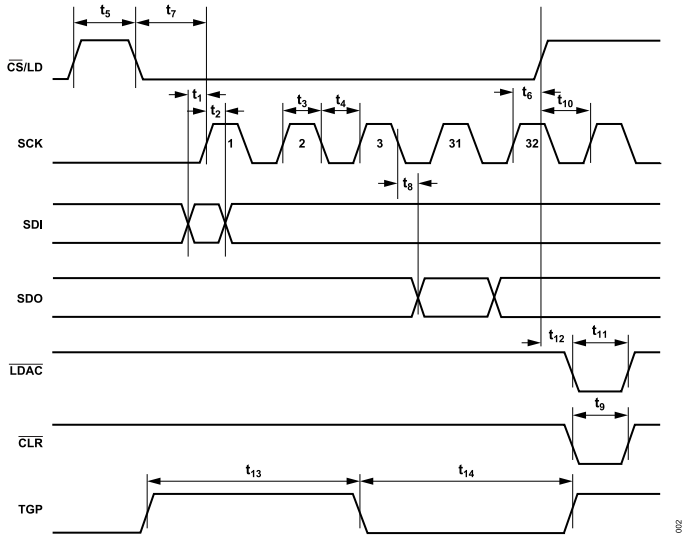


Figure 2. Serial Interface Timing

SPECIFICATIONS

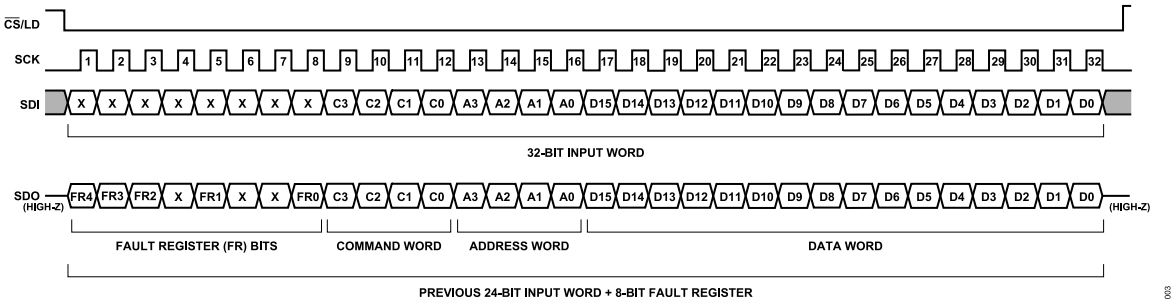


Figure 3. AD5778R 32-Bit Load Sequence

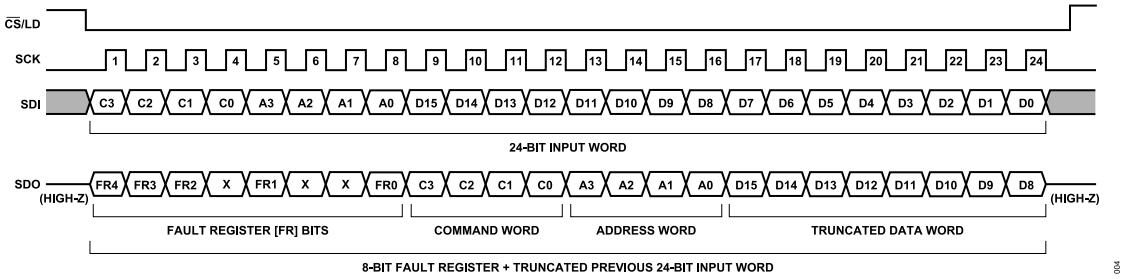


Figure 4. AD5778R 24-Bit Load Sequence

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

Parameter	Rating
V_{CC} to GND	–0.3 V to +6 V
IOV_{CC} to GND	–0.3 V to +6 V
V_- to GND	–16.5 V to +0.3 V
V_+ to GND	–0.3 V to (V_- + 36 V)
V_{DDx} to GND	–0.3 V to (V_+ + 0.3 V)
Output Supply Voltages to GND	
OUT0, OUT1	(V_- – 0.3 V) to (V_{DDx} + 0.3 V)
MUX	(V_- – 0.3 V) to (V_+ + 0.3 V)
REF, REFCOMP, and FSADJ to GND	–0.3 V to minimum (V_{CC} + 0.3 V, 6 V)
$\overline{CS}$/LD, SCK, SDI, $\overline{LDAC}$, $\overline{CLR}$, and TGP to GND	–0.3 V to +6 V
$\overline{FAULT}$ to GND	–0.3 V to +6 V
SDO to GND	–0.3 V to minimum (IOV_{CC} + 0.3 V, 6 V)
Temperature	
Operating T_J Range	–40°C to +125°C
Maximum T_J	150°C
Storage Range	–65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Thermal characteristics are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. Thermal resistance values specified in Table 4 are simulated based on JEDEC specifications using a 2S2P thermal test board (see JEDEC JESD51), except for θ_{JC-TOP}, which uses a JEDEC 1S test board.

θ_{JA} is the junction to ambient thermal resistance, measured in a JEDEC natural convection environment.

θ_{JC-TOP} is the junction to case thermal resistance, measured at the center of the package top surface, with an infinite heat sink attached to the package surface.

θ_{JB} is the junction to board thermal resistance, measured at a point on the board 1 mm from the package edge, along the package center line, measured in a JEDEC θ_{JB} environment.

Ψ_{JB} is the junction to board thermal characterization parameter, measured in a JEDEC natural convection environment.

Ψ_{JT} is the junction to package top thermal characterization parameter, measured in a JEDEC natural convection environment.

Do not use θ_{JA}, θ_{JC-TOP}, and θ_{JB} thermal resistances to perform direct calculation or measurement of the die temperature because doing so results in incorrect values. The thermal resistances assume 100% of the power that is dissipated along the specified path between the measurement points. The thermal resistances are directly dependent on the PCB design and environment.

If direct measurement of the package is required, the Ψ_{JT} and Ψ_{JB} values must be used because those values more accurately reflect the true thermal dissipation paths.

θ_{JC-TOP} must only be used where an external heat sink is attached directly to the package.

System level thermal simulation is highly recommended.

For more details about the thermal resistances, refer to *JEDEC51-12: Guidelines for Reporting and Using Electronic Package Thermal Information*.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC-TOP}	Ψ_{JT}	Ψ_{JB}	Unit
05-08-1693[1]	28.34	9.27	17.33	0.11	9.20	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no bias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD5778R

Table 5. AD5778R, 32-Lead QFN

ESD Model	Withstand Voltage (V)	Class
HBM	3000	2
FICDM	1500	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

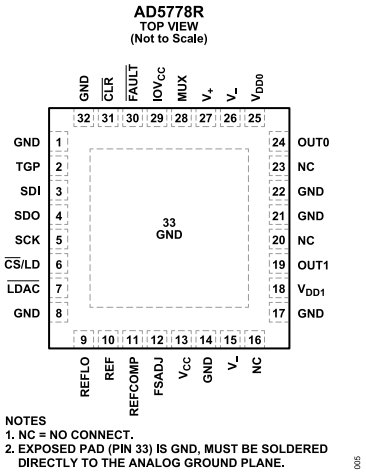


Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 14, 17, 21, 22, 32	GND	Ground. The ground pins and the exposed pad must be tied directly to a solid ground plane.
2	TGP	Asynchronous Toggle Pin. A falling edge updates the DAC register with data from Input Register A. A rising edge updates the DAC register with data from Input Register B. Toggle operations only affect those DAC channels with their toggle select bit (Tx) set to 1. Tie the TGP pin to IOV_{CC} when toggle operations are done through software. Tie the TGP pin to GND if the toggle operations are unused. The logic levels are determined by IOV_{CC}.
3	SDI	Serial Data Input. Data on the SDI is clocked into the DAC on the rising edge of the SCK. The AD5778R accepts input word lengths of 24, 32, or multiples of 32 bits. Logic levels are determined by IOV_{CC}.
4	SDO	Serial Data Output. The serial output of the 32-bit shift register appears at the SDO pin. The data transferred to the device via the SDI pin is delayed 32 SCK rising edges before being output at the next falling edge. The SDO pin can be used for data echo readback or daisy-chain operation and becomes high impedance when $\overline{CS}$/LD is high. Logic levels are determined by IOV_{CC}.
5	SCK	Serial Clock Input. Logic levels are determined by IOV_{CC}.
6	$\overline{CS}$/LD	Serial Interface Chip Select/Load Input. When the $\overline{CS}$/LD is low, SCK is enabled for shifting SDI data into the register. In addition, the SDO is enabled when the $\overline{CS}$/LD is low. When the $\overline{CS}$/LD is taken high, the SDO and SCK are disabled, and the specified command (see Table 7) is executed. Logic levels are determined by IOV_{CC}.
7	$\overline{LDAC}$	Active Low Asynchronous DAC Update Pin. The $\overline{LDAC}$ pin allows updates independent of SPI timing. If the $\overline{CS}$/LD is high, a falling edge on the $\overline{LDAC}$ updates all DAC registers with the contents of the input registers. The $\overline{LDAC}$ is gated by the $\overline{CS}$/LD and has no effect if $\overline{CS}$/LD is low. Logic levels are determined by IOV_{CC}. If not used, tie the $\overline{LDAC}$ to IOV_{CC}.
9	REFLO	Reference Low. Signal ground for the reference. Tie the REFLO pin directly to GND.
10	REF	Reference Input and Output. The voltage at the REF pin proportionally scales the full-scale output current of each DAC output channel. By default, the internal 1.25 V reference is routed to the REF pin. The REF pin must be buffered when driving external DC load currents. If the reference is disabled (see the Reference Modes section in the Theory of Operation section), the output is disconnected, and the REF pin becomes a high-impedance input that accepts a precision external reference. For low noise and reference stability, tie a capacitor from the REF pin to GND. The value must be less than the capacitance tied to the REFCOMP pin ($C_{REFCOMP}$). The allowable external reference input range is 1.225 V to 1.275 V.
11	REFCOMP	Internal Reference Compensation Pin. For low noise and reference stability, tie a 0.1 µF capacitor from the REFCOMP pin to GND. Tying the REFCOMP pin to GND causes the device to power up with the internal reference disabled, which allows the use of an external reference at startup.
12	FSADJ	Full-Scale Current Adjust Pin. The FSADJ pin is used either to produce nominal, internally-calibrated output ranges or to produce incrementally-tunable ranges. In either case, the V_{REF} is forced across a resistor (R_{FSADJ}) to define a reference current that scales the outputs for all ranges and channels. Full-scale currents are proportional to the voltage at the REF pin and inversely proportional to R_{FSADJ}. If FSADJ is tied to V_{CC}, an internal R_{FSADJ} (20 kΩ) is selected, resulting in nominal output ranges. An external resistor of 19 kΩ to 41 kΩ can be used instead by simply connecting the resistor between the FSADJ pin and GND. In this case, the external resistor controls the scaling

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
		of ranges, and the internal resistor is automatically disconnected. See Table 9 for details. When using an external resistor, FSADJ is sensitive to stray capacitance, and the pin should be compensated with a snubber network consisting of a series combination of 1 kΩ and 1 µF, connected in parallel to R_{FSADJ}. With the recommended compensation, the FSADJ pin is stable, driving stray capacitance of up to 50 pF.
13	V_{CC}	Analog Supply Voltage. 2.85 V ≤ V_{CC} ≤ 5.5 V. Bypass to GND with a 1 µF capacitor.
15, 26	V_-	Negative Supply Voltage. –15.75 V ≤ V_- ≤ GND. Bypass to GND with a 1 µF capacitor unless V_- is connected to GND.
16, 20, 23	NC	No Connect.
18, 25	V_{DD1} to V_{DD0}	Output Supply Voltages. 2.85 V ≤ $V_{DD0/1}$ ≤ V_+. These two positive supply inputs provide independent supplies for each of the two DAC current output pins, OUT0 and OUT1, respectively. Bypass each supply input to GND separately with a 1 µF capacitor.
19, 24	OUT1 to OUT0	DAC Analog Current Outputs. Each current output pin has a dedicated analog supply pin, V_{DD0} and V_{DD1}. The operational voltage level range at these pins is V_- ≤ V_{OUTx} ≤ V_{DDx}.
27	V_+	Positive Supply Voltage. 2.85 V ≤ V_+ ≤ V_- + 33 V. The V_+ must always be greater than or equal to the largest of the two DAC positive supply voltages (V_{DD0} and V_{DD1}) and V_{CC}. The supply voltage difference (V_+ – V_-) cannot exceed 33 V maximum. Bypass to GND with a 1 µF capacitor.
28	MUX	Analog Multiplexer Output. Pin voltages and currents can be monitored by measuring the voltage at the MUX pin. When the multiplexer (mux) is disabled, the MUX pin becomes high impedance. The available mux selections are given in Table 10.
29	IOV_{CC}	Digital Input and Output Supply Voltage. 1.71 V ≤ IOV_{CC} ≤ V_{CC} + 0.3 V. Bypass to GND with a 0.1 µF capacitor.
30	$\overline{FAULT}$	Active-Low Fault Detection Pin. This open-drain N-channel output pulls low when any valid fault condition is detected. The $\overline{CLR}$ pin is released on the next $\overline{CS}$/LD rising edge. A pull-up resistor is required.
31	$\overline{CLR}$	Active-Low Asynchronous Clear Input. A logic low at this level-triggered input clears the device to the default reset code and output ranges, which are zero-scale and high-impedance (high-Z) outputs. The control registers are cleared to zero. Logic levels are determined by IOV_{CC}.
33	EXPOSED PAD	Ground. Solder this pad directly to the analog ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = IOV_{CC} = 5 V, V_- = –5 V, V_{DDx} = 5 V, V_+ = 5 V, FSADJ = V_{CC}, and V_{REF} = 1.25 V external unless otherwise specified.

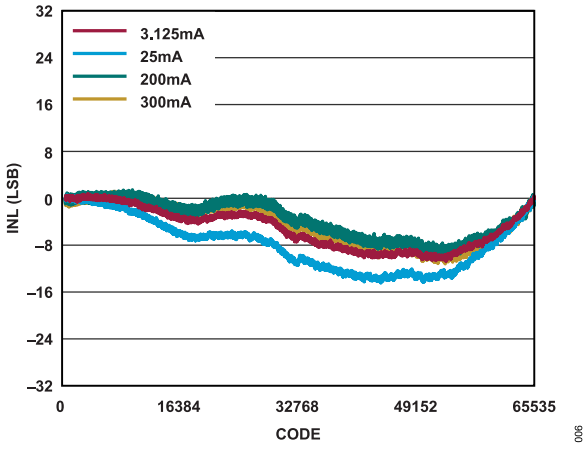


Figure 6. AD5778R Integral Nonlinearity (INL)

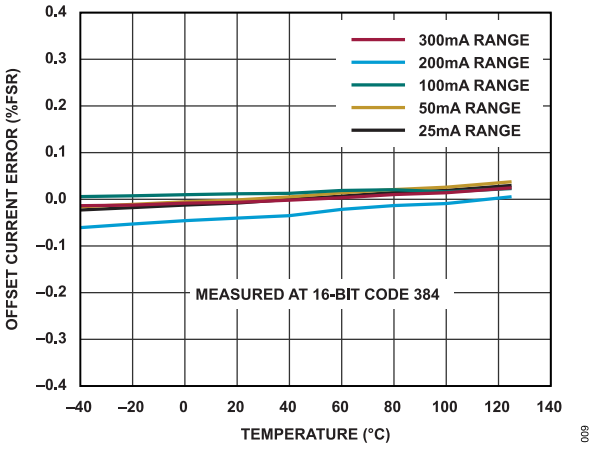


Figure 9. Offset Current Error vs. Temperature

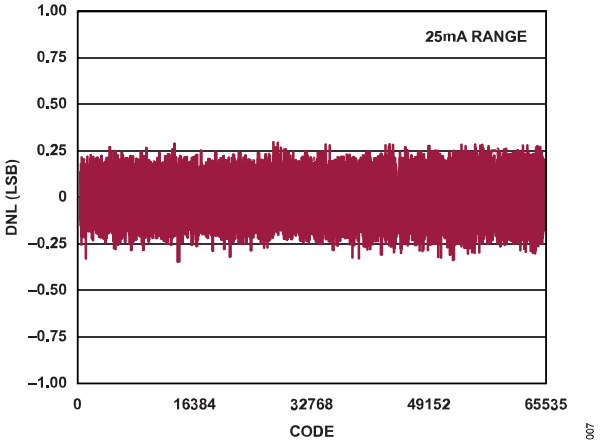


Figure 7. AD5778R Differential Nonlinearity (DNL)

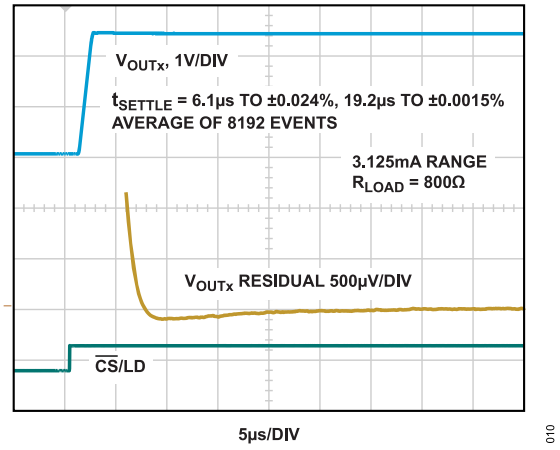


Figure 10. Settling 0 mA to 3.125 mA Step

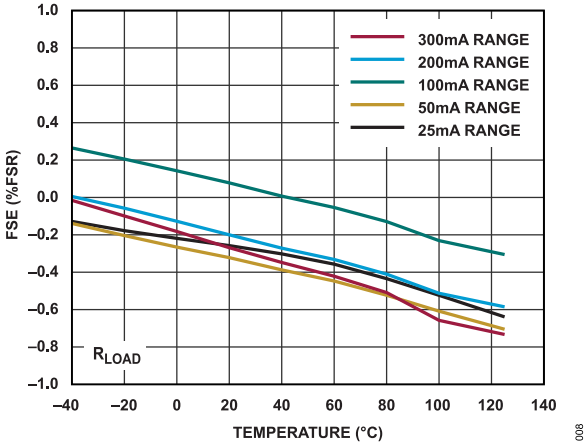


Figure 8. Full-Scale Current Error (FSE) vs. Temperature

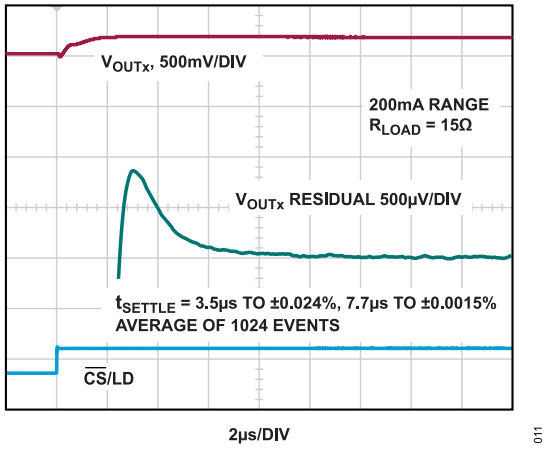


Figure 11. Settling 145 mA to 155 mA Step

TYPICAL PERFORMANCE CHARACTERISTICS

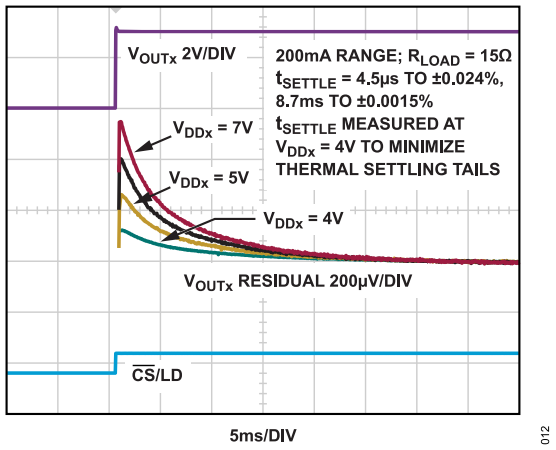


Figure 12. Settling 0 mA to 200 mA Step

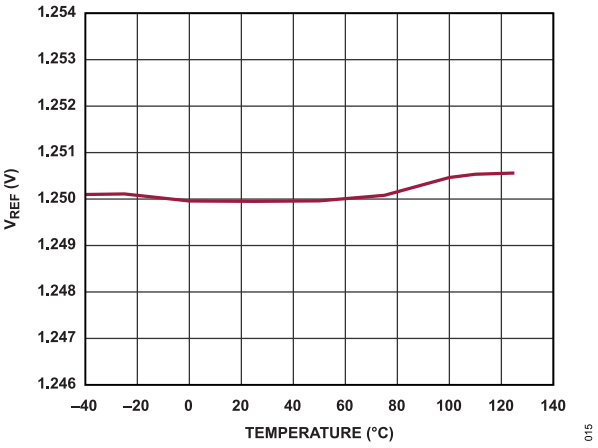


Figure 15. V_{REF} vs. Temperature

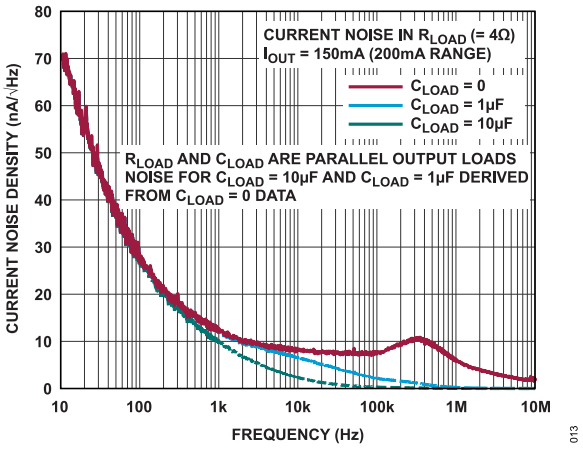


Figure 13. Current Noise Density vs. Frequency

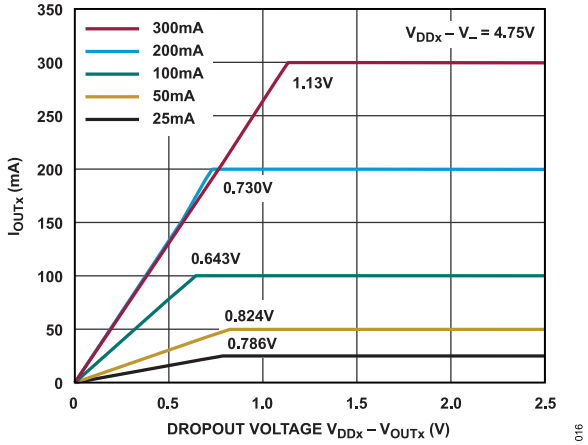


Figure 16. I_{OUTx} vs. $V_{DROPOUT}$

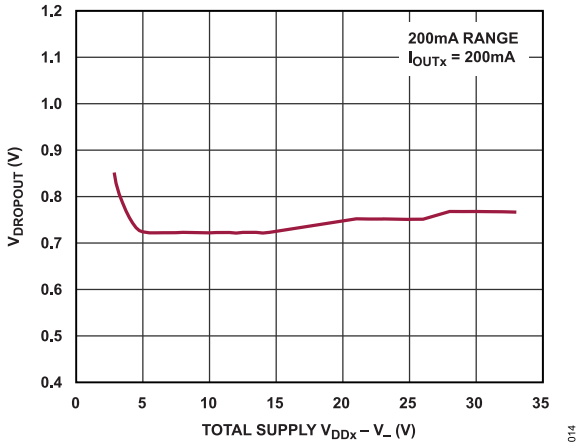


Figure 14. $V_{DROPOUT}$ vs. Total Supply Voltage

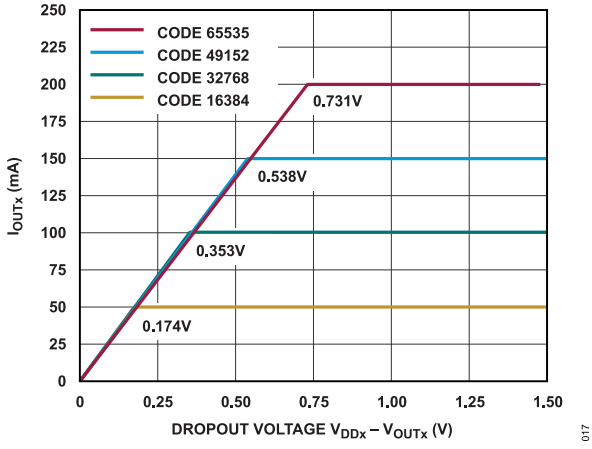


Figure 17. I_{OUTx} vs. $V_{DROPOUT}$, 200 mA Range

TYPICAL PERFORMANCE CHARACTERISTICS

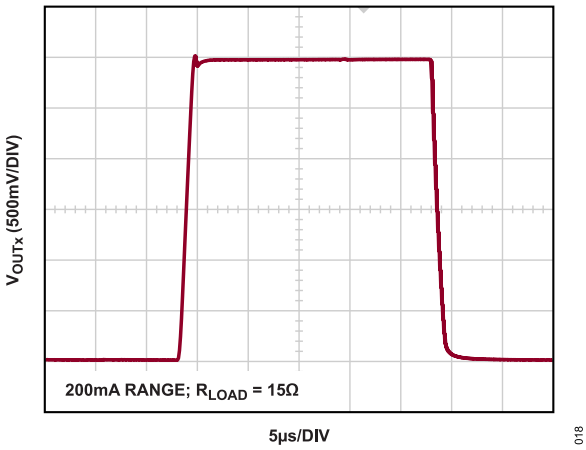


Figure 18. Large Signal Response

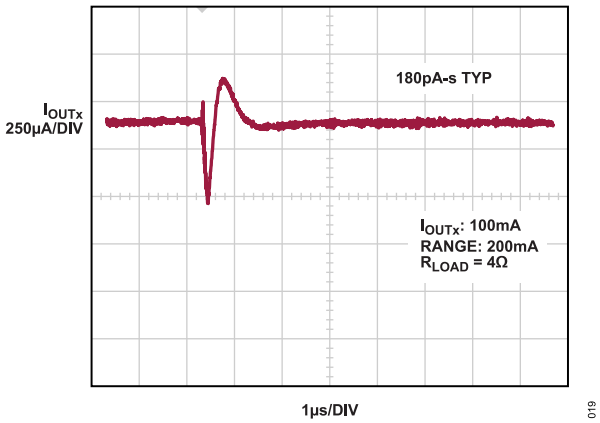


Figure 19. Midscale Glitch

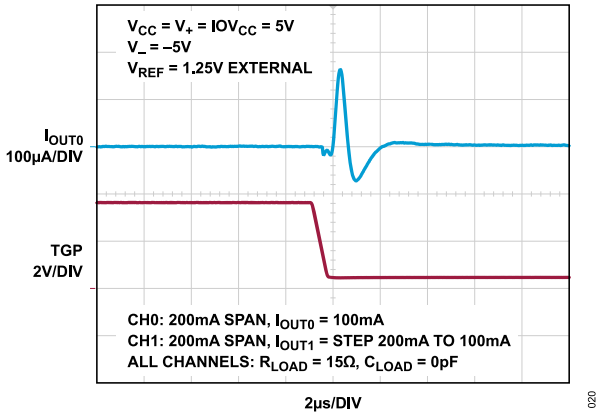


Figure 20. DAC-to-DAC Crosstalk (Falling)

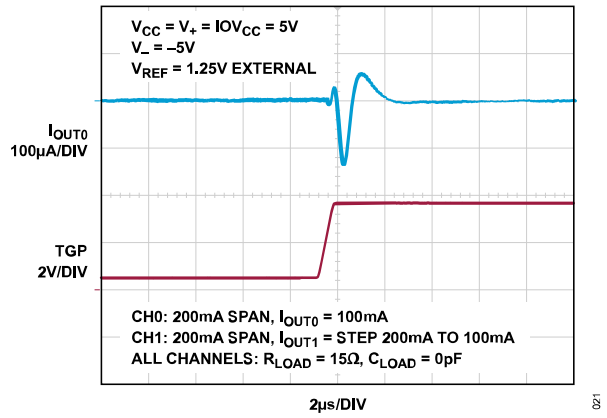


Figure 21. DAC-to-DAC Crosstalk (Rising)

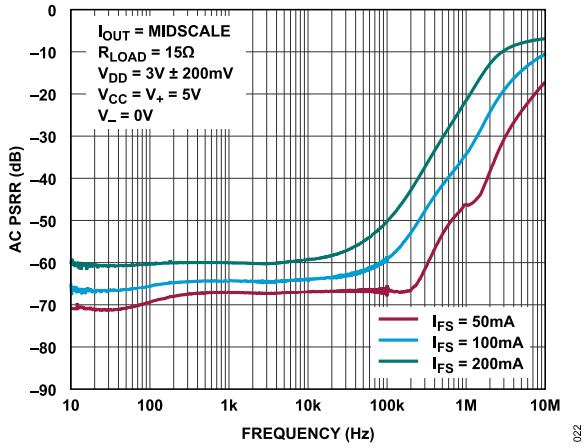


Figure 22. AC PSRR vs. Frequency

THEORY OF OPERATION

The AD5778R is a 2-channel, current source output DAC with selectable output ranges, precision reference, and a high-voltage mux for surveying the channel output voltages and currents. Each output draws current from a separate dedicated positive supply pin that accepts voltages of 2.85 V to 33 V, allowing the optimization of power dissipation and headroom for a wide range of loads. Internal 12 Ω switches allow any output pin to be connected to an optional negative V^- supply voltage and sink up to 80 mA.

POWER-ON RESET

The outputs reset to a high-impedance state on power up, making the system initialization consistent and repeatable. After power-on initialization, select the output range via SPI bus using Table 7, Table 8, and Table 9.

POWER SUPPLY SEQUENCING AND STARTUP

The supplies (V_{CC}, IOV_{CC}, V_+, V_-, V_{DD0}, and V_{DD1}) may be powered up in any convenient order. If an external reference is used, do not allow the input voltage at the REF pin to rise above V_{CC} + 0.3 V during supply turn-on and turn-off sequences (see the Absolute Maximum Ratings section).

After startup, the IOV_{CC} must be within the V_{CC}, and supplies must not exceed the V_+. DC reference voltages of 1.225 V to 1.275 V are acceptable.

Supply bypassing is critical to achieving the best possible performance. Use at least 1 µF of low-effective series resistance (ESR) capacitance to ground on all supply pins, and position the capacitor as close to the device as possible. A 0.1 µF capacitor may be used for the IOV_{CC}.

DATA TRANSFER FUNCTIONS

The DAC input-to-output transfer functions for all resolutions and output ranges greater than or equal to 25 mA are shown in Figure 23. The input code is in straight binary format for all ranges.

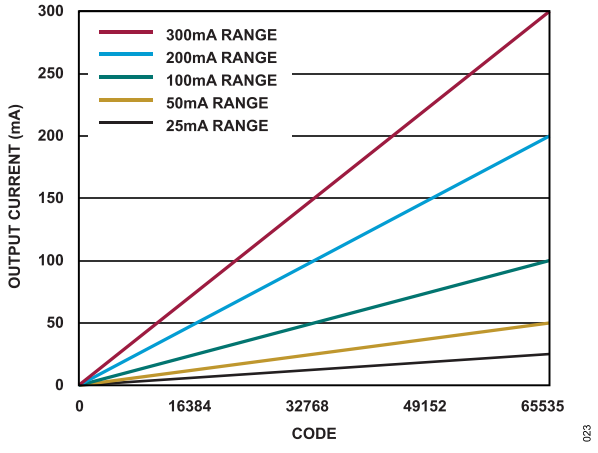


Figure 23. AD5778R Transfer Function

SERIAL INTERFACE

When the $\overline{CS}$/LD pin is taken low, the data on the SDI pin is loaded into the shift register on the rising edge of the clock (the SCK pin). The 4-bit command [C3:C0] is loaded first, followed by the 4-bit DAC address [A3:A0], and finally, the 16-bit data word in straight binary format. For the AD5778R, the data word comprises the 16-bit input code, ordered MSB-to-LSB. Data can only be transferred to the AD5778R when the $\overline{CS}$/LD signal is low. The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to carry out the action specified in the 24-bit input word.

Table 7. Command Codes

Command				
C3	C2	C1	C0	
0	0	0	0	Write code to n
1	0	0	0	Write code to all
0	1	1	0	Write span to n
0	0	0	1	Update n (power up)
1	0	0	1	Update all (power up)
0	0	1	1	Write code to n, update n (power up)
0	0	1	0	Write code to n, update all (power up)
1	0	1	0	Write code to all, update all (power up)
0	1	0	0	Power down n
0	1	0	1	Power down chip
1	0	1	1	Monitor mux
1	1	0	0	Toggle select
1	1	0	1	Global toggle
0	1	1	1	CONFIG command
1	1	1	1	No operation
Others				Invalid command codes

Table 8. DAC Addresses, n

Address[1]				
A3	A2	A1	A0	
0	0	0	0	DAC 0
0	0	1	1	DAC 1
Others				Invalid DAC addresses

[1] Any DAC address code used other than the codes given in Table 8 causes the command to be ignored.

While the minimum input word is 24 bits, it may optionally be extended to 32 bits. To use the 32-bit word width, 8 don't care bits must be transferred to the device first, followed by the 24-bit word, as described earlier in this section. The 32-bit word is required for daisy-chain operation. It also provides accommodation for processors that have a minimum word width of 16 or more bits. The complete 24-bit and 32-bit sequences are shown in Figure 3 and Figure 4. Note that the fault register outputs appear on the SDO pin for either word width.

THEORY OF OPERATION

Note that any write to invalid command codes or invalid DAC addresses can result in unexpected device behavior or fault conditions. It is recommended to avoid writing to invalid command codes and invalid DAC addresses. Reset the device in case of any write to invalid command codes or invalid DAC addresses.

INPUT AND DAC REGISTERS

The AD5778R has five internal registers for each DAC, in addition to the main shift register. Each DAC channel has two sets of double-buffered registers: one set for the code data and one set for the span (output range) of the DAC. Double buffering provides the capability to simultaneously update the span and code, which allows smooth current transitions when changing output ranges. It also permits the simultaneous updating of multiple DACs.

Each set of double-buffered registers comprises an input register and a DAC register as follows:

- Input register: The write operation shifts data from the SDI pin into a chosen register. The input registers are holding buffers, and write operations do not affect the DAC outputs.
  In the code data path, there are two input registers, A and B, for each DAC register. Register B is an alternate register used only in the toggle operation, while Register A is the default input register.
- DAC register: The update operation copies the contents of an input register to the associated DAC register. The content of a DAC register directly controls the DAC output current or range. The update operation also powers up the selected DAC if it had been in power-down mode.

Note that updates always refresh both code and span data, but the values held in the DAC registers remain unchanged unless the associated input register values have been changed via a write operation. For example, if a new code is written and the channel updated, the code is updated while the span is refreshed unchanged. A channel update can come from a serial update command, an $\overline{\text{LDAC}}$ negative pulse, or a toggle operation.

OUTPUT RANGES AND SOFTSPAN OPERATION

The AD5778R is a 2-channel current DAC with selectable output ranges. The full set of current output ranges is available only through SPI programming.

Figure 25 shows a simplified diagram of a single channel of the AD5778R. The full-scale current range of the AD5778R is selected via four control bits [S3:S0] on a per channel basis. Also included is the ability to provide an external reference or to use a precision external resistor at Pin FSADJ to reduce the overall gain drift over temperature of the AD5778R.

The AD5778R initializes at power on with all channel outputs (OUT0 and OUT1) at high-Z. The range and code of each channel are then fully programmable through SoftSpan as given in Table 9.

Each channel has a set of double-buffered registers for range information. Program the span input register using the **write span to n** command or **write span to all** command (0110b and 1110b, respectively). Figure 24 shows the syntax, and Table 9 shows the span codes and ranges.

As with the double-buffered code registers, update operations copy the span input registers to the associated span DAC registers.

Table 9. Span Codes

				Output Range	
S3	**S2**	**S1**	**S0**	**External R_{FSADJ}**	**FSADJ = V_{CC}**
0	0	0	0	(High-Z)	
0	0	0	1	$50 \times V_{REF}/R_{FSADJ}$	3.125 mA
0	0	1	0	$100 \times V_{REF}/R_{FSADJ}$	6.25 mA
0	0	1	1	$200 \times V_{REF}/R_{FSADJ}$	12.5 mA
0	1	0	0	$400 \times V_{REF}/R_{FSADJ}$	25 mA
0	1	0	1	$800 \times V_{REF}/R_{FSADJ}$	50 mA
0	1	1	0	$1600 \times V_{REF}/R_{FSADJ}$	100 mA
0	1	1	1	$3200 \times V_{REF}/R_{FSADJ}$	200 mA
1	1	1	1	$4800 \times V_{REF}/R_{FSADJ}$	300 mA
1	0	0	0	(Switch to V_)	

As shown in Table 9, there are two additional selections (Code 0000 and Code 1000) which place the output(s) in a high-Z mode or in a mode where a low on resistance (≤12 Ω) negative channel metal-oxide semiconductor (NMOS) device shunts the DAC output to the negative supply V_. When the NMOS device is enabled, the OUTx pin driver is disabled for that channel(s). Span codes not listed in Table 9 default to the high-Z output range.

THEORY OF OPERATION

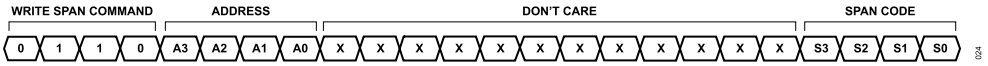


Figure 24. Write Span Syntax

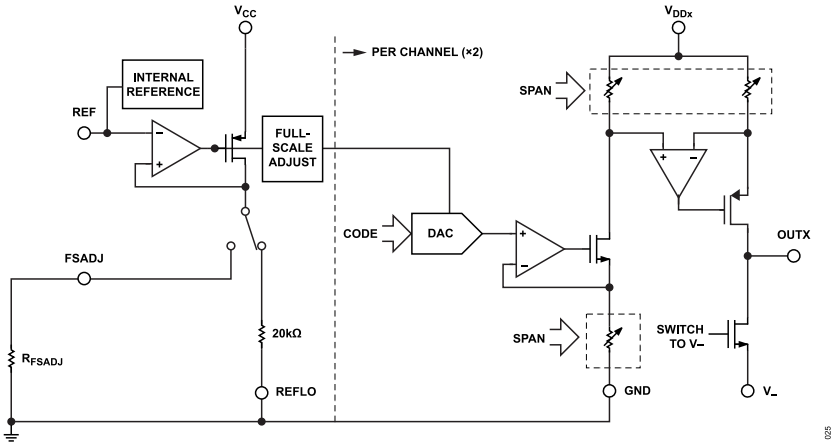


Figure 25. AD5778R Single Channel Simplified Diagram

THEORY OF OPERATION

MONITOR MUX

The AD5778R includes a high-voltage mux for monitoring both the voltages and currents at the two current output pins (OUT0 and OUT1). Additionally, the V_{DD0} and V_{DD1}, the V_+ and V_-, the V_{CC}, the V_{REF}, and the die temperature can all be monitored.

The MUX pin is intended for use with high-impedance inputs only. The impedance at the pin is typically 15 kΩ. A continuous DC output current at the MUX pin must be limited to ±1 mA to avoid damaging the internal circuitry.

The operating range of the mux extends rail-to-rail from V_- to V_+, and the output is disabled (high impedance) at power up.

The syntax and codes for the **monitor mux** command are shown in Figure 26 and Table 10.

Table 10. Monitor Mux Control Codes

M4	M3	M2	M1	M0	MUX Pin Output	Notes
0	0	0	0	0	Disabled (high-Z)	
0	0	0	0	1	OUT0 current measurement	$I_{OUT0} = I_{FS} \times V_{MUX}/V_{REF}$
0	0	1	0	0	OUT1 current measurement	$I_{OUT1} = I_{FS} \times V_{MUX}/V_{REF}$
0	0	1	1	0	V_{CC}	
0	1	0	0	0	V_{REF}	
0	1	0	0	1	V_{REFLO}	DAC Reference GND
0	1	0	1	0	Die temperature (T_J)	$T_J = 25°C + (1.4\ V - V_{MUX})/(0.0037\ V/°C)$
1	0	0	0	0	V_{DD0}	
1	0	0	1	1	V_{DD1}	
1	0	1	0	1	V_+	
1	0	1	1	0	V_-	
1	0	1	1	1	GND	
1	1	0	0	0	OUT0 pin voltage	
1	1	0	1	1	OUT1 pin voltage	
Others					Invalid channels	Invalid codes

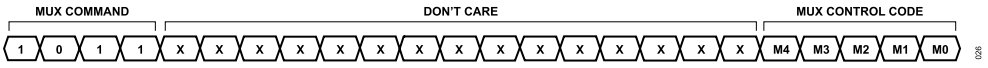


Figure 26. Monitor Mux Command

THEORY OF OPERATION

Current Measurement Using the Mux

Measure the current of any output pin by using the **monitor mux** command (1011b) along with one of the mux current measurement codes from Table 10. The mux responds by outputting a voltage proportional to the actual output current. The proportionality factor is given by the following equation:
$I_{OUTX} = I_{FS} \times V_{MUX}/V_{REF}$.

The MUX pin voltage (V_{MUX}) has the same excellent linearity as the current outputs, but calibrating for slope error (±15% FSR) is necessary for accurate results. The ±1% FSR accuracy is easily achievable with a one- or two-point calibration.

Note that for a given V_{REF} and DAC code, the V_{MUX} is constant and does not vary by range, but the I_{FS} has a different value for each output range. If the range of the channel is set to high-Z or short to V_, or if it is in dropout (flagged by the fault register, Bits[FR0:FR1]), the voltage is not representative of the pin current.

Die Temperature Measurement Using the Mux

Measure the die temperature by using the **monitor mux** command along with the Mux Control Code, 01010b. The V_{MUX} in this case is linearly related to the die temperature by a temperature coefficient of –3.7 mV/°C. The measured T_J is as follows:
$T_J = 25°C + (1.4\ V - V_{MUX})/(3.7\ mV/°C)$.

If needed, the temperature monitor can be calibrated by measuring the initial temperature and voltage and then substituting these values for 25°C and 1.4 V, respectively, in the equation.

Monitor Mux Precharge Considerations

The analog mux in the AD5778R is unbuffered. This unbuffered condition obviates error terms from amplifier offsets. However, without buffers, a charge transfer when the MUX pin is connected may disturb the high-impedance current output. The AD5778R contains circuitry that suppresses charging glitches on the output pins (OUT0 and OUT1) by precharging the MUX pin before connecting it to the output.

Due to the precharge behavior, the mux output becomes valid approximately 7 µs after the **monitor mux** command is given ($\overline{CS}$/LD rising). Residual charging transients can be further reduced by adding capacitance to the output pins if needed. Do not add capacitance to the MUX pin, because this potentially increases the disturbance to the outputs during mux switching. Up to 100 pF on the MUX pin is allowable.

TOGGLE OPERATIONS

Some systems require that the DAC outputs switch repetitively between two output levels (that is switching between an on state and an off state). The AD5778R toggle function facilitates these kinds of operations by providing two input registers (A and B) per DAC channel.

Toggling between A and B is controlled by three signals. The first of these is the **toggle select** command, which acts on the data field of 5 bits with each bit controlling a single channel (see Figure 27). The second is the **global toggle** command, which controls all selected channels using the global toggle bit (TGB) (see Figure 28). Finally, the TGP pin allows the use of an external clock or logic signal to toggle the DAC outputs between A and B. The signals from these controls are combined as shown in Figure 29.

If the toggle function is not needed, tie the TGP pin to ground and leave the toggle select register in its power-on reset state (cleared to zero). Input Registers A then function as the sole input registers, and Registers B are not used.

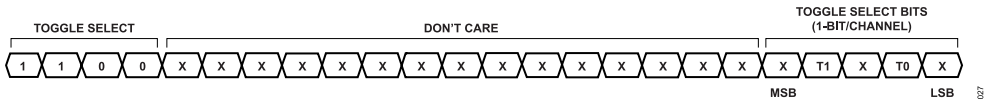


Figure 27. Toggle Select Syntax

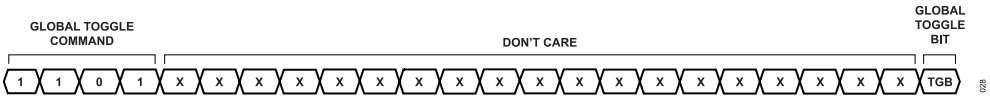


Figure 28. Global Toggle Syntax

THEORY OF OPERATION

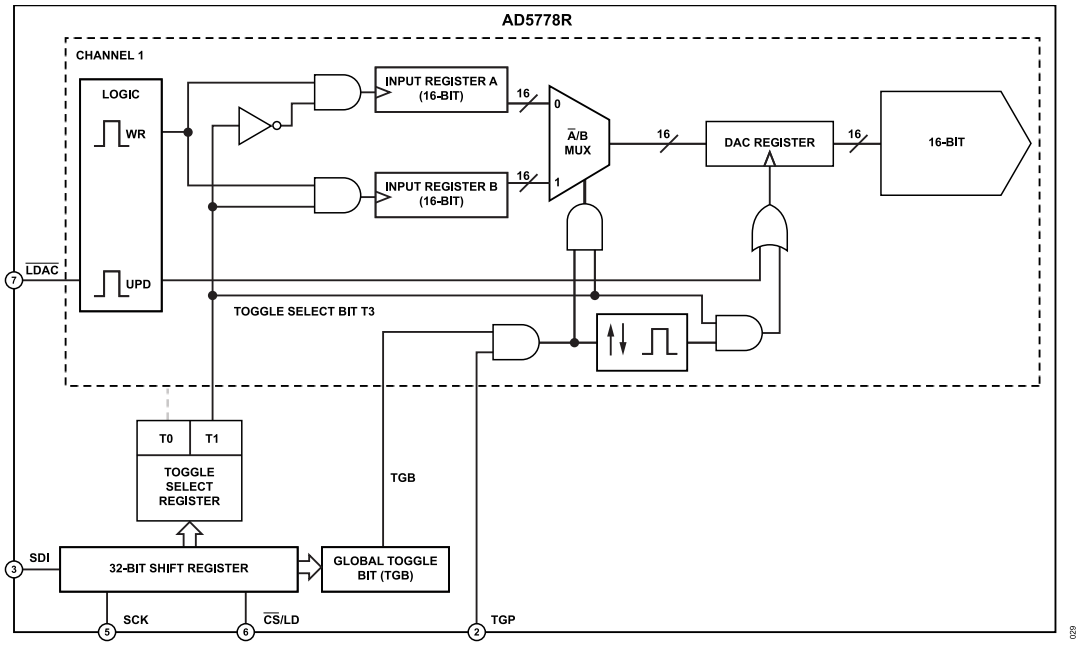


Figure 29. Conceptual Block Diagram—Toggle Functionality

Toggle Select Register (TSR)

The **toggle select** command (1100b) syntax is shown in Figure 27. Each bit in the 5-bit TSR data field controls the DAC channel of the same name as follows: T0 controls Channel 0 and T1 controls Channel 1.

The toggle select bits [T0:T1] have a dual function. First, each toggle select bit controls which input register (A or B) receives data from a write-code operation. When the toggle select bit of a given channel is high, write-code operations are directed to Input Register B of the addressed channel. When the bit is low, write-code operations are directed to Input Register A. Second, each toggle select bit enables the corresponding channel for a toggle operation.

Writing to Input Registers A and Input Registers B

Having selected the channels to toggle, write the desired codes to Input Registers A for the selected channels. Then, set the toggle select bits of the channels by using the **toggle select** command. Finally, write the desired codes to Input Registers B. Once these steps are completed, the channels are ready to toggle. For example, to set up Channel 1 to toggle between Code 4096 and Code 4200 complete the following steps:

1. Write code Channel 1 (Code = 4096) to Register A
   - 00000011 00010000 00000000
2. Toggle select (set Bit T1)
   - 11000000 00000000 00001000
3. Write code Channel 1 (Code = 4200) to Register B
   - 00010000 01101000

The write code of Step 3 is directed to Register B, because in Step 2, Bit T1 was set to 1. Channel 1 now has Input Registers A and Input Registers B holding the two desired codes and is prepared for the toggle operation.

Note: After writing to Register B, the code for Register A can still be changed. The state of the toggle select bit determines to which register (A or B) a write is directed.

- First, Toggle Select Bit T1 has to be reset to 0 with the following instruction:
  - 11000000 00000000 00000000
- Then write the new Register A code. If the new code is 4300, the instruction is as follows:
  - 00000011 00010000 11001100

After, set the Toggle Select Bit T1 to 1 again (Step 2). It is not necessary to write to Register B again, and Channel 1 is ready for the toggle operation.

Toggling Between Register A and Register B

Once Input Registers A and Input Registers B have been written to for all desired channels with the corresponding toggle select bits set high, as in the previous example, the channels are ready for toggling.

The AD5778R supports three types of toggle operations. In the first toggle operation, all selected channels are toggled together using the SPI port. All selected channels are toggled together using an external clock or logic signal in the second toggle operation. In the third toggle operation, any combination of channels can be

THEORY OF OPERATION

instructed to update from either Input Register A or Input Register B.

The internal toggle update circuit is edge triggered, so only transitions (of TGB or TGP) trigger an update from the respective input register.

To toggle all selected channels together using the SPI port, ensure the TGP pin and the bits in the toggle select register corresponding to the desired channels are high. Use the **global toggle** command (1101b) to alternate codes, sequentially changing the Global Toggle Bit TGB (see Figure 28). Changing TGB from 1 to 0 updates the DAC registers from their respective Input Registers A. Changing TGB from 0 to 1 updates the DAC registers from their respective Input Registers B. Note that in this way, one or both channels may be toggled with just one serial command.

To toggle all selected channels using an external logic signal, ensure that both the TGB bit in the global toggle register and the bits corresponding to the desired channels in the toggle select register are high. Apply a clock or logic signal to the TGP pin to alternate codes. The TGP falling edges update the DAC registers from their associated Input Registers A. The TGP rising edges update the DAC registers from their associated Input Registers B. Note that once the input registers are set up, all toggling is triggered by the signal applied to the TGP pin, with no further SPI instructions needed.

To cause any combination of channels to update from either Input Register A or Input Register B, ensure the TGP pin and the TGB bit in the global toggle register are high. Using the **toggle select** command, set the toggle select bits as needed to select the input register (A or B) with which each channel is to be updated. Then update all channels, either by using the serial command (**update all (power up)**, 1001b) or by applying a negative pulse to the $\overline{\text{LDAC}}$ pin. Any channels where the toggle select bits are zero update from Input Register A. Channels where the toggle select bits are one update from Input Register B (see Figure 29). By alternating toggle select and update operations, more than one channel can be simultaneously switched to A or B as needed.

DAISY-CHAIN OPERATION

The serial output of the shift register appears at the SDO pin. Data transferred to the device from the SDI input is delayed 32 SCK rising edges before being output at the next SCK falling edge, suitable for clocking into the microprocessor on the next 32 SCK rising edges.

The SDO output can be used to facilitate control of multiple serial devices from a single 3-wire serial port (SCK, SDI, and $\overline{\text{CS}}$/LD). Such a daisy-chain series is configured by connecting the SDO of each upstream device to the SDI of the next device in the chain. The shift registers of the devices are thus connected in series, effectively forming a single input shift register that extends through the entire chain. Because of this, the devices can be addressed and controlled individually by simply concatenating their input words.

The first instruction addresses the last device in the chain and so forth. The SCK and $\overline{\text{CS}}$/LD signals are common to all devices in the series.

In use, $\overline{\text{CS}}$/LD is first taken low. Then, the concatenated input data is transferred to the chain using the SDI of the first device as the data input. When the data transfer is complete, $\overline{\text{CS}}$/LD is taken high, completing the instruction sequence for all devices simultaneously. A single device can be controlled by using the **no operation** command (1111b) for all other devices in the chain. When $\overline{\text{CS}}$/LD is taken high, the SDO pin presents a high impedance output, so a pull-up resistor is required at the SDO of each device (except the last) for daisy-chain operation.

ECHO READBACK

The SDO pin can be used to verify data transfer to the device. During each 32-bit instruction cycle, SDO outputs the previous 32-bit instruction for verification. The 8-bit don't care prefix is replaced by four fault register status bits, followed by the 4-bit command and address words and the full 16-bit data-word (see Figure 3). The SDO sequence for a 24-bit instruction cycle is the same, except that the data-word is truncated to 8 bits (see Figure 4). When $\overline{\text{CS}}$/LD is high, SDO presents a high-impedance output, releasing the bus for use by other SPI devices.

FAULT REGISTER (FR)

The AD5778R provides notifications of operational fault conditions. The fault register (FR) status bits comprise the first data byte (8 bits) of each 24- or 32-bit SDO word, outputted to the SDO pin during every SPI transaction. See Figure 3 and Figure 4 for sequences.

A fault register bit is set when its trigger condition is detected, and the bit is clocked to SDO during the next SPI transaction. The fault register information is updated with each SPI transaction. Note that if a fault condition is corrected by the action of an SPI instruction, the cleared fault register flag for that condition is observable at SDO on the next SPI transaction.

Table 11 lists the fault register bits and their associated trigger conditions.

Table 11. Fault Register

FR Bit	Fault Condition
FR0	Open-circuit condition detected on OUT0.
FR1	Open-circuit condition detected on OUT1.
FR2	Overtemperature. If the die temperature T_J > 175°C, FR2 is set, and the thermal protection is activated. The FR2 bit can be disabled using the **CONFIG** command (0111b).
FR3	Power Limit. If $V_{DDx} - V_{OUTx}$ > 10 V and the current range is ≥ 200mA, FR3 is set, and the range for that channel is reduced to 100 mA. The FR3 bit can be disabled using the **CONFIG** command (0111b).

THEORY OF OPERATION

Table 11. Fault Register (Continued)

FR Bit	Fault Condition
FR4	Invalid SPI sequence length. Valid sequence lengths are 24, 32, and multiples of 32 bits. For all other lengths, FR4 is set, and the SPI instruction is ignored.

Fault Indicator Pin ($\overline{\text{FAULT}}$)

The $\overline{\text{FAULT}}$ pin is an open-drain N-channel output that pulls low when a fault condition is detected. The $\overline{\text{FAULT}}$ pin is released on the next rising $\overline{\text{CS}}$/LD edge. The pin is an open-drain output suitable for wired-OR connection to an interrupt bus, but a pull-up resistor on the bus is required.

Fault Conditions and Thermal Overload Protection

There are four types of fault conditions that cause the $\overline{\text{FAULT}}$ pin to pull low. First, the FR0 and FR1 flag an open-circuit (OC) condition on any of the output pins (OUT0 and OUT1, respectively) when an output channel enters dropout due to insufficient voltage from V_{DDx} to OUTx. Independent open-circuit detection is provided for each of the two DAC current output pins.

The FR2 bit provides a detection flag that is set when the die temperature exceeds 175°C. The overtemperature condition also forces both DAC channels to power down and the open-drain $\overline{\text{FAULT}}$ pin to pull low. The FR3 bit remains set, and the device stays in shutdown until the die cools. Below approximately 150°C, the DAC channels can be returned to normal operation. Note that a $\overline{\text{CS}}$/LD rising edge releases the $\overline{\text{FAULT}}$ pin regardless of the die temperature.

Because any DAC channel can source up to 300 mA, die heating potential of the system design should be evaluated carefully. The FR4 bit, a power-limit protection flag, is provided to help prevent accidental damage to the current output device(s). The power-limit fault condition is triggered for the 200 mA and 300 mA full-scale current spans when the voltage difference between an output supply pin (V_{DDx}) and its current output pin (OUTx) is ≥ 10 V.

Finally, the FR4 bit is provided to flag invalid SPI word lengths. Valid word lengths are 24 bits, 32 bits, and integer multiples of 32 bits. Any other length causes the FR4 flag to set, the $\overline{\text{FAULT}}$ pin to assert, and the instruction itself to be ignored.

CONFIG COMMAND

The **CONFIG** command has four arguments—open circuit detection disable (OC), power limit protection disable (PL), thermal shutdown disable (TS), and reference disable (RD) (see Figure 30).

Setting the OC bit disables the open-circuit detection (FR0 and FR1). Likewise, the PL bit disables power-limit protection (FR3), and the TS bit disables thermal protection (FR2). Use these options with caution, particularly the PL bit and the TS bit.

The RD bit is used to select the external-reference operation. The REFCOMP pin must be grounded for external reference use whether the RD bit is set or not.

Figure 30. CONFIG Command Syntax: OC, PL, TS, and RD

THEORY OF OPERATION

POWER-DOWN MODE

For power-constrained applications, power-down mode can be used to reduce the supply current when less than two DAC outputs are needed. When in power-down, the voltage-to-current output drivers and reference buffers are disabled. The current DAC outputs are put into a high-impedance state. Register contents are not disturbed during power-down.

Any channel or combination of channels can be put into power-down mode by using Command 0100b in combination with the appropriate DAC address. In addition, all the DAC channels and the integrated reference together can be put into power-down using the **power down chip** command, 0101b. The 16-bit data-word is ignored for all power-down commands.

Normal operation resumes by executing any command which includes a DAC update—either in software, as shown in Table 7 or by toggling (see the Toggle Operations section). The selected DAC channel is powered up as it is updated with the new code value. When updating a powered-down DAC, add wait time to accommodate the extra power-up delay. If the channels have been powered down (Command 0100b) prior to the update command, the power-up delay time is 30 µs. Alternatively, if the chip has been powered down (command 0101b), the power-up delay time is 35 µs.

SWITCH TO V_ MODE

Span Code 1000b can be used to pull outputs below GND. In Switch to V_ mode, the output current is turned off for the addressed channel(s), and the channel voltage V_{OUTx} pulls to V_. The pull-down switch can sink up to 80 mA at an effective resistance of 12 Ω maximum.

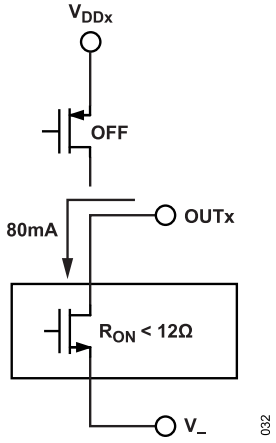


Figure 31. Switch to V_ Mode

The switch to V_ mode can be invoked with the **write span to all** command or the **write span to n** command and the desired address. Span codes are shown in Table 9, and a diagram of an output in switch to V_ mode is shown in Figure 31.

GAIN ADJUSTMENT USING THE FSADJ PIN

The full-scale output currents are proportional to the reference voltage, and the full-scale output currents are inversely proportional to the resistance associated with FSADJ. That is explained in the following equation:

$I_{OUTFS} \sim V_{REF}/R_{FSADJ}$.

If the FSADJ pin is tied to V_{CC}, the AD5778R uses an internal R_{FSADJ} = 20 kΩ. Optionally, FSADJ can instead be connected to a grounded external resistor to tune the default current ranges to the application or, for the best possible temperature coefficient, using an appropriately specified precision resistor. Values from 19 kΩ to 41 kΩ are supported. The new current ranges can easily be calculated using the external R_{FSADJ} column of Table 9. The internal resistor is automatically disconnected when using an external resistor.

When using an external resistor, FSADJ is sensitive to stray capacitance. Therefore, the pin should be compensated with a snubber network consisting of a series combination of 1 kΩ and 1 µF connected in parallel to R_{FSADJ}. With the recommended compensation, the pin is stable driving stray capacitance of up to 50 pF.

REFERENCE MODES

The AD5778R can be used with either an internal or external reference. As with voltage DACs, the reference voltage scales the outputs so that the outputs reflect any errors in the reference. Full-scale output currents are limited to 300 mA maximum per channel regardless of reference voltage.

The internal 1.25 V reference has a typical temperature drift of ±3ppm/°C and an initial output tolerance of ±2 mV maximum. It is trimmed, tested, and characterized independently of the DACs. The DACs are tested and characterized with an ideal external reference.

To use the internal reference, the REFCOMP pin should be left floating with no DC path to GND. In addition, the RD bit in the CONFIG register must have a value of zero. This value is reset to zero at power-up, or it can be reset using the **CONFIG** command, 0111b. Figure 30 shows the command syntax.

For reference stability and low noise, a 0.1µF capacitor should be tied between REFCOMP and GND. In this configuration, the internal reference can drive up to 0.1 µF with excellent stability. To ensure stable operation, the capacitive load on the REF pin should not exceed that on the REFCOMP pin. A buffer is needed if the internal reference is to drive external circuitry.

To use an external reference, tie the REFCOMP pin to GND. This disables the output of the internal reference at startup, so that the REF pin becomes a high-impedance input. Apply the reference voltage at the REF pin after powering up. Set the RD bit to one using the **CONFIG** command, 0111b. The REF input voltage range is 1.225 V to 1.275 V.

APPLICATIONS INFORMATION

VALID SUPPLY RANGES

The valid supply ranges for the AD5778R have several restrictions as described in the Table 1 section (Power Requirements) and the Pin Configuration and Function Descriptions section. The voltage at V_+ must be greater than or equal to all other supply voltages, and V_+ is allowed to be up to 33 V above V_-. The two output supplies (V_{DD0} and V_{DD1}) may be independently set between 2.85 V and V_+. The negative supply, V_-, may be any voltage between –15.75 V and GND, but V_+ must be no more than 33 V above V_-.

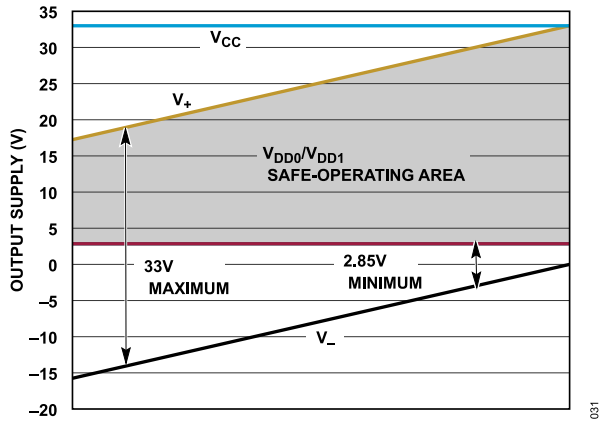


Figure 32. Output Supply Safe Operating Area

CURRENT OUTPUTS

The AD5778R incorporates a high-gain voltage-to-current converter at each current output pin. The INL and DNL are guaranteed for all ranges from 3.125 mA to 300 mA if the minimum dropout voltage ($V_{DDx} – V_{OUTx}$) is met for all DAC codes.

If sufficient dropout voltage is maintained, the DC output impedances of the current outputs (OUT0 and OUT1) are very high. Each current output has a dedicated positive supply pin, V_{DD0} and V_{DD1}, to allow the tailoring of the current compliance and power dissipation of each channel.

OFFSET CURRENT AND CODE ZERO

The offset current error of the AD5778R is guaranteed ±0.4% FSR maximum. If the offset of a given channel is positive, some nonzero current flows at Code 0. If the current is negative, the current is zero (leakage only) for a range of codes close to zero. Offset and linearity endpoints are measured at Code 384 for AD5778R , guaranteeing that the DAC is operating with a measurable output current at the point of measurement.

A channel with a positive offset error may not completely turn off, even at Code 0. To turn an output completely off, set the range to high-Z (Span Code 0000b from Table 9), and update the channel.

BOARD LAYOUT

The excellent load regulation and DC crosstalk performance of the AD5778R device is achieved in part by minimizing common-mode resistance of signal and power grounds.

As with any high resolution converter, clean board grounding is important. A low impedance analog ground plane is necessary, as are star-grounding techniques. Keep the board layer used for star-ground continuous to minimize ground resistances (that is, use the star-ground concept without using separate star traces). Resistance from the REFLO pin to the star point should be as low as possible. The exposed pad is recommended as the star ground point.

For best performance, stitch the ground plane with arrays of vias on 150 mil to 200 mil centers connecting it with the ground pours from the other board layers. This reduces the overall ground resistance and minimizes ground loop area.

APPLICATIONS INFORMATION

TYPICAL APPLICATION

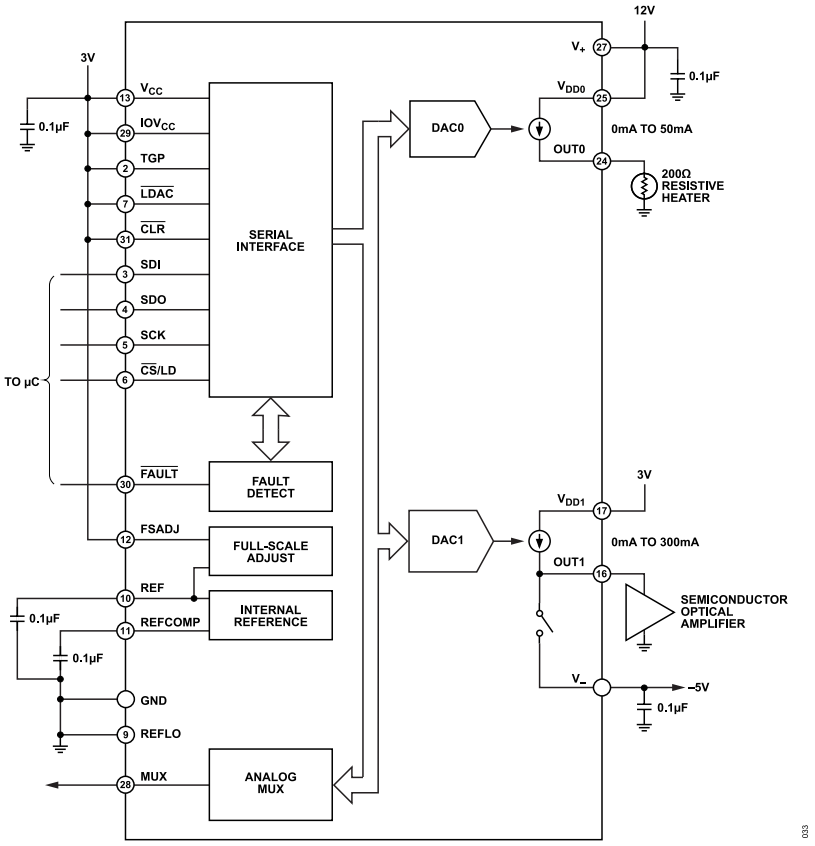
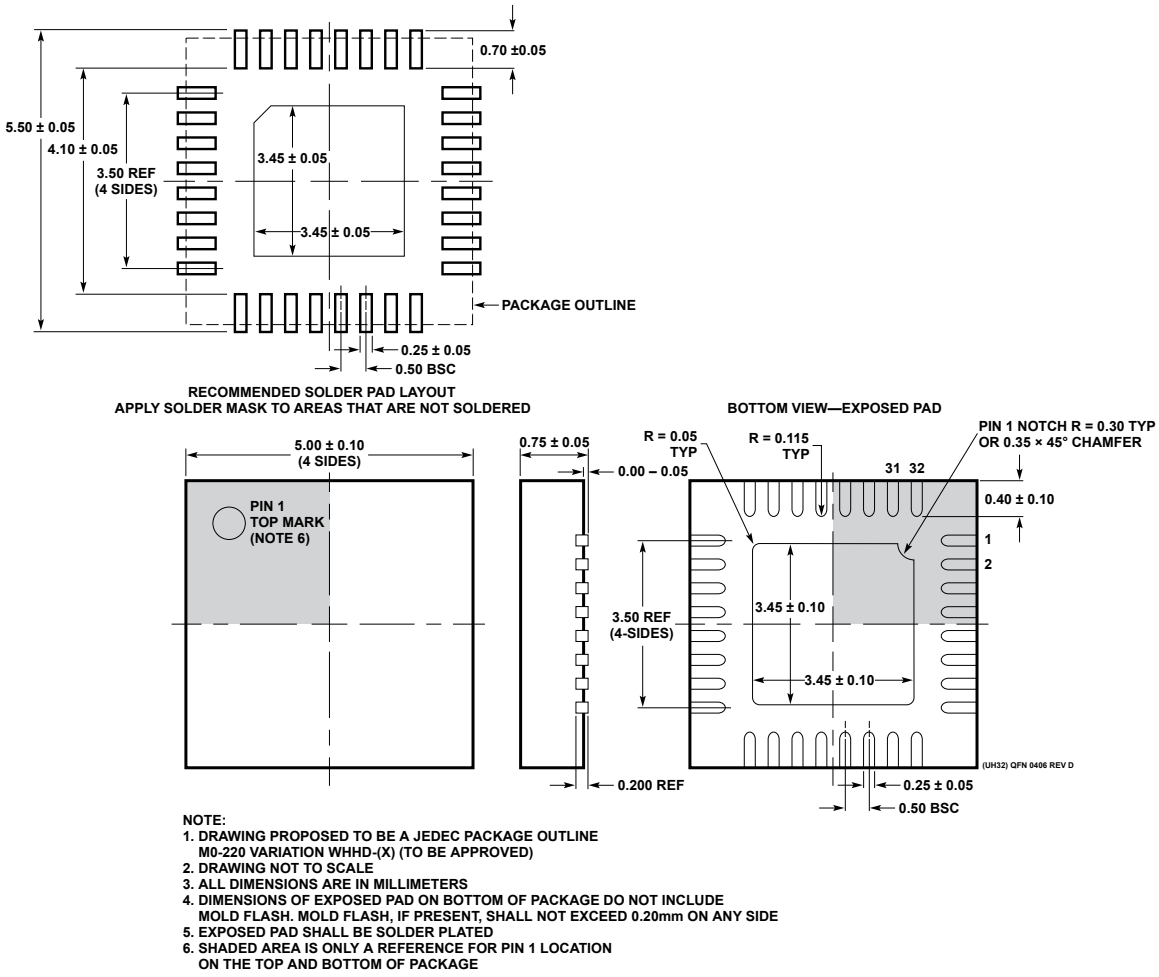


Figure 33. Typical Application Example

RELATED PRODUCTS

Part Number	Description	Comments
LTC2672	5-channel, current output DAC with internal reference and SPI	Software-programmable, current output ranges from 3.125 mA to 300 mA with flexible 2.1 V to 5.5 V supply voltage per channel, 3.5 mm × 3.6 mm WLCSP and 5 mm × 5 mm QFN packages
LTC2662	5-channel, 300 mA current-source-output 16-/12-bit SoftSpan DACs	Software-programmable, current output ranges from 3.125 mA to 300 mA with flexible 2.85 V to 33 V supply voltage per channel, 5 mm × 5 mm QFN package
AD5770R	6-channel, 14-bit, current output DAC with on-chip reference, SPI interface	Software-programmable, output ranges from −60 mA to 300 mA with flexible 0.8 V to 5.1 V per channel, 4 mm × 4 mm QFN package
REFERENCES		
LTC6655	0.25 ppm noise, low drift precision references	0.025% maximum tolerance 2 ppm/°C maximum, 0.25 ppm p-p, 0.1 Hz to 10 Hz noise
LT6654	Precision wide supply high output drive low noise reference	0.05% maximum tolerance 10 ppm/°C maximum, 1.6 ppm p-p, 0.1 Hz to 10 Hz noise

OUTLINE DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Figure 34. 32-Lead (5 mm x 5 mm) Plastic QFN Package
(05-08-1693)
Dimensions shown in millimeters

Updated: April 03, 2024

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD5778RBCPZ	−40°C to +125°C	32-Lead QFN (5 mm x 5 mm x 0.75 mm w/ EP)	05-08-1693

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 12. Evaluation Boards

Model[1]	Description
DC2692A-A	Evaluation Board

[1] The DC2692A-A is an RoHS Compliant Part.