Dual, 188 dB Range, 10 pA to 25 mA, Logarithmic Converter

FEATURES

- 188 dB electrical dynamic range and 94 dB optical dynamic range
- Dual-channel current inputs for direct optical gain measurements
- Accurately trimmed logarithmic response:
  - Logarithmic slope 200 mV/decade
  - Logarithmic conformance error ±0.4 dB over temperature
  - Offset trimmed at 70°C to reduce dark current
- Integrated LDO: 26 dB PSRR at 60 Hz and 100 pA input current (V_{CC} = 3.0 V)
- I^{2}C adjustable:
  - Photodiode bias voltage
  - Trade-off between noise and response time at low input currents
- Integrated 14-bit ADC
- Requires minimal external components
- 2.040 mm × 1.640 mm, 20-lead WLCSP

APPLICATIONS

- Automatic test equipment
- Optical power monitoring
- Machine automation
- Optical modules

GENERAL DESCRIPTION

The ADL5309 contains dual monolithic logarithmic transimpedance amplifiers that are optimized for measuring low-frequency and wide dynamic range optical signal power in fiber optic systems.

The device produces highly accurate, temperature compensated output voltages that are proportional to the logarithm of the ratio between the input current at the INP1 and INP2 pins and the internally generated reference currents. The logarithmic slope and intercept are both accurately trimmed to a nominal value of 200 mV/decade and 10 pA, respectively. The low-impedance OUT1 and OUT2 logarithmic outputs have the capability to drive a wide range of analog-to-digital converters (ADCs) and other circuits.

A digital representation of the OUT1 and OUT2 outputs is available through the inter-IC bus (I^{2}C) interface. A 14-bit successive approximation register (SAR) ADC, controlled through the I^{2}C interface, samples the OUT1 and OUT2 channel outputs along with a built-in digital temperature sensor.

Adaptive photodiode biasing is supported through the PDB1 and PDB2 interfaces. At low diode currents, the photodiode reverse bias is kept small to minimize the dark current. At higher input currents, the bias voltage scales linearly with the current to avoid nonlinearity due to photodiode saturation. Both the starting bias level and the scale factor at higher currents are configurable through I^{2}C.

The ADL5309 is specified for operation from −40°C to +105°C ambient temperature and is offered in a small 2.040 mm × 1.640 mm, 20-lead wafer level chip scale package (WLCSP).
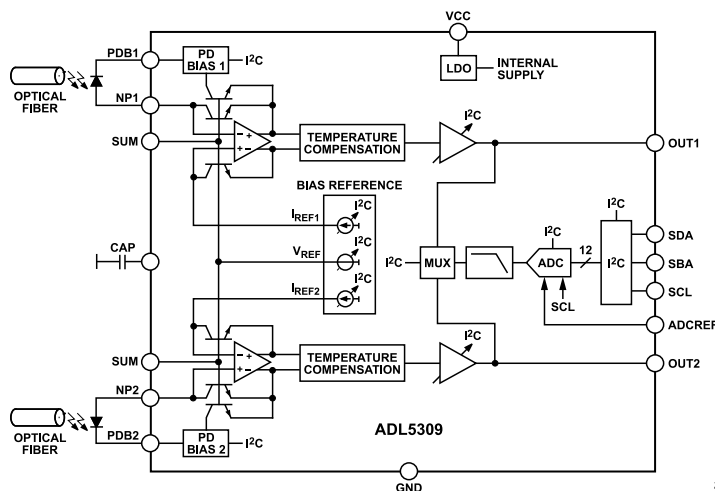
FUNCTIONAL BLOCK DIAGRAM

Figure 1. Functional Block Diagram

DOCUMENT FEEDBACK

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REVISION HISTORY

6/2024—Revision 0: Initial Version

SPECIFICATIONS

Supply voltage (V_{CC}) = 3.0 V, T_A = 25°C, and default register settings unless otherwise noted.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT INTERFACES	Pin B1 = INP1 and Pin C1 = INP2				
Input Current Range (I_{INP1}, I_{INP2})		10			pA
				25	mA
Input Node Voltage (V_{INP1}, V_{INP2})	10 pA < I_{INP1} and I_{INP2} < 3 mA		1.6 to 1.8		V
	10 pA < I_{INP1} and I_{INP2} < 25 mA		1.6 to 2.5		V
SUM Voltage			1.6		V
PHOTODIODE BIAS	Pin A2 = PDB1 and Pin D2 = PDB2				
Output Voltage (V_{PDB1}, V_{PDB2})	I_{INP1} = I_{INP2} = 1 nA		1.6		V
	I_{INP1} = I_{INP2} = 10 mA; V_{CC} = 5 V		4.2		V
Absolute Offset Voltage, T_C = 70°C	(V_{PDB1} − V_{INP1}), (V_{PDB2} − V_{INP2}), and I_{INP1} = I_{INP2} = 1 nA		0.4		mV
Transresistance (R_T)	(V_{PDB1} − V_{INP1})/I_{INP1} and/or (V_{PDB2} − V_{INP2})/I_{INP2}		231		Ω
I_{INP1}, I_{INP2} Threshold (I_{TH})	Constant photodiode bias voltage below I_{TH}		220		µA
LOGARITHMIC OUTPUT	Pin A5 = OUT1 and Pin D5 = OUT2				
Logarithmic Slope	Over 1 nA < I_{INP1} and I_{INP2} < 1 mA range	198	200	202	mV/dec
Logarithmic Intercept			10		pA
Logarithmic Conformance Error	1 nA < I_{INP1} and I_{INP2} < 1 mA		±0.3		dB
	100 pA < I_{INP1} and I_{INP2} < 10 mA		±0.6		dB
Logarithmic Conformance Error over Temperature	1 nA < I_{INP1}, I_{INP2} < 1 mA, and T_A = 5°C to 70°C		±0.4		dB
	100 pA < I_{INP1}, I_{INP2} < 10 mA, and T_A = 5°C to 70°C		±0.8		dB
Output Voltage (V_{OUT1}, V_{OUT2})	I_{INP1} and I_{INP2} = 100 pA		0.403		V
	I_{INP1} and I_{INP2} = 1 µA		0.999		V
	I_{INP1} and I_{INP2} = 10 mA		1.808		V
Small Signal Bandwidth	I_{INP1} and I_{INP2} = 10 nA and capacitor feedback (CF) = 15 (Default register state)		75		kHz
	I_{INP1} and I_{INP2} = 10 nA and CF = 0		550		kHz
Rise and Fall Times	I_{INP1} a I_{INP2} from 10 nA to 100 nA, measured at 10% and 90% of steady state V_{OUT1} and V_{OUT2}		1.6/3.8		µs
Short Circuit Output Current	I_{INP1} and I_{INP2} = 1 nA, V_{OUT1} and V_{OUT2} = 0.7 V		32		mA
	I_{INP1} and I_{INP2}= 10 mA, V_{OUT1} and V_{OUT2} = 1.5 V		15		mA
Channel-to-Channel Isolation	DC isolation to OUT1 for I_{INP2} = 25 mA and I_{INP1} = 1 nA or OUT2 for I_{INP1} = 25 mA and I_{INP2} = 1 nA		2		mV
POWER SUPPLY	Pin A3 = VCC				
Positive Supply Voltage		2.85	3	5.25	V
Quiescent Current	I_{INP1} and I_{INP2} = 1 µA		57		mA
Power Supply Rejection Ratio (PSRR)	I_{INP1} and I_{INP2} = 100 pA at 60 Hz		26		dB
DATA ACQUISITION					
ADC Resolution			14		Bits
LOG Output Conversion Slope			74.5		LSB/dB
Output Data Rate				22	kHz
Output Noise	I_{INP1}, I_{INP2} = 1 µA		6.6		LSB rms
SERIAL BUS ADDRESS (SBA) INTERFACE	Pin A4 = SBA				
Serial Bus Address 0x6C		−0.05 V_{CC}		+0.15 V_{CC}	V
Serial Bus Address 0x6D		0.35 V_{CC}		0.65 V_{CC}	V
Serial Bus Address 0x6E		0.85 V_{CC}		1.05 V_{CC}	V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
I²C INTERFACE	Pin B5 = SDA and Pin C5 = SCL				
Input Low Voltage (V_{INL})	SDA and SCL input voltage (V_{IN}) = 5 V and V_{CC} = 3.0 V			0.9	V
Input High Voltage (V_{INH})	V_{IN} = 5 V and V_{CC} = 3.0 V	2.1		5.5	V
Input Leakage Current (I_{IN})	V_{IN} = 5 V and V_{CC} = 3.0 V			0.2	µA
Input Leakage Current (I_{IN3V})	V_{IN} = 5 V and V_{CC} = 3.0 V			10	µA
Input Hysteresis (V_{HYST})	V_{IN} = 5 V and V_{CC} = 3.0 V		250		mV
Input Capacitance (C_{IN})	V_{IN} = 5 V and V_{CC} = 3.0 V		1		pF
Glitch Rejection	V_{IN} = 5 V and V_{CC} = 3.0 V			50	ns

SERIAL INTERFACE TIMING SPECIFICATIONS
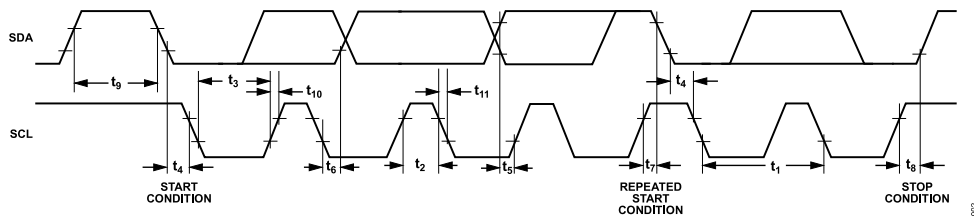
Figure 2. I²C Timing Diagram

Table 2. Serial Interface Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
$f_{SCL(MAX)}$ = $1/t_1$	Maximum SCL clock frequency	400			kHz
t_2	Minimum SCL high period		50	600	ns
t_3	Minimum SCL low period		0.65	1.3	µs
t_4	Minimum hold time after (repeated) start condition		140	600	ns
t_5	Minimum data setup time input		30	100	ns
t_6	Minimum data hold time input		−100	0	ns
t_6	Minimum data hold time output	300	600	900	ns
t_7	Minimum repeated start condition setup time		30	600	ns
t_8	Minimum stop condition setup time		30	600	ns
t_9	Minimum bus free time between stop condition and start condition		0.12	1.3	µs
t_{10}	SCL and SDA rise time			0.3	µs
t_{11}	SCL and SDA fall time			0.3	µs
$t_{SP(MAX)}$	Maximum suppressed spike pulse width	50	110	250	ns
C_X	SCL and SDA input capacitance		5	10	pF

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

Parameter	Rating
V_{CC}	5.5 V
Current into INP1 and INP2	100 mA
DC Voltage	
SDA and SCL	−0.3 V to 5.5 V
SBA, PDB1, and PDB2	−0.3 V to V_{CC} + 0.3 V
SUM, INP1, INP2, OUT1, OUT2, CAP, and ADCREF	−0.3 V to +3.0 V
Output Short Circuit Duration	
OUT1, OUT2, PDB1, and PDB2	Indefinite
Temperature	
Operating T_A Range	−40°C to +105°C
Maximum T_J	135°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}	Unit
CB-20-16	61.6	°C/W

[1] Test Condition 1: Thermal impedance simulated values are based upon use of a JEDEC 2S2P thermal test board.

ELECTROSTATIC DISCHARGE (ESD) RATING

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADL5309

Table 5. ADL5309, 20-Lead WLCSP

ESD Model	Withstand Threshold (V)	Class
HBM	2500	2
FICDM	1250	C5

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
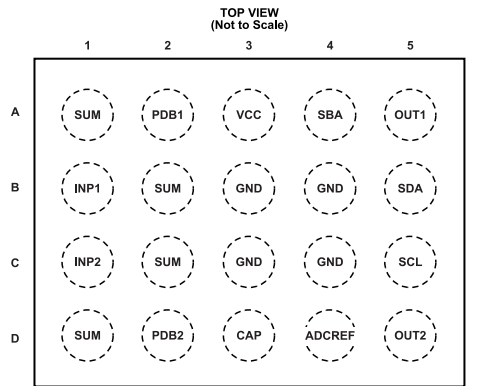
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

TOP VIEW
(Not to Scale)

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin Number	Mnemonic	Description
A1, D1, B2, C2	SUM	Guard Pins. The SUM pins shield current lines to INP1 and INP2 and are internally connected together. Do not ground.
B1	INP1	Channel 1 Photocurrent Input. Connected to the photodiode anode (current flows into INP1 pin).
C1	INP2	Channel 2 Photocurrent Input. Connected to the photodiode anode (current flows into INP2 pin).
A2	PDB1	Channel 1 Photodiode Bias. May be connected to the photodiode cathode to provide adaptive bias control. For lowest photodiode cathode to anode offset at low input currents, avoid resistive loading at the PDB1 pin. Leave floating if not used.
D2	PDB2	Channel 2 Photodiode Bias. May be connected to the photodiode cathode to provide adaptive bias control. For lowest photodiode cathode to anode offset at low input currents, avoid resistive loading at the PDB2 pin. Leave floating if not used.
A3	VCC	Positive Power Supply. Decoupling with 1 nF and 4.7 µF capacitors to ground is recommended at the VCC pin.
B3, C3, B4, C4	GND	Analog and Digital Ground. Connect all ground pins to a low impedance ground plane on PCB.
D3	CAP	Connect an optional 0.1 µF capacitor between the CAP pin and GND to reduce the OUT1 and/or OUT2 noise at low input currents.
D4	ADCREF	ADC Reference. Reference voltage input for improved ADC readout accuracy. Connect to ground if not used.
A4	SBA	Serial Bus Address. The voltage applied to the SBA pin sets the I^{2}C bus address to one of three possible settings. Connect SBA to VCC, GND, or leave floating. Refer to Table 1.
A5	OUT1	Channel 1 Logarithmic Output. The voltage at the OUT1 pin changes logarithmically with the current applied to INP1.
D5	OUT2	Channel 2 Logarithmic Output. The voltage at the OUT2 pin changes logarithmically with the current applied to INP2.
B5	SDA	I^{2}C Interface Data Input and Output.
C5	SCL	I^{2}C Interface Clock Input.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.0 V, T_A = 25°C, input current (I_{INP}) = 10 nA, and default register settings, unless otherwise noted.

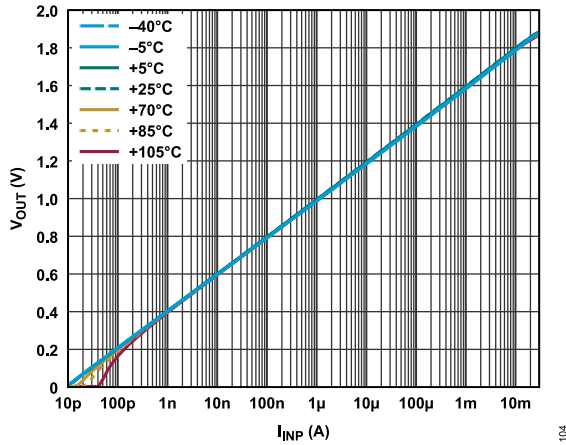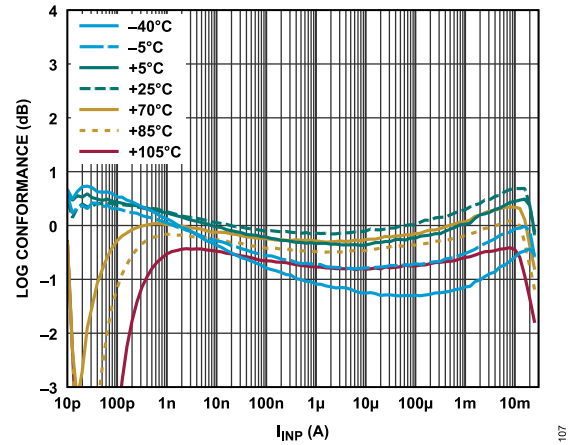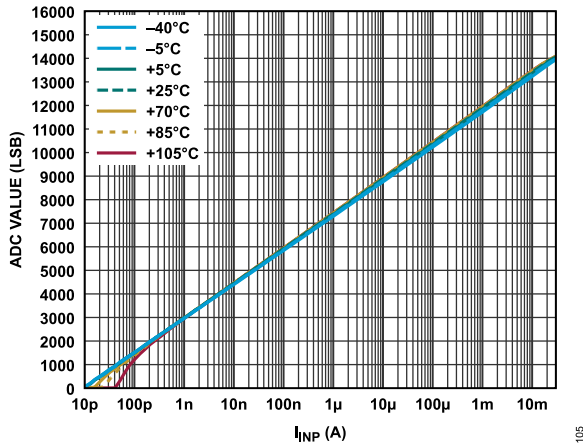Figure 4. V_{OUT} vs. I_{INP} for Multiple Temperatures

Figure 5. ADC Value vs. I_{INP} for Multiple Temperatures

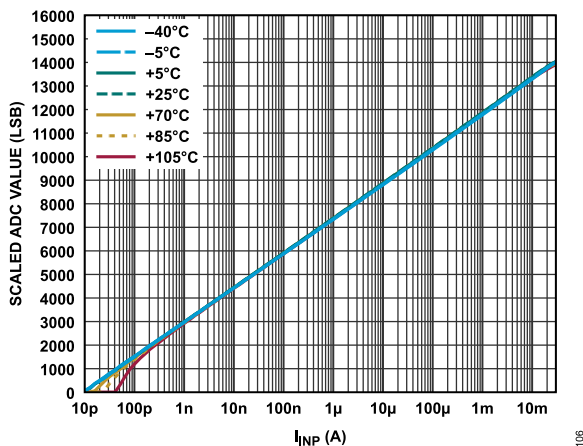Figure 6. Scaled ADC Value vs. I_{INP} for Multiple Temperatures with ADCREF = 2.000 V

Figure 7. Logarithmic (Log) Conformance vs. I_{INP} for Multiple Temperatures, Normalized to 25°C

Figure 8. ADC Value Logarithmic Conformance vs. I_{INP} for Multiple Temperatures, Normalized to 25°C

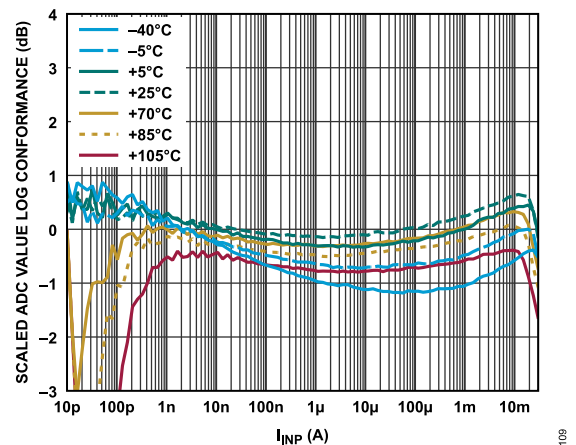

Figure 9. Scaled ADC Value Logarithmic Conformance vs. I_{INP} for Multiple Temperatures with ADCREF = 2.000 V, Normalized to 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

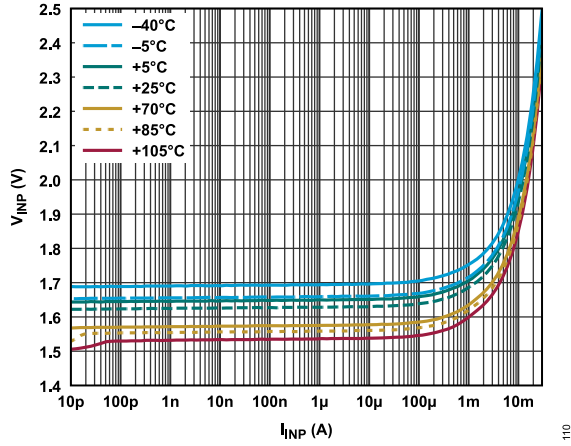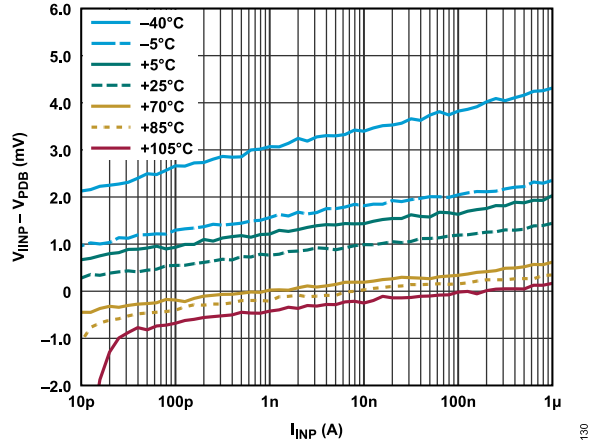*Figure 10. Input Voltage (V_{INP}) vs. I_{INP} at Different Temperatures*

Figure 13. Offset Voltage ($V_{INP} − V_{PDB}$) vs. I_{INP} at Different Temperatures
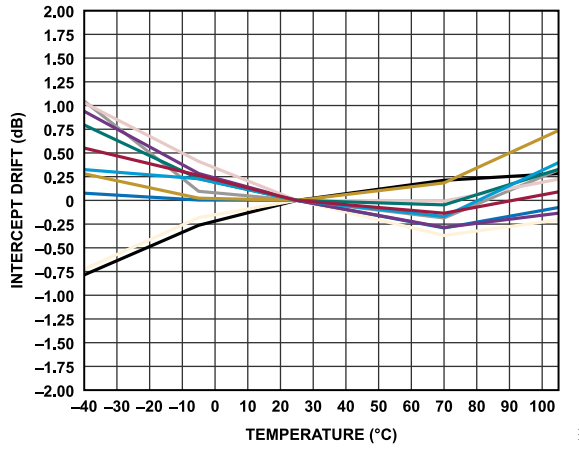

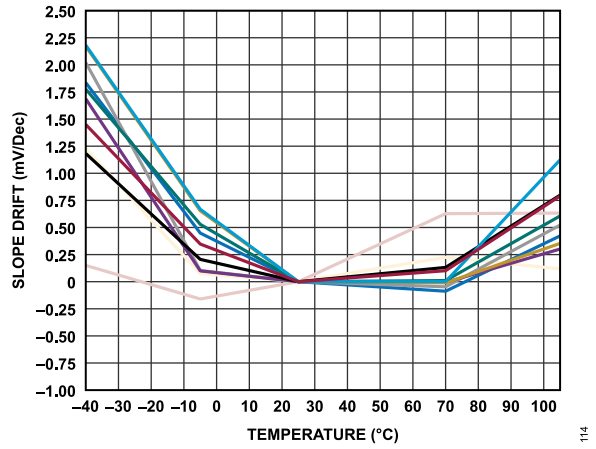*Figure 11. Intercept Drift vs. Temperature Over 10 Samples*
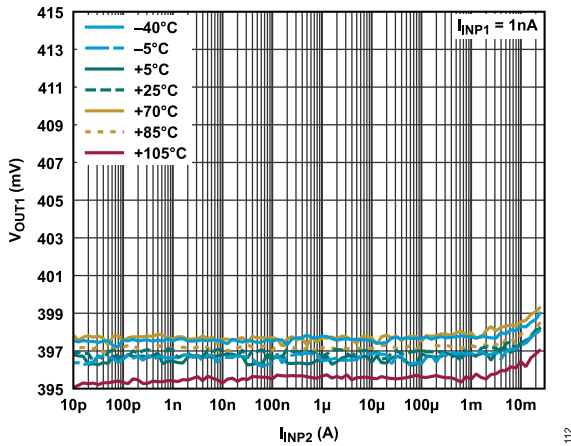

Figure 14. Slope Drift vs. Temperature Over 10 Samples

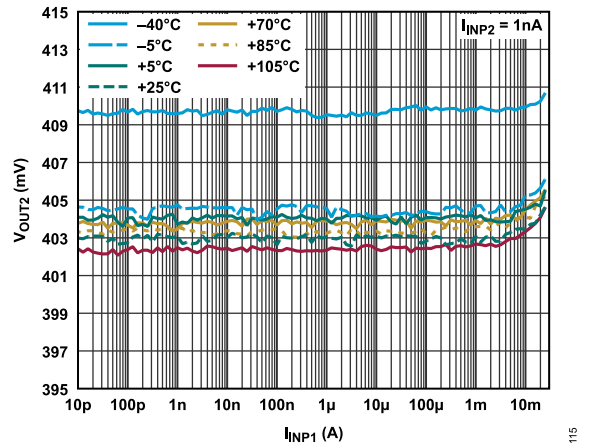*Figure 12. V_{OUT1} vs. I_{INP2} for I_{INP1} = 1 nA*

Figure 15. V_{OUT2} vs. I_{INP1} for I_{INP2} = 1 nA
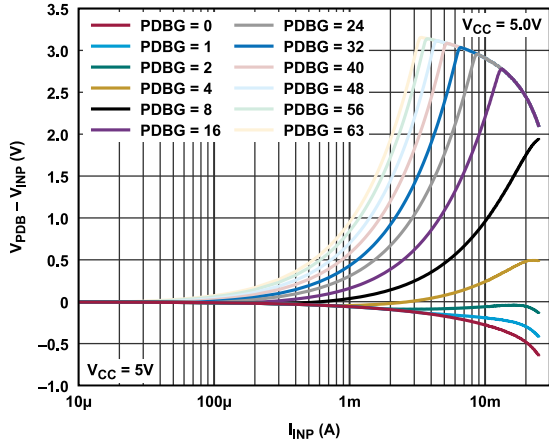
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 16. $V_{PDB} - V_{INP}$ vs. I_{INP} for Various PDBG Register Values, with PDBG_Fix = 0 at V_{CC} = 5.0 V
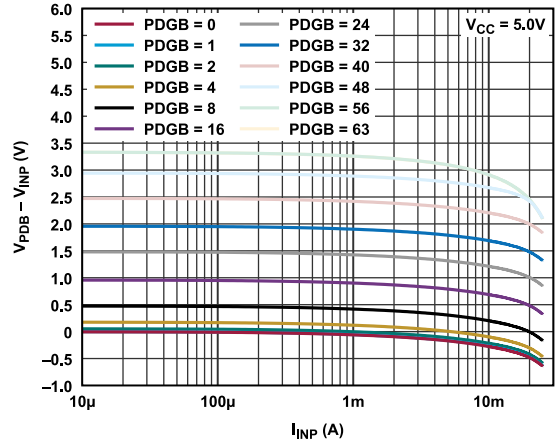
Figure 19. $V_{PDB} - V_{INP}$ vs. I_{INP} for Various PDBG Register Values with PDBG_Fix = 1 at V_{CC} = 5.0 V

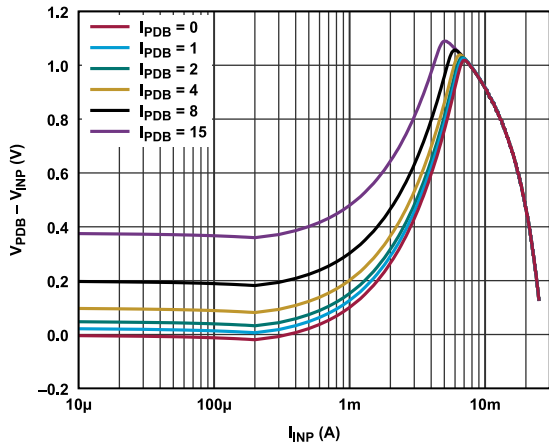Figure 17. $V_{PDB} - V_{INP}$ vs. I_{INP} at Various IPDB register Values
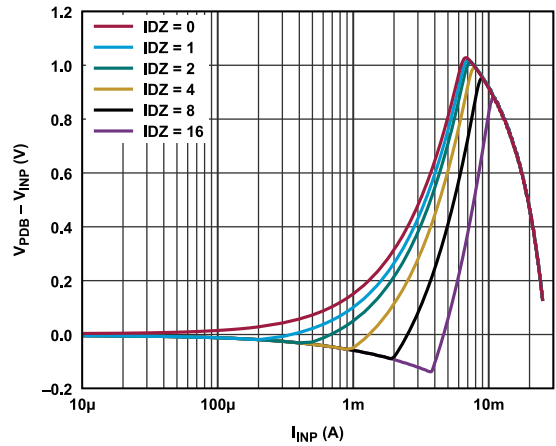
Figure 20. $V_{PDB} - V_{INP}$ vs. I_{INP} at Various IDZ Register Values
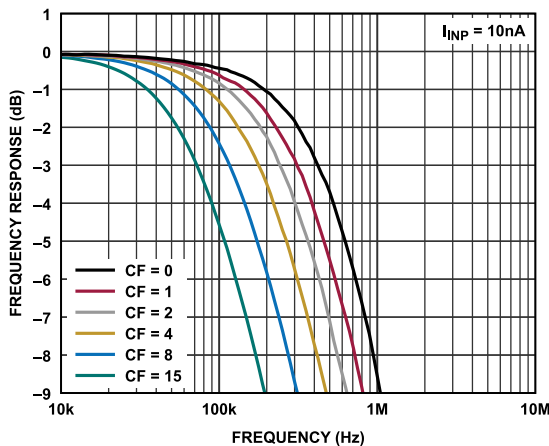
Figure 18. Small Signal AC Response from I_{INP} to V_{OUT} for I_{INP} = 10 nA at Various CF Register Values
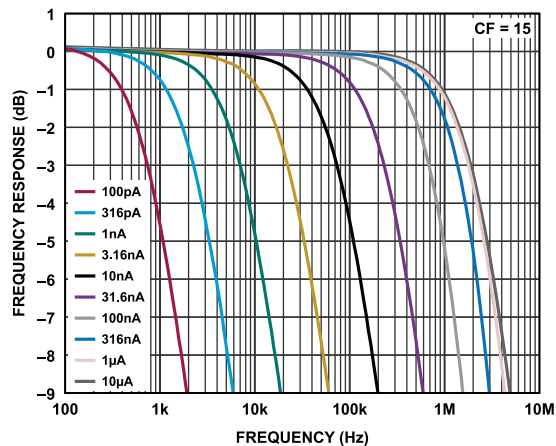
Figure 21. Small Signal AC Response from I_{INP} to V_{OUT} at Various I_{INP} Values in Half-Decade Steps for CF = 15

TYPICAL PERFORMANCE CHARACTERISTICS
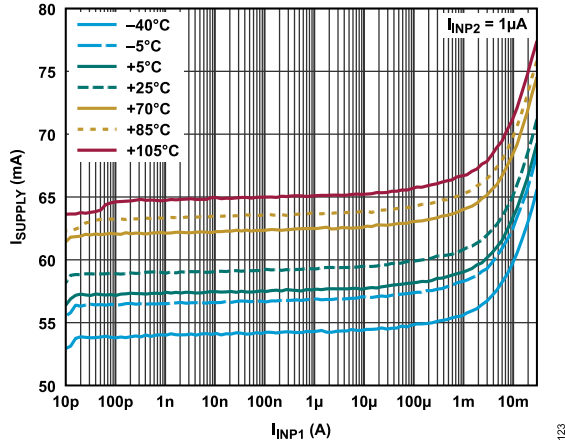
Figure 22. Supply Current (I_{SUPPLY}) vs. I_{INP1} with I_{INP2} = 1 μA
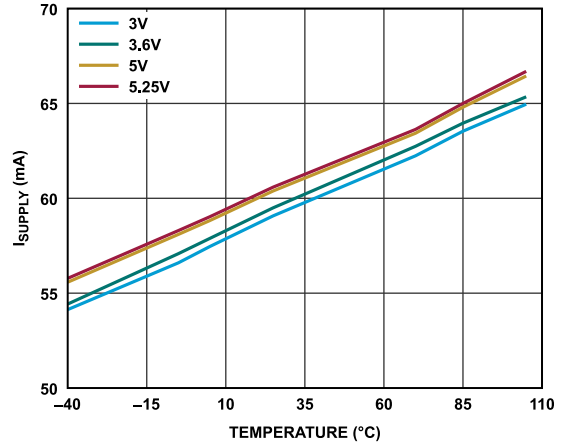
Figure 25. I_{SUPPLY} vs. Temperature for I_{INP1}, I_{INP2} = 10 nA
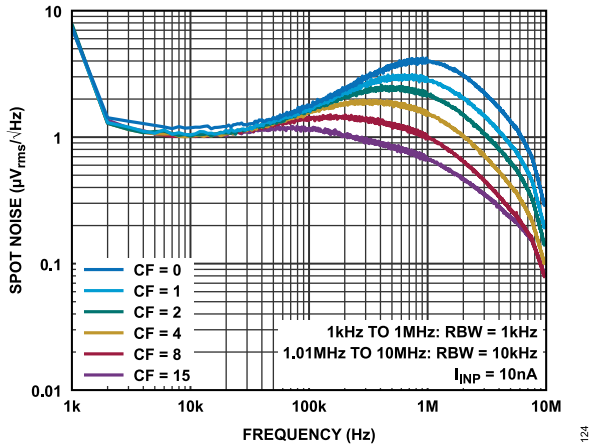
Figure 23. Spot Noise Spectral Density at V_{OUT} for I_{INP} = 10 nA at Various CF register values
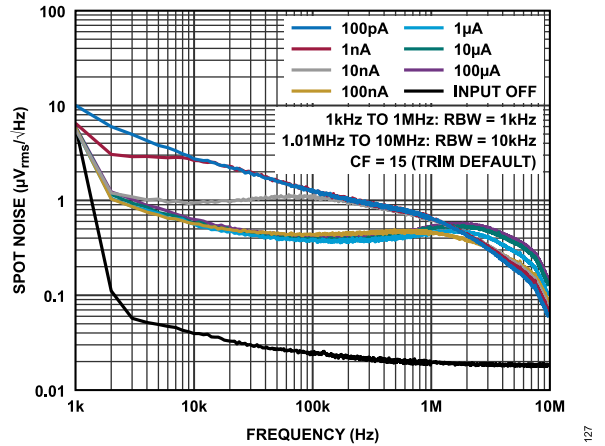
Figure 26. Spot Noise Spectral Density for V_{OUT} vs. I_{INP} at CF = 15
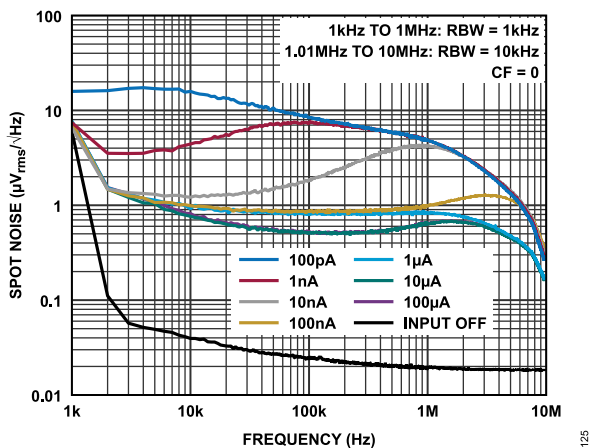
Figure 24. Spot Noise Spectral Density for V_{OUT} vs. I_{INP} at CF = 0
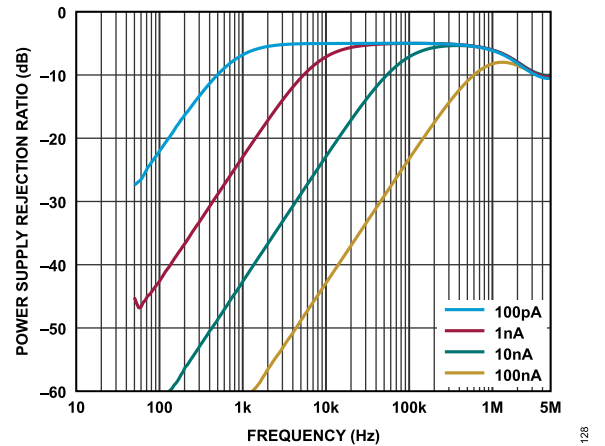
Figure 27. PSRR for Various I_{INP} values

TYPICAL PERFORMANCE CHARACTERISTICS
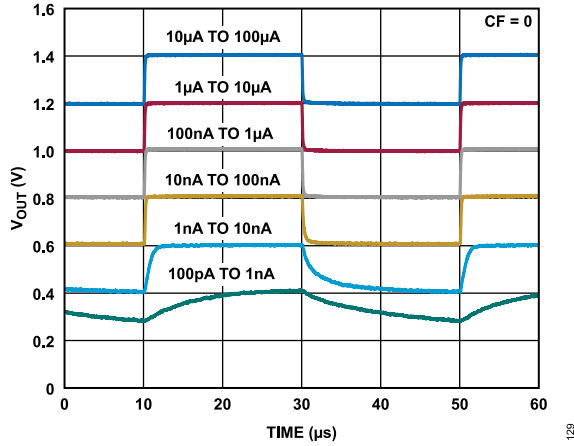
Figure 28. Pulse Response for I_{INP} in Decade Steps for CF = 0

Figure 29. $V_{INP} - V_{PDB}$ vs. Temperature at I_{INP} = 100 pA

Figure 30. Offset Voltage Distribution

Figure 31. Pulse Response for I_{INP} in Decade Steps for CF = 15

Figure 32. Offset Voltage vs. Temperature at I_{INP} = 1 nA
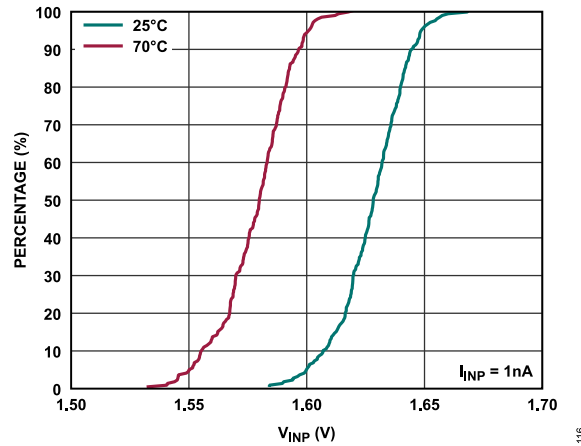
Figure 33. Input Voltage Distribution at I_{INP} = 1 nA

TYPICAL PERFORMANCE CHARACTERISTICS
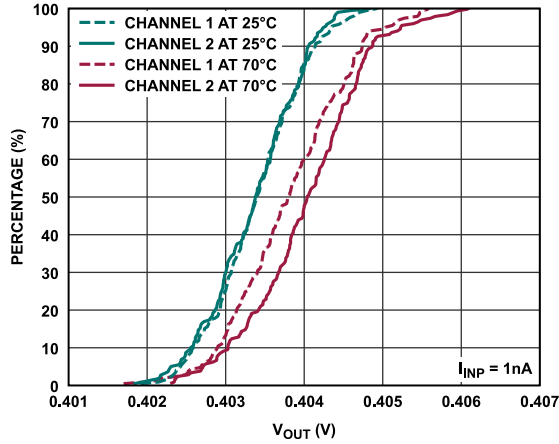
Figure 34. Output Voltage Distribution at I_{INP} = 1 nA

Figure 37. Channel Mismatch Distribution at 25°C

Figure 35. Output Voltage Distribution at I_{INP} = 1 μA
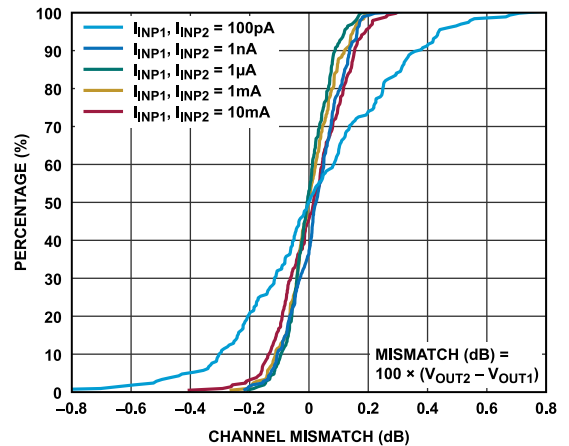
Figure 38. Channel Mismatch Distribution at 70°C

Figure 36. Output Voltage Distribution at I_{INP} = 10 mA
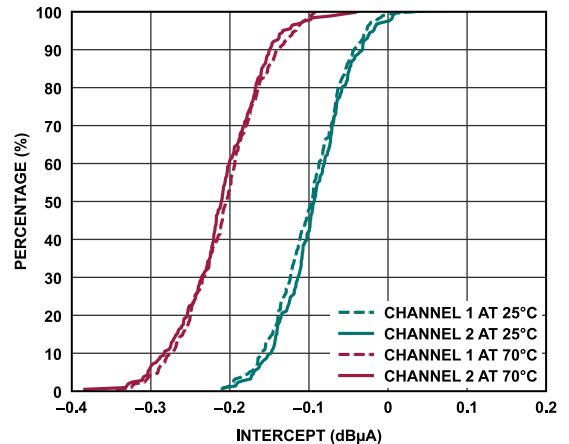
Figure 39. (V_{OUT} − 1.0 V) Intercept Distribution

TYPICAL PERFORMANCE CHARACTERISTICS
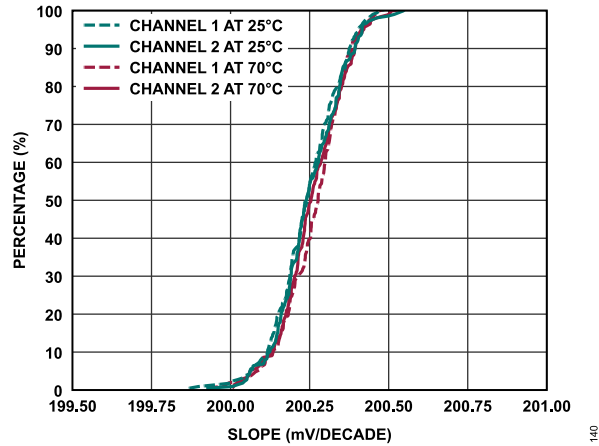
Figure 40. Slope Distribution
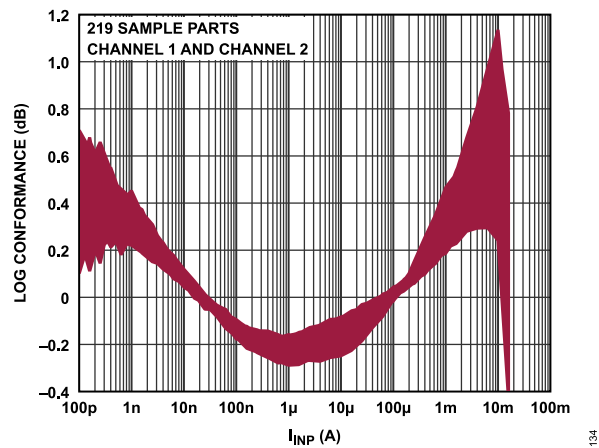
Figure 41. Logarithmic Conformance vs. I_{INP} for 219 Sample Parts, Both Channels

THEORY OF OPERATION

The ADL5309 performance and feature set is optimized for high dynamic range and high accuracy optical power measurements. The temperature compensated and factory trimmed logarithmic transimpedance amplifiers enable accurate measurements over 9 decades of input current, the equivalent to 9 decades of optical power. The amplifier output voltage can be measured with a more relaxed dynamic range, without loss of accuracy, due to the inherent dynamic range compression of the logarithmic transfer. Therefore, the 14-bit built-in ADC has more than sufficient dynamic range and resolution to provide an accurate digitized result. The built-in adaptive photodiode bias function minimizes the impact of nonidealities such as dark current and diode series resistance on the measurement accuracy. The built-in I²C interface can be used to control various internal analog functions and to read out the ADC. A total of three possible choices for the I²C device address allow up to three devices to communicate independently over a single I²C bus.

LOGARITHMIC TRANSFER

The logarithmic transimpedance amplifiers (TIAs) produce an output voltage that is (approximately) linearly related to the logarithm of the input current (I_{PD}) as follows:

$$V_{OUT} = SLOPE \times \log_{10}\left(\frac{I_{PD}}{I_Z}\right) \tag{1}$$

where:
SLOPE is the logarithmic slope that represents the amount by which the output voltage (V_{OUT}) changes for each factor of 10 (decade) change in I_{PD}.
I_Z is the (extrapolated) I_{PD} for which the V_{OUT} is zero.

The actual device never reaches zero but saturates to the starting voltage of 17 mV for input currents below 10 pA. Both SLOPE and I_Z can be obtained by linear regression of the measured amplifier output voltage vs. a range of input current levels. The ADL5309 logarithmic slope and intercept of the $V_{OUT} - 1.0$ V curve are accurately factory trimmed to 200 mV/dec and 1 µA, respectively. The reason 1.0 V is subtracted from the V_{OUT} curve (the ideal value of V_{OUT} at 1 µA) is to place the x-intercept in the geometric middle of the specified input current range. As a result, the residual slope differences have a minimum impact on the x-intercept, and the equation can be written as follows:

$$V_{OUT} - 1.0 = SLOPE \times \log_{10}\left(\frac{I_{PD}}{I_{Z1}}\right) \tag{2}$$

Expressed in dB of input current, Equation 3 can be written as follows:

$$V_{OUT} - 1.0 = SLOPE \times \left(I_{PD, \, dB} - I_{Z1, \, dB}\right) \tag{3}$$

where:
$I_{PD, \, dB}$ is the input current in dBA.
$I_{Z1, dB}$ is the intercept current in dBA (−120 dBA in this case).

The measurement accuracy obtained with a logarithmic amplifier is determined by the following two factors:

▸ The logarithmic conformance error
▸ The temperature drift error

The logarithmic conformance error describes the deviation of the actual TIA transfer from the ideal log-linear relationship (see Equation 3) and is expressed in dB of input current by the following equation:

$$E_{LC} = \frac{20 \times V_{OUT}(T)}{SLOPE} + I_{Z1, \, dB} - I_{PD, \, dB} \tag{4}$$

where: E_{LC} is the measurement error.

Thus, E_{LC} shows the resulting measurement error when V_{OUT} of a logarithmic TIA is measured, and Equation 3 is used to determine the input current that the device is sensing. Since SLOPE and I_Z are usually determined at room temperature only, E_{LC} typically also contains a contribution due to drift of the TIA transfer over temperature.

The temperature drift error (E_{DRIFT}) describes the measurement error introduced solely due to the temperature drift of the TIA transfer, excluding discrepancies of the actual TIA transfer to the ideal log-linear relationship (logarithmic conformance).

$$E_{DRIFT}(T) = \frac{20}{SLOPE} \times [V_{OUT}(T) - V_{OUT}(T_O)] \tag{5}$$

where:
T is the operating temperature.
T_O is the reference temperature.

The error, the difference between the V_{OUT} measured at the operating temperature and the actual V_{OUT} measured at the reference temperature, usually 25°C, is input referred and expressed in dB (of I_{PD}) using SLOPE. This is accurate as long as the error is relatively small and the TIA transfer is approximately logarithmic (linear in dB).

OPTICAL MEASUREMENTS

A high dynamic range optical power monitor can be constructed by connecting the anode of a reverse biased photodiode to the input of the logarithmic TIA, such that the TIA senses the photon-generated diode current. Therefore, it is important to understand the transducer aspects of a photodiode to interpret the photodiode current relative to the incident optical power. In purely electrical circuits, the power dissipated in a resistive load is proportional to the square of the current, or, vice versa, the current through the load is proportional to the square root of the dissipated power:

$$I_R = \sqrt{P_{DISS}/R} \tag{6}$$

where:
I_R is the adaptive photodiode current.
P_{DISS} is the dissipated power from the photodiode.
R is the resistive load from the photodiode.

THEORY OF OPERATION

In a reverse biased photodiode, however, the photon-generated I_{PD} itself is directly proportional to the optical power (P_{OPT}) absorbed in the detector, as shown in the following equation:

$$I_{PD} = \rho \times P_{OPT} \tag{7}$$

where:
ρ is the responsivity (that is, the conversion gain from the optical power to the electrical current.
P_{OPT} is the absorbed optical power.

The proportionality constant ρ, representing the conversion gain from optical power to electrical current, is called the responsivity of the photodiode. Using the same responsivity, the logarithmic intercept current (I_Z) of the TIA can be related to an optical intercept power level (P_Z) for which the ideal log-linear transfer produces an output voltage equal to zero. The transfer from measured optical power to amplifier output voltage can therefore be expressed as the following equation:

$$V_{OUT} = SLOPE \times \log_{10}\left(\frac{P_{OPT}}{P_Z}\right) \tag{8}$$

For incident optical power expressed in dB, Equation 8 becomes Equation 9.

$$P_{OPT,\ dB} = 10 \times \log_{10}(P_{OPT}) \tag{9}$$

$$V_{OUT} = \frac{SLOPE}{10} \times \left(P_{OPT,\ dB} - P_{Z,\ dB}\right) \tag{10}$$

Thus, the logarithmic slope in mV/dB optical power equals twice the logarithmic slope in mV/dB of input current I_{PD} (see Equation 3). Similarly, the optical dynamic range of the TIA in dB equals half the electrical dynamic range in dB, that is, 90 dB optical vs. 180 dB electrical.

PHOTODIODE BIAS

The photodiode bias function maximizes the dynamic range of optical power measurements by minimizing the impact of dark current and series resistance on the measurement accuracy.

Dark current is a small leakage current through the diode that does not change proportionally to the incident optical power, and therefore, limits the sensitivity of an optical power measurement. Because dark current generally increases with the reverse bias voltage, a low reverse bias voltage minimizes the dark current and maximizes the sensitivity of the optical power measurement.

The series resistance introduces measurement errors at high current levels through the photodiode. The voltage drop across this resistance reduces the reverse bias voltage across the photodiode junction itself. A sufficiently high reverse bias voltage, preferably proportional to the diode current to maintain constant reverse bias across the junction, is needed to minimize the impact of the photodiode series resistance.

The photodiode bias function of the ADL5309 adjusts the reverse bias across the photodiode as a function of the current through the

photodiode, as shown in Figure 42. At low photodiode currents, the reverse bias is kept at a specified low-level offset voltage (V_{OS}) to minimize the impact of the dark current. As the photodiode current increases, the reverse bias increases accordingly to minimize the impact of the series resistance. To use this function, the cathode of the photodiode should be connected to the PDB pin.

The ADL5309 photodiode bias can be optimized for specific photodiodes through the I²C interface. The reverse bias level at low input currents V_{OS}, the R_T (that is, the change in bias voltage for a given change in bias current), and the I_{TH} (R_T takes effect when a current is greater than the I_{TH}) can all be adjusted through the I²C interface.

For input currents greater than the I_{TH}, ringing could be observed on the PDB pin due to the positive feedback of the adaptive photodiode bias via the photodiode capacitance. Typically, the frequency of the ringing is around 65 MHz and does not propagate noticeably to the V_{OUT}, because it is attenuated strongly because its bandwidth is much lower. For photodiodes with capacitance less than 8 pF, no sustained ringing (oscillation) is observed even at cold temperatures. It is possible, however, that sustained ringing may occur for photodiodes with larger capacitance. In that case, it is recommended to connect a snubber network consisting of a 10 Ω resistor in series with a 220 pF capacitor between the PDB pin and ground to reduce ringing. The ringing depends on the capacitance of the photodiode vs. the reverse voltage of the photodiode, series resistance, and PCB layout, it is good practice to measure the ringing on the PDB pin using a pulsed optical source that generates an input current greater than I_{TH} to prevent excessive ringing. If needed, the 220 pF capacitor can be scaled up, or the PDBG register contents, which set the R_T, can be scaled down.
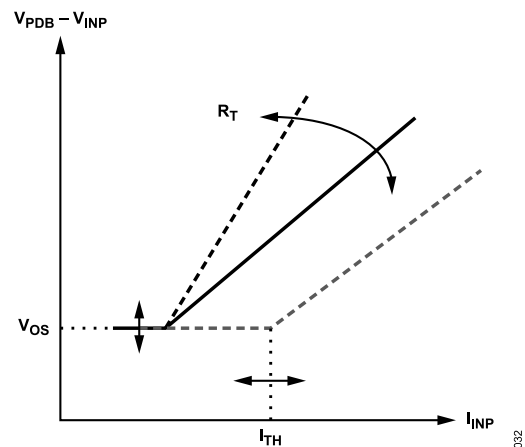
Figure 42. Adaptive Photo Diode Bias Principle of Operation

The R_T can be enabled or disabled (that is, effectively set to zero) through the PDBG_FIX flag in SREG_07 (see Table 9). When disabled (PDBG_FIX = 1), the reverse bias voltage across the diode does not change with the diode current but remains constant over the entire input current range. When enabled (PDBG_FIX = 0), the PDBG bit field adjusts the R_T value in 15.625 Ω steps. An expression for R_T in terms of the SREG_07 register bit fields is

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given in Equation 11. Note that setting either PDBG_FIX = 1 or PDBG = 0 disables the R_T.

$$R_T = 15.625 \times (1 - PDBG\_FIX) \times PDBG \qquad (11)$$

The R_T becomes effective with values greater than the I_{TH}, and the I_{TH} is controlled by PDBG in SREG_07 and IDZ in SREG_08. It can be expressed as the following equation:

$$I_{TH} = 32 \quad \mu A \times \left(\frac{100 \times IDZ - PDBG}{PDBG \times (1 - PDBG\_FIX)} \right) \qquad (12)$$

Because the minimum functional value for IDZ is 1, the smallest value for I_{TH} is obtained for IDZ = 1 and PDBG = 63, resulting in I_{TH} = 18 µA. When PDBG_FIX = 1, I_{TH} becomes infinite, effectively disabling R_T. If IDZ is set to zero, the offset calibration is lost.

The initial bias voltage (or offset voltage) between the PDB pin and the INP pin, can be adjusted using Register SREG_08, Register SREG_0A, and Register SREG_0B. Additionally, the initial bias voltage is dependent on PDBG and PDBG_FIX. The bit field IPDB in Register SREG_08 provides a coarse adjustment in 25 mV steps that is the same for both channels. The contribution of PDBG in SREG_07 is dependent on the state of the PDBG_FIX flag. For input currents less than the I_{TH}, the offset voltage in mV is given by the following equation:

$$V_{OS} = 62.5 \times PDBG \times PDBG\_FIX + 25 \\ \times IPDB + 0.15 \times (OS - 128) \qquad (13)$$

Note that |V_PDB1 − V_INP1| and |V_PDB2 − V_INP2| are minimized in the factory at low input currents for IPDB = 0 and PDBG_FIX = 0 by trimming OS1 and OS2 and therefore V_OS is not necessarily 0 mV for OS1 = OS2 = 128. Further insight into this relationship between bandwidth and input current can be obtained from Figure 21.

BANDWIDTH

The bandwidth of logarithmic TIAs changes with the I_{PD}, resulting in low bandwidth at low input currents that gradually increases to higher bandwidths at higher current levels. In general, bandwidth and gain have an inverse relationship to each other, so increasing the gain of an amplifier typically reduces its bandwidth and vice versa. Logarithmic TIAs are no exception to this rule. Using Equation 1, the small-signal gain (R_T) of a TIA, (that is, the change in output voltage due to a (small) change in I_{PD}) can be expressed as the following equation:

$$Z_t = \frac{dV_{OUT}}{dI_{PD}} = \frac{SLOPE}{\ln(10) \times I_{PD}} \qquad (14)$$

where: Z_t is the small signal gain.

Due to the inherent dynamic range compression by the logarithm, the TIA gain at low input levels is very high, so low bandwidth is to be expected. Similarly, the R_T at high input currents is much lower and expected to result in higher bandwidth. Further insight into this relationship between bandwidth and input current can be obtained from Figure 1, depicting a simplified schematic of a logarithmic TIA.

Usually, the overall topology is a negative feedback amplifier using a diode or the base-emitter junction of a bipolar transistor to establish the logarithmic transfer from I_{IN} to V_{OUT}. Without feedback, that is if the gain of the operational amplifier (op amp) were zero, the impedance (to ground) at the input node would be high. Most of the current from the source should flow into the diode, so a small parasitic capacitance of the photodiode or circuit board has a major impact on the (open-loop) bandwidth of the circuit. The loop gain in the amplifier reduces the impedance at the input node by a factor approximately equal to the loop gain, which is roughly the product of the op amp gain, input impedance, and the feedback diode transconductance. If the loop gain were infinite, the closed-loop input impedance of the TIA would become zero, that is, a virtual ground, and the current through the feedback diode would be precisely equal to the source current (I_S). In a practical amplifier where the op amp has high but finite gain, an increase of the R_T gain (Z_T) corresponds to a decrease of the diode transconductance (which ideally equals the inverse of Z_T), and thus, the amplifier loop gain decreases. In turn, a decrease of the loop gain increases the closed-loop input impedance of the amplifier and (given that the input capacitance is roughly fixed) decreases the amplifier bandwidth. In order to maintain a bandwidth that is as wide as possible, it is critical to minimize capacitive loading of the TIA input pins.

NOISE

The noise level produced by a logarithmic TIA is also dependent on the I_{INP}. The V_{OUT} noise is highest at low input currents (corresponding to the highest small-signal gain), and lowest at high input current levels. Figure 24 and Figure 26 show the spot noise spectral density vs. I_{INP} graph for CF = 0 and CF = 15. For low input currents, one of the most dominant noise sources is the 1/f noise of the input negative channel metal-oxide semiconducter (NMOS). shown in Figure 43, which produces a 1/f noise voltage at the input node.

With a capacitive load at the input, this noise voltage causes an input 1/f noise current and can produce a hill-shaped spot noise spectral density curve. Therefore, it is important to minimize the source capacitance by choosing a photodiode with the lowest possible equivalent parallel capacitance and shortest possible trace to the input node. A trade-off between noise density and bandwidth at low I_{INP} can be made by setting register CF (as shown in Figure 23 and Figure 18) with the minimum bandwidth and lowest noise density for CF = 15 (default) and the maximum bandwidth and highest noise density for CF = 0.

APPLICATIONS INFORMATION

INP1 AND INP2 INTERFACES

The photocurrent input, from the anode of the photodiode, flows into the INP pin. The maximum operating input current is 25 mA.
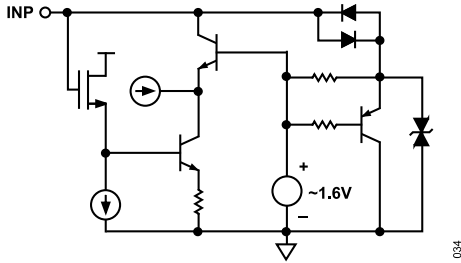

Figure 43. Simplified Input Interface

OUT1 AND OUT2 INTERFACES

The logarithmic V_{OUT} changes logarithmically with the current applied to INP. The nominal slope is 200 mV/dec in the range of 100 pA to 25 mA of the current input over the entire operating temperature.
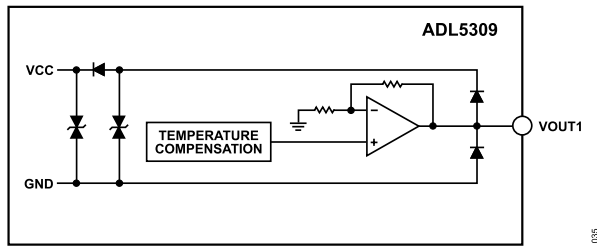

Figure 44. Simplified Output Interface

PDB1 AND PDB2 INTERFACES

The PDB interface pin is shown in Figure 45. The purpose of this pin is to generate a bias voltage to be used with photodiodes.

In an optical system, the photodiode produces an output current proportional to the optical input power. This results in an output dynamic range that is twice (in dB) the optical input power dynamic range and can be high. At low input power, the input current can be small (on the order of pA). With an I_{IN} it is necessary to minimize the dark current leakage of the photodiode by keeping the voltage drop across the diode as small as possible. At higher input powers, the photodiode current can be relatively large (up to 10s of mA). This photocurrent, impressed on the internal series resistance of the diode, results in an increasing voltage drop for increasing optical power.

To address the dark current issue, the ADL5309 provides a photodiode bias that keeps the cathode-to-anode voltage of the photodiode close to zero for low input current, therefore reducing any dark currents. For higher current operation, the photodiode bias interface tracks the input current and produces an output voltage directly proportional to the input current, with the gain adjustable by using the PDBG register. The R_T can be disabled by asserting the

PDBG_FIX bit or setting PDBG = 0. The photodiode bias V_{OUT} is limited by the V_{CC}.
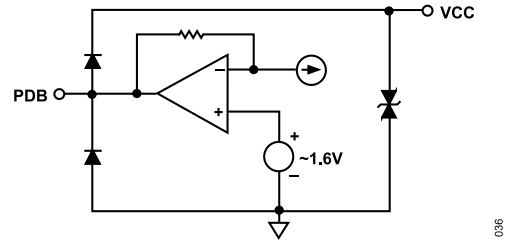
Figure 45. Simplified Photodiode Bias Interface

SUM INTERFACE

A large voltage difference between nodes can cause a significant leakage current, even if the impedance between the nodes is relatively high. Guarding reduces the errors due to leakages. The concept of guarding is to surround the high-impedance conductor with another conductor (guard) driven to the same voltage potential. If there is no voltage across the insulation resistance (between the high-impedance conductor and guard), there can be no current flowing through it.

Reducing errors from external sources in a current-sensing circuit requires a different approach than the voltage sensing input of the typical high-impedance op amp circuit. Leakage can be a significant source of error for highly sensitive logarithmic amplifiers (log amps), especially at the low end of amplifier's range. For example, a 1 GΩ leakage path to the ground from the current line INP with SUM set to the default 1.6 V generates a 1.6 nA offset.

The ADL5309 uses the SUM node as guard pins that shield the input current lines INP. The SUM node has an internal 500 Ω resistor connected to a 1.6 V voltage reference buffer.
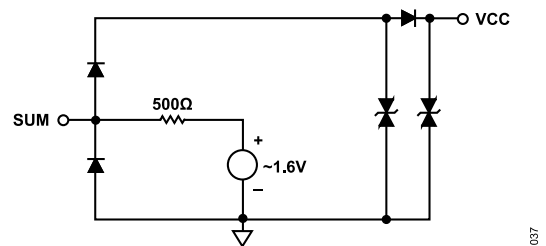
Figure 46. Simplified SUM Interface

ADCREF INTERFACE

The input current measurement accuracy using the internal ADC as illustrated in Figure 5 and Figure 8 can be improved by applying a stable reference voltage to the ADCREF pin. This reference voltage can be sampled by the ADC by setting registers ADCREF_PIN_SEL (0x0A) = 0x2C, ADC_MUX_CTRL (0x04) = 0x08 and ADCREF_MUX_SEL (0x07) = 0x03. An ideal ADC value is calculated by the following equation:

$$ADCREF\_value\_ideal = \frac{V(ADCREF) \times 16383}{2.2} \qquad (15)$$

APPLICATIONS INFORMATION

As an example, applying a 2.000 V reference voltage will result in an ideal ADC value of 14894. By applying a correction value of ADCREF_value_ideal/ADCREF_value for every current measurement and multiplying this with the measured ADC value of the input current by setting ADC_MUX_CTRL (0x04) = 0x02 for Channel 1 and ADC_MUX_CTRL (0x04) = 0x04 for Channel 2. A scaled ADC measurement result, as seen in Figure 6 and Figure 9, improves accuracy.
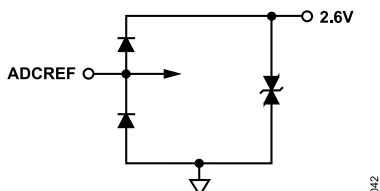
Figure 47. ADCREF Interface

SDA, SCL, AND SBA INTERFACES

Figure 48 shows the bidirectional SDA interface. The SDA output driver is open drain and requires an off-chip pull-up resistor at the receiver. The pull-up resistor can be connected to a maximum positive supply of 5.5 V. During a register write operation, the SDA output driver is high impedance, and the SDA input receiver should be driven by a driver capable of driving the input pin capacitance of 0.8 pF at the 200 kHz maximum SDA frequency. A driver output impedance less than 20 kΩ is recommended.
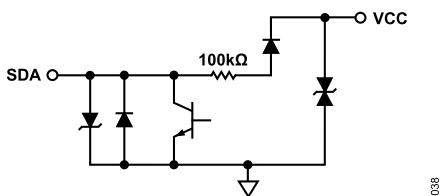
Figure 48. Simplified SDA Interface

Figure 49 shows the SCL interface for the serial clock input to the I²C controller. This input is high impedance and should be driven by a driver capable of driving the input pin capacitance of 0.8 pF at the 400 kHz maximum SCL frequency. A driver output impedance less than 10 kΩ is recommended.
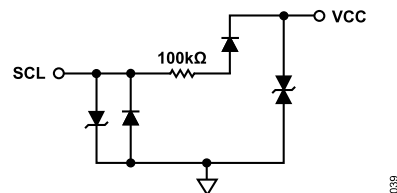
Figure 49. Simplified SCL Interface

Figure 50 shows the SBA Interface A voltage source applied to SCL sets the I²C bus device address to one of three possible settings. These settings include connecting the pin to V_{CC} for a device address of 0x6E, leaving the pin floating for a device address of 0x6D, or connecting the pin to ground for a device address of 0x6C. A source impedance of 10 kΩ or less is recommended for this pin.
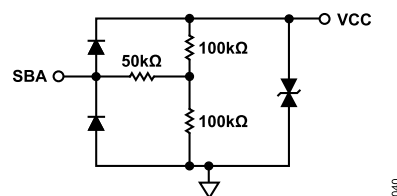
Figure 50. Simplified SBA Interface

SERIAL PORT INTERFACE

PROTOCOL

The ADL5309 can be connected to an I^2C bus interface as a target device to control and monitor several internal (analog) functions. Up to three ADL5309 devices can be connected to the same I^2C bus, each with its own unique device address. See Table 2 for detailed timing requirements. Data is transferred one byte at a time, with the MSB first. Each instruction consists of one address byte, followed by one or more data bytes. The ADL5309 supports single-byte read and write methods, as well as autoincrement read/write instructions.

ADDRESS SELECTION

The ADL5309 I^2C device address can be selected from three choices by connecting the SBA pin to either ground, the positive supply, or by leaving the pin floating (see Table 1). The I^2C address selected through the SBA pin can also be read from Register 0x01. The selected 7-bit device address is followed by one read/ write LSB address bit. The LSB address bit equals '0' for a write instruction and '1' for a read instruction. For example, the write address corresponding to the I^2C device Address 0x6C is obtained by adding an LSB = 0, equivalent to a left-shift of one bit position (multiply-by-two), resulting in 0xD8. The bus read address equals the write address with the LSB changed from '0' to '1', which equals 0xD9.

SUPPORTED READ AND WRITE METHODS

The ADL5309 supports several I^2C read and write methods:

▶ Read/write a single register
▶ Read/write multiple registers in a single operation through auto-increment
▶ Read/write a single shadow register using indirect addressing

Figure 51 summarizes the procedure for each method. Each transaction on the I^2C bus is initiated by the controller and starts with sending a start condition, a high to low transition on the SDA line while SCK is high. Subsequently, the 8-bit device address (of the selected target) is transmitted, one bit per SCK clock pulse. All addresses and data are transmitted over the bus with the MSB first.

The ninth clock pulse is reserved to transmit the ACK (acknowledge) signal from the target to the controller to indicate that the address was received. To send an ACK, the target pulls the SDA line low. A NACK (not acknowledge) results if the SDA line remains high. Depending on the transaction, a series of byte read/write transfers follow, each ending with an ACK or NACK bit. The transaction ends with a stop condition sent by the controller and a low to high transition on the SDA line while SCK is high.

The autoincrement feature provides read/write access to multiple consecutive registers in a single transaction. Each data byte is read from/written to the next register, with address one higher than the previous.

The indirect addressing methods are used to access the ADL5309 shadow registers, as explained in more detail in the Shadow Access Registers section.

DIRECT WRITE:
START | DEVICE ADDRESS | ACK | REGISTER ADDRESS | ACK | WRITE DATA | ACK | STOP

DIRECT WRITE – AUTO INCREMENT:
START | DEVICE ADDRESS | ACK | REGISTER ADDRESS | ACK | WRITE DATA | ACK | WRITE DATA (n) | ACK | STOP

DIRECT READ:
START | DEVICE ADDRESS | ACK | REGISTER ADDRESS | ACK | START | DEVICE ADDRESS | ACK | READ DATA | NACK | STOP

DIRECT READ – AUTO INCREMENT:
START | DEVICE ADDRESS | ACK | REGISTER ADDRESS | ACK | START | DEVICE ADDRESS | ACK | READ DATA | ACK | READ DATA (N) | NACK | STOP

INDIRECT READ:
START | DEVICE ADDRESS | ACK | 0x83 | ACK | SHADOW ADDRESS | ACK | STOP
START | DEVICE ADDRESS | ACK | 0x84 | ACK | START | DEVICE ADDRESS | ACK | READ SHADOW DATA | NACK | STOP

INDIRECT WRITE:
START | DEVICE ADDRESS | ACK | 0x80 | ACK | SHADOW ADDRESS | ACK | WRITE SHADOW DATA | ACK | 0x01 | ACK | STOP
START | DEVICE ADDRESS | ACK | 0x82 | ACK | 0x00 | ACK | STOP

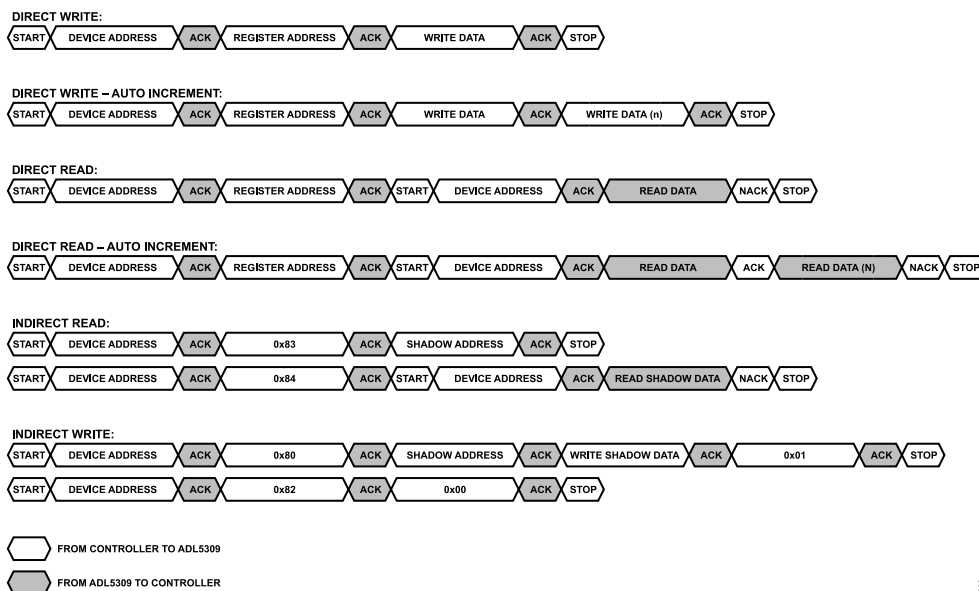☐ FROM CONTROLLER TO ADL5309
▨ FROM ADL5309 TO CONTROLLER

Figure 51. ADL5309 Serial Bus Read/Write Sequences

SERIAL PORT INTERFACE

RESET, ADDRESS, AND ID REGISTERS

Table 7. ADL5309 RESET, ADDRESS, AND ID Registers Details

Address	Name	Bits	Field Name	Description	Default	Access
0x00	REG_00	0	SOFTRESET	Writing '1' to this bit resets all registers to their default values.	0x0	R/W
0x01	REG_01	[6:0]	DEVICE_ADDRESS	Active I^{2}C device address, selected through the SBA pin. Voltage level. Refer to Table 1.	0x6X	R
0x0D	REG_0D	[7:0]	CHIP_ID	ID for ADL5309.	0x6C	R

ADC REGISTERS

The ADL5309 has a built-in 14-bit, 22 kSPS ADC that samples any combination of three input data streams, including the following:

▶ V_{OUT} of Channel 1
▶ V_{OUT} of Channel 2
▶ Built-in temperature sensor

Register REG_05 and Register REG_06 support streaming of the ADC output words and behave differently from the other registers in the map. By using the I^{2}C read method with autoincrement to read REG_05, multiple ADC samples can be read in a single operation. If 2 bytes are read, then the MSB in REG_05 will be read first, followed by the LSB in REG_06. If more than 2 bytes are read, however, the address pointer is moved back to REG_05 and the MSB of the next ADC sample is read. In this way, an autoincrement read of 10 bytes starting from REG_05 will return five sequential 2-byte ADC words read from REG_05 and REG_06.

The ADC can digitize samples from up to three different input streams, selected through the MUX_CTRL bit field in REG_04. Writing a nonzero value to MUX_CTRL initiates the ADC multi-stream, multisample read operation. One sample is digitized from each active input stream at a time, then the next input stream is digitized, starting with the active stream corresponding to the lowest significant bit in MUX_CTRL. Thus in order to retrieve *n* samples from a single input stream, a total of 2*n* bytes need to be read. If more than one input stream is selected the first active input stream sample is repeated, and can be disregarded, bringing the total bytes to read to 2*m*n+2, where m = number of input streams.

The performance using the ADC can be improved when using multiple samples to average and using the on-chip dither. Writing 0x1F to REG_08 will enable 32-bit dither, and writing 0x2F to REG_08 will enable 64-bit dither. Writing 0x3F to REG_08 will enable both 32-bit and 64-bit dither bits. The default value of REG_08 is 0x03, for which the dither is disabled.

SERIAL PORT INTERFACE

Table 8. ADL5309 ADC Register Details

Address	Name	Bits	Field Name	Description	Default	Access
0x04	REG_04	4	ADC_BUSY	Equals '1' if a conversion is in progress. REG_05 and REG_06 always contain the result of the last completed conversion.	0x0	R
		[3:0]	MUX_CTRL	Selects the ADC input stream(s) to digitize by setting the corresponding bit to '1', as follows: ▶ Bit 0: digital thermometer ▶ Bit 1: V_{OUT} of Channel 1 ▶ Bit 2: V_{OUT} of Channel 2 ▶ Bit 3: ADCREF Test Input The ADC cycles sequentially through all active input streams, taking one 14-bit sample for each at a time.	0x0	R/W
0x05	REG_05	[5:0]	ADC_DATA[13:8]	MSB of ADC data	0x00	R
0x06	REG_06	[7:0]	ADC_DATA[7:0]	LSB of ADC data	0x00	R
0x08	REG_08	[5:0]	ADC_CONF	ADC dither configuration register as follows: ▶ Write 0x1F to enable 32-bit dither ▶ Write 0x2F to enable 64-bit dither ▶ Write 0x3F to enable both 32-bit and 64-bit dither ▶ Write 0x03 to disable dither	0x03	R/W
0x07	REG_07	[3:0]	AD-CREF_MUX_SEL	ADCREF MUX select. To use ADCREF input, set this to 0x3.	0x0	R/W
0x09	REG_09	1	ADC_RESET	Setting this bit to '1' restarts the A/D conversion.	0x0	R/W
		0	ADC_ENABLE	ADC is enabled when set to '1'.	0x1	R/W
0x0A	REG_0A	[4:3]	ADCREF_PIN_SEL	ADCREF PIN select. To use ADCREF input, set this to 0x1.	0x0	R/W

SERIAL PORT INTERFACE

SHADOW REGISTERS

The shadow registers enable detailed configuration of the adaptive photodiode bias circuits in both channels, enabling more advanced features than the default settings provide. Access to these registers is provided through an indirect addressing method using the shadow access registers (see the Shadow Access Registers section). Table 9 summarizes the available registers. For a detailed explanation of available photodiode bias configuration see the Photodiode Bias section. By default, the shadow registers are locked and accessible for read only. To unlock the registers and obtain write access, first write 0xE5 to SREG_20 (using indirect addressing). The unlocked state will remain in effect until these are locked again by writing 0x00 to SREG_20, or a (soft) reset is issued.

Table 9. ADL5309 Shadow Register Details

Address	Name	Bits	Field Name	Description	Default	Access
0x07	SREG_07	6	PDBG_FIX	Photodiode bias transresistance is disabled (effectively set to zero) if this bit is set, making the photodiode bias voltage constant vs. input current.	0x00	R/W
		[5:0]	PDBG	Photodiode bias transresistance control when PDBG_FIX is not set, coarse photodiode bias voltage control when PDBG_FIX is set.		
0x08	SREG_08	[7:4]	IDZ	Photodiode bias transresistance threshold control.	0x00	R/W
		[3:0]	IPDB	Controls the photodiode bias voltage of both channels at zero input current in 25 mV steps.		
0x0A	SREG_0A	[7:0]	OS1	Channel 1 V_PDB - V_INP offset control in 150 µV steps.	0xXX	R/W
0x0B	SREG_0B	[7:0]	OS2	Channel 2 V_PDB - V_INP offset control in 150 µV steps.	0xXX	R/W
0x0C	SREG_0C	[7:4]	IMAX	The IMAX register (four MSBs in shadow register 0x0C) sets the maximum sourcing current of the PDB pin. It is trimmed in the factory to about 30 mA. If the IMAX is changed, it may affect the precision of the OS factory trims (Shadow Register 0x0A and Shadow Register 0x0B) and is recommended to be re-calibrated.	0xXF	R/W
		[3:0]	CF	Capacitor feedback. Sets low input current bandwidth.		R/W
0x20	SREG_20	[7:0]	UNLOCK	Write 0xE5 to unlock for read/write, and write 0x00 to lock shadow registers for read-only.	0x00	R/W

SERIAL PORT INTERFACE

SHADOW ACCESS REGISTERS

The registers at Address 0x80 through Address 0x84 listed in Table 10 are used to access the shadow registers listed in Table 9 through an indirect addressing method.

To read a shadow register, its address first has to be written to REG_83. Then, the data can be read from REG_84. In order to enable a write operation, the shadow registers first need to be

unlocked by writing 0xE5 to SREG_20 through an indirect write. To perform an indirect write, use the autoincrement write method to write the shadow register address to REG_80, the data to be written to REG_81, and finally, set the WRITE_ENBL flag by writing 0x01 to REG_82, all in a single transaction. Subsequently, in a new write operation, clear the WRITE_ENBL bit by writing 0x00 to REG_82.

Table 10. ADL5309 Shadow Access Register Details

| Address	Name	Bits	Bit Name	Description	Default	Access
0x80	REG_80	[7:0]	WRITE_ADDR	Address of shadow register to write	0x00	R/W
0x81	REG_81	[7:0]	WRITE_DATA	Data to write to shadow register specified in register 0x80	0x00	R/W
0x82	REG_82	0	WRITE_ENBL	Set to '1' to enable a write to REG_80, REG_81	0x00	R/W
0x83	REG_83	[7:0]	READ_ADDR	Address of shadow register to read	0x00	R/W
0x84	REG_84	[7:0]	READ_DATA	Data read from shadow register specified in register 0x83.	0x00	R

EVALUATION BOARD SCHEMATIC
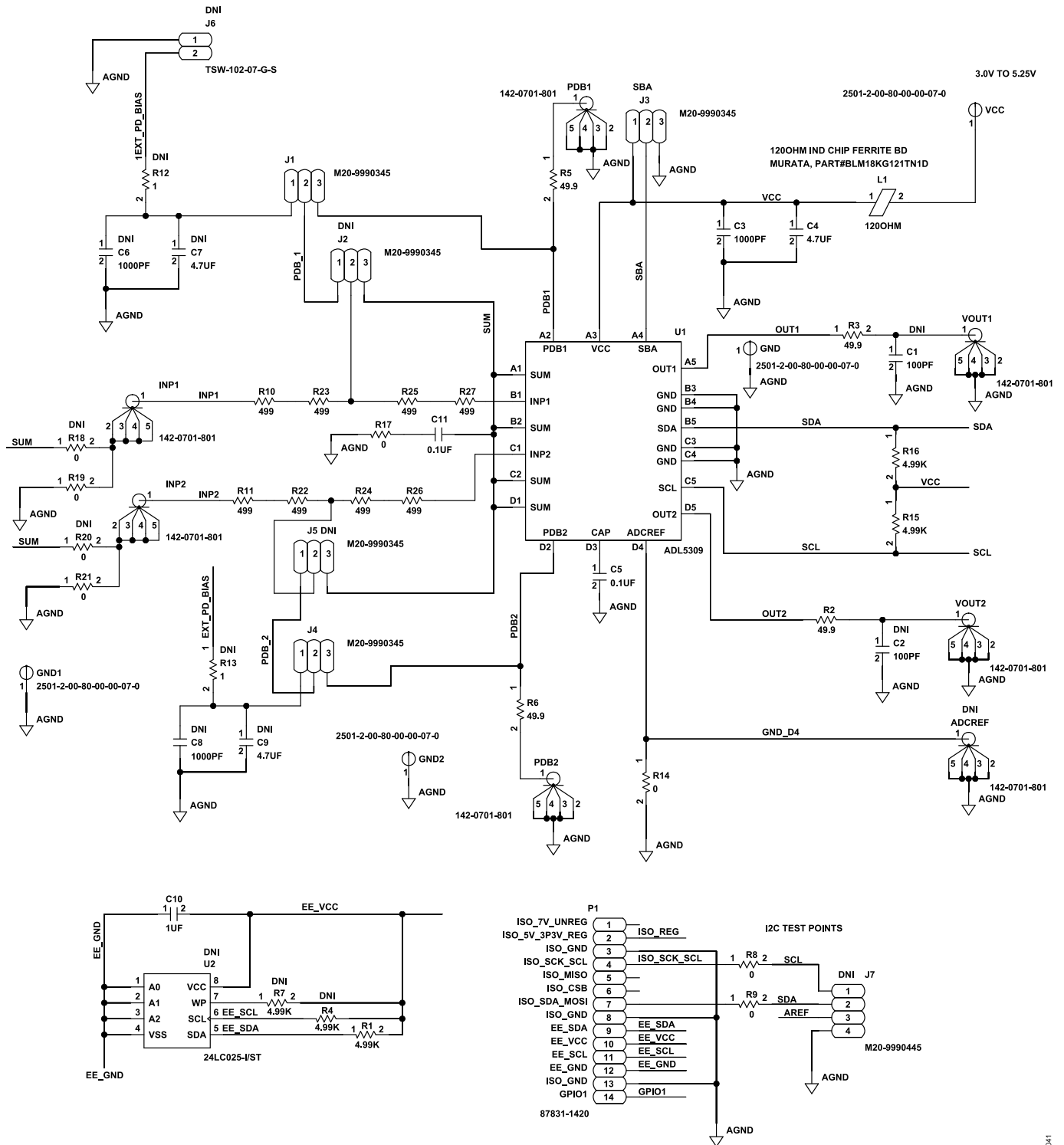
Figure 52. Evaluation Board Schematic

OUTLINE DIMENSIONS
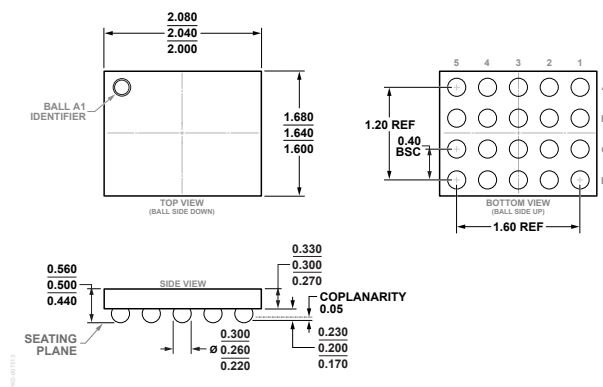
Figure 53. 20-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-20-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL5309ACBZ	−40°C to +105°C	20-Ball WLCSP (2.040 mm × 1.640 mm)	Tape, 3000	CB-20-16
ADL5309ACBZ-R7	−40°C to +105°C	20-Ball WLCSP (2.040 mm × 1.640 mm)	Reel, 3000	CB-20-16
ADL5309ACBZ-RL	−40°C to +105°C	20-Ball WLCSP (2.040 mm × 1.640 mm)	Reel, 5000	CB-20-16

[1] Z = RoHS Compliant Part.

EVALUATION BOARD

Table 11. Evaluation Board

Model[1, 2, 3]	Description
ADL5309-EVALZ	Evaluation Board
ADL5309-KIT-EVALZ	Evaluation Board Kit

[1] Z = RoHs Compliant Part.

[2] The ADL5309-EVALZ package includes the evaluation board only.

[3] A DC2026C Linduino One controller board is included with the ADL5309-KIT-EVALZ.