Data Sheet

ADA4510-2

Precision, 40 V, ±70 nV/°C, Rail-to-Rail Input and Output Op Amp with DigiTrim

FEATURES

- Low offset voltage drift: ±70 nV/°C typical
- Low offset voltage: ±5 µV typical, ±20 µV maximum
- Low voltage noise: 1 µV p-p from 0.1 Hz to 10 Hz typical
- Low voltage noise density: 5 nV/√Hz typical at f = 1 kHz
- High common-mode rejection: 140 dB typical
- Low input bias current: ±10 pA maximum
- Wide gain bandwidth product: 10.4 MHz typical
- High slew rate: 19 V/µs typical
- Low THD: −134 dB at f = 1 kHz
- Low quiescent supply current: 1.45 mA per amplifier typical
- Wide supply voltage operation: 6 V to 40 V, ±3 V to ±20 V
- Integrated EMI filter
- Multiplexer compatible inputs
  - Rail-to-rail high impedance: differential and common-mode
  - Fast settling time
- Rail-to-rail and output
- No phase reversal
- Heavy capacitive load drive capability: 1 nF
- Wide specified temperature range: −40°C to +125°C
- Available in 8-lead, SOIC_N and 8-lead, MSOP packages

APPLICATIONS

- Multiplexed data acquisition systems
- Electronic test and measurement
- Automated test equipment
- Medical instruments
- Energy monitoring
- Precision current sensing and precision buffer
- Transimpedance amplifiers

GENERAL DESCRIPTION

The ADA4510-2[1] is a dual-channel, 40 V, high precision, low input bias current, low offset voltage, low offset voltage drift, low noise, rail-to-rail input and output operational amplifier that can be used at any point of the signal chain, including sensing, conditioning, and output drive. Through the use of Analog Devices, Inc., proprietary DigiTrim™ technique, the ADA4510-2 achieves best-in-class low offset drift (±70 nV/°C typical, ±500 nV/°C maximum) and low offset voltage (±5 µV typical, ±20 µV maximum), simplifying temperature calibrations in precision designs.

The ADA4510-2 delivers excellent DC precision and outstanding AC performance, making it a top choice for a wide variety of signal chain applications. By integrating a robust mux-compatible architecture, the ADA4510-2 effectively solves common system distortion and settling problems and provides the superior accuracy required in multiplexed multichannel precision signal chains. The ADA4510-2 is specified from −40°C to +85°C and −40°C to +125°C and is available in an 8-lead, SOIC_N and 8-lead, MSOP.

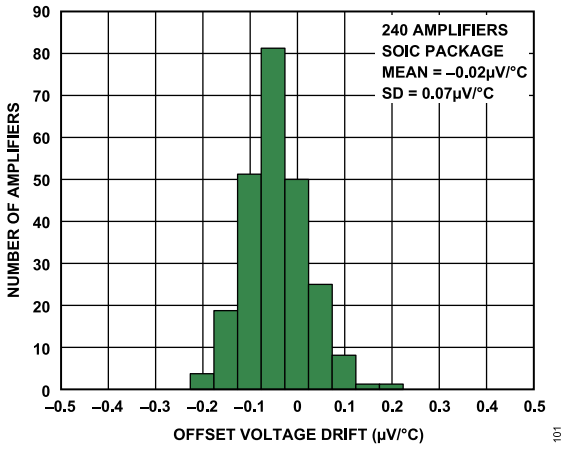

Figure 1. Ultralow Offset Voltage Drift for Precision Design

TYPICAL APPLICATION CIRCUIT

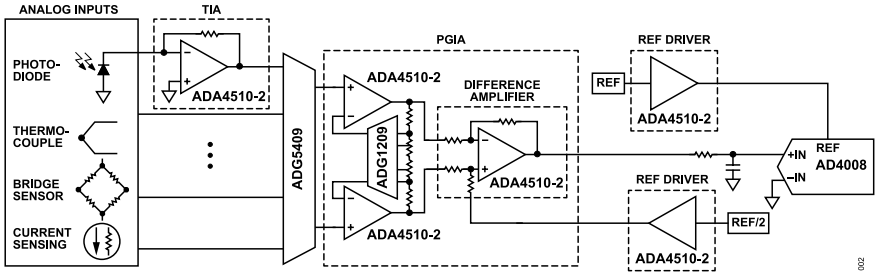

Figure 2. Multiplexed Data Acquisition Signal Chain

[1] Protected by U.S. patent number 11,329,612; other patents pending.

Rev. B

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

TABLE OF CONTENTS

REVISION HISTORY

6/2024—Rev. A to Rev. B

Added 8-Lead, MSOP Package (Universal) ... 1
Changes to Features Section ... 1
Changes to Applications Section ... 1
Changes to Companion Products Section ... 3
Changes to Table 1 ... 4
Changes to Table 2 ... 6
Changes to Table 3 ... 9
Changes to Table 4 ... 9
Changes to Typical Performance Characteristics Section ... 11
Added Figure 9; Renumbered Sequentially ... 11
Added Figure 10, Figure 11, and Figure 14 ... 12
Added Figure 27 ... 14
Added Figure 32 ... 15
Added Solder Heat Effect Section and Figure 92 ... 30
Updated Outline Dimensions ... 32
Changes to Ordering Guide ... 32
Changes to Evaluation Boards ... 32

10/2023—Rev. 0 to Rev. A

Changes to Data Sheet Title ... 1
Changes to Features Section ... 1
Changes to General Description Section ... 1
Changes to Offset Voltage Drift ($\Delta V_{OS}/\Delta T$) Parameter, Table 1 ... 4
Changes to Figure 65 ... 22
Change to Design Example Section ... 26

7/2023—Revision 0: Initial Version

COMPANION PRODUCTS

- **ADC:** AD4695/AD4696, AD4697/AD4698, AD4002/AD4006/AD4010, AD4000/AD4004/AD4008
- **ADC Drivers:** ADA4945-1, AD8475
- **DAC:** AD5791, AD3551R
- **Voltage References:** LTC6655, ADR4525
- **Power:** LT3032, ADP5070, LT3093, LT3042

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS FOR T_A = −40°C TO +85°C

Supply voltage (V_{SY}) = (V+) − (V−) = ±3 V to ±20 V, common-mode voltage (V_{CM}) = 0 V, load resistor (R_L) = 10 kΩ to midsupply, unless otherwise noted.

Table 1. Electrical Specifications for T_A = −40°C to +85°C

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Offset Voltage (V_{OS})[1]	V_{CM} = 0 V, T_A = 25°C		±5	±20	µV
	0°C < T_A < +85°C, SOIC_N			±40	µV
	0°C < T_A < +85°C, MSOP			±50	µV
	−40°C < T_A < +85°C			±50	µV
	V_{CM} = (V+) − 1.5 V, T_A = 25°C		±10	±40	µV
	0°C < T_A < +85°C, SOIC_N			±60	µV
	0°C < T_A < +85°C, MSOP			±80	µV
	−40°C < T_A < +85°C, SOIC_N			±120	µV
	−40°C < T_A < +85°C, MSOP			±140	µV
	V_{CM} = (V−) − 0.15 V, T_A = 25°C		±8	±35	µV
	0°C < T_A < +85°C			±90	µV
	−40°C < T_A < +85°C			±110	µV
Offset Voltage Drift ($\Delta V_{OS}/\Delta T$)	V_{CM} = 0 V				
	0°C < T_A < +85°C, SOIC_N		±0.07	±0.5	µV/°C
	0°C < T_A < +85°C, MSOP		±0.14	±0.7	µV/°C
	−40°C < T_A < +85°C, SOIC_N		±0.12	±0.5	µV/°C
	−40°C < T_A < +85°C, MSOP		±0.15	±0.75	µV/°C
	V_{CM} = (V+) − 1.5 V				
	0°C < T_A < +85°C, SOIC_N		±0.1	±0.7	µV/°C
	0°C < T_A < +85°C, MSOP		±0.16	±0.9	µV/°C
	−40°C < T_A < +85°C, SOIC_N		±0.15	±1.0	µV/°C
	−40°C < T_A < +85°C, MSOP		±0.18	±1.2	µV/°C
Input Bias Current (I_B)	T_A = 25°C		±2.5	±10	pA
	−40°C < T_A < +85°C			±0.8	nA
Input Offset Current (I_{OS})	T_A = 25°C		±0.5	±5	pA
	−40°C < T_A < +85°C			±0.15	nA
Input Voltage Range (IVR)	Guaranteed by CMRR	(V−) − 0.15		V+	V
Common-Mode Rejection Ratio (CMRR)	−20.15 V < V_{CM} < 17 V, T_A = 25°C	121	140		dB
	−40°C < T_A < +85°C	118			dB
	−20.15 V < V_{CM} < 20 V, T_A = 25°C	100	112		dB
	−40°C < T_A < +85°C	100			dB
		99			dB
Open-Loop Voltage Gain (A_{VOL})	R_L = 10 kΩ, −19.7 V < V_{OUT} < 19.7 V, T_A = 25°C	126	140		dB
	−40°C < T_A < +85°C	124			dB
	R_L = 2 kΩ, −19.1 V < V_{OUT} < 19.1 V, T_A = 25°C	121	134		dB
	−40°C < T_A < +85°C	120			dB
Input Capacitance					
Differential Mode (C_{INDM})	T_A = 25°C		20		pF
Common Mode (C_{INCM})	T_A = 25°C, V_{SY} = ±5 V to ±20 V		2		pF
Input Resistance					
Differential Mode (R_{INDM})	T_A = 25°C		1		TΩ
Common Mode (R_{INCM})	T_A = 25°C		10		TΩ

SPECIFICATIONS

Table 1. Electrical Specifications for T_A = −40°C to +85°C (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE					
Voltage Noise ($e_{n\ p-p}$)	0.1 Hz to 10 Hz, T_A = 25°C		1		µV p-p
	0.1 Hz to 10 Hz, V_{CM} = (V+) − 1.5 V, T_A = 25°C		2.7		µV p-p
Voltage Noise Density (e_n)	f = 100 Hz, T_A = 25°C		8		nV/√Hz
	f = 1 kHz, T_A = 25°C		5		nV/√Hz
	f = 100 Hz, V_{CM} = (V+) − 1.5 V, T_A = 25°C		20		nV/√Hz
	f = 1 kHz, V_{CM} = (V+) − 1.5 V, T_A = 25°C		10		nV/√Hz
Current Noise Density (I_n)	f = 10 Hz, T_A = 25°C		4		fA/√Hz
OUTPUT CHARACTERISTICS					
Output Swing High (V_{OH})	((V+) − V_{OUT})				
	R_L = 10 kΩ, T_A = 25°C		100	116	mV
	−40°C < T_A < +85°C			160	mV
	R_L = 2 kΩ, T_A = 25°C		430	473	mV
	−40°C < T_A < +85°C			655	mV
Output Swing Low (V_{OL})	(V_{OUT} − (V−))				
	R_L = 10 kΩ, T_A = 25°C		73	85	mV
	−40°C < T_A < +85°C			120	mV
	R_L = 2 kΩ, T_A = 25°C		310	342	mV
	−40°C < T_A < +85°C			487	mV
Output Current (I_{OUT})	(V_{OH}, V_{OL}) < 1 V, T_A = 25°C		±22		mA
Short-Circuit Current (I_{SC})	Sourcing/sinking, T_A = 25°C		55/70		mA
Closed-Loop Output Impedance (Z_{OUT})	f = 1 kHz , T_A = 25°C				
	Gain = 1		19		mΩ
	Gain = 10		190		mΩ
	Gain = 100		1.9		Ω
Open-Loop Output Impedance (Z_O)	f = 1 kHz to 1 MHz, T_A = 25°C		190		Ω
POWER SUPPLY					
V_{SY} ((V+) − (V−))	Guaranteed by PSRR	6		40	V
Power Supply Rejection Ratio (PSRR)	V_{SY} = ±3 V to ±20 V, T_A = 25°C	121	140		dB
	−40°C < T_A < +85°C	117			dB
Supply Current per Amplifier (I_{SY})	I_{OUT} = 0 mA, T_A = 25°C		1.45	1.55	mA
	−40°C < T_A < +85°C			1.85	mA
DYNAMIC PERFORMANCE					
Slew Rate	V_{OUT} = ±5 V, gain = +1, 10% to 90%, T_A = 25°C		19		V/µs
Gain Bandwidth Product (GBP)	f = 100 kHz, T_A = 25°C		10.4		MHz
−3 dB Bandwidth	Gain = 1, T_A = 25°C		13.5		MHz
Settling Time (t_S)	T_A = 25°C				
	To 0.01%				
	Gain = −1, V_{OUT} = 5 V step		1.9		µs
	Gain = −1, V_{OUT} = 10 V step		2.2		µs
	To 0.001%				
	Gain = −1, V_{OUT} = 5 V step		3.1		µs
	Gain = −1, V_{OUT} = 10 V step		3.5		µs
Output Overload Recovery Time	Gain = −10, T_A = 25°C, positive/negative		300/100		ns

SPECIFICATIONS

Table 1. Electrical Specifications for T_A = −40°C to +85°C (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Total Harmonic Distortion (THD)	V_{OUT} = 10 V p-p, gain = 1, T_A = 25°C				
	f = 1 kHz		0.00002		%
	f = 1 kHz		−134		dB
	f = 50 kHz		0.0045		%
	f = 50 kHz		−87		dB
ELECTROMAGNETIC INTERFERENCE REJECTION RATIO (EMIRR)	EMIRR = 20 × $\log_{10}(\Delta V_{IN}/\Delta V_{OS})$, ΔV_{IN} = 200 mV p-p, T_A = 25°C				
	f = 1000 MHz		71		dB
	f = 2400 MHz		81		dB
CROSSTALK	V_{IN} = 4 V p-p, T_A = 25°C				
	DC		165		dB
	f = 1 kHz		164		dB
	f = 100 kHz		130		dB

[1] In rare cases, solder reflow can cause a non permanent V_{os} shift. See the Applications Information section for information regarding maintaining the specified V_{os} performance after soldering.

ELECTRICAL SPECIFICATIONS FOR T_A = −40°C TO +125°C

Supply voltage (V_{SY}) = (V+) − (V−) = ±3 V to ±20 V, common-mode voltage (V_{CM}) = 0 V, load resistor (R_L) = 10 kΩ to midsupply, unless otherwise noted.

Table 2. Electrical Specifications for T_A = −40°C to +125°C

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Offset Voltage (V_{OS})[1]	V_{CM} = 0 V, T_A = 25°C		±5	±20	µV
	−40°C < T_A < +125°C, SOIC_N			±100	µV
	−40°C < T_A < +125°C, MSOP			±140	µV
	V_{CM} = (V+) − 1.5 V, T_A = 25°C		±10	±40	µV
	−40°C < T_A < +125°C, SOIC_N			±380	µV
	−40°C < T_A < +125°C, MSOP			±430	µV
	V_{CM} = V−, T_A = 25°C		±9	±35	µV
	−40°C < T_A < +125°C			±160	µV
Offset Voltage Drift ($\Delta V_{OS}/\Delta T$)	V_{CM} = 0 V				
	−40°C < T_A < +125°C, SOIC_N		±0.12	±0.7	µV/°C
	−40°C < T_A < +125°C, MSOP		±0.15	±0.9	µV/°C
	V_{CM} = (V+) − 1.5 V				
	−40°C < T_A < +125°C		±0.5	±2.4	µV/°C
Input Bias Current (I_B)	T_A = 25°C		±2.5	±10	pA
	−40°C < T_A < +125°C, SOIC_N			±18	nA
	−40°C < T_A < +125°C, MSOP			±45	nA
Input Offset Current (I_{OS})	T_A = 25°C		±0.5	±5	pA
	−40°C < T_A < +125°C			±5	nA
Input Voltage Range (IVR)	Guaranteed by CMRR	V−		V+	V
Common-Mode Rejection Ratio (CMRR)	−20 V < V_{CM} < 17 V, T_A = 25°C	121	140		dB
	−40°C < T_A < +125°C	109			dB
	−20 V < V_{CM} < 20 V, T_A = 25°C	100	112		dB
	−40°C < T_A < +125°C	95			dB

SPECIFICATIONS

Table 2. Electrical Specifications for T_A = −40°C to +125°C (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Open-Loop Voltage Gain (A_{VOL})	R_L = 10 kΩ, −19.7 V < V_{OUT} < 19.7 V, T_A = 25°C	126	140		dB
	−40°C < T_A < +125°C	112			dB
	R_L = 2 kΩ, −19.1 V < V_{OUT} < 19.1 V, T_A = 25°C	121	134		dB
	−40°C < T_A < +125°C	106			dB
Input Capacitance					
Differential Mode (C_{INDM})	T_A = 25°C		20		pF
Common Mode (C_{INCM})	T_A = 25°C, V_{SY} = ±5 V to ±20 V		2		pF
Input Resistance					
Differential Mode (R_{INDM})	T_A = 25°C		1		TΩ
Common Mode (R_{INCM})	T_A = 25°C		10		TΩ
NOISE PERFORMANCE					
Voltage Noise ($e_{n\ p-p}$)	0.1 Hz to 10 Hz, T_A = 25°C		1		μV p-p
	0.1 Hz to 10 Hz, V_{CM} = (V+) − 1.5 V, T_A = 25°C		2.7		μV p-p
Voltage Noise Density (e_n)	f = 100 Hz, T_A = 25°C		8		nV/√Hz
	f = 1 kHz, T_A = 25°C		5		nV/√Hz
	f = 100 Hz, V_{CM} = (V+) − 1.5 V, T_A = 25°C		20		nV/√Hz
	f = 1 kHz, V_{CM} = (V+) − 1.5 V, T_A = 25°C		10		nV/√Hz
Current Noise Density (I_n)	f = 10 Hz, T_A = 25°C		4		fA/√Hz
OUTPUT CHARACTERISTICS					
Output Swing High (V_{OH})	((V+) − V_{OUT})				
	R_L = 10 kΩ, T_A = 25°C		100	116	mV
	−40°C < T_A < +125°C			187	mV
	R_L = 2 kΩ, T_A = 25°C		430	473	mV
	−40°C < T_A < +125°C			765	mV
Output Swing Low (V_{OL})	(V_{OUT} − (V−))				
	R_L = 10 kΩ, T_A = 25°C		73	85	mV
	−40°C < T_A < +125°C			142	mV
	R_L = 2 kΩ, T_A = 25°C		310	342	mV
	−40°C < T_A < +125°C			573	mV
Output Current (I_{OUT})	(V_{OH}, V_{OL}) < 1 V, T_A = 25°C		±22		mA
Short-Circuit Current (I_{SC})	Sourcing/sinking, T_A = 25°C		55/70		mA
Closed-Loop Output Impedance (Z_{OUT})	f = 1 kHz , T_A = 25°C				
	Gain = 1		19		mΩ
	Gain = 10		190		mΩ
	Gain = 100		1.9		Ω
Open-Loop Output Impedance (Z_O)	f = 1 kHz to 1 MHz, T_A = 25°C		190		Ω
POWER SUPPLY					
V_{SY} ((V+) − (V−))	Guaranteed by PSRR	6		40	V
Power Supply Rejection Ratio (PSRR)	V_{SY} = ±3 V to ±20 V, T_A = 25°C	121	140		dB
	−40°C < T_A < +125°C	116			dB
Supply Current per Amplifier (I_{SY})	I_{OUT} = 0 mA, T_A = 25°C		1.45	1.55	mA
	−40°C < T_A < +125°C			2	mA
DYNAMIC PERFORMANCE					
Slew Rate	V_{OUT} = ±5 V, gain = 1, 10% to 90%, T_A = 25°C		19		V/μs
Gain Bandwidth Product (GBP)	f = 100 kHz, T_A = 25°C		10.4		MHz
−3 dB Bandwidth	Gain = 1, T_A = 25°C		13.5		MHz

SPECIFICATIONS

Table 2. Electrical Specifications for T_A = −40°C to +125°C (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Settling Time (t_S)	T_A = 25°C				
	To 0.01%				
	Gain = −1, V_{OUT} = 5 V step		1.9		µs
	Gain = −1, V_{OUT} = 10 V step		2.2		µs
	To 0.001%				
	Gain = −1, V_{OUT} = 5 V step		3.1		µs
	Gain = −1, V_{OUT} = 10 V step		3.5		µs
Output Overload Recovery Time	Gain = −10, T_A = 25°C, positive/negative		300/100		ns
Total Harmonic Distortion (THD)	V_{OUT} = 10 V p-p, gain = 1, T_A = 25°C				
	f = 1 kHz		0.00002		%
	f = 1 kHz		−134		dB
	f = 50 kHz		0.00445		%
	f = 50 kHz		−87		dB
ELECTROMAGNETIC INTERFERENCE REJECTION RATIO (EMIRR)	EMIRR = 20 × $\log_{10}(\Delta V_{IN}/\Delta V_{OS})$, ΔV_{IN} = 200 mV p-p, T_A = 25°C				
	f = 1000 MHz		71		dB
	f = 2400 MHz		81		dB
CROSSTALK	V_{IN} = 4 V p-p, T_A = 25°C				
	DC		165		dB
	f = 1 kHz		164		dB
	f = 100 kHz		130		dB

[1] In rare cases, solder reflow can cause a non permanent V_{os} shift. See the Applications Information section for information regarding maintaining the specified V_{os} performance after soldering.

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

Parameter	Rating
V_{SY} ((V+) − (V−))	−0.3 V to +45 V
Input V_{CM}	
(+IN A, −IN A, +IN B, −IN B) − (V−)	−0.3 V to +45 V
(+IN A, −IN A, +IN B, −IN B) − (V+)	+0.3 V to −45 V
Differential Input Voltage	
(+IN A) − (−IN A), (+IN B) − (−IN B)	±45 V
Input Current	±10 mA
Output Short-Circuit Duration[1]	Continuous
Temperature Range	
Storage	−65°C to +150°C
Operating	−40°C to +125°C
T_J	150°C
Lead (soldering, 10 seconds)	300°C
T_C	260°C

[1] A heatsink may be required to keep the T_J below the absolute maximum rating when the output is shorted indefinitely.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction-to-case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
R-8	108.5	34.12	°C/W
RM-8	141.24	51.87	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001-2017.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002-2018.

ESD Ratings for ADA4510-2

Table 5. ADA4510-2, 8-Lead SOIC_N, 8-Lead MSOP

ESD Model	Withstand Threshold (V)	Class
HBM	±1000	1C
FICDM	±400	C1

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

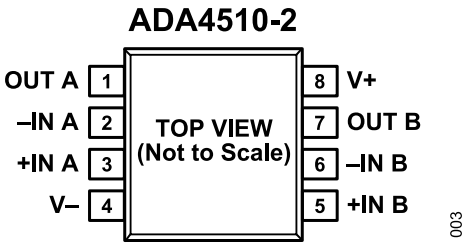

Figure 3. 8-Lead SOIC_N and 8-Lead MSOP Pin Configuration

Table 6. Pin Function Descriptions, 8-Lead SOIC_N and 8-Lead MSOP

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A.
2	−IN A	Inverting Input, Channel A.
3	+IN A	Noninverting Input, Channel A.
4	V−	Negative Supply Voltage.
5	+IN B	Noninverting Input, Channel B.
6	−IN B	Inverting Input, Channel B.
7	OUT B	Output, Channel B.
8	V+	Positive Supply Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{SY} = ±20 V, V_{CM} = 0 V, R_L = 10 kΩ to midsupply, T_A = 25°C, unless otherwise noted.

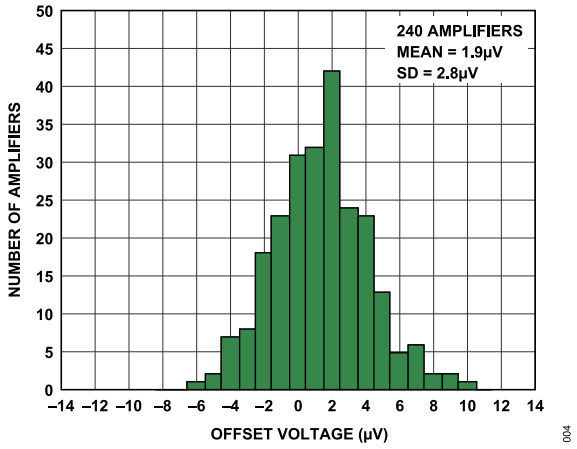

Figure 4. V_{OS} Distribution at 25°C

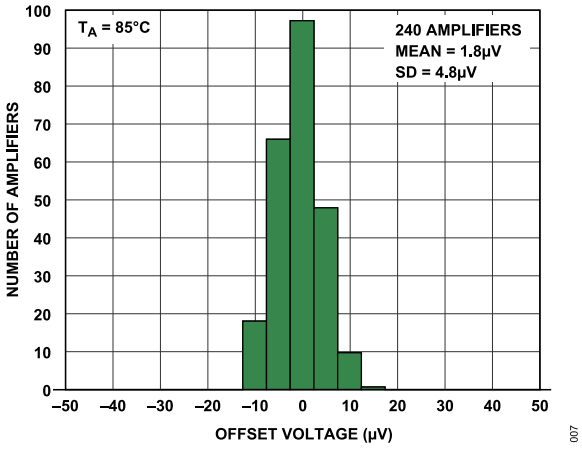

Figure 7. V_{OS} Distribution at 85°C

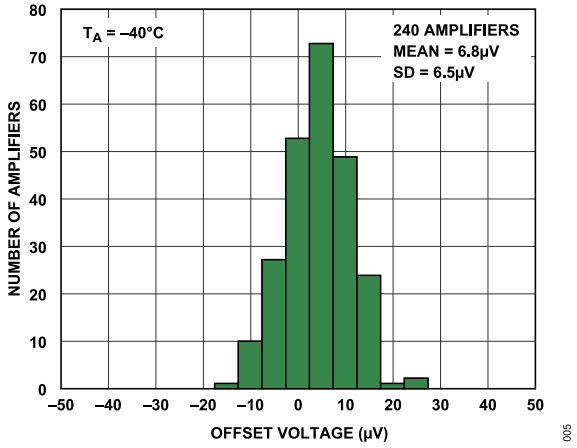

Figure 5. V_{OS} Distribution at −40°C

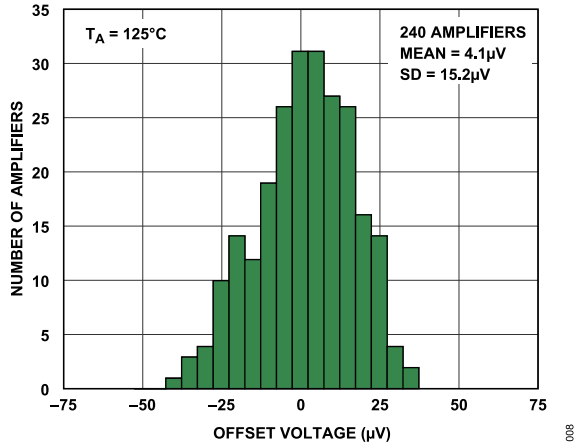

Figure 8. V_{OS} Distribution at 125°C

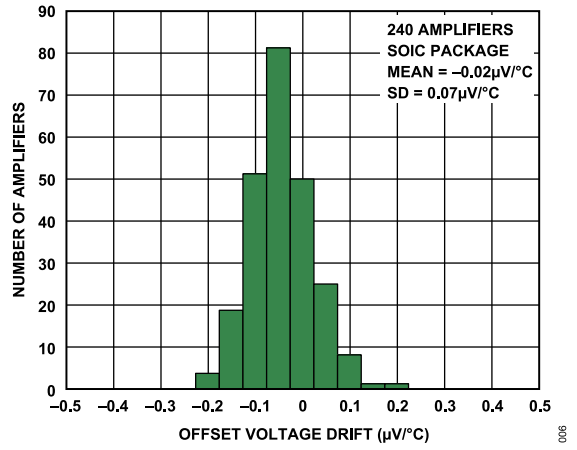

Figure 6. Input Offset Voltage Drift (TCV_{OS}) Distribution from 0°C to +85°C, SOIC_N

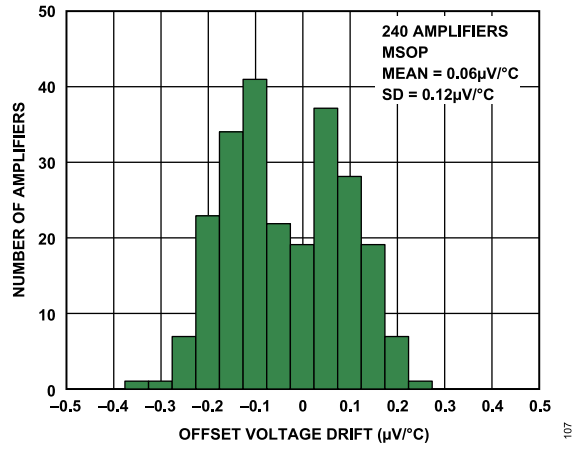

Figure 9. Input Offset Voltage Drift (TCV_{OS}) Distribution from 0°C to +85°C, MSOP

TYPICAL PERFORMANCE CHARACTERISTICS

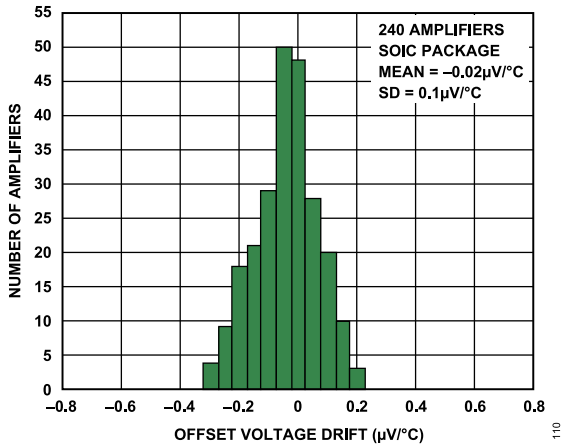

Figure 10. TCV_{OS} Distribution from −40°C to +125°C, SOIC_N

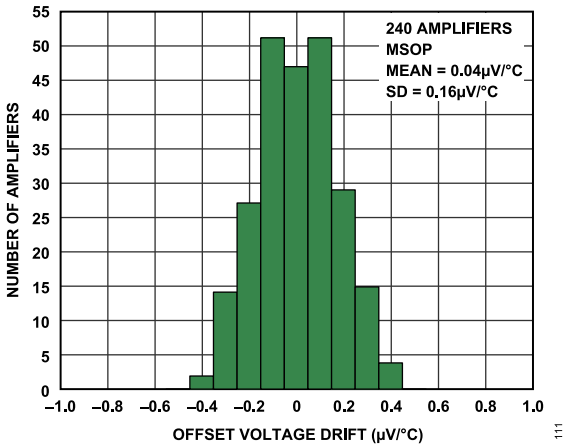

Figure 11. TCV_{OS} Distribution from −40°C to +125°C, MSOP

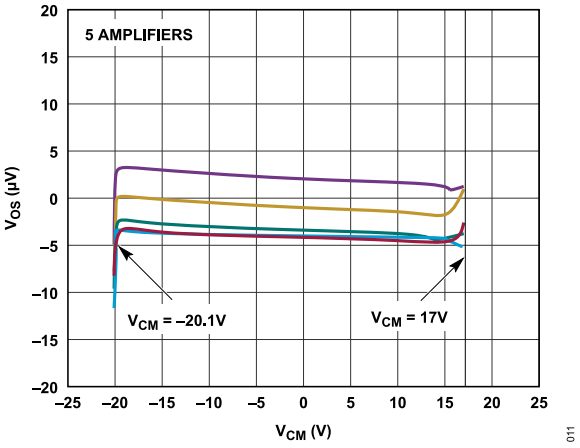

Figure 12. V_{OS} vs. V_{CM}

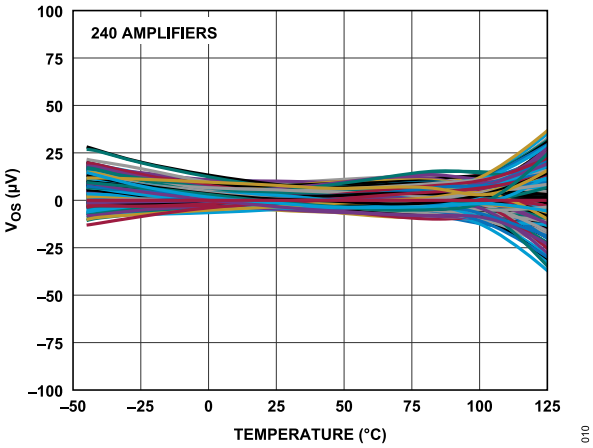

Figure 13. V_{OS} vs. Temperature, SOIC_N

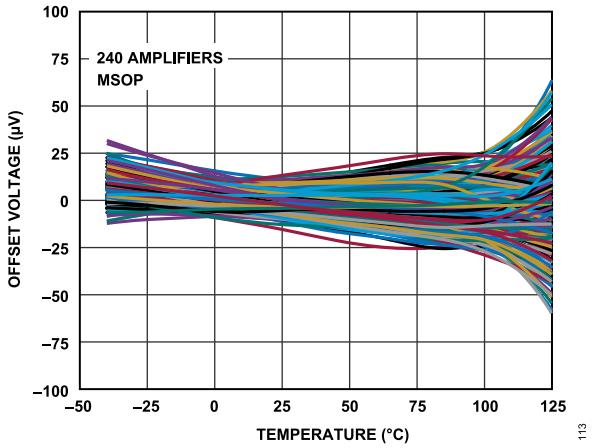

Figure 14. V_{OS} vs. Temperature, MSOP

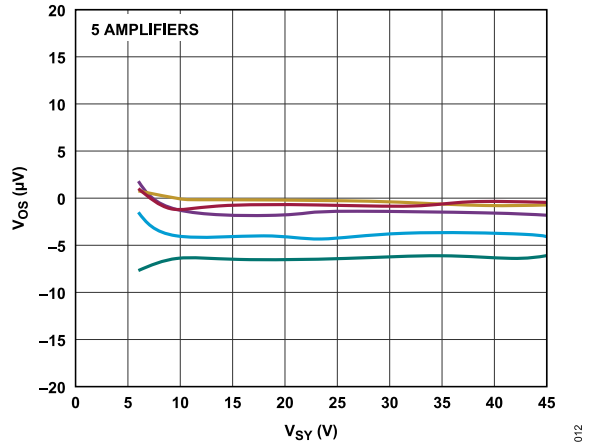

Figure 15. V_{OS} vs. V_{SY}

TYPICAL PERFORMANCE CHARACTERISTICS

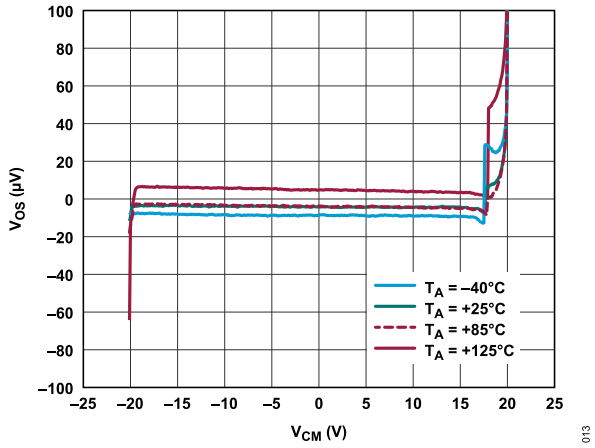

Figure 16. V_{OS} vs. V_{CM}, Four Temperatures

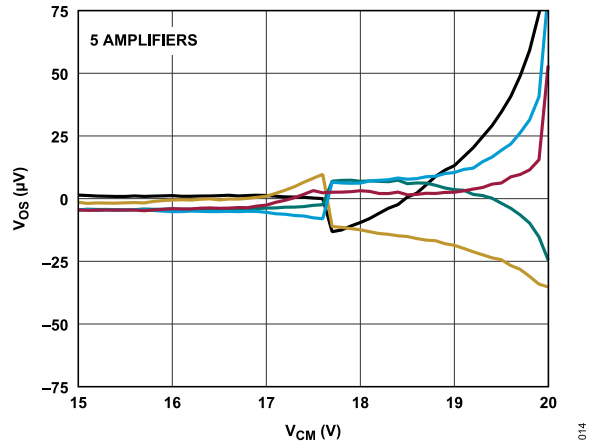

Figure 17. V_{OS} vs. V_{CM}, High V_{CM} Operation

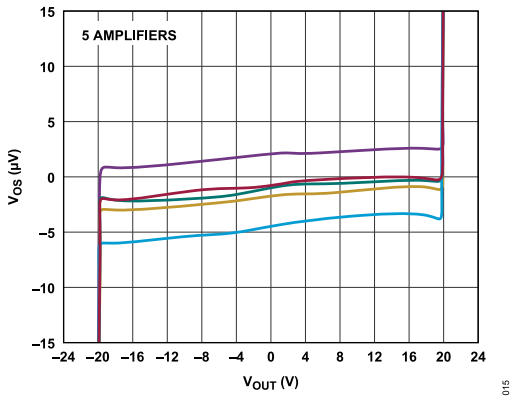

Figure 18. V_{OS} vs. V_{OUT}

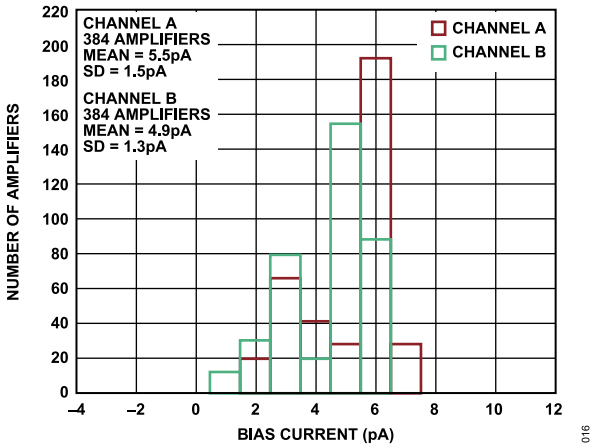

Figure 19. I_B Distribution at 25°C

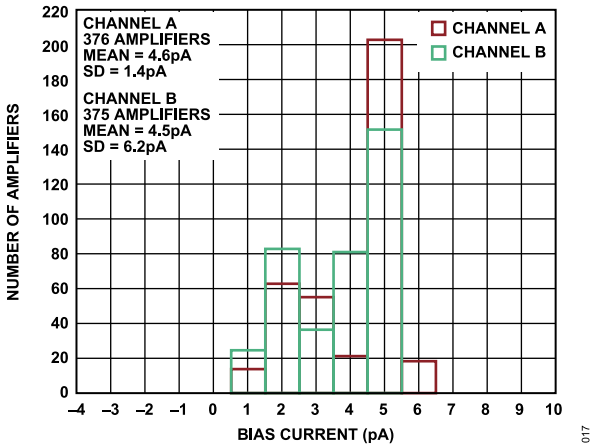

Figure 20. I_B Distribution at −40°C

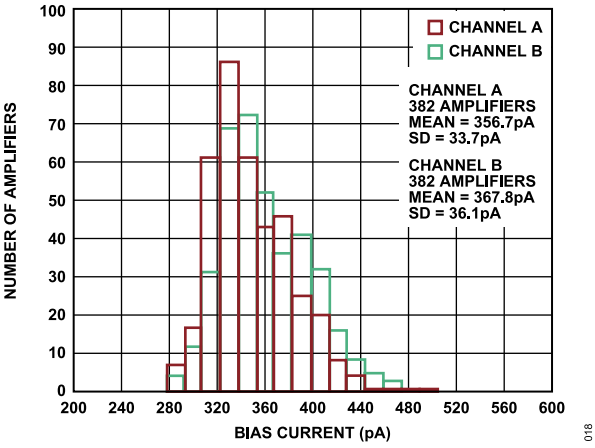

Figure 21. I_B Distribution at 85°C

TYPICAL PERFORMANCE CHARACTERISTICS

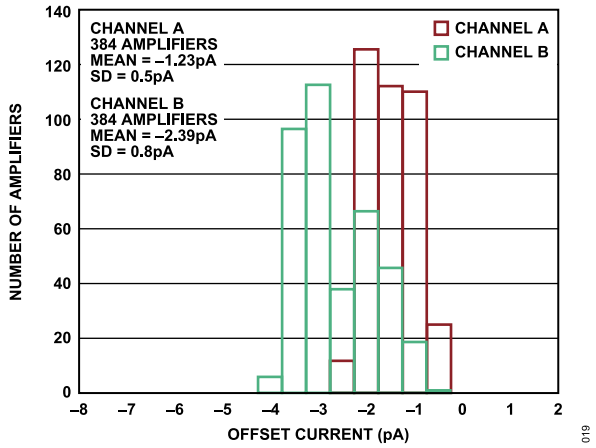

Figure 22. I_{OS} Distribution at 25°C

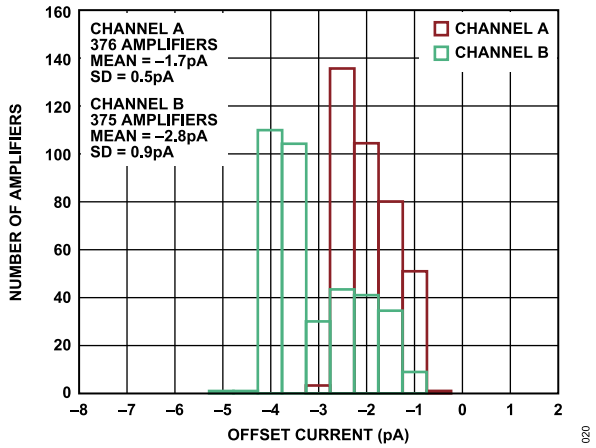

Figure 23. I_{OS} Distribution at −40°C

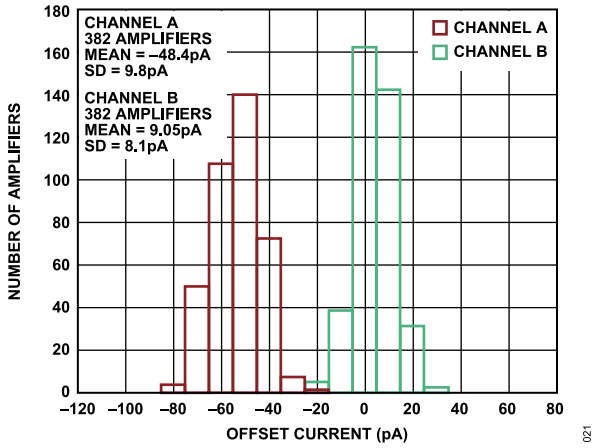

Figure 24. I_{OS} Distribution at 85°C

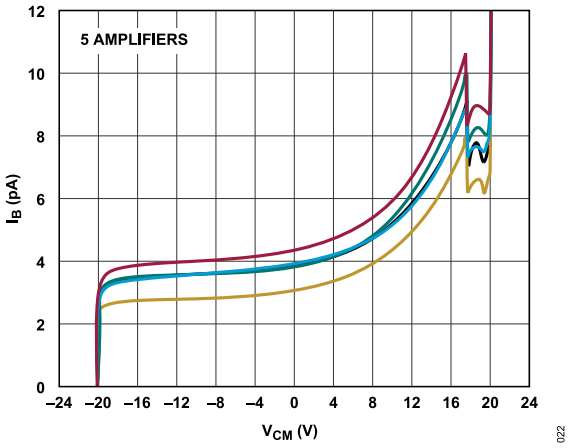

Figure 25. I_B vs. V_{CM}

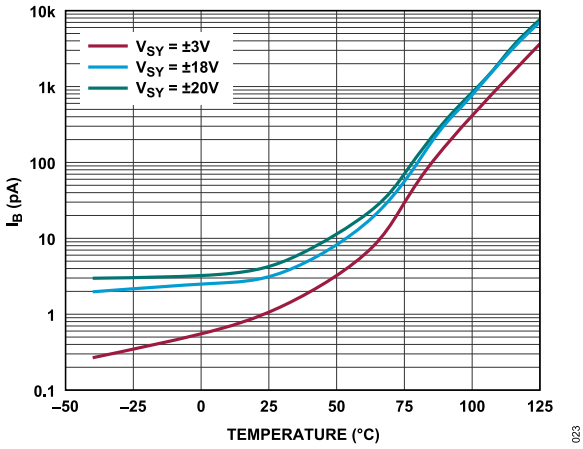

Figure 26. I_B vs. Temperature, SOIC_N

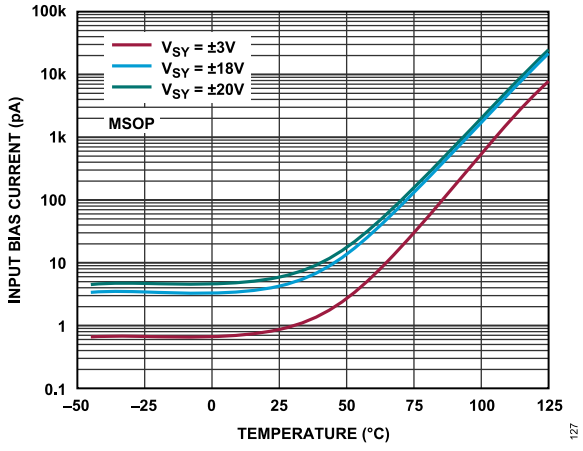

Figure 27. I_B vs. Temperature, MSOP

TYPICAL PERFORMANCE CHARACTERISTICS

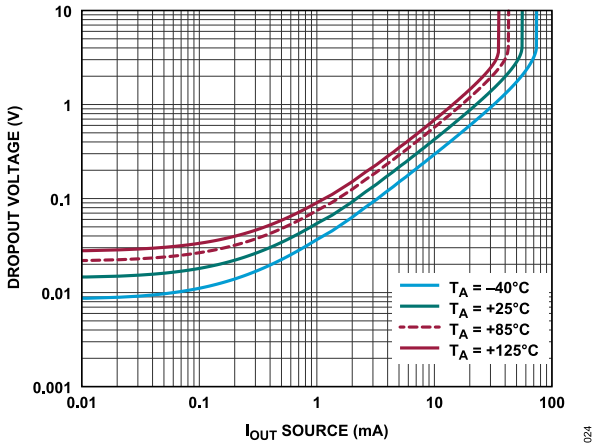

Figure 28. $V_{DROPOUT}$ ((V+) − V_{OUT}) vs. I_{OUT} Source

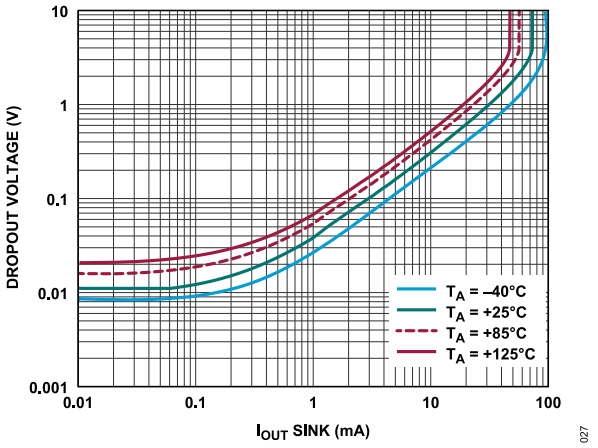

Figure 31. $V_{DROPOUT}$ (V_{OUT} − (V−)) vs. I_{OUT} Sink

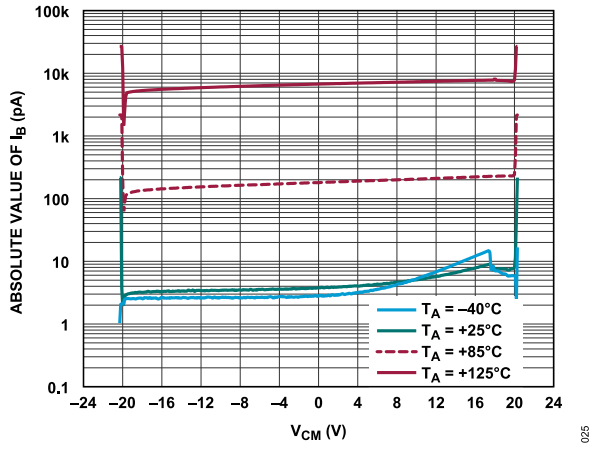

Figure 29. I_B vs. V_{CM}, Four Temperatures, SOIC_N

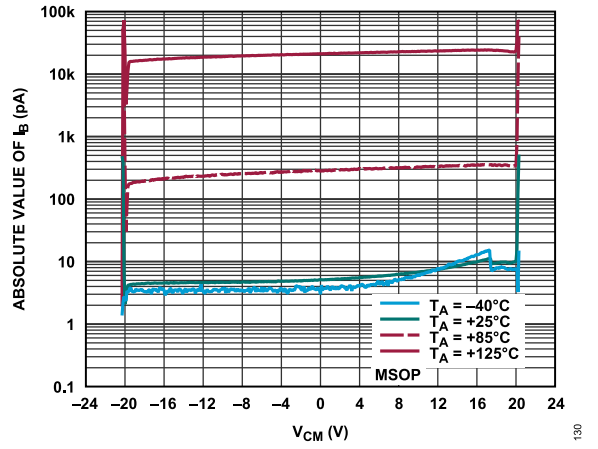

Figure 32. I_B vs. V_{CM}, Four Temperatures, MSOP

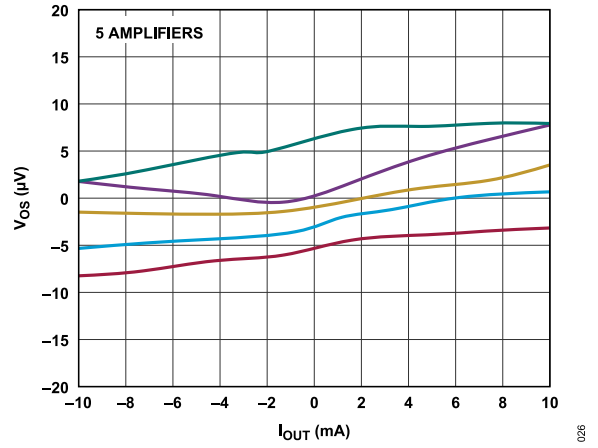

Figure 30. V_{OS} vs. I_{OUT}

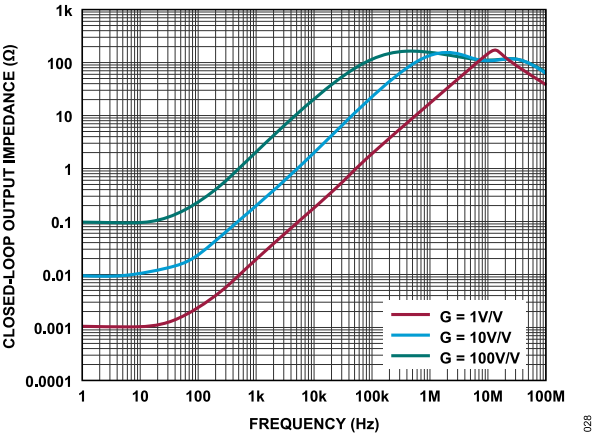

Figure 33. Z_{OUT} vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

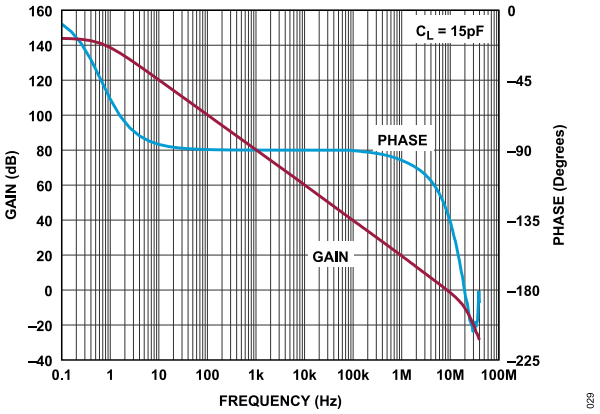

Figure 34. Open-Loop Gain and Phase vs. Frequency

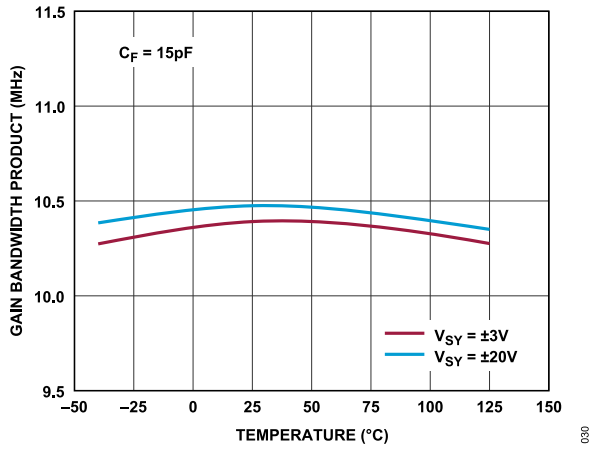

Figure 35. Gain Bandwidth Product vs. Temperature

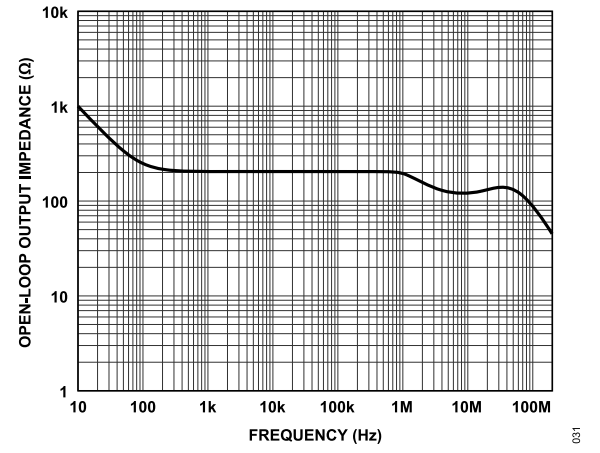

Figure 36. Z_O vs. Frequency

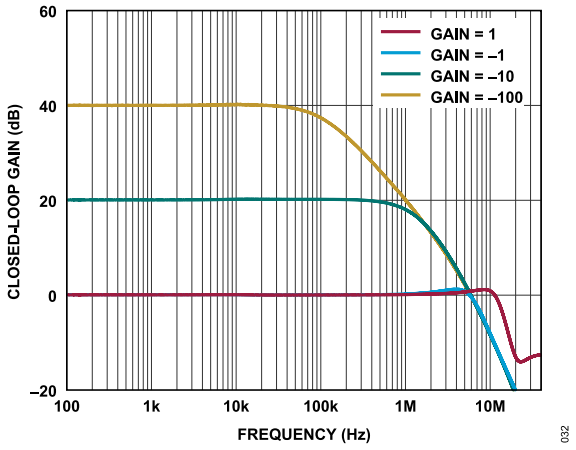

Figure 37. Closed-Loop Gain vs. Frequency

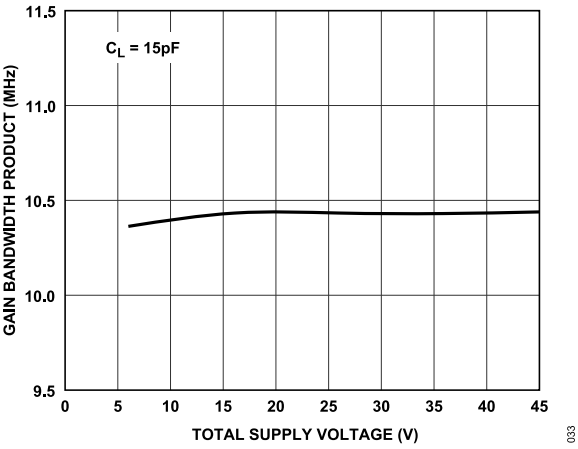

Figure 38. Gain Bandwidth Product vs. Total Supply Voltage

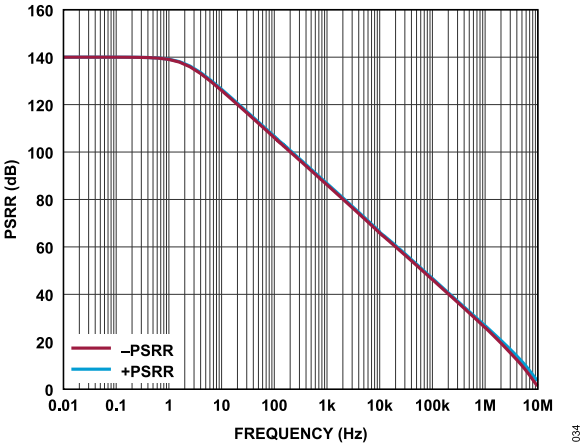

Figure 39. PSRR vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

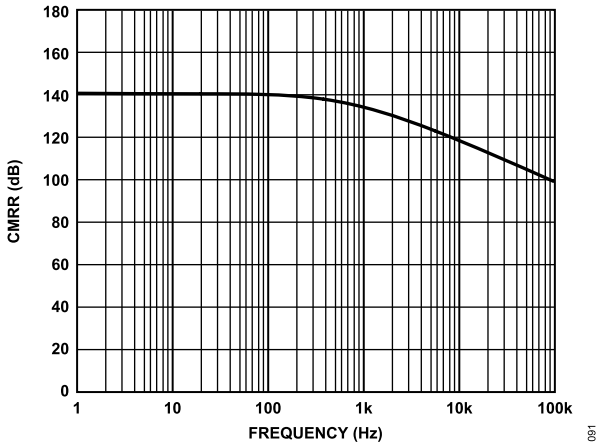

Figure 40. CMRR vs. Frequency

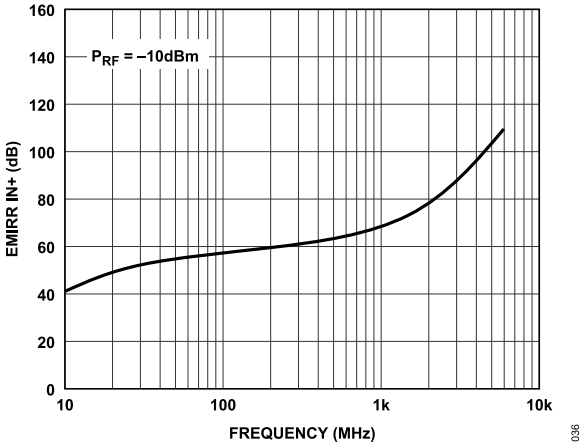

Figure 41. EMIRR IN+ vs. Frequency (P_{RF} Is RF Power.)

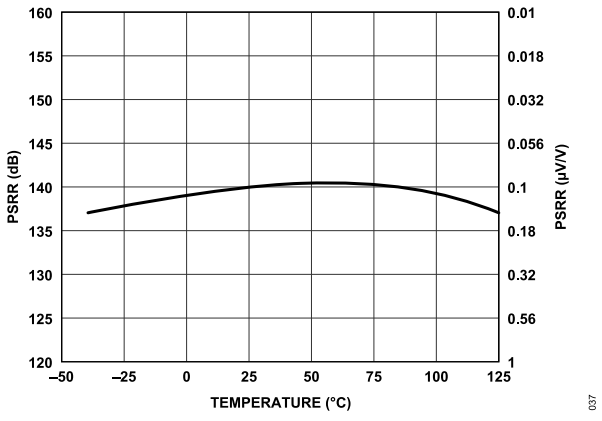

Figure 42. PSRR vs. Temperature

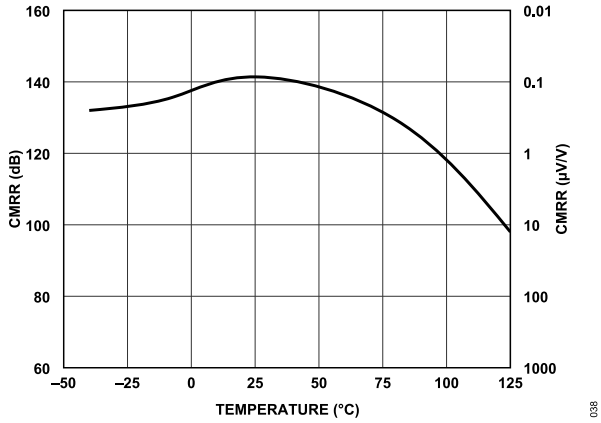

Figure 43. CMRR vs. Temperature

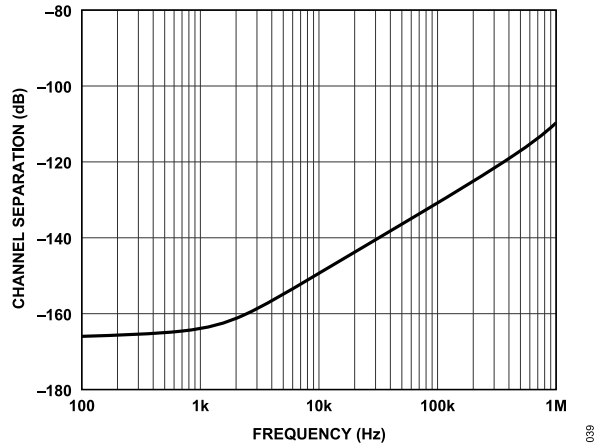

Figure 44. Channel Separation vs. Frequency

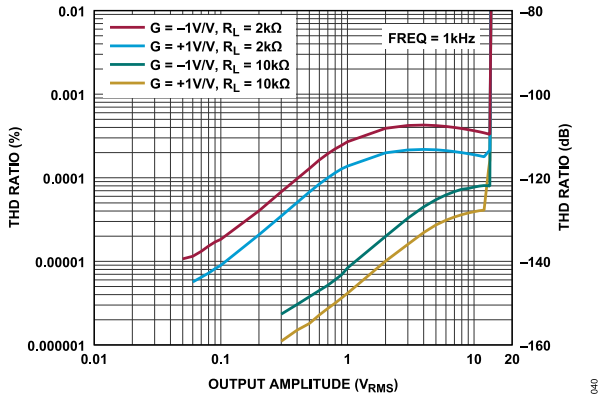

Figure 45. THD Ratio vs. Output Amplitude

TYPICAL PERFORMANCE CHARACTERISTICS

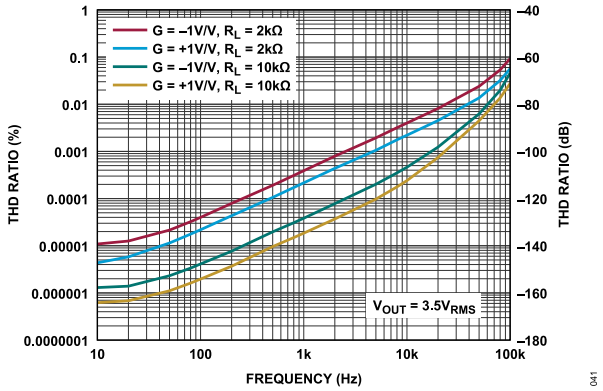

Figure 46. THD Ratio vs. Frequency

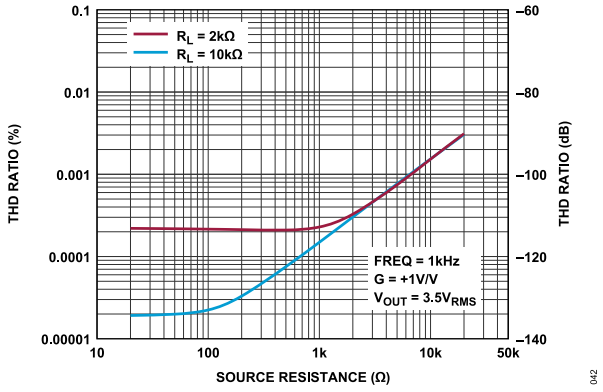

Figure 47. THD Ratio vs. Source Resistance

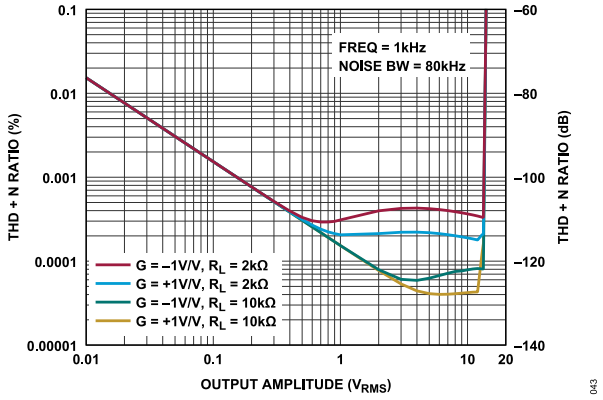

Figure 48. THD Plus Noise (THD + N) Ratio vs. Output Amplitude

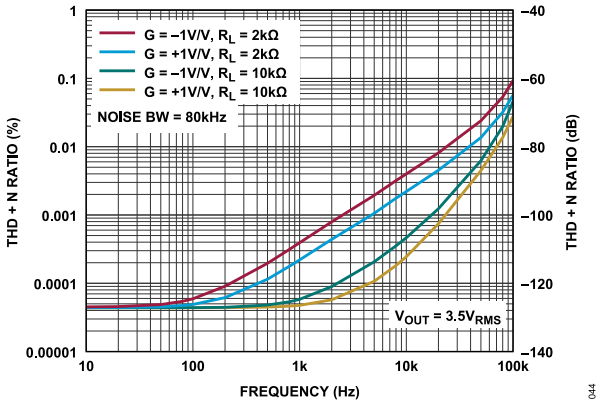

Figure 49. THD + N vs. Frequency

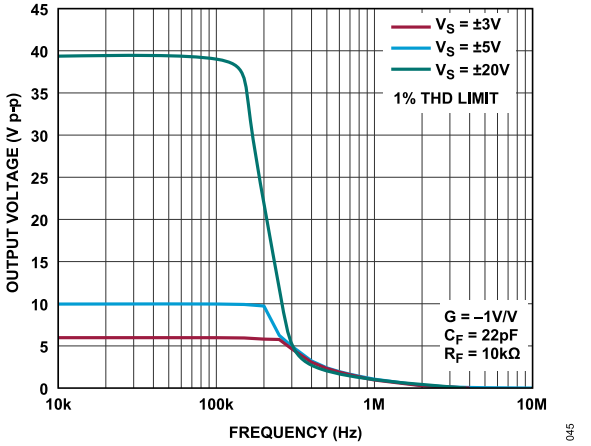

Figure 50. Maximum Undistorted Output Swing vs. Frequency

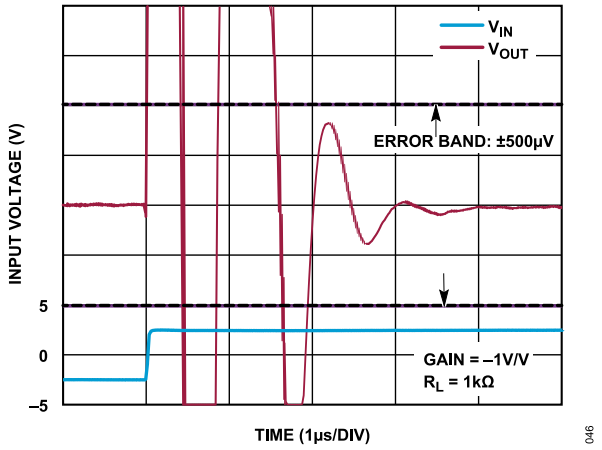

Figure 51. Positive Step Settling Time to 0.01%, V_{OUT} = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

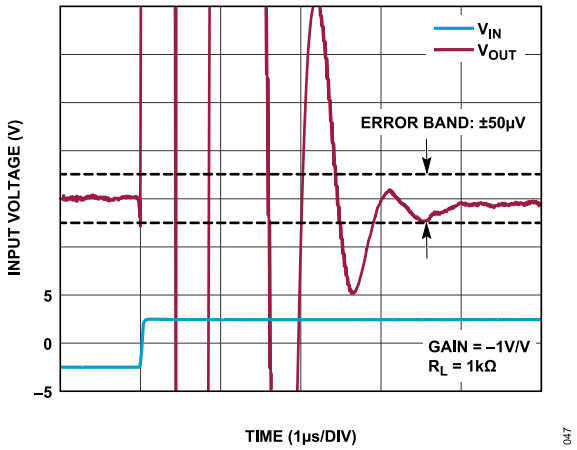

Figure 52. Positive Step Settling Time to 0.001%, V_{OUT} = 5 V

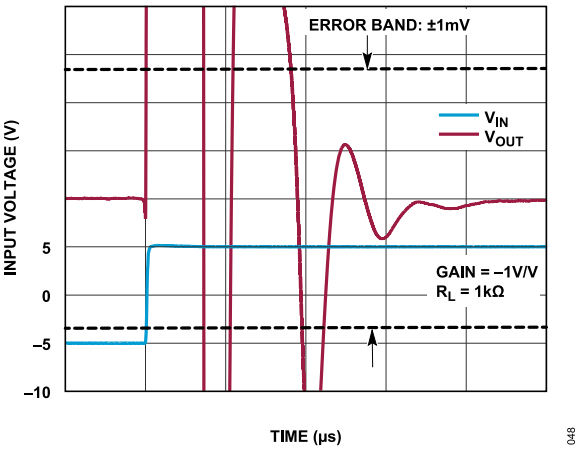

Figure 53. Positive Step Settling Time to 0.01%, V_{OUT} = 10 V

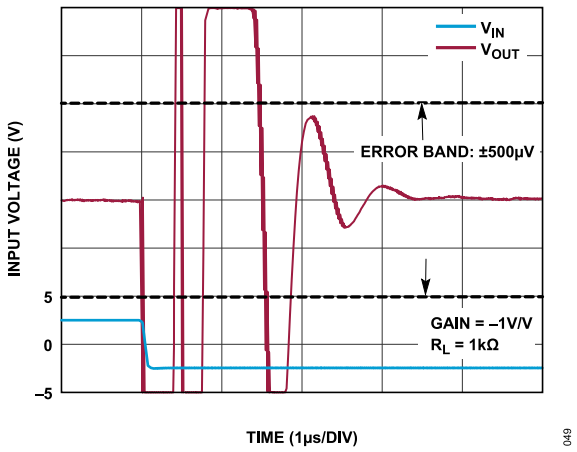

Figure 54. Negative Step Settling Time to 0.01%, V_{OUT} = 5 V

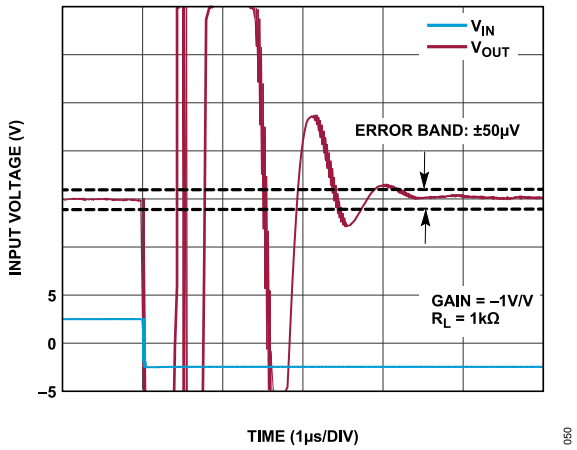

Figure 55. Negative Step Settling Time to 0.001%, V_{OUT} = 5 V

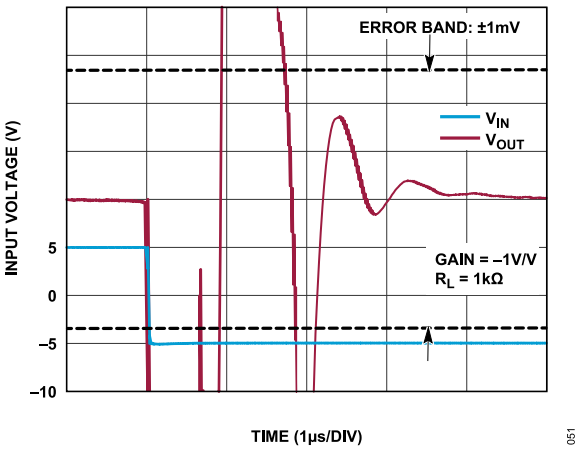

Figure 56. Negative Step Settling Time to 0.01%, V_{OUT} = 10 V

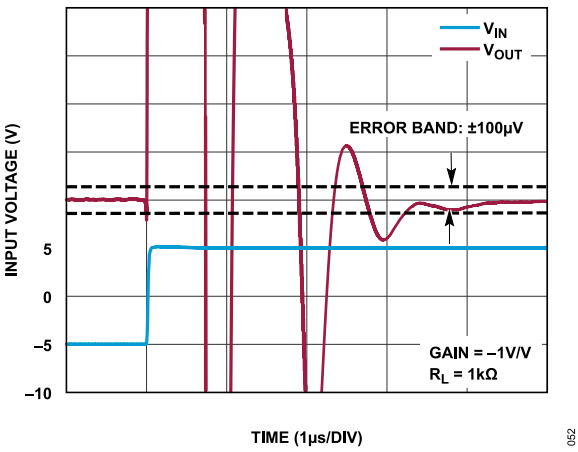

Figure 57. Positive Step Settling Time to 0.001%, V_{OUT} = 10 V

TYPICAL PERFORMANCE CHARACTERISTICS

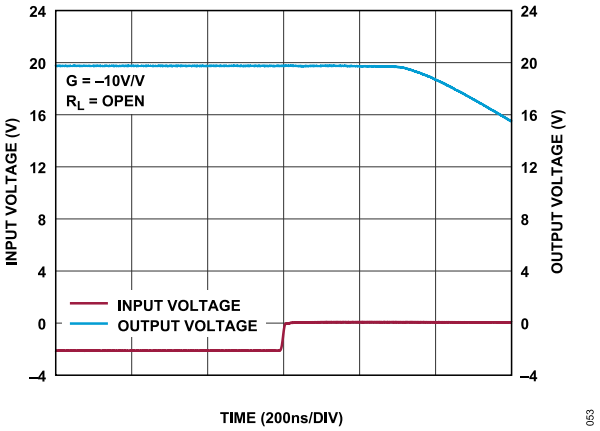

Figure 58. Positive Overload Recovery

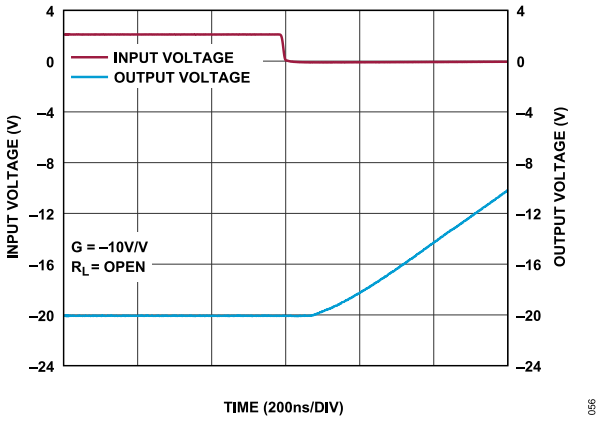

Figure 61. Negative Overload Recovery

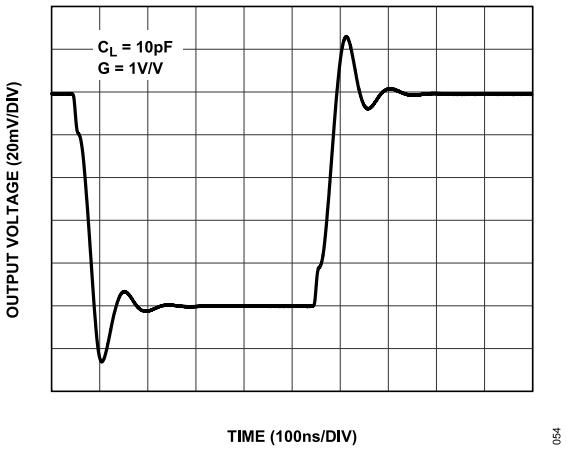

Figure 59. Small Signal Transient Response, G = 1 V/V

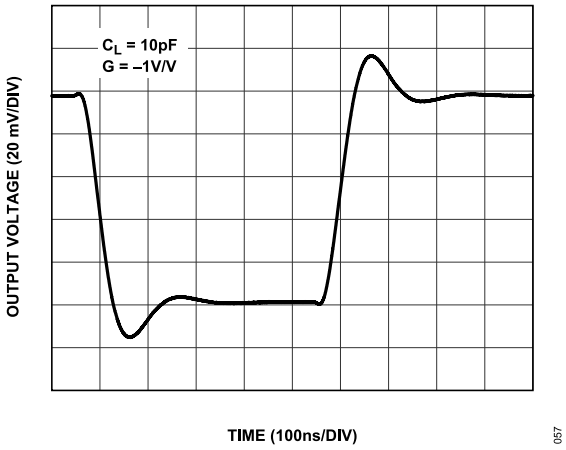

Figure 62. Small Signal Transient Response, G = −1 V/V

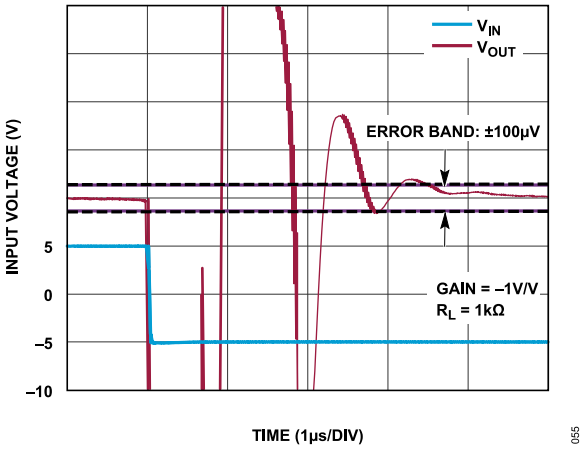

Figure 60. Negative Step Settling Time to 0.001%, V_{OUT} = 10 V

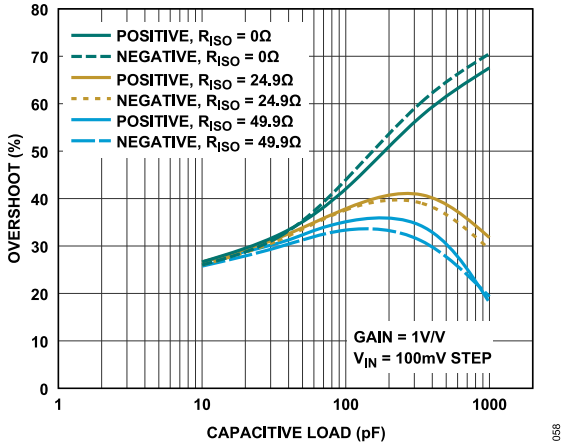

Figure 63. Overshoot vs. Capacitance Load, G = 1 V/V

TYPICAL PERFORMANCE CHARACTERISTICS

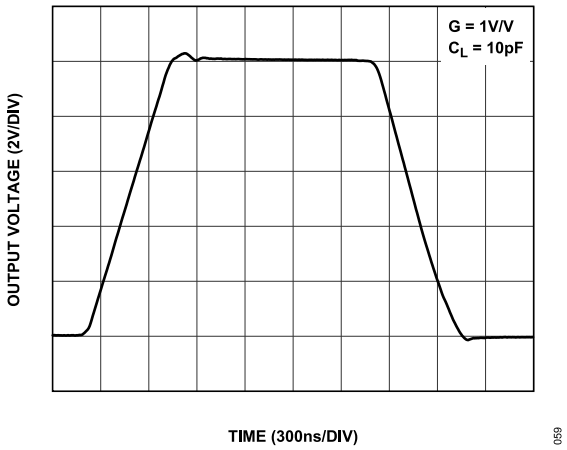

Figure 64. Large Signal Transient Response, G = 1 V/V

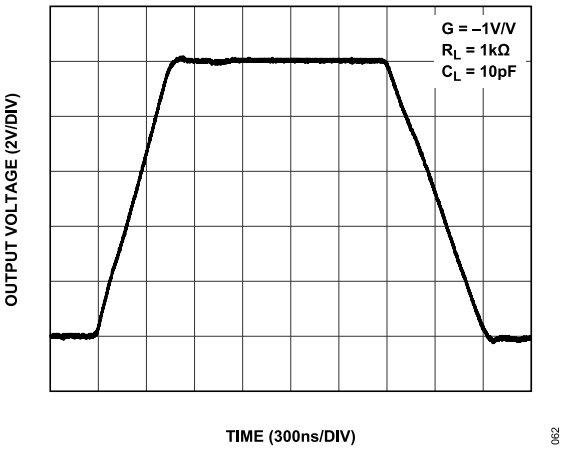

Figure 67. Large Signal Transient Response, G = −1 V/V

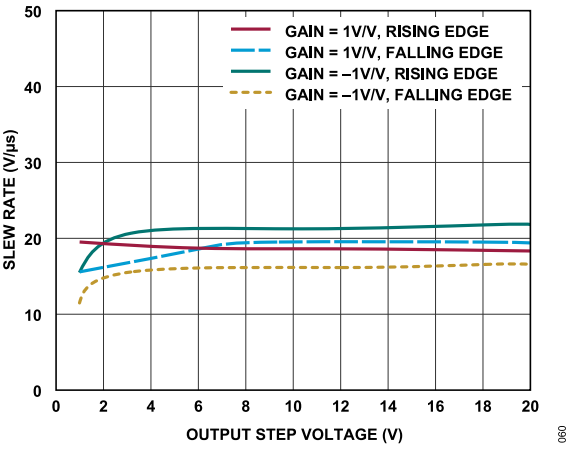

Figure 65. Slew Rate vs. Output Step Voltage

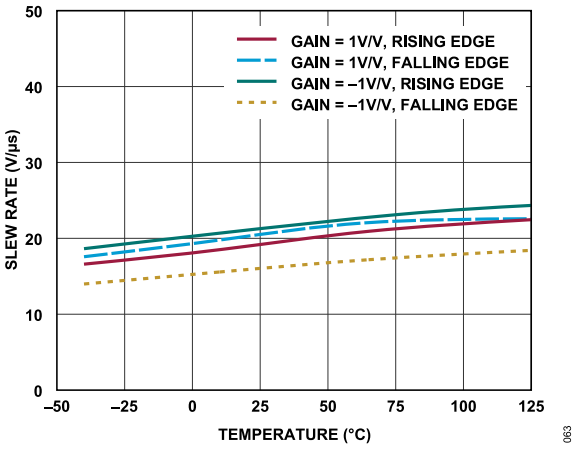

Figure 68. Slew Rate vs. Temperature

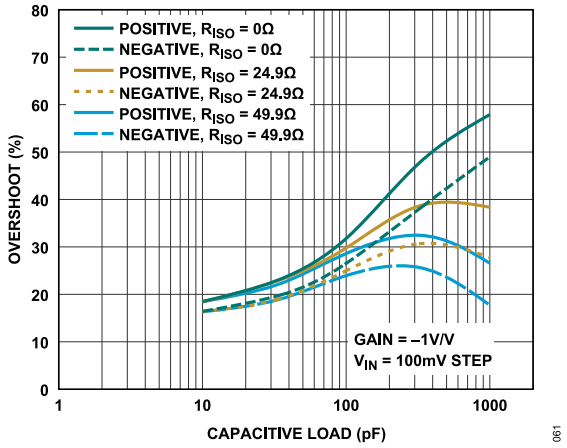

Figure 66. Overshoot vs. Capacitance Load, G = −1 V/V

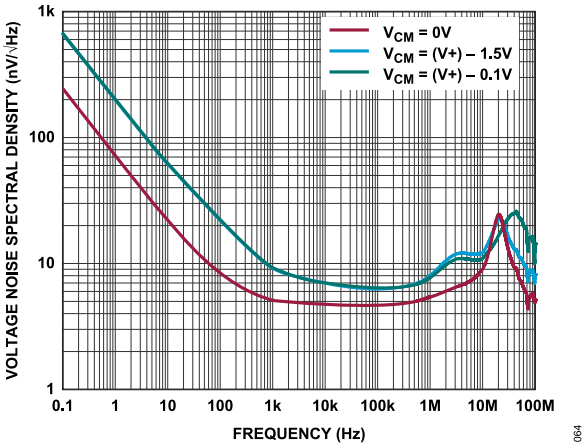

Figure 69. Input Voltage Noise Spectral Density vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

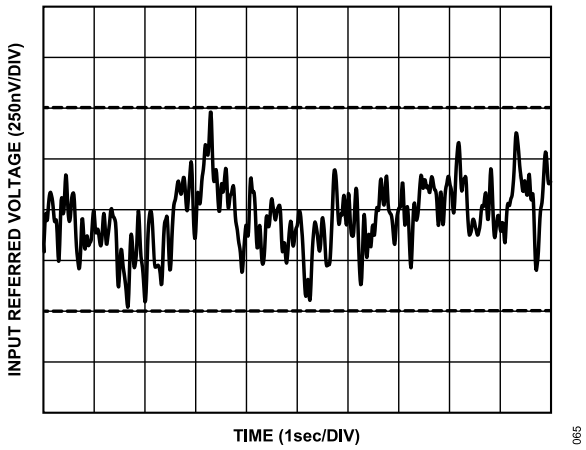

Figure 70. 0.1 Hz to 10 Hz Voltage Noise

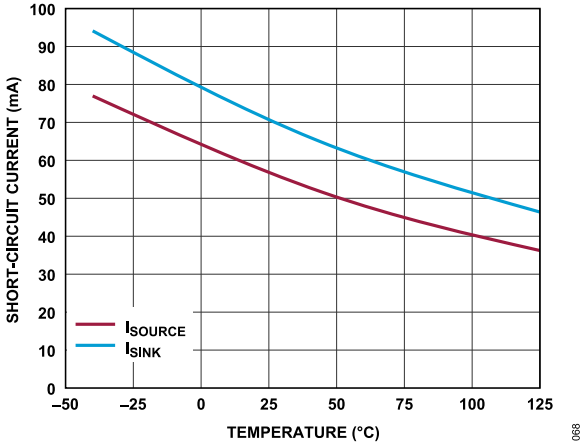

Figure 73. Short-Circuit Output Current vs. Temperature

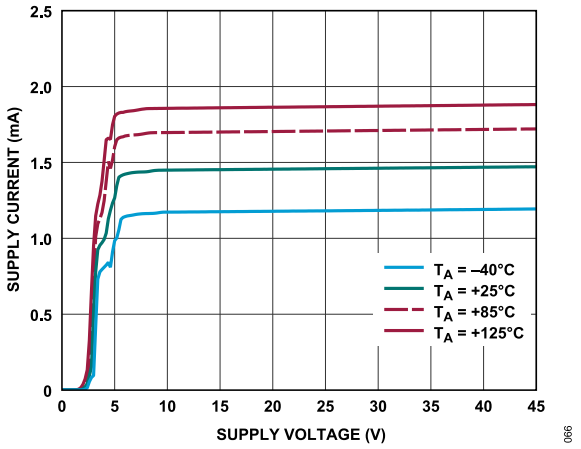

Figure 71. I_S per Amplifier vs. Supply Voltage at Various Temperatures

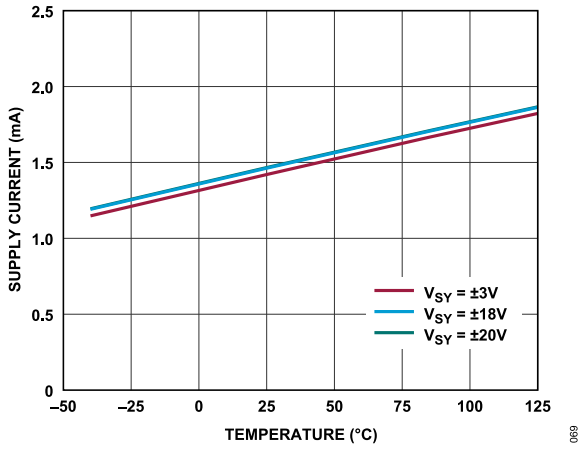

Figure 74. I_S per Amplifier vs. Temperature for Various Supplies

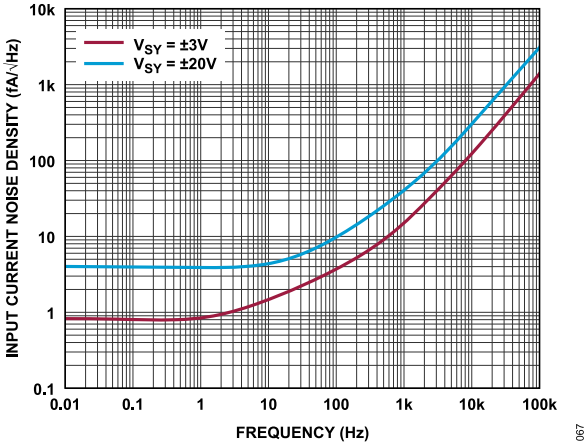

Figure 72. Current Noise Spectral Density vs. Frequency

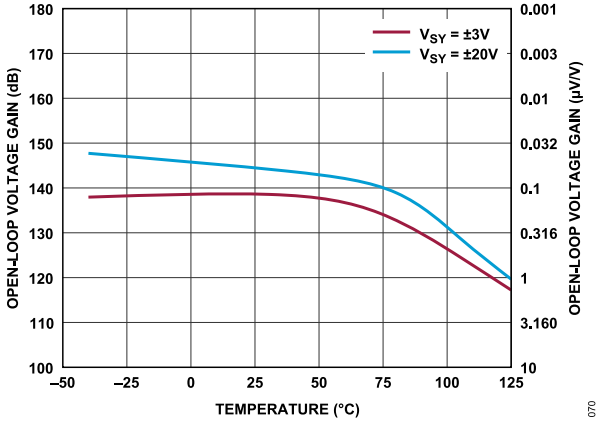

Figure 75. DC Open-Loop Gain vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

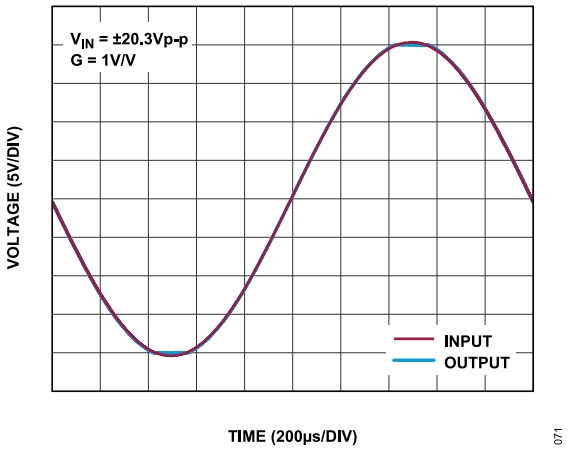

Figure 76. No Phase Reversal

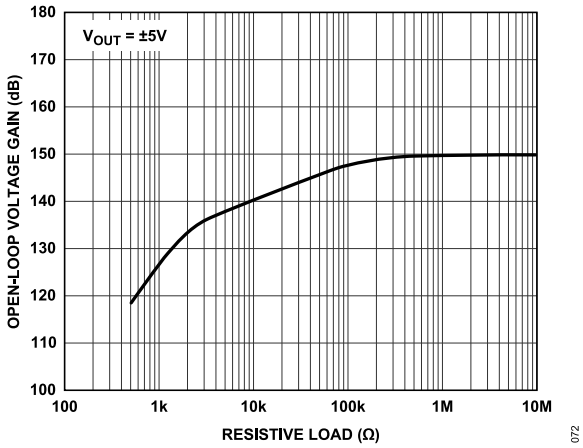

Figure 77. DC Open-Loop Gain vs. R_L

THEORY OF OPERATION

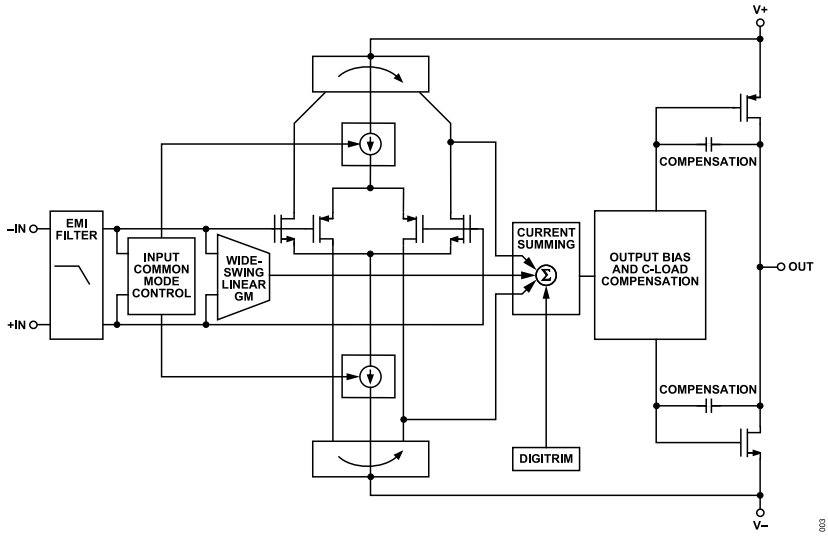

Figure 78. Simplified Schematic

The ADA4510-2 is a dual-channel, low-power, rail-to-rail input and output, precision CMOS op amp that operates over a wide supply voltage range of 6 V to 40 V. This amplifier uses the Analog Devices DigiTrim technique to achieve a higher degree of precision compared to previous CMOS amplifiers. The DigiTrim technique is a method of trimming the offset voltage and the offset voltage temperature drift of an amplifier after assembly. This technique corrects any offset voltages and drifts caused by mechanical stresses during assembly.

INPUT AND GAIN STAGES

Figure 78 shows the simplified circuit diagram for the ADA4510-2. The input architecture provides high-impedance, rail-to-rail differential and common-mode input swing, low noise, low input bias current, and low offset voltage.

An integrated EMI filter increases the signal robustness and helps prevent EMI signals from coupling into the amplifier. Depending on the input common-mode voltage, either the negative channel metal-oxide semiconductor (NMOS) or the positive channel metal-oxide semiconductor (PMOS) input stage can be active at any time. The low offset voltage and low offset voltage drift specifications are possible by using the DigiTrim technique on both the NMOS and PMOS input stages.

The ADA4510-2 includes circuitry that extends the linear input range, providing higher slew rates than a traditional input differential pair and improving the THD. The wide gain bandwidth product of 10.4 MHz is achieved through internal Miller compensation.

OUTPUT STAGE

The output of the ADA4510-2 swings rail-to-rail to within 100 mV of either supply rail. A capacitive load compensation block senses the load capacitor and adds additional phase margin, if required, to drive a large capacitor (at least 1 nF) and maintain amplifier stability.

EMI REJECTION

High-frequency EMI is a threat to precision amplifier performance in an intended application. Op amps must accurately amplify input signals despite low signal strength and long transmission lines. All operational amplifier pins are susceptible to EMI signals. These high-frequency signals are coupled into an operational amplifier by various means, such as conduction, near-field radiation, or far-field radiation. For example, wires and printed circuit board (PCB) traces act as antennas to pick up high-frequency EMI signals.

Op amps do not amplify EMI or RF signals due to the relatively low bandwidth of the amplifier. However, due to the nonlinearities of the input devices, op amps can rectify these out-of-band signals, which then appear as a DC offset at the output.

The ADA4510-2 is designed with integrated EMI filters at the input stage of the op amp. The EMIRR describes the ability of the ADA4510-2 to perform as intended in the presence of electromagnetic energy. The EMIRR is specified for the noninverting pin in Table 1. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20 \log \times (\Delta V_{IN}\_PEAK / \Delta V_{OS})$$

EMIRR performance of ADA4510-2 is shown in Figure 41.

NO PHASE INVERSION

The ADA4510-2 does not suffer from output voltage phase reversal that occurs in some op amps when the specified input V_{CM} range is exceeded. Output voltage phase reversal causes the output voltage to swing to the opposite rail until the input comes back within the common-mode range. Typically, the inputs of conventional op amps fail to reach or exceed the common-mode limit toward the negative range. Phase-reversal is most often associated with junction field effect transistor (JFET) and/or bipolar field effect transistor (BiFET) amplifiers, but some bipolar single-supply amplifiers are

THEORY OF OPERATION

also susceptible phase-reversal. The ADA4510-2 guarantees no phase inversion beyond the entire specified input V_{CM} range all the way to the absolute maximum input voltage limit.

CAPACITIVE LOAD DRIVE CAPABILITY

The ADA4510-2 is stable with any capacitive load up to 1 nF. This is accomplished by dynamically sensing the load-induced output pole and adjusting the compensation at the internal gain node of the amplifier. As the capacitive load increases, the bandwidth will decrease. The phase margin may increase or decrease with different capacitive loads, so there may be overshoot in the transient response for some capacitive loads (see Figure 63 and Figure 66). Coaxial cable less than 1 nF can be driven directly, but, for best pulse fidelity, the cable should be properly terminated by placing a resistor of a value equal to the characteristic impedance of the cable (for example 50 Ω) in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

Figure 63 and Figure 66 show the overshoot of the ADA4510-2 with various capacitive loads in unity gain and gain of −1 configurations. To further improve the capacitive load drive of the ADA4510-2, an isolation resistor (R_{ISO}) may be used in series with the output to significantly reduce the overshoot and ringing to stabilize the amplifier.

Table 7. Capacitive Load Drive at Various R_{ISO}

Capacitive Load	100 pF			1000 pF		
R_{ISO}	0 Ω	24.9 Ω	49.9 Ω	0 Ω	24.9 Ω	49.9 Ω
Positive Overshoot Percent	42%	38%	35%	68%	32%	18%
Negative Overshoot Percent	43%	38%	30%	71%	29%	19%

APPLICATIONS INFORMATION

MUX-COMPATIBLE DATA ACQUISITION SYSTEM

Data acquisition in multichannel systems can be accomplished by multiplexing as shown in Figure 79. This technique is very popular in instrumentation, industrial process control, and automated test equipment (ATE), because it reduces the number of components needed to sense multiple sensors, saving significant power, size, and cost.

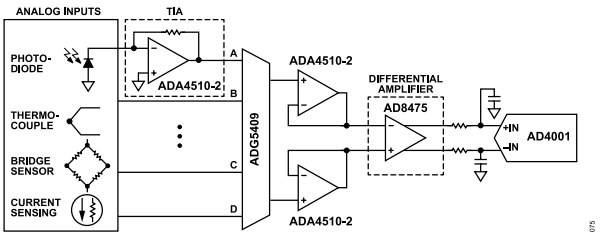

Figure 79. Multiplexed Data Acquisition System

One risk in designing this system is the possibility of exposing the buffer amplifier to a large differential voltage due to the fast switching from a large positive voltage to a large negative voltage by the mux. If the buffer amplifier is not chosen properly, it may experience a large inrush current that can degrade the performance of the system or, worse, permanently damage the part.

The ADA4510-2 solves this problem using a robust mux-compatible architecture that can tolerate large differential voltages up to the supply rails without the use of differential back-to-back diodes. This significantly reduces inrush current, improves settling and distortion performance without experiencing any input loading effect compared to classic op amps with back-to-back diodes, as shown in Figure 80.

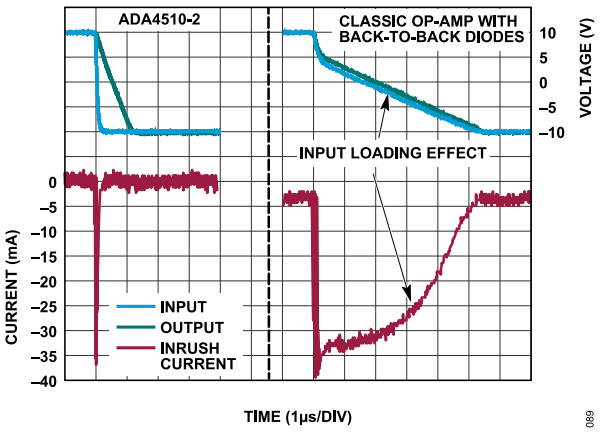

Figure 80. ADA4510-2 Inrush Current Reduction

Design Example

The circuit shown in Figure 81 is a classic multichannel data acquisition signal chain consisting of a mux, amplifiers, and an analog-to-digital converter (ADC). The architecture allows fast sampling of multiple channels using a single ADC, providing low cost and excellent channel-to-channel matching. Channel-to-channel switching speed is limited by the settling time of the various components following the mux in the signal chain, because the mux can present a full-scale step V_{OUT} to the downstream amplifier and the ADC. The components in this circuit have been specifically chosen to minimize settling time and maximize channel-to-channel switching speed.

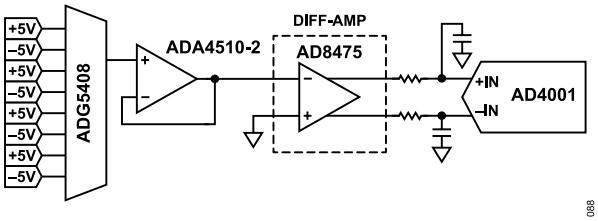

Figure 81. 16-bit, 8-Channel, Single-ended to Differential, Multiplexed Data Acquisition System

This circuit operates in continuous switching mode. The multiplexer ADG5408 switches continuously with a switching rate that is in sync with the ADC conversion cycle. The signal is buffered by the ADA4510-2 and drives to the AD8475, which attenuates, level shifts, and converts the signal from single-ended to a differential output. An RC filter is used at the input of the ADC to minimize out-of-band noise and attenuate the kickback from the switched capacitor at the ADC input.

To calculate the settling time, the circuit can be divided into parts shown in Figure 82.

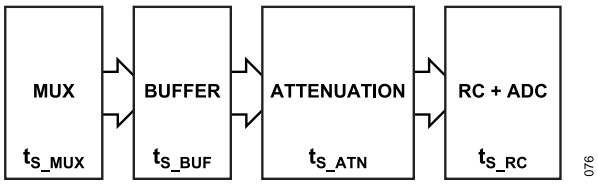

Figure 82. Block Diagram for Settling Time Analysis

The entire settling time is then approximated as the RSS of the settling time of each stage.

APPLICATIONS INFORMATION

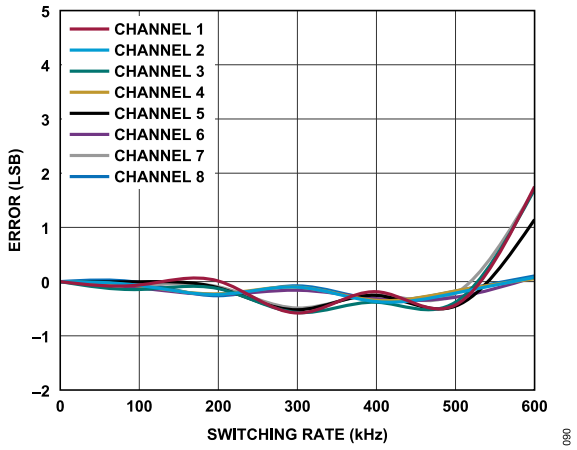

Figure 83. Error (LSB) vs. Switching Rate, 8-Channel 10 V Step

Figure 83 shows the error in LSB vs. switching rate for an 8-channel 10 V step mux data acquisition system. An LSB error <1 is achieved up to 570 kHz switching rate.

TRANSIMPEDANCE AMPLIFIER

The ADA4510-2 is an excellent choice for low noise transimpedance amplifier (TIA) applications. The low voltage and current noise of the ADA4510-2 maximize signal-to-noise ratio (SNR), and the low V_{OS} and I_B of the ADA4510-2 minimize the DC error at the amplifier output.

Common applications for current-to-voltage conversion include photodiode circuits where the amplifier converts a current emitted by a diode placed at the negative input terminal into an output voltage. Some photodiode applications include fiber optic controls, motion sensors, and barcode readers. The circuit shown in Figure 84 shows one channel of the ADA4510-2 as a current-to-voltage converter with an electrical model of a photodiode.

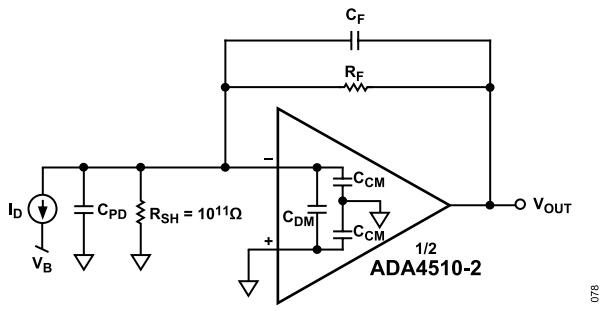

Figure 84. Equivalent TIA Circuit

Photodiodes operate in either photovoltaic mode (zero bias) or photoconductive mode (with an applied reverse-bias across the diode). Mode selection depends on the speed and dark current requirements of the application and the choice of photodiode. In photovoltaic mode, the dark current is at a minimum and is preferred for low frequency and/or low light level applications (that is, PN photodiodes). Photoconductive mode is better for applications that require faster and linear responses (that is, PIN photodiodes); however, the tradeoffs include increases in dark and noise currents.

The following transfer function describes the transimpedance gain of Figure 84:

$$V_{OUT} = \frac{I_D R_F}{1 + sC_F R_F} \quad (1)$$

where:
V_{OUT} is the desired output DC voltage of the op amp.
I_D is the output current of the photodiode.
R_F is the feedback resistor.
C_F is the feedback capacitor.
The parallel combination of R_F and C_F sets the signal bandwidth.
s is the complex frequency variable jω.
j is the imaginary unit.
ω is the angular frequency.

Set R_F such that the maximum attainable V_{OUT} corresponds to the maximum diode I_{OUT}. Because signal levels increase directly with R_F, while the noise due to R_F increases with the square root of the resistor value, employing the full output swing maximizes the SNR.

It is important to distinguish between the transimpedance gain and the loop gain, because the loop gain characteristics determine the net circuit stability. The closed-loop transfer function takes the form shown in the following equation:

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \quad (2)$$

where:
A is the open loop gain of the amplifier.
β is the feedback network.
$A\beta$ is the loop gain.

In this application β is given by the following:

$$\beta = \left(\frac{R_{SH}}{R_{SH} + R_F}\right)\frac{1 + sR_F C_F}{1 + s(R_F \parallel R_{SH})(C_{IN} + C_F)} \quad (3)$$

where:
R_{SH} is the diode shunt resistance.
C_{IN} is the total input capacitance consisting of the sum of the diode shunt capacitance (C_{PD}), the input capacitance of the amplifier ($C_{DM} + C_{CM}$), and the external stray capacitance.

C_{IN}, R_F, C_F, and R_{SH} produce a zero in the 1/β transfer function. The zero frequency (f_Z) is as in the equation that follows:

$$f_Z = \frac{1}{2\pi\,(R_F \parallel R_{SH})(C_{IN} + C_F)} \quad (4)$$

Because the photodiode shunt resistance $R_{SH} >> R_F$, the circuit behavior is not impacted by the effect of the junction resistance, and f_Z simplifies to the following:

$$f_Z = \frac{1}{2\pi R_F (C_{IN} + C_F)} \quad (5)$$

APPLICATIONS INFORMATION

Figure 85 shows the TIA 1/β curve superimposed upon the open loop gain of the amplifier. For the system to be stable, the 1/β curve must have a slope of less than 20 dB/decade when it intersects with the open loop response. In Figure 85 the dotted line shows an uncompensated 1/β response (C_F = 0 pF) intersecting with the open loop gain at the frequency (f_X) with a slope of 20 dB/decade which indicates an unstable condition.

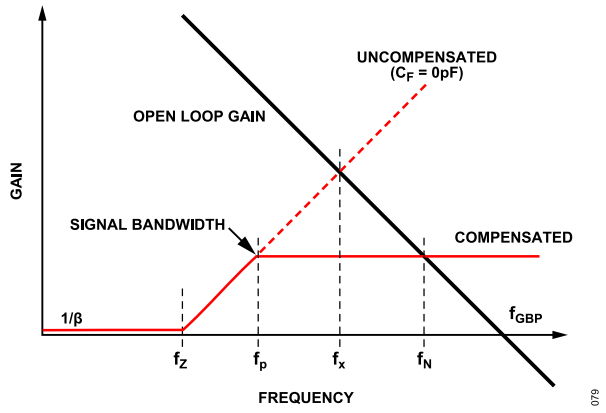

Figure 85. Generalized TIA 1/β and Transfer Function

The instability caused by C_{IN} can be compensated by adding C_F to introduce a pole at a frequency equal to or lower than f_X. The pole frequency is as follows:

$$f_P = \frac{1}{2\pi R_F C_F} \quad (6)$$

Setting the pole at the f_X frequency maximizes the signal bandwidth with a 45° phase margin but is marginal for stability, as indicated by the dashed line. Because f_X is the geometric mean of f_Z and the gain bandwidth product frequency (f_{GBP}) of the amplifier, calculate f_X by the following equation:

$$f_X = \sqrt{f_Z f_{GBP}} \quad (7)$$

Substituting Equation 5 and Equation 6 into Equation 7, the C_F value that produces f_X follows:

$$C_F = \frac{1 + \sqrt{1 + 8\pi R_F C_{IN} f_{GBP}}}{4\pi R_F f_{GBP}} \quad (8)$$

If $8\pi \times R_F \times C_{IN} \times f_{GBP} >> 1$, Equation 8 simplifies to the following:

$$C_F = \sqrt{\frac{C_{IN}}{2\pi R_F f_{GBP}}} \quad (9)$$

Adding C_F also sets the signal bandwidth at f_P. Substitute Equation 9 into Equation 6 and rearrange the equation for the signal bandwidth in terms of f_{GBP}, R_F, and C_{IN} as follows:

$$f_P = \sqrt{\frac{f_{GBP}}{2\pi R_F C_{IN}}} \quad (10)$$

Notice the attainable signal bandwidth is a function of the time constant $R_F C_{IN}$ and the f_{GBP} of the amplifier. To maximize the signal bandwidth, choose an op amp with high bandwidth and low input capacitance, and operate the photodiode in reverse bias to reduce its junction capacitance.

Design Example

As a design example, Figure 86 shows one channel of the ADA4510-2 configured as a TIA amplifier in a photodiode preamp application. Assuming the photodiode has a C_D of 5 pF, an I_D of 2 µA, and the desired full-scale V_{OUT} is 100 mV, R_F is 49.9 kΩ according to Equation 1.

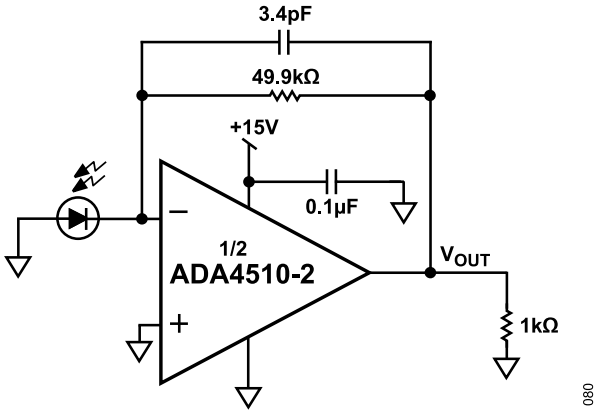

Figure 86. Single-Supply TIA Circuit Using the ADA4510-2

The ADA4510-2 input capacitance (C_{CM} + C_{DM}) is 22 pF, so the total input capacitance (C_{IN}) is 27 pF. By substituting C_{IN} = 27 pF, R_F = 49.9 kΩ, and f_{GBP} = 10 MHz into Equation 8 and Equation 10, the resulting C_F value and the −3 dB signal bandwidth (f_P) are 3.1 pF and 1.1 MHz, respectively.

Figure 87 and Figure 88 show the compensations of the TIA circuit. The system has a bandwidth of 1.1 MHz when it is maximized for a signal bandwidth with C_F = 3.1 pF. Increasing C_F to 5.5 pF reduces the bandwidth to 579 kHz. However, increasing the C_F greatly reduces the overshoot (see Figure 89). In practice, an optimum C_F value is determined experimentally by varying it slightly to optimize the output pulse response.

Use the Analog Devices Analog Photodiode Wizard to design a transimpedance amplifier circuit to interface with a photodiode.

APPLICATIONS INFORMATION

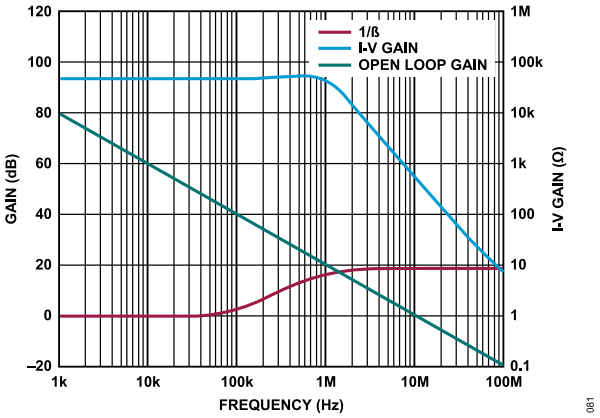

Figure 87. Compensating the TIA, C_F = 3.1 pF

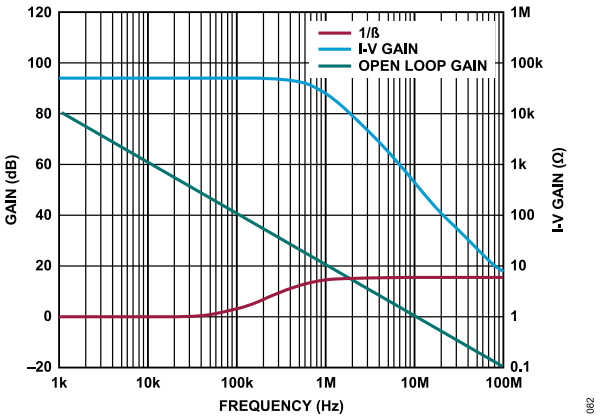

Figure 88. Compensating the TIA, C_F = 5.5 pF

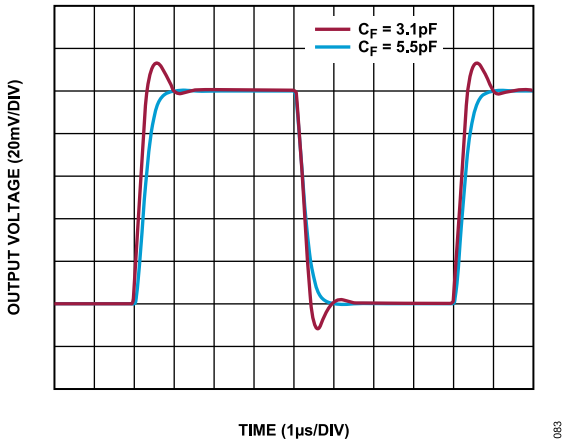

Figure 89. Pulse Response for Various C_F

ACTIVE FILTER

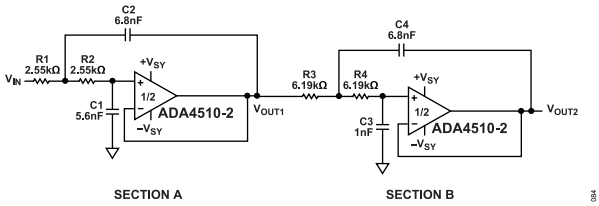

Figure 90. 4-Pole Low Pass Filter with −3dB Bandwidth of 10kHz

Active filters are used to separate signals, passing signals of interest and attenuating signals at unwanted frequencies. For example, low-pass filters are often used as antialiasing filters in data acquisition systems or as noise filters to limit high frequency noise.

The high input impedance, high bandwidth, low input bias current, and DC precision make the ADA4510-2 a good fit for active filter applications. Figure 90 shows the ADA4510-2 in a 4-pole Sallen-Key Butterworth low-pass filter configuration. The 4-pole low-pass filter has two complex conjugate pole pairs and is implemented by cascading two 2-pole low-pass filters. Section A and Section B are configured as 2-pole low-pass filters in unity gain. Table 8 shows the quality factor (Q) requirement and pole position associated with each stage of the Butterworth filter. Refer to Chapter 8, Analog Filters, in Linear Circuit Design Handbook, available at www.analog.com/AnalogDialogue, for pole locations on the s plane and Q requirements for filters of a different order.

Table 8. Q Requirements and Pole Positions

Section	Poles	Q
A	−0.9239 ± j0.3827	0.5412
B	−0.3827 ± j0.9239	1.3065

The Sallen-Key topology is widely used due to its simple design with few circuit elements. This topology provides the user the flexibility of implementing either a low-pass or a high-pass filter by simply interchanging the resistors and capacitors. The ADA4510-2 is configured in unity gain with a corner frequency at 10 kHz. An active filter requires an op amp with a unity-gain bandwidth that is at least 100 times greater than the product of the corner frequency (f_C) and the Q. The resistors and capacitors are also important in determining the performance over manufacturing tolerances, time, and temperature. At least 1% or better tolerance resistors and 5% or better tolerance capacitors are recommended.

Figure 91 shows the frequency response of the low-pass Sallen-Key filter, where:
V_{OUT1} is the output of the first stage.
V_{OUT2} is the output of the second stage.

V_{OUT1} shows a 40 dB/decade roll-off and V_{OUT2} shows an 80 dB/decade roll-off. The transition band becomes sharper as the order of the filter increases.

APPLICATIONS INFORMATION

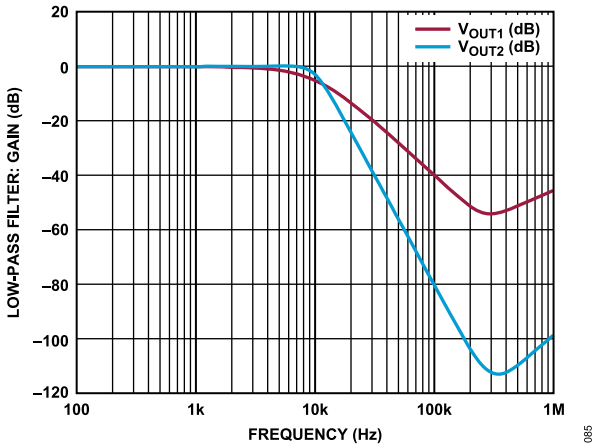

Figure 91. Low-Pass Filter: Gain vs. Frequency

FEEDBACK COMPONENTS

When feedback resistors are used to set up gain, care must be taken to ensure that the pole formed by the resistors and the parasitic capacitance at the inverting input does not degrade stability. If the pole formed is near the desired crossover frequency of the amplifier, the stability will be negatively impacted.

In general, if the parasitic pole lies within the closed-loop bandwidth of the amplifier, add a capacitor in parallel with the R_F to introduce a zero that has a frequency close to the frequency of the pole to improve stability.

For a more detailed discussion, see the Analog Dialogue article: Truth About Voltage Feedback Resistors.

PRECISION BUFFER

The overall precision of high-resolution systems with ADCs and digital-to-analog converters (DACs) depends on the accuracy, stability, and drive capability of the voltage reference of the system. Typically, the best performance requires a costly external reference, because on-chip references and buffers often have poor performance or insufficient drive.

With its low noise specs, the ADA4510-2 can be used to preserve the accuracy of the chosen reference for successive approximation register (SAR) ADC reference inputs. The Voltage Reference Design for Precision Successive-Approximation ADCs Analog Dialogue Article details several considerations and how to compute for noise from the reference circuit to ensure that ADC performance is not affected.

DAC outputs that drive real world sensors also depend on the accuracy of the reference voltage. The low V_{OS}, ΔV_{OS} / ΔT, I_B, e_n p-p, and very high linearity, in combination with the fast settling time and slew rate, make the ADA4510-2 an ideal fit for an output DAC buffer.

RECOMMENDED POWER SOLUTION

Analog Devices, Inc. has a wide range of power management products that meet the requirements of most high performance signal chains. For a dual-supply application, the ADA4510-2 may need as high as ±20 V supply. Low dropout (LDO) linear regulators such as the LT3042 for the positive supply and the LT3093 for the negative supply help improve the PSRR at high frequency and generate a low noise power rail. In addition, if a negative supply is not available, the ADP5070 can generate the negative supply from a positive supply. Table 9 shows the list of the recommended Power Management Devices for ADA4510-2.

Table 9. Recommended Power Management Devices

Product	Description
ADP5070	DC-to-dc switching regulator with independent positive and negative outputs
LT3032	Dual 150mA positive/negative low noise LDO linear regulator
LT3093	−20 V, 200 mA, ultralow noise, ultrahigh PSRR negative linear regulator
LT3042	20 V, 200 mA, ultralow noise, ultrahigh PSRR RF linear regulator

It is recommended to use a low ESR, 0.1 µF bypass capacitor close to each of the power supply pins of the ADA4510-2 and ground to reduce errors coupling in from the power supplies. For noisy power supplies, place an additional 10 µF capacitor in parallel with the 0.1 µF for better performance.

LAYOUT GUIDELINES

The ADA4510-2 has extremely high impedance inputs. Shunt impedances from leakage resistance and parasitic capacitance in the PCB layout can severely degrade the performance of the low bias input. Protect against parasitic leakage currents by using guarding techniques to reduce the voltage gradient seen by the input node. Physically, a guard is a low impedance conductor that surrounds a high impedance node and is driven to the voltage of that node. It serves to buffer leakage by diverting the leakage away from the sensitive node and into the low impedance guard. Remove the solder mask from the guard traces to guard against surface leakage due to contamination. Place any input resistors close to the ADA4510-2 inputs to avoid interaction with trace parasitics. If one of the channels is not in use, connect the input to a voltage that is within the linear range of the channel to avoid overdrive conditions that can interfere with other channels. Leave the output unconnected. Place decoupling capacitors, such as 0.1 µF, near the ADA4510-2. Larger capacitors, such as 10 µF, can be used farther away from the op amp.

SOLDER HEAT EFFECT

All high precision electronic components are susceptible to specification shifts due to mechanical stresses, such as those stresses encountered during high temperature reflow soldering. Such me-

APPLICATIONS INFORMATION

chanical stresses can arise from differences of coefficient of thermal expansion (CTE), the rate at which different materials expand when exposed to heat. During the soldering process, the rapidly changing high temperatures cause the packaging materials surrounding the silicon die to expand at a different rate from the silicon. This mismatch in expansion exerts mechanical stress on the die, which can affect the component electrical properties and cause performance shift if not mitigated.

By baking the PCB assembly for 30 minutes at 125°C after reflow soldering, adverse effects of mechanical stress on the ADA4510-2 can be effectively mitigated ensuring optimal specified performance. Figure 92 shows how the V_{OS} of representative ADA4510-2 operational amplifiers is affected by stimulated high temperature reflow (SHR) and subsequent post solder bake.

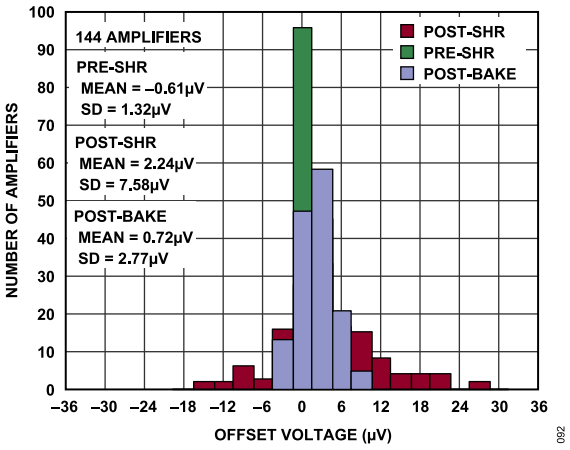

Figure 92. V_{OS} Shift due to Solder Heat

OUTLINE DIMENSIONS

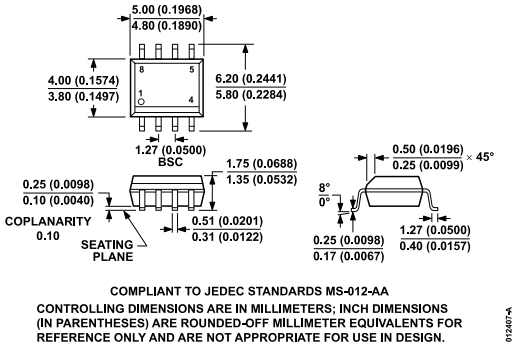

Figure 93. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions show in millimeters and (inches)

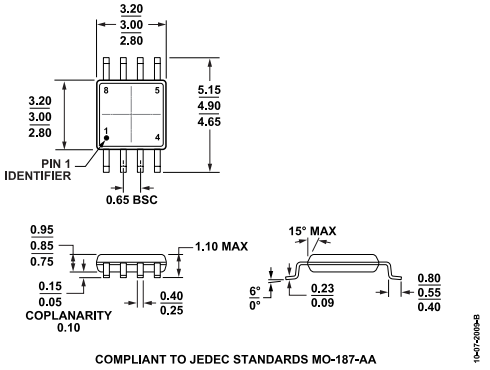

Figure 94. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions Shown in millimeters

Updated: July 24, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADA4510-2ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	Tube, 98	R-8
ADA4510-2ARZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	Reel, 1000	R-8
ADA4510-2ARZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	Reel, 2500	R-8
ADA4510-2ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	Tube, 50	RM-8
ADA4510-2ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	Reel, 1000	RM-8
ADA4510-2ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	Reel, 3000	RM-8

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADA4510-2ARZ	Evaluation Board for 8-Lead Standard Small Outline Package [SOIC_N]
EVAL-ADA4510-2ARMZ	Evaluation Board for 8-Lead Mini Small Outline Package [MSOP]

[1] Z = RoHS Compliant Part.