



# PSMN2R3-80SSF

NextPower 80 V, 2.3 mOhm, 240 Amp, N-channel MOSFET in LFPAK88 package

3 July 2024

Product data sheet

## 1. General description

NextPower 80 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial and consumer applications.

## 2. Features and benefits

- Low  $Q_{rr}$  for higher efficiency and lower spiking
- 240 Amps  $I_{D(max)}$  continuous current rating
- Low  $Q_G \times R_{DS(on)}$  FOM for high efficiency switching applications
- Strong avalanche energy rating ( $E_{as}$ )
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFPAK88 package

## 3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch in DC-DC
- BLDC motor control
- Full-bridge and half-bridge applications
- Battery protection

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	-	240	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	341	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 12</a>	-	1.7	2.3	mΩ
		$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 100\text{ °C}$ ; <a href="#">Fig. 13</a>	-	2.6	3.5	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 40\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	7	22	51	nC
$Q_{G(tot)}$	total gate charge		61	123	184	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 78\text{ A}$ ; $V_{sup} \leq 80\text{ V}$ ; $R_{GS} = 50\text{ Ω}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; $t_p = 163\text{ μs}$ ; <a href="#">Fig. 4</a>	[1]	-	663	mJ

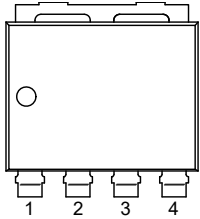
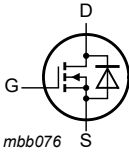
NextPower 80 V, 2.3 mOhm, 240 Amp, N-channel MOSFET in LFAK88 package

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$Q_r$	recovered charge	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 40\text{ V}$ ; $T_J = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 18</a>	-	47	-	nC

[1] Protected by 100% test

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>LFAK88 (SOT1235)</p>	
2	S	Source		
3	S	Source		
4	S	Source		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R3-80SSF	LFAK88	plastic, single-ended surface-mounted package (LFAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R3-80SSF	X2F3S80S

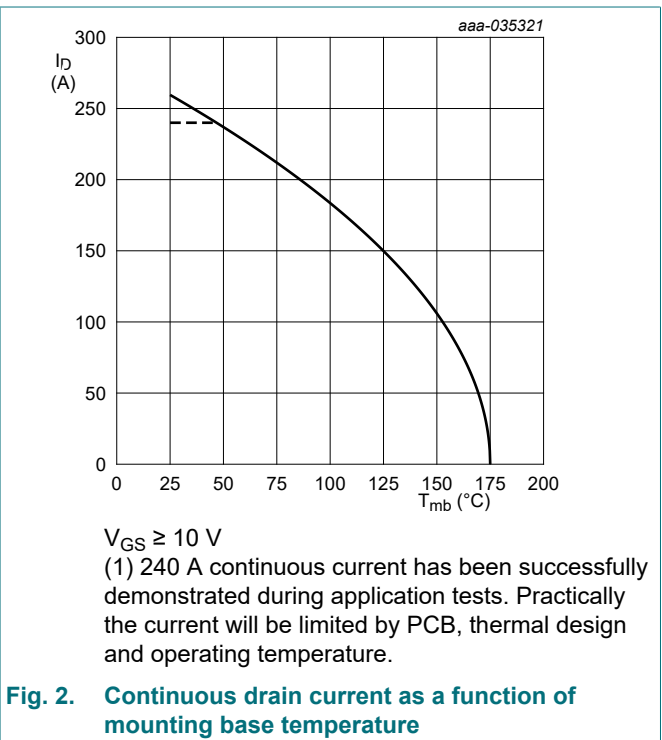
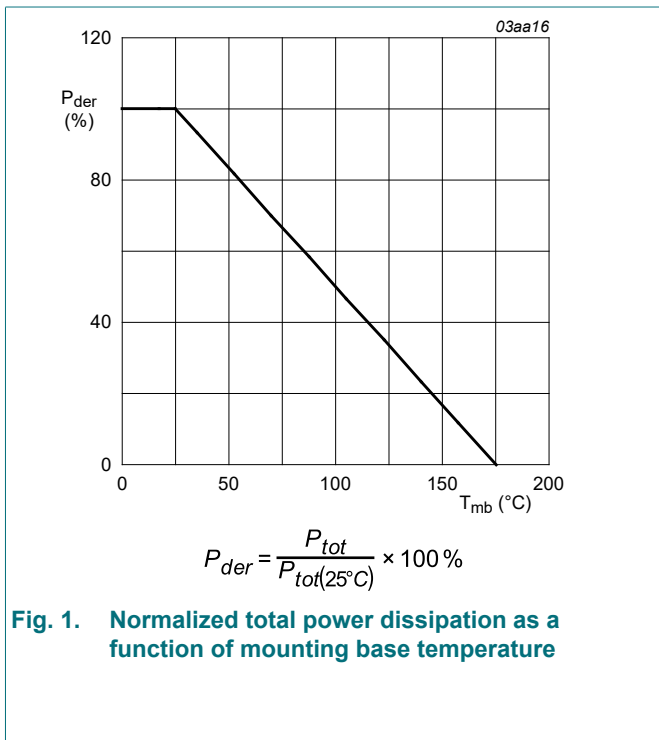
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_j = 25\text{ °C}$  unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	80	V
$V_{DGR}$	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	80	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	341	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	240	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; <a href="#">Fig. 2</a>	-	183	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 3</a>	-	1038	A
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	240	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	1038	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 78\text{ A}$ ; $V_{sup} \leq 80\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; unclamped; $t_p = 163\text{ }\mu\text{s}$ ; <a href="#">Fig. 4</a>	[1]	-	663 mJ
$I_{AS}$	non-repetitive avalanche current	$V_{sup} \leq 80\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $R_{GS} = 50\text{ }\Omega$ ; <a href="#">Fig. 4</a>	[1]	-	78 A

[1] Protected by 100% test



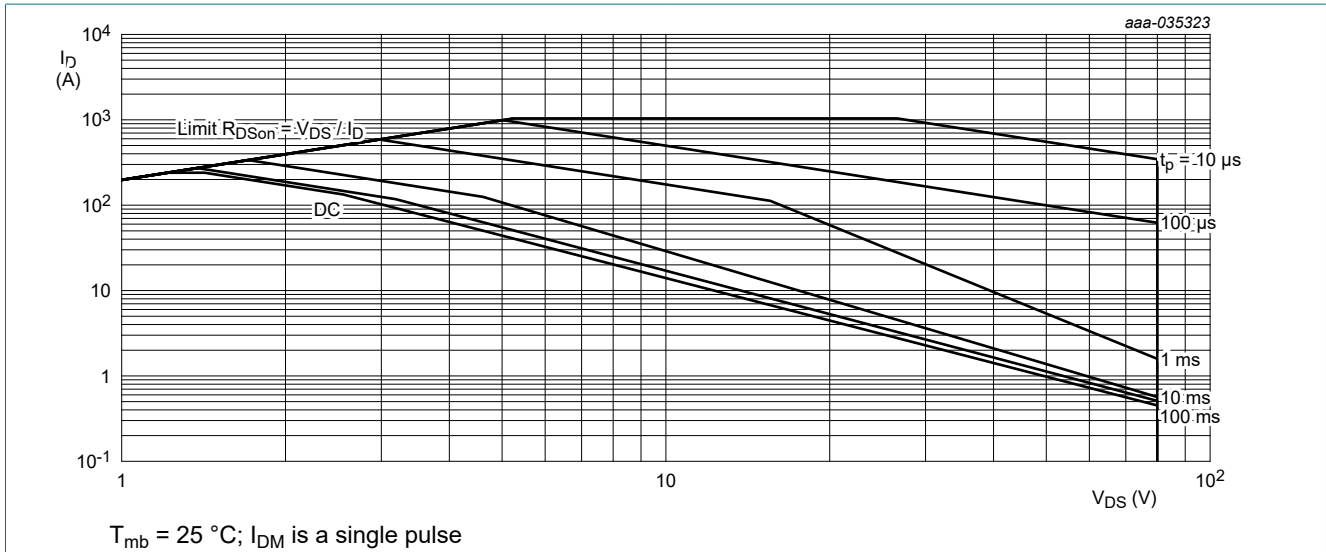


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

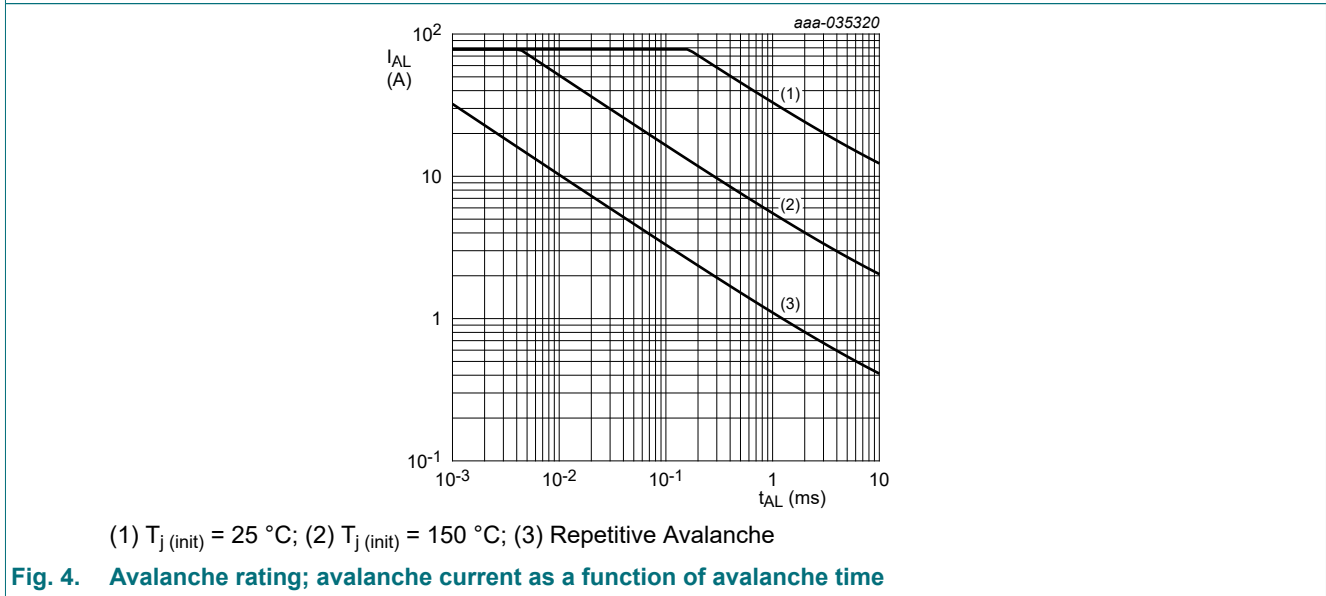
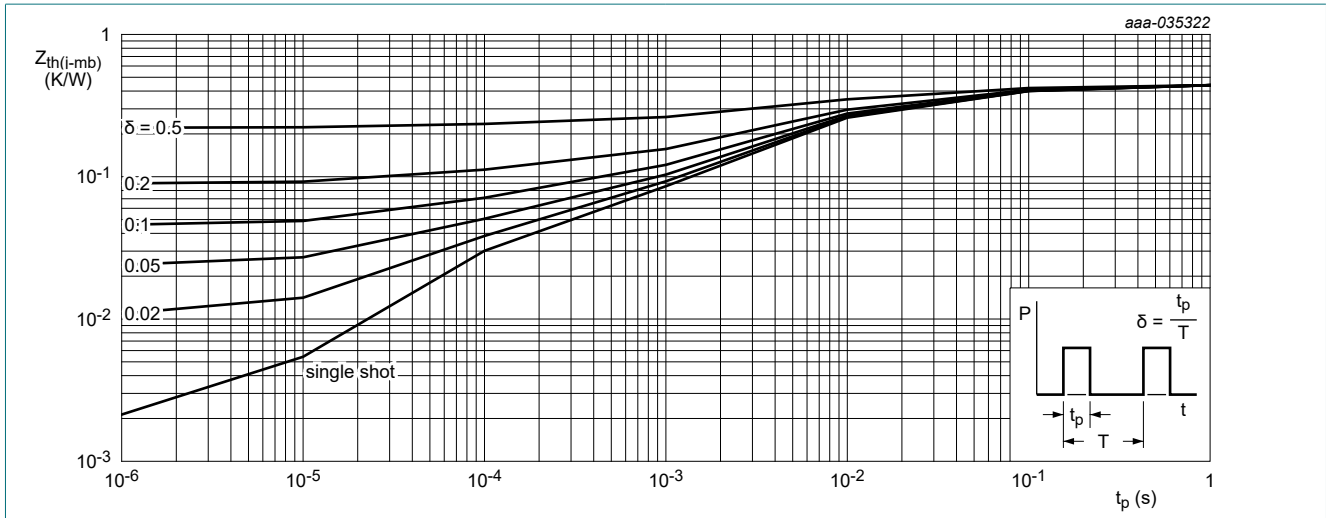


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

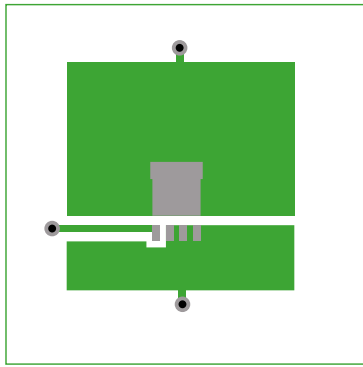
## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	0.22	0.44	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 6</a>	-	35	-	K/W
		<a href="#">Fig. 7</a>	-	70	-	K/W

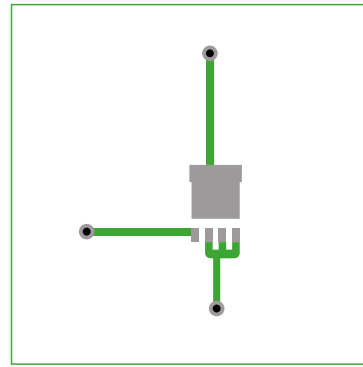


**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**



Copper square 25.4 mm square; 70 μm thick on FR4 board

**Fig. 6. PCB layout for thermal resistance from junction to ambient**



70 μm thick copper on FR4 board

**Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient**

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.6	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$	-	3.5	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-8.4	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.08	1	$\mu A$
		$V_{DS} = 80 V; V_{GS} = 0 V; T_j = 125 \text{ }^\circ C$	-	26	100	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	1.7	2.3	m $\Omega$
		$V_{GS} = 7 V; I_D = 25 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	2.1	3.4	m $\Omega$
		$V_{GS} = 10 V; I_D = 25 A; T_j = 100 \text{ }^\circ C;$ <a href="#">Fig. 13</a>	-	2.6	3.5	m $\Omega$
		$V_{GS} = 10 V; I_D = 25 A; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 13</a>	-	3.6	5.1	m $\Omega$
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.5	1	2	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V;$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 14;</a> <a href="#">Fig. 15</a>	61	123	184	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V;$ $T_j = 25 \text{ }^\circ C$	-	64	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V;$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 14;</a> <a href="#">Fig. 15</a>	21	35	49	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	24	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	11	-	nC
$Q_{GD}$	gate-drain charge		7	22	51	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A; V_{DS} = 40 V; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 14;</a> <a href="#">Fig. 15</a>	-	4.3	-	V
$C_{iss}$	input capacitance	$V_{DS} = 40 V; V_{GS} = 0 V; f = 0.5 \text{ MHz};$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 16</a>	5280	8800	12320	pF
$C_{oss}$	output capacitance		1530	2550	4080	pF
$C_{rss}$	reverse transfer capacitance		9	87	260	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 40 V; R_L = 1.6 \text{ } \Omega; V_{GS} = 10 V;$ $R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	32	-
$t_r$	rise time		-	28	-	ns
$t_{d(off)}$	turn-off delay time		-	82	-	ns
$t_f$	fall time		-	40	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; Fig. 17	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;	-	49	-	ns
$Q_r$	recovered charge	$V_{DS} = 40\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; Fig. 18	-	47	-	nC

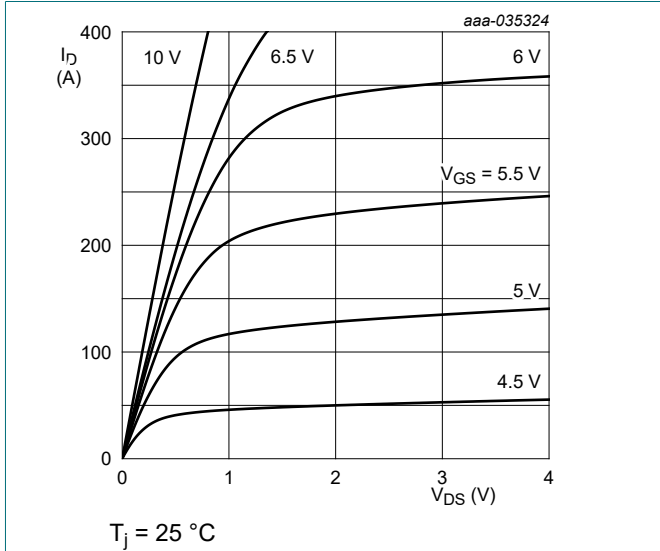


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

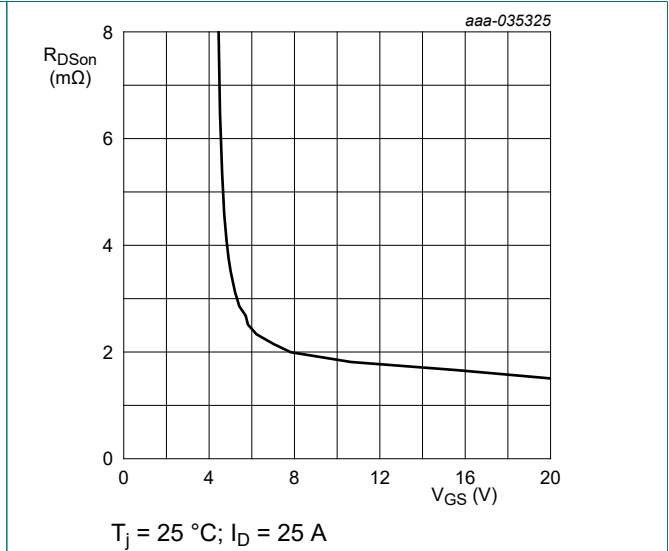


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

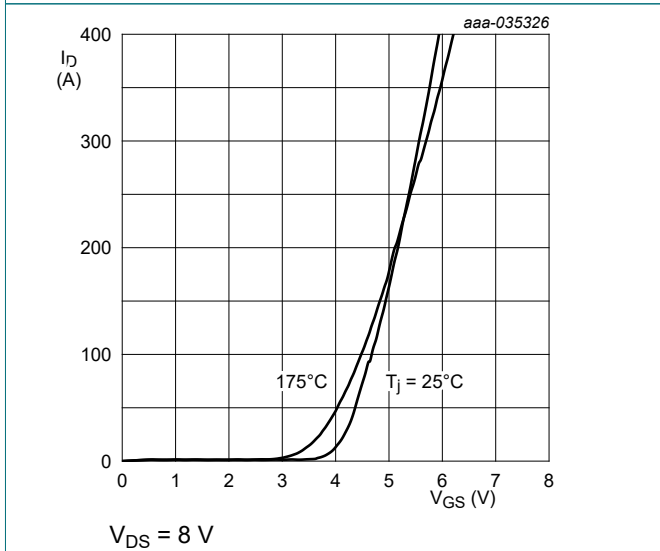


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

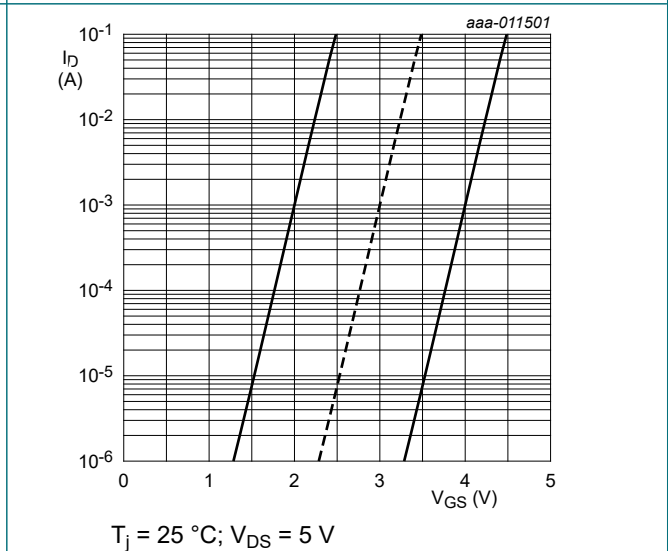


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

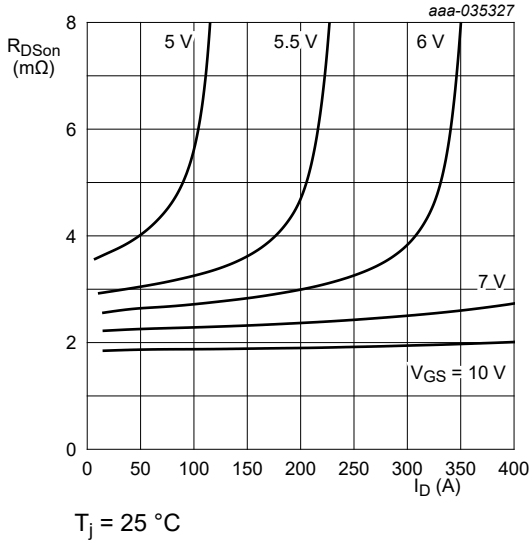
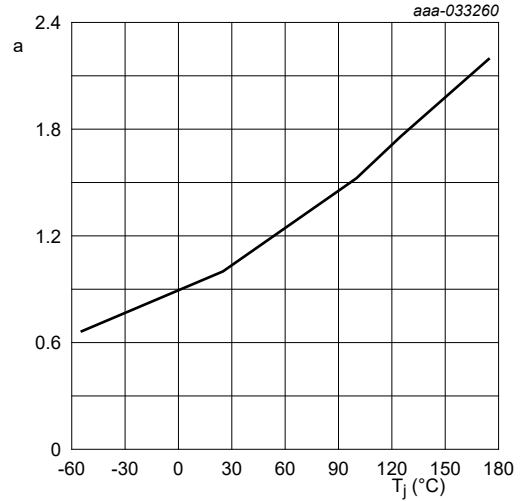


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

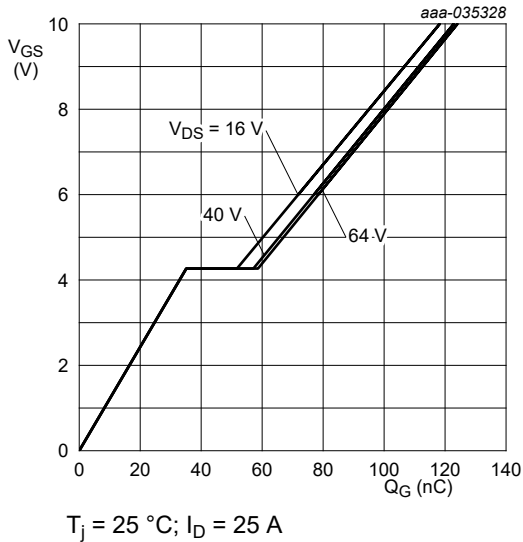


Fig. 14. Gate-source voltage as a function of gate charge; typical values

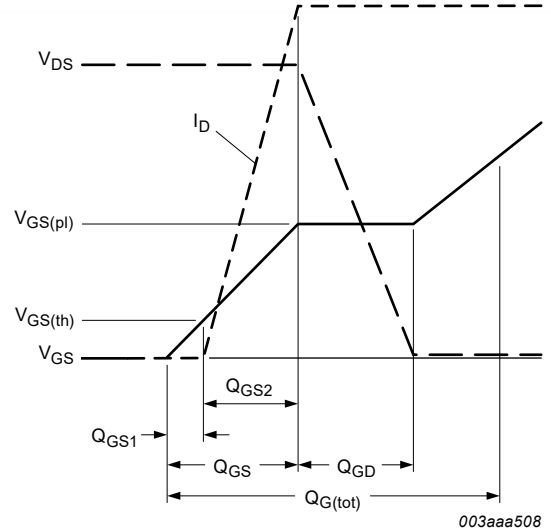
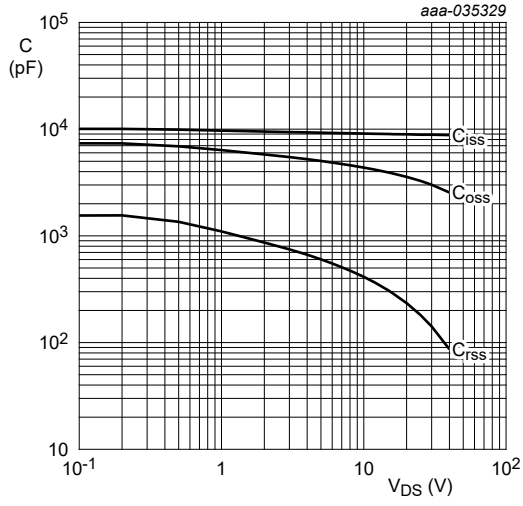


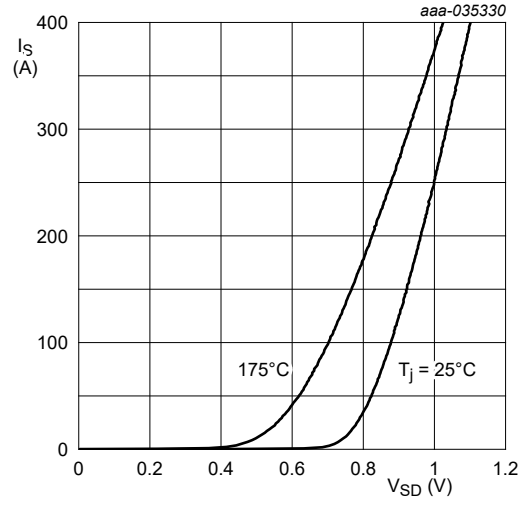
Fig. 15. Gate charge waveform definitions





$V_{GS} = 0$  V;  $f = 1$  MHz

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0$  V

Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

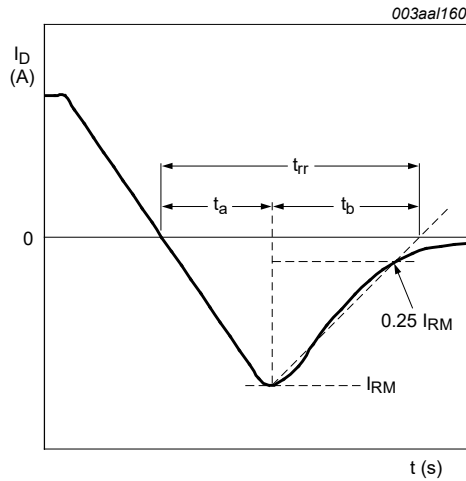


Fig. 18. Reverse recovery timing definition

### 11. Package outline

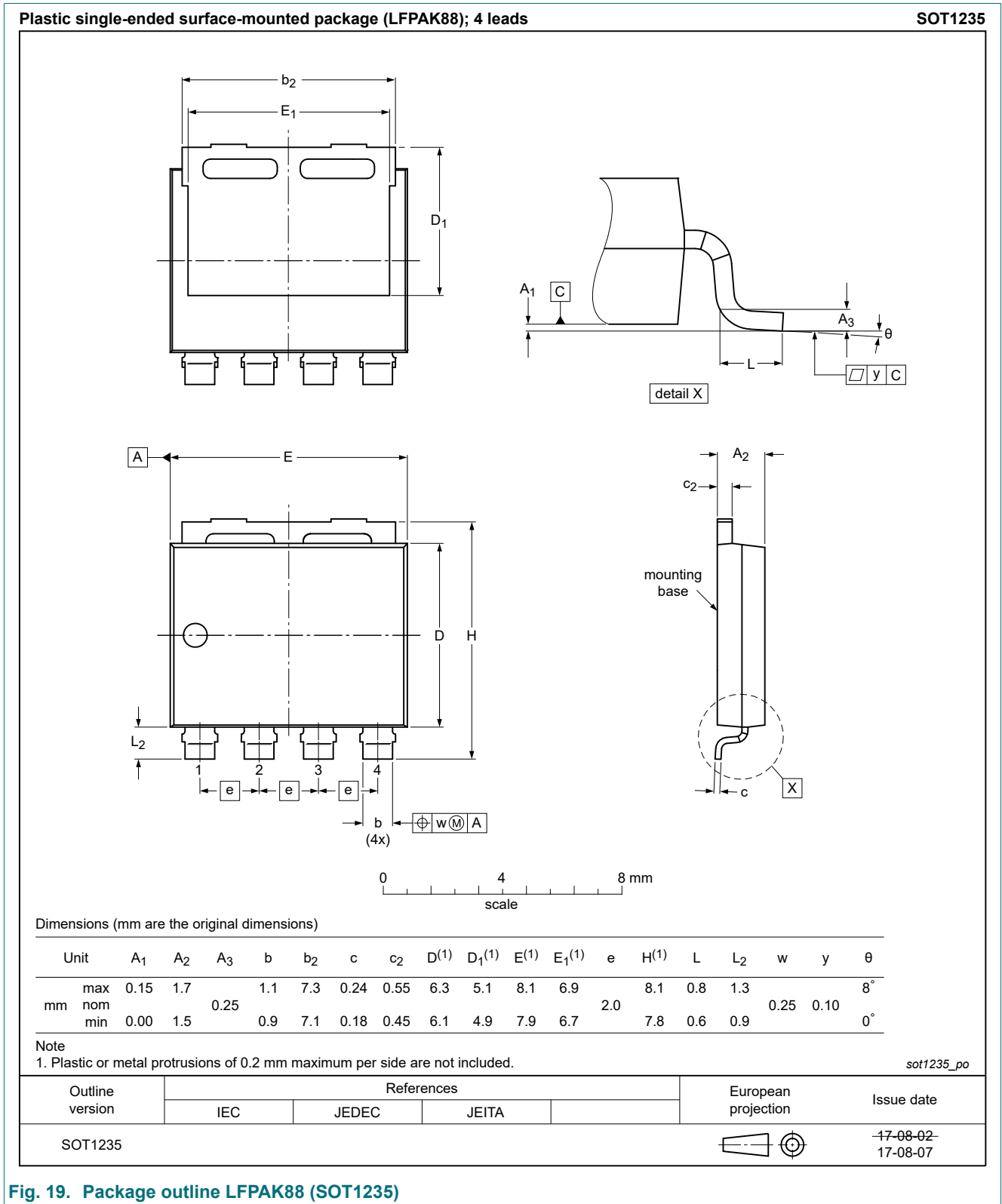


Fig. 19. Package outline LPAK88 (SOT1235)

## 12. Soldering

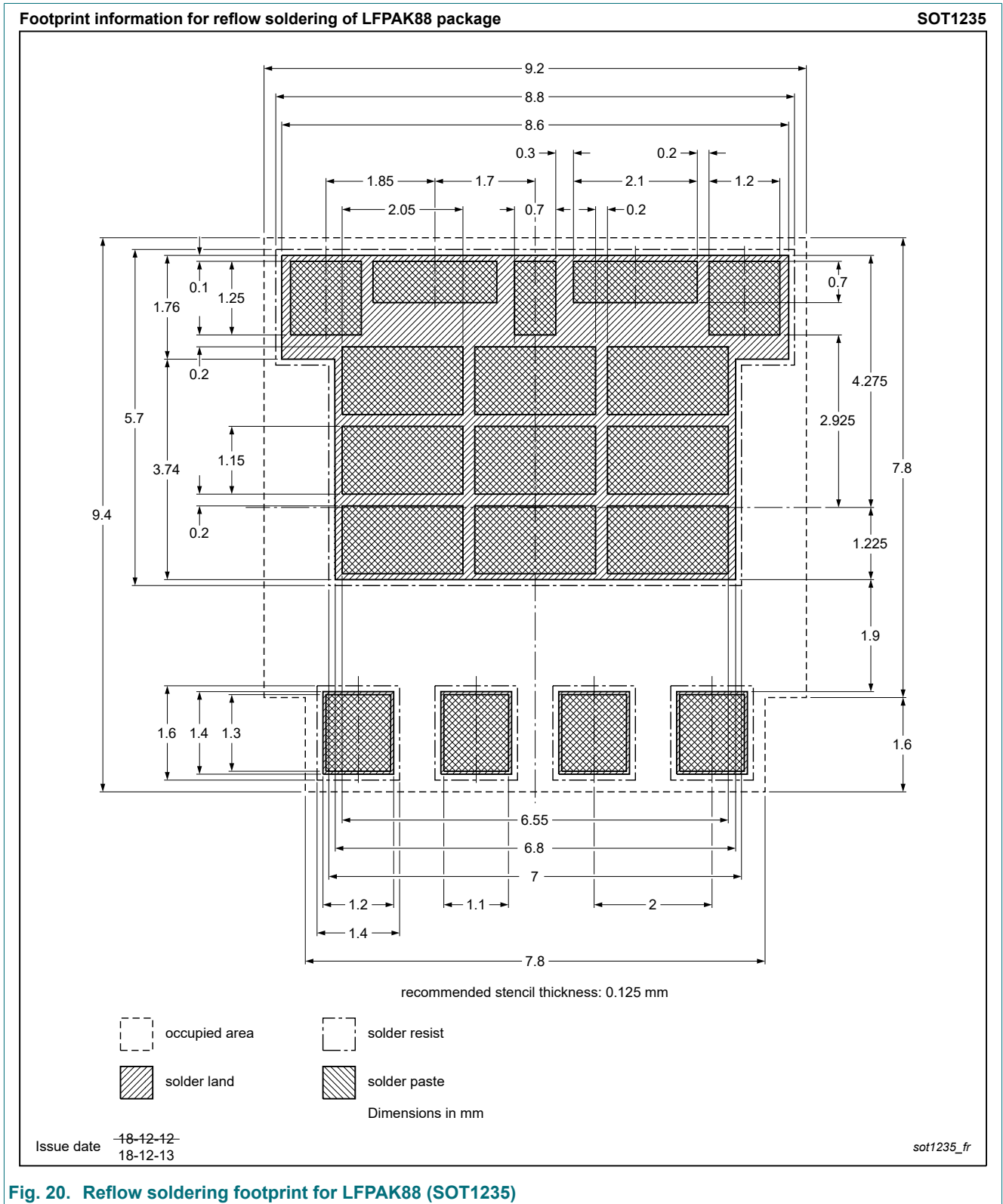


Fig. 20. Reflow soldering footprint for LPAK88 (SOT1235)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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